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Exercise 7:
The MOS Transistor

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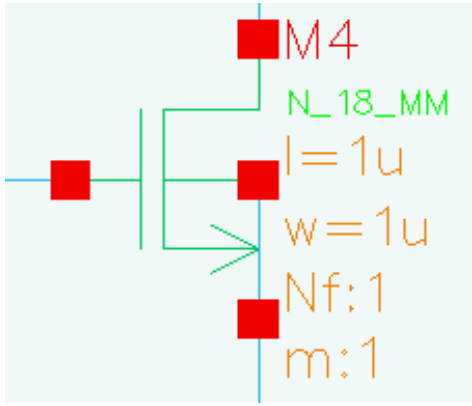
Exercise 6.1: NMOS in Linear Region



- Use an *NMOS* transistor of type N_18_MM from library UMC_18_CMOS with W=L=1µm
- Connect
  - source and bulk to ground
  - the gate to 2 V
- Sweep V_{DS} from -0.1V to 0.1 V and observe the current
- Extract the resistivity of the channel
- Double W *or* L and simulate & extract again.
  - Are the results as expected ? Compare W=L=1µ and W=L=2µ!
- Now sweep the *gate* voltage from 0.6 V to 2 V. Explain!
- Now sweep the *drain* voltage from 0V to 1V. Verify the saturation point for a few gate voltages.
- What happens if you sweep the drain voltage from -1V on?

Exercise 6.2: Transfer Charact. & Transconductance

- For an NMOS of W=L=1µm with V_{BS} = 0, keep the drain at 1.8 V and sweep the gate voltage from 0 to 1.8 V. This is the *transfer characteristic* of the MOS.
  - Observe the drain current
  - Plot the square root of the current. Do you find a straight line as expected?
  - Plot the current in log scale. Can you see the sub-threshold region?
  - What is the transconductance at V_{GS} = 1V (make a derivative!)?
- Make a parametric sweep changing W from 0.24µm to 2µm
  - Is the current proportional to W?
- Repeat this for a L-sweep (start with 180nm)

- Plot the transfer curve for two different values of V_{BS}, for instance 0 V and -2 V

Exercise 6.3: Output Characteristic, Saturation

- Now plot the output characteristic, i.e. I_D as a function of V_{DS} for a fixed V_{GS} (for instance V_{GS} = 1.0 V)
  - Can you see the linear region and the saturated region?
- Extract the output resistance for instance for V_{GS}=1.8V and V_{DS}=1.8V (derivative!).
- Plot the output characteristic for V_{GS} =0..1.8V in 0.2V steps
  - Observe how the current changes
  - Observe how the saturation voltage changes
  - Observe how the output resistance changes (Early voltage ?)

- Now use two NMOS with different W (for instance 0.5µm and 2µm).
  - Search for gate voltages so that the currents for a given V_{DS} (for instance for 1.8 V) are similar.
  - Compare the output characteristics & saturation voltages

Exercise 6.4: PMOS

- Simulate transfer and output characteristic for a PMOS
  - Note that the source of the transistor is now ‚on top'
  - Gate and drain must be negative with respect to source

- Simulate in parallel a NMOS of the same size.
  - Plot the drain current of NMOS and PMOS simultaneously.
  - How big is the difference?