RUPRECHT-KARLS-
UNIVERSITÄT
HEIDELBERG

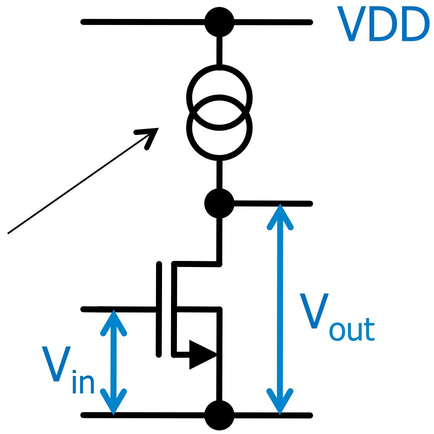
Exercise 9:
Gain Stage

Prof. Dr. P. Fischer

Lehrstuhl für Schaltungstechnik und Simulation
Uni Heidelberg

9.1 Basic Gain Stage

- Implement a NMOS gain stage.
  - Use a NMOS with W/L = 1µ/0.2µ
  - Use a PMOS of same dimension as a current source
  - Bias the PMOS with a *mirror* to 10µA
  - Operate at VDD = 1.8 V



- Sweep V_{in} and observe V_{out}
- What is the largest gain (derivative!) ?
- Change
  - the bias current
  - W of the input transistor
  - L of the PMOS

and observe what happens. Explain!

9.2 Comparing Gain to Theory

- In the previous circuit, fix an operation point in the high gain region (i.e. pick a V_{in} and note the corresponding V_{out})
- Determine the gain by calculating the derivative of the transfer function
- Compare this to an AC sweep at the operation point

- Now extract
  - g_m of the NMOS (at the operation point!)
  - r_{ds} of NMOS and PMOS (at the operation point!)
- Calculate the gain. Does it match?

9.3 Bandwidth

- Load the gain stage with a capacitor (1 pF)
- Observe the bandwidth

- Modify the load capacitor
  - Is bandwidth inversely proportional to C_L?

- Modify I_D
  - Make a Parametric Sweep with 2-3 values (1µA, 10µA, 100µA)
  - Do you find what you expect?

9.3.b Effect of Load Dimension

- Use a simple gain stage with an NMOS and a PMOS (mirror) load
- Introduce a self-bias (automatic setting of the operation point, see lecture slides) to $V_{in} = V_{out}$ with
  - a large (1 GΩ) resistor between input and output and
  - a large (1 F) capacitor to ac couple the input signal

- Check with an AC sweep that the circuit works
  - A DC sweep will NOT work with this same circuit! (why?)
- At constant bias, change L of the load (and the mirror) and see how the (dc) gain varies
- Repeat this for a longer input NMOS

9.4 Cascoded Gain stage

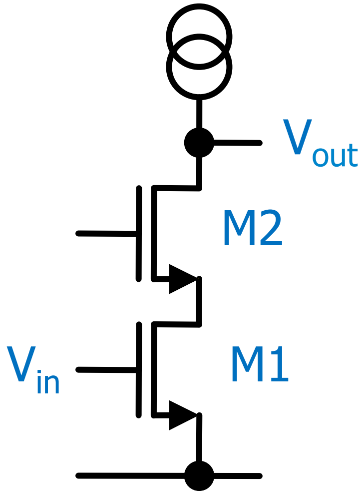
- Set up a cascoded gain stage
  - Use W/L = 5µ / 0.2µ for all 4 MOS
  - Use I_{bias} = 10 uA
  - Use a stacked mirror on the PMOS side
  - Use a 'safe' cascode voltage for the NMOS
  - Make a DC sweep

- Use the self bias presented in the lecture to set a good operation point
  - First check with the DC sweep that $v_{out} = v_{in}$ is a good operation point

- What is the gain?

9.5 Transfer Function of the Cascoded Gain Stage

- Calculate the transfer function of the cascoded gain stage
  - Assume an ideal load (current source)
  - Consider a load capacitor C_L



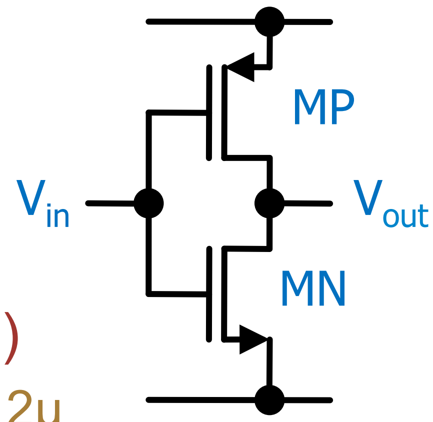
- What are
  - the DC gain?
  - the unity gain bandwidth?

- Compare to the case with no cascode

- Use the simulation from 9.4 to verify your finding

9.6 The Inverter

- The PMOS 'load' in the gain stage supplies a more or less constant current
- In the CMOS Inverter shown, the PMOS is switched with the input signal, it acts as the NMOS



- Simulate the DC transfer function $V_{out}(V_{in})$
  - For instance $L_N = L_N = 0.2\mu$, $W_N = 1\mu$, $W_P = 2\mu$
  - What is different from the normal gain stage ?
  - What is the maximum gain ?
- Use a small signal analysis to find the gain