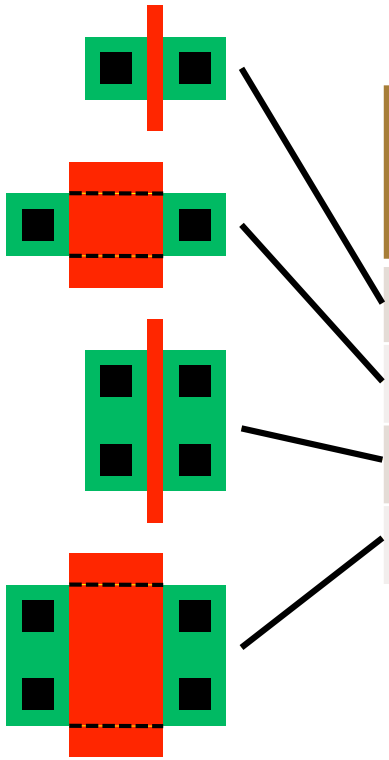
Basic Circuits

Current Mirror, Gain stage, Source Follower, Cascode,
Differential Pair,…

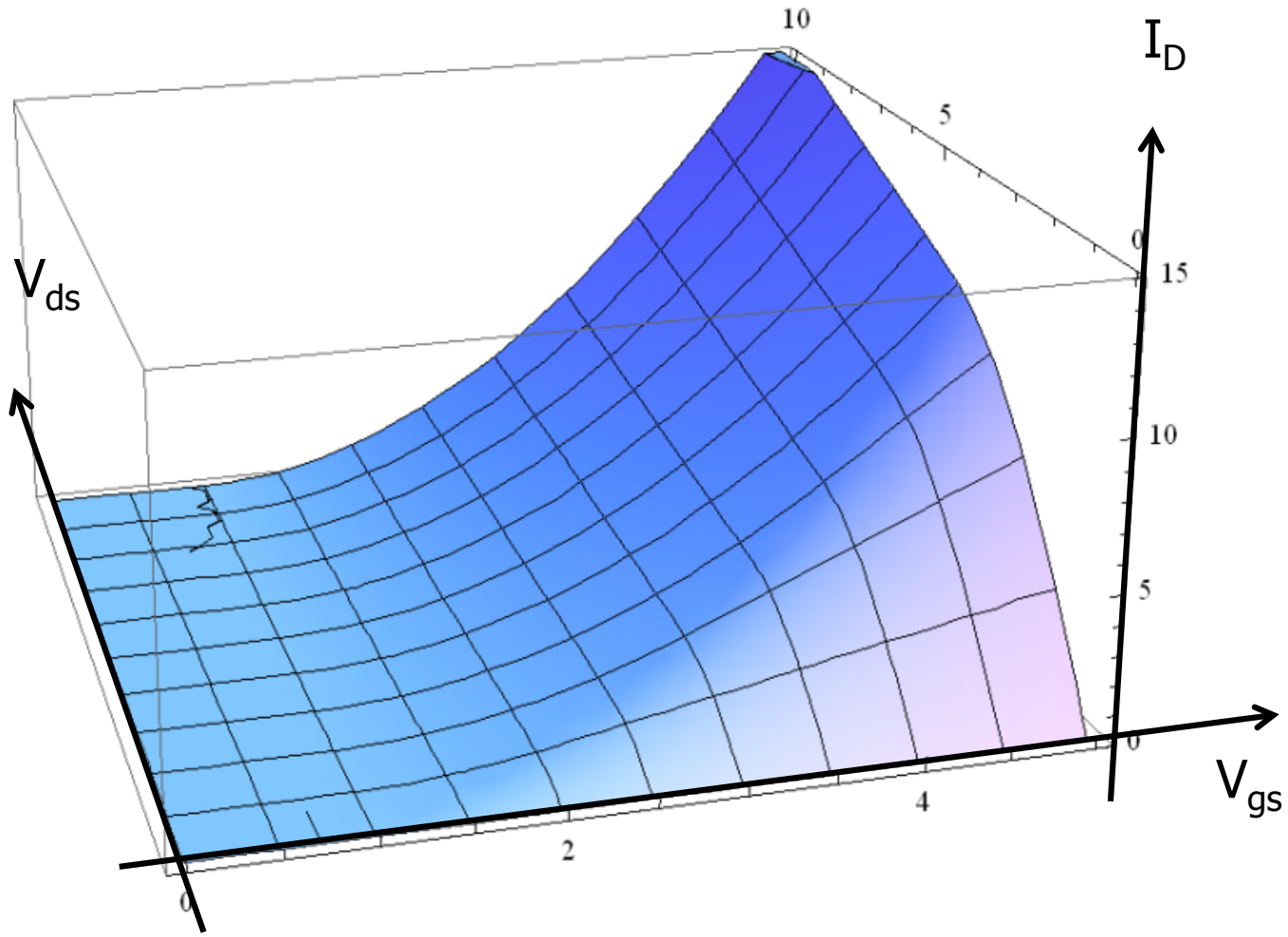
Reminder: Effect of Transistor Sizes

- Very crude classification:



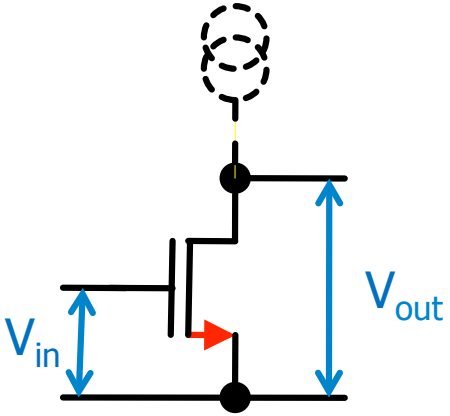
W	L	Current (const. V_{GS})	Output Resistance (const. V_{GS})	Gate Capacitance
small	small	0	low	small
small	large	-	high	high
large	small	+	low	high
large	large	0	high	very high

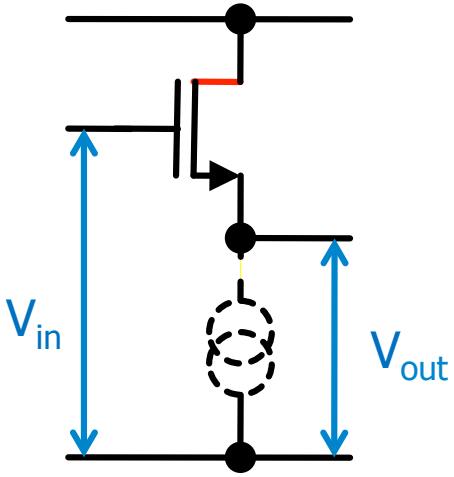
Reminder: Transistor Characteristics

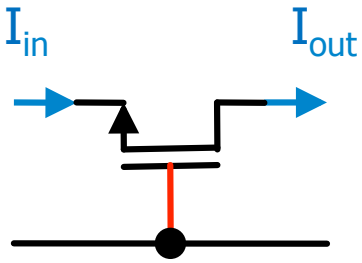


The Three Basic Configurations:

- 'Common xxx configuration' means:
  Terminal xxx of the MOS is common to input and output







- common *source* config.
- 'gain stage'
- inverting voltage gain
- *high* input impedance
- *high* output impedance

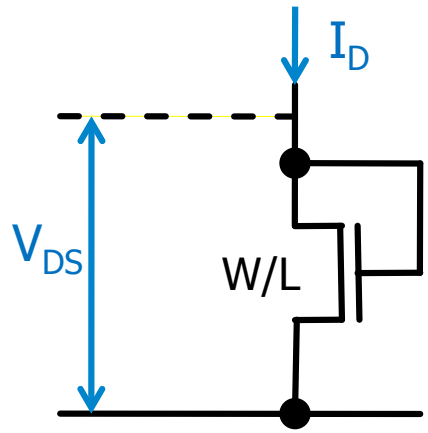
- common *drain* config.
- 'source follower'
- voltage gain <~ 1
- *high* input impedance
- *low* output impedance

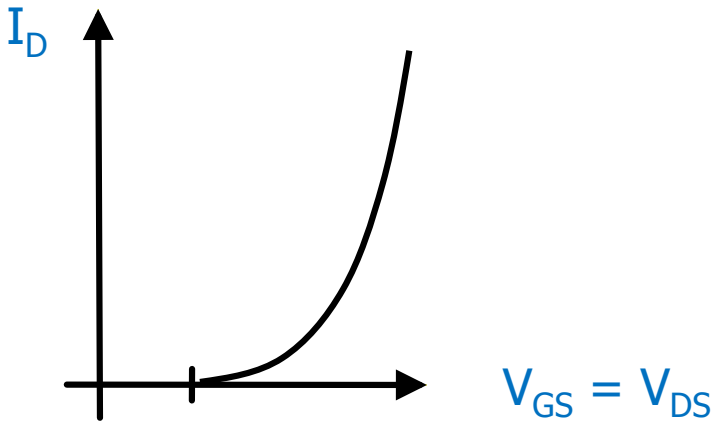
- common *gate* config.
- 'cascode'
- current gain = 1
- *low* input impedance
- *high* output impedance

The Diode-Connect MOS

- Consider a MOS with Drain and Gate connected
- $\mathbf{V_{DS} = V_{GS}} \rightarrow \mathbf{V_{DS}} = V_{GS} > V_{GS} - V_T = \mathbf{V_{DSat}}$

→ A diode connected MOS is always in saturation!





$$I_D = K/2\ W/L\ (V_{DS}-V_T)^2\ (1+\lambda\ V_{DS})$$

(in 'strong inversion')

- Important:

For *any* current I_D, V_{GS} adjust so that this current can flow!

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THE CURRENT MIRROR

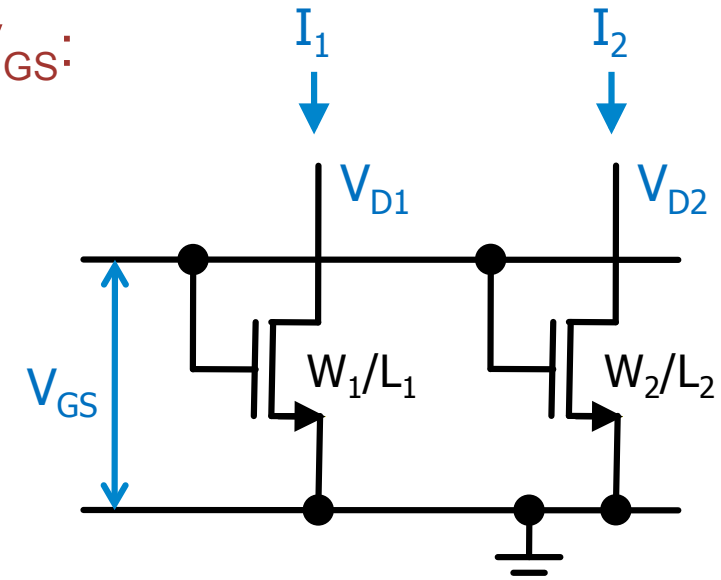
What You Should Learn

- In this first part, you should learn / understand
  - What ‘saturation’ is
  - How transistor geometry affects circuit properties
  - How circuit properties can be improved by *transistor geometry*
  - How small signal models can be applied
  - How circuit properties can be improved by *better circuits*

  - What a current mirror is
  - How several scaled currents can be generated
  - What a bias voltage is

Transistors with same V_{GS}

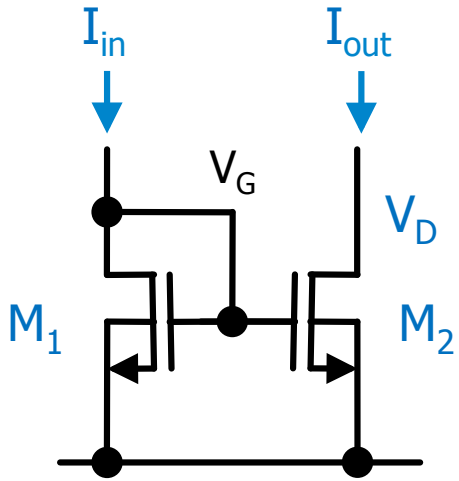
- Consider 2 NMOS with same V_{GS}:



- Assuming saturation:
  - $I_1 = \frac{K}{2}\frac{W_1}{L_1}(V_G - V_T)^2(1 + \lambda_1 V_{D1})$
  - $I_2 = \frac{K}{2}\frac{W_2}{L_2}(V_G - V_T)^2(1 + \lambda_2 V_{D2})$
- $\rightarrow \frac{I_2}{I_1} = \frac{W_2/L_2}{W_1/L_1}\frac{1 + \lambda_2 V_{D2}}{1 + \lambda_1 V_{D1}}$
- The Early effect leads to a ‚small' deviation
- For $L_1 = L_2$:
  - The ratio of input/output current is given by the ratio of the Ws
  - The Early effects cancel if $V_{D1} = V_{D2}$ (must watch λ)

The Current 'Mirror'

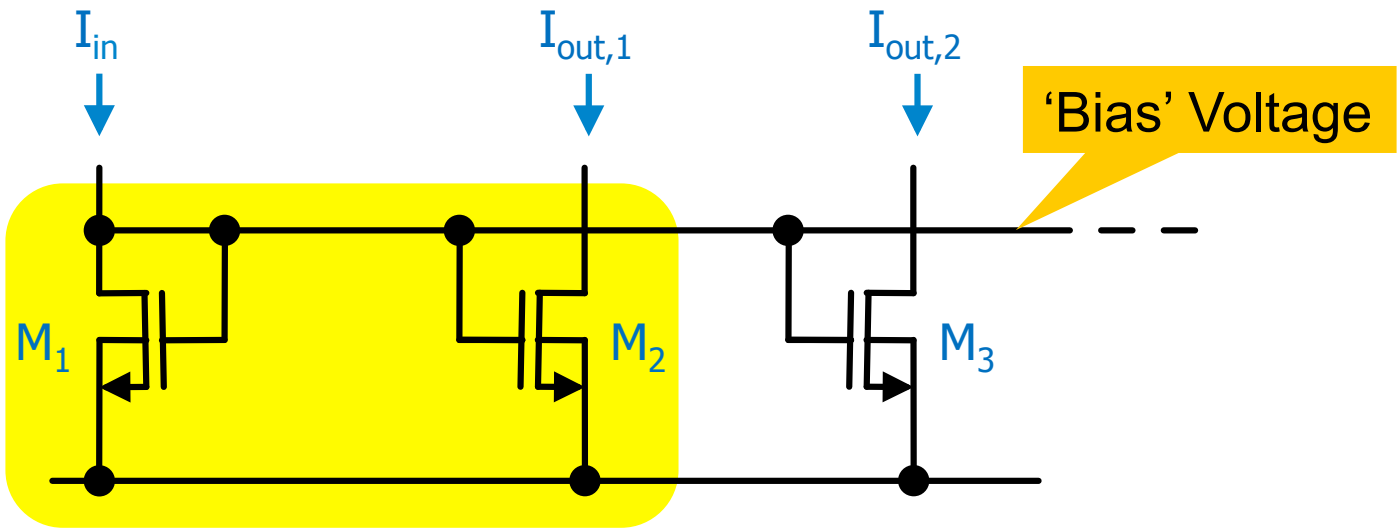
- First, we assume that M_1 and M_2 are identical
  - $W_1 = W_2$, $L_1 = L_2$
- Now connect M_1 as a diode
  - V_G adjusts such that I_{in} flows into M_1
- M_2 and M_1 have the same gate voltage → $I_{out} = I_{in}$
  - The current is 'mirrored' from the input to the output



- In more detail, Early Effect must be taken into account
  - $I_{out} = I_{in}$ *exactly* only for $V_D = V_G$ (do you understand why?)

Varying the Output Current

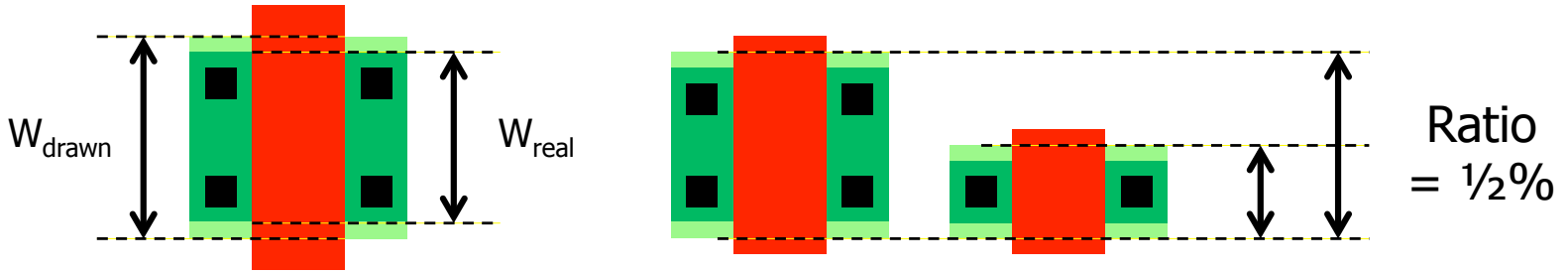
- If $W_2 \neq W_1$ (assuming still $L_1=L_2$), then $I_{out} = W_2/W_1\ I_{in}$
- $L_1 \neq L_2$ should be avoided because Early Effects are different
- Additional MOS can be connected to give further outputs



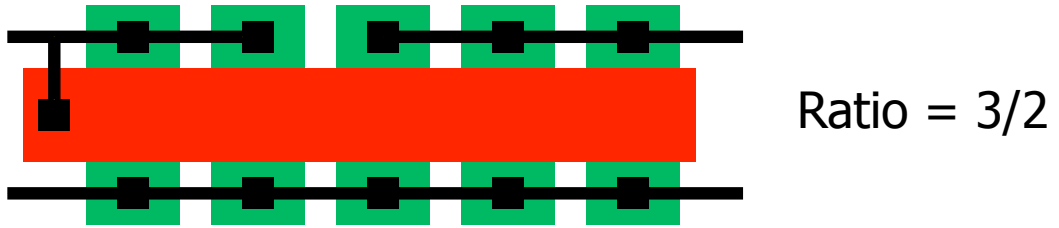
- The gate voltage of the sources is called a *'Bias'* Voltage

Large W vs. Multiple MOS

- The *ratio* W_2/W_1 is used for current multiplication
- If this implemented by MOSs with different layouts, *edge effects* can lead to unknown ratios.
  - To be more precise, the real W of a device is often $W_{real} = W_{drawn} - W_{offset}$ (W_{offset} can have both signs)



- It is much safer to use *multiple identical* devices!
- For a non-integer ratio A/B, use B MOS on diode side and A MOS on output side.



Exercise: NMOS Mirror

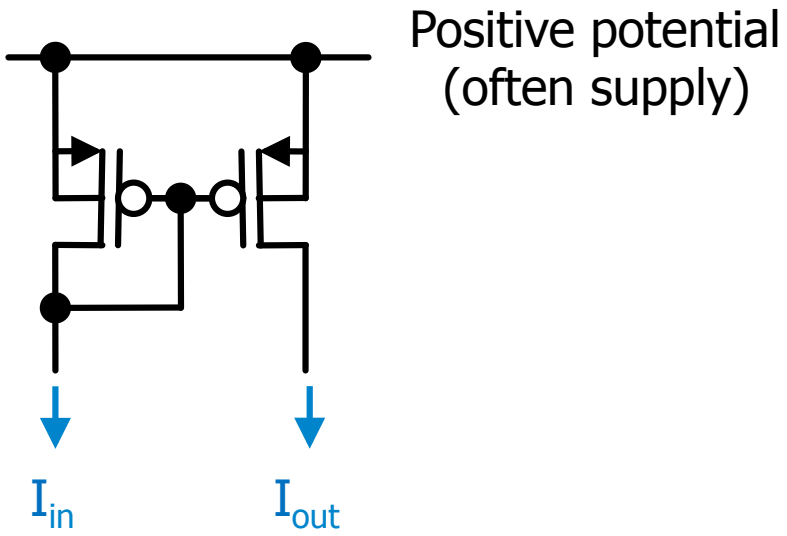
- Design a NMOS current mirror arrangement which converts an *input current of 10µA* into two output currents of 10µA and 30µA.
  - Chose W/L = 1µm / 1µm
  - Connect the outputs to VDD = 1.8V
- What is the gate voltage?
- Compare it to the threshold voltage of the MOS!
- What is the lowest voltage at the outputs for which you expect the mirror to work? Is it the same for both outputs?
- Verify this with simulation by forcing the outputs to some voltage V_{out} and perform a DC sweep of V_{out}.
- How can you make the mirror still work at lower output voltages? Simulate this!
- For which output voltage is I_{out} 'perfect', i.e. exactly 10/30µA?

Exercise: PMOS Mirror

- Design a PMOS 1:1 current mirror
- Verify its operation by simulation

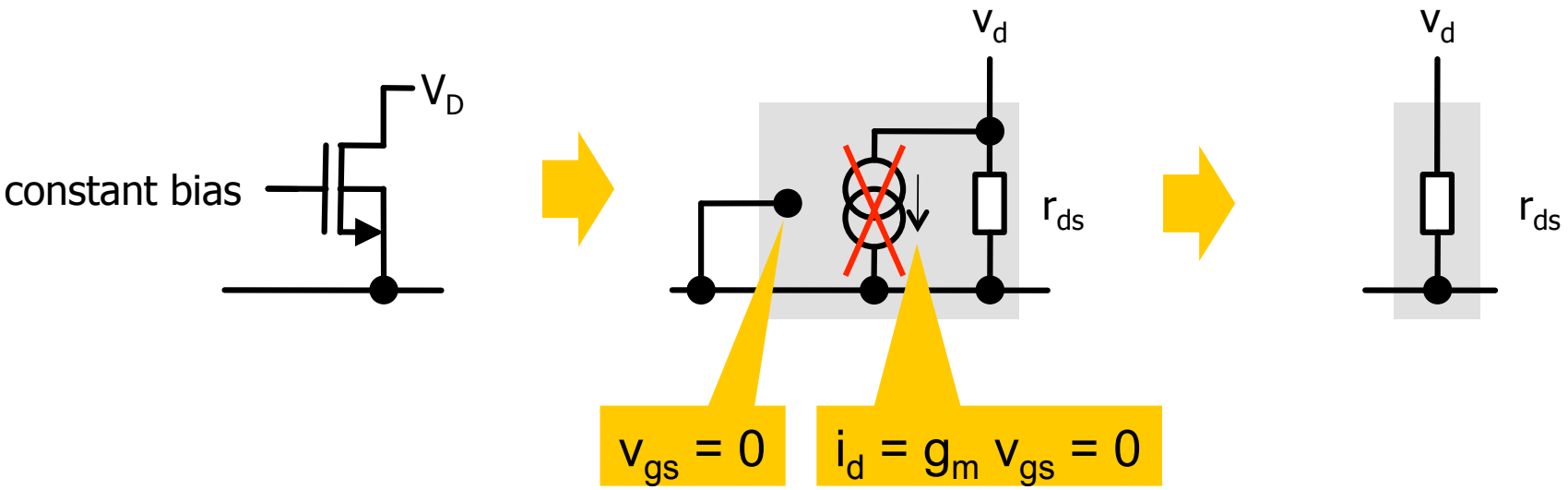
The PMOS mirror

- Here is how the PMOS mirror looks like:



Output Resistance

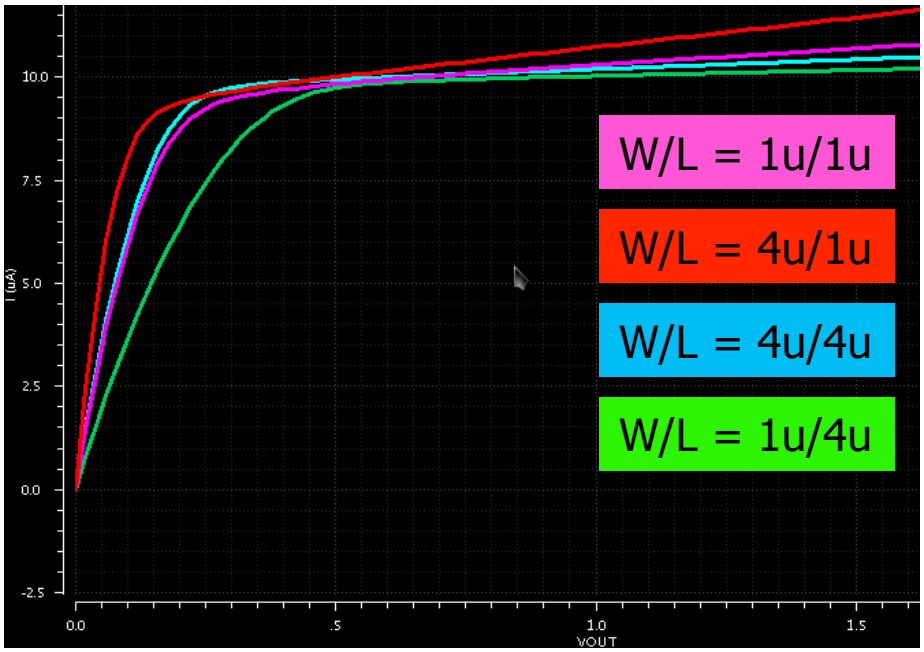
- The Output Resistance r_{out} of the Mirror is just that of the (output) MOS
- This is obvious from the small signal model
  - The Gate voltage is *constant*, so there is *no small signal*: $v_{gs} = 0$

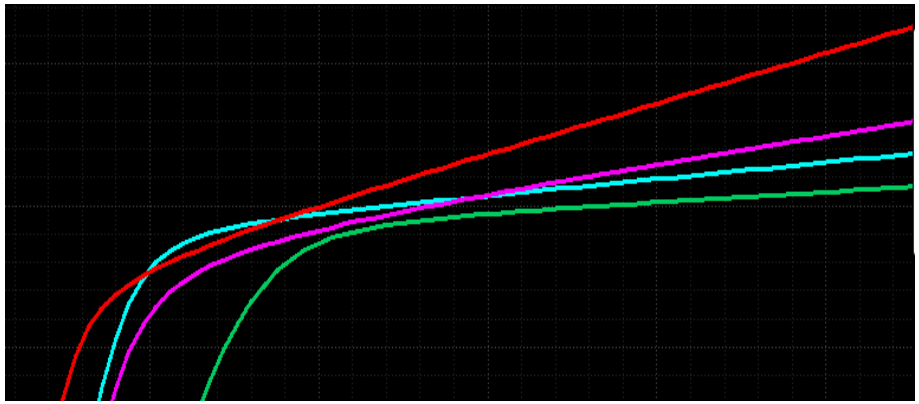


- r_{ds} depends on the current and on the geometry (W,L)

Good and Bad Mirrors

- Normally, the output MOS of the mirror is used as a current source. We therefore want
  - high output resistance r_{ds} → we need small I_D, large L
  - low saturation voltage → we need small I_D, small L, large W





- Therefore: Good mirrors must have large L and W
  - large L to increase output resistance
  - large W to lower saturation voltage

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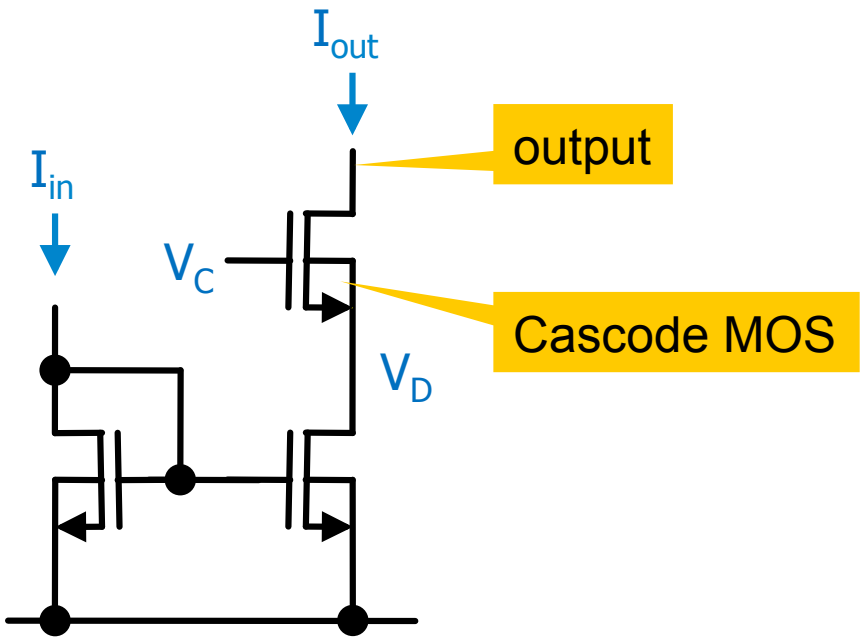
THE CASCODE

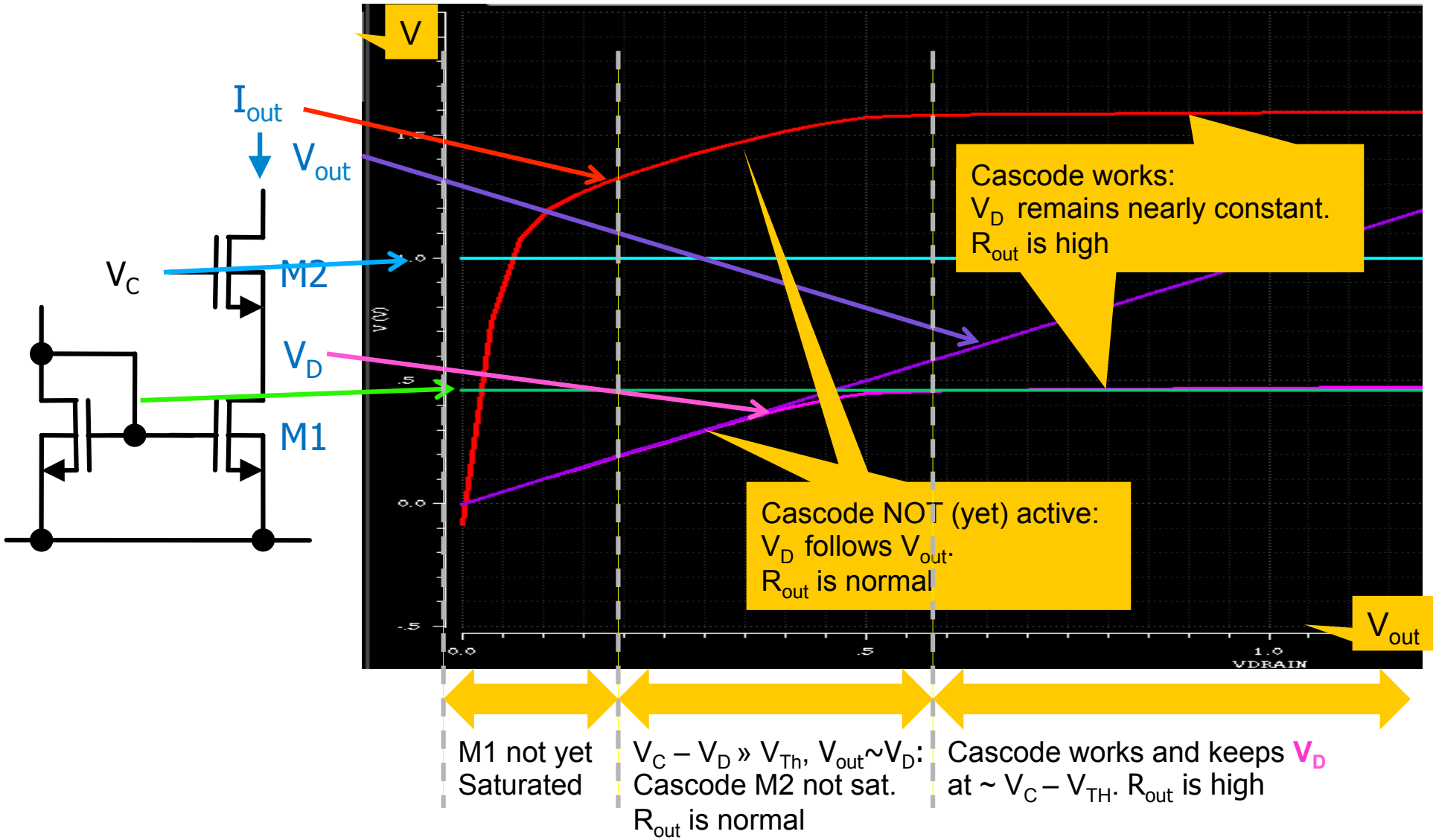
Improving the Mirror: The Cascode

- The output current in a normal mirror changes, because output voltage = drain voltage
- By inserting another MOS *between* output and drain, the drain voltage is kept (more) constant
  - the current changes (less)
  - the output resistance is higher :-)
- The upper MOS is called a **CASCODE**



The Cascoded Current Source in Action

- Simulation for V_C = 1V (not optimal, see later...)

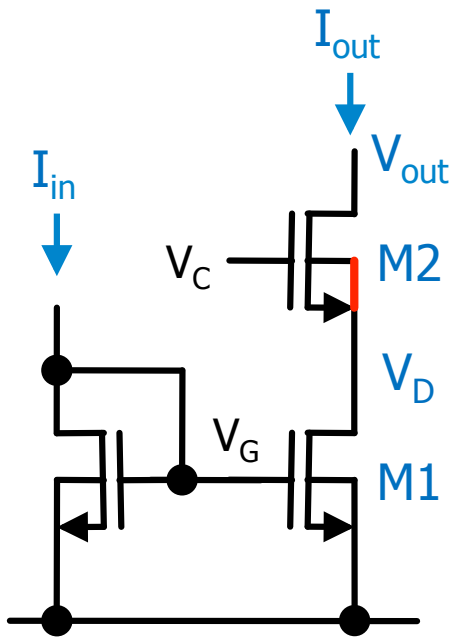


Biasing the Cascode

- The *gate* voltage of the cascode MOS M2, V_C, defines the *drain* voltage V_D of the 'current setting' MOS M1
  - V_D is *roughly one threshold* voltage below V_C
  - More precisely, $V_D = V_C - V_T - \mathrm{Sqrt}(I_D\ 2/K\ L/W)$
  - (This holds when Bulk and Source are connected (-), otherwise, the Substrate Effect lowers V_D)

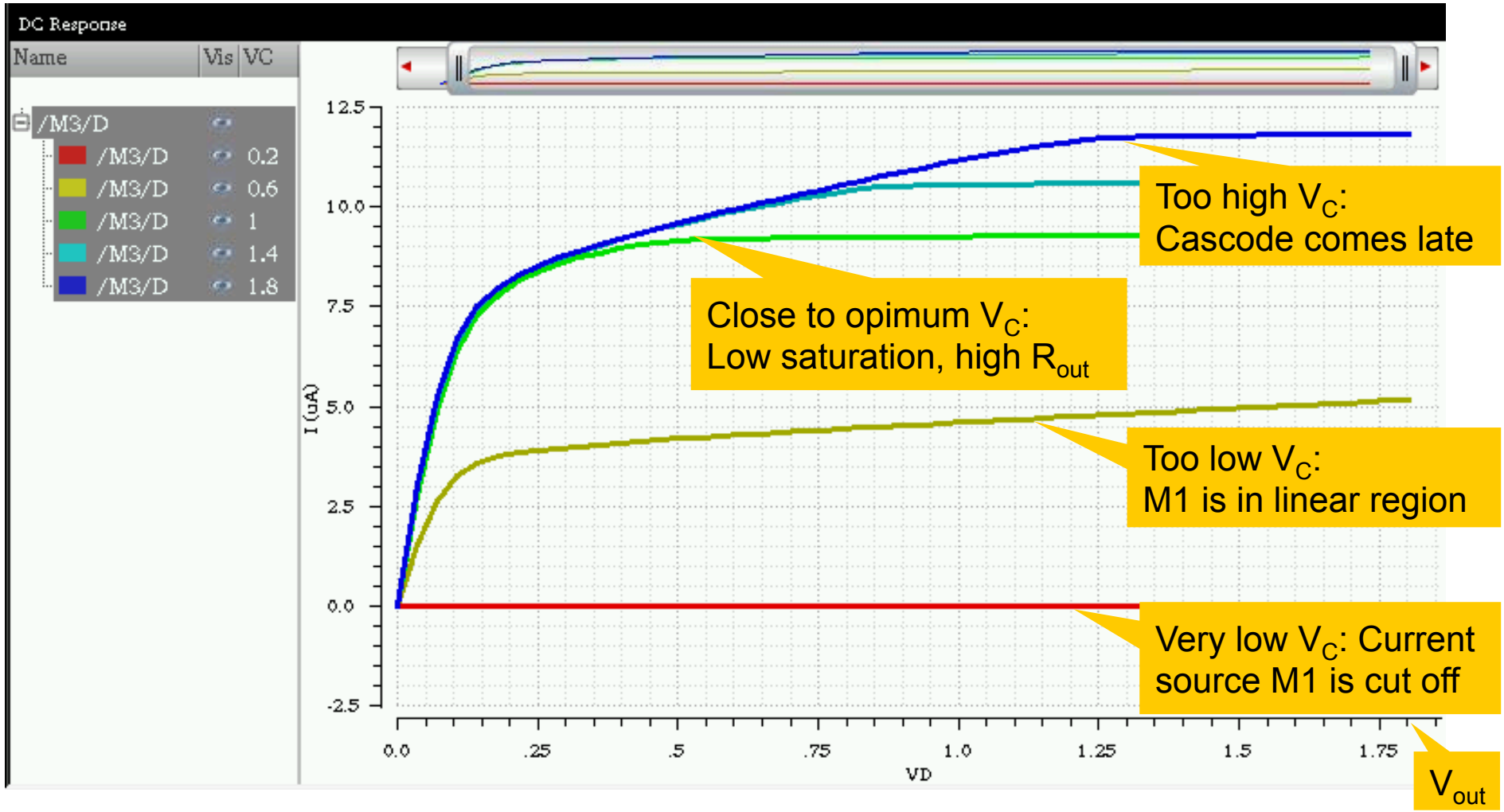
- V_D (and thus V_C) should be chosen
  - *High enough* to keep M1 'just' saturated
  - *As low* as possible so that V_{out} can be low

- The ‚total' saturation voltage at the output for optimal V_D / V_C is ~ twice that of M1 (if M1 and M2 have same sizes)



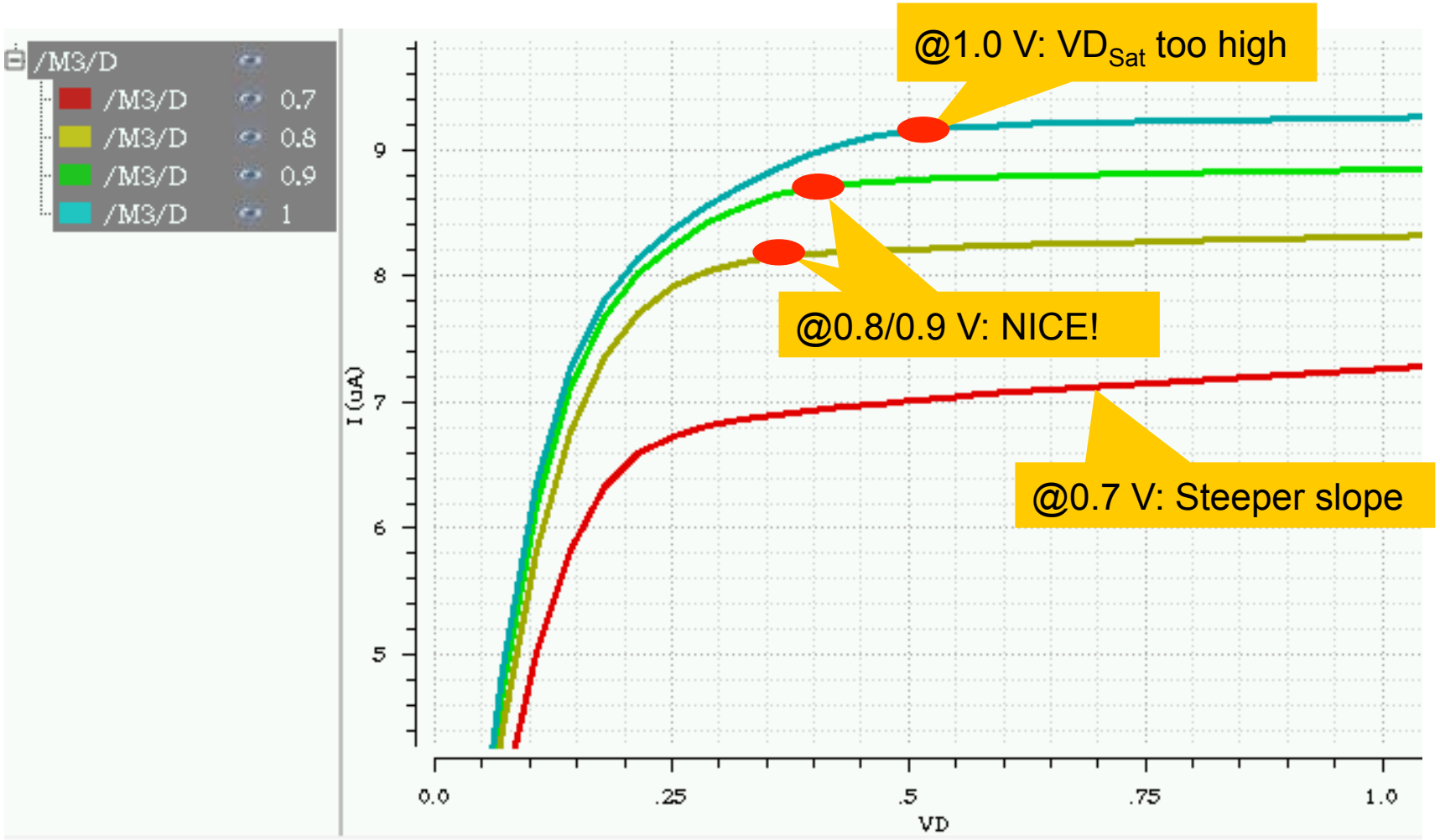
Simulation: Varying V_C

- Sweep V_C from 0.2...1.8 V:



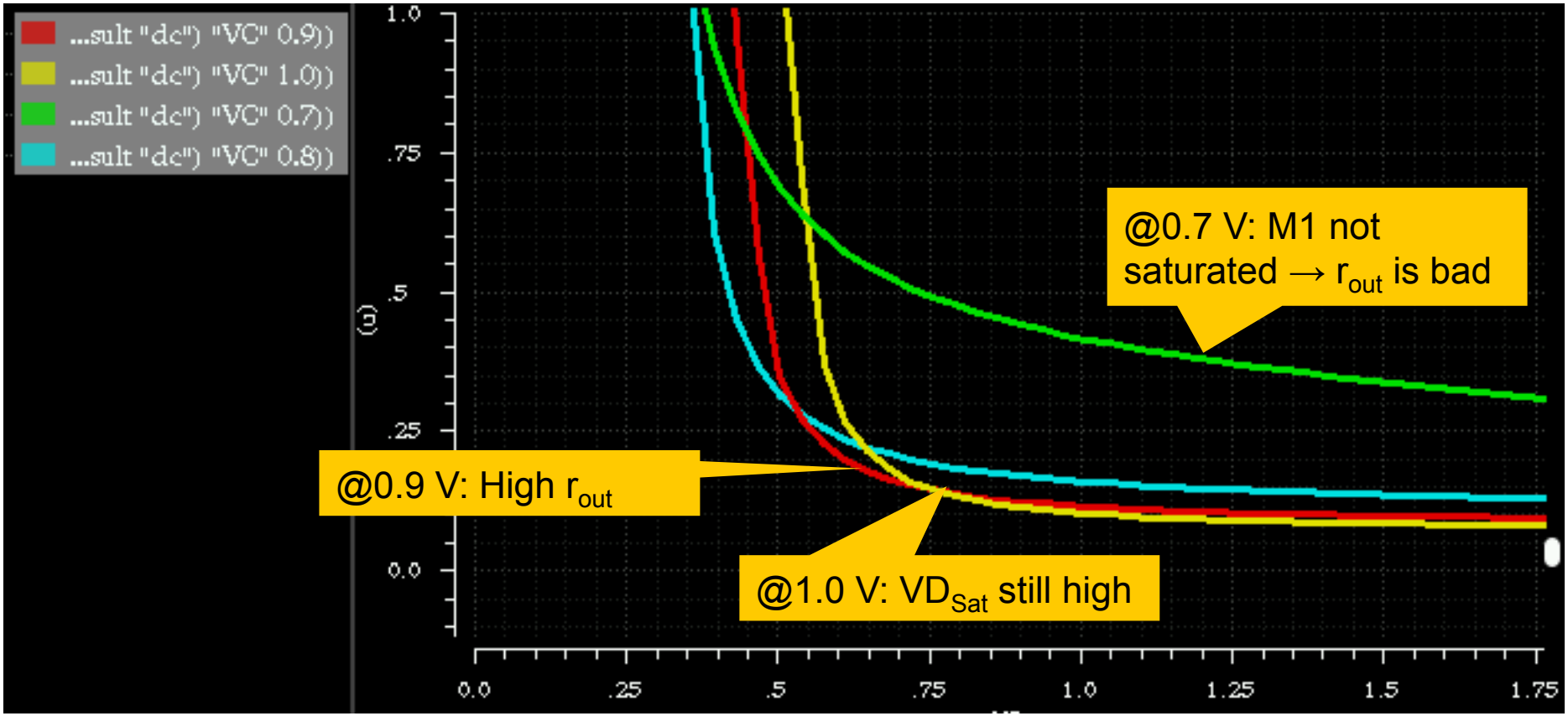
Zoom of 'Optimum' V_C:

- Sweep 0.7...1.0 V



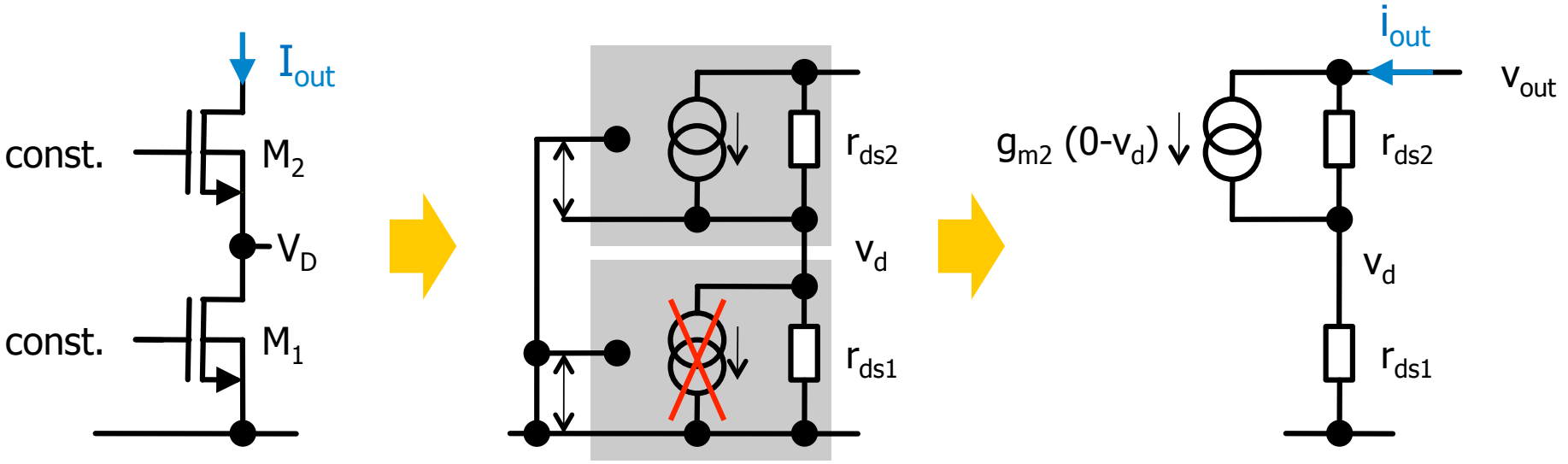
R_{out} and *dynamic range* in more detail

- Look at derivative of output characteristic ($\partial I_{out}/\partial V_{out} = 1/r_{out}$)
  - Small is good
- Again, blue (0.8 V) or red (0.9 V) are best...



Output Resistance of Cascoded MOS

- Small signal analysis
  - We only need to consider the output part
  - Fixed voltages are equivalent to ground
  - Current source M1 delivers no current (V_{GS} = fix)



- Current sums:
  - $i_{out} = (v_{out} - v_d)/r_{ds2} - g_{m2}\, v_d = v_d / r_{ds1}$ $\rightarrow v_d = \ldots \rightarrow r_{out} = v_{out}/i_{out}$

$\rightarrow r_{out} = r_{ds1} + r_{ds2} + g_{m2}\, r_{ds1}\, r_{ds2}$ $\rightarrow$ $r_{out} \cong r_{ds1} \times (g_{m2}\, r_{ds2})$

The Calculation

$$\frac{v_{out} - v_d}{r_{ds2}} - g_{m2} v_d = \frac{v_d}{r_{ds1}}$$

$= i_{out}$

$$\frac{v_{out}}{r_{ds2}} = \frac{v_d}{r_{ds1}} + \frac{v_d}{r_{ds2}} + g_{m2} v_d$$

$$\frac{1}{v_d} = \frac{r_{ds2}}{v_{out}} \left(\frac{1}{r_{ds1}} + \frac{1}{r_{ds2}} + g_{m2} \right)$$

$$r_{out} = \frac{v_{out}}{i_{out}} = \frac{v_{out} r_{ds1}}{v_d}$$

$i_{out} = v_d / r_{ds1}$

$$= v_{out} r_{ds1} \frac{r_{ds2}}{v_{out}} \left(\frac{1}{r_{ds1}} + \frac{1}{r_{ds2}} + g_{m2} \right)$$

$$= r_{ds2} + r_{ds1} + g_{m2} r_{ds1} r_{ds2}$$

Summary: The Cascoded Current Source

- A cascode MOS stabilizes the drain voltage of the current source
- The output resistance increases by a *factor* $g_{m2}\, r_{ds2}$
  - This is the 'intrinsic gain' of M2
  - It is typically >20 (depending on geometry and current)
- The cascode bias voltage should be chosen such that the current source is *just above* the *edge* of saturation
- The overall saturation voltage of the cascoded source is ~ 2 times the 'unit' saturation voltage
- For advanced circuits, see the exercises!

Design Goals for Current Sources

- High output resistance
  - large L, cascode, regulation
- Low saturation voltage
  - large W, optimal biassing
- Matching
  - Same Drain voltages (and of course same geometries)
- Speed (sometimes)
  - small devices, high current

Advanced Current Source Circuits

- See Exercises

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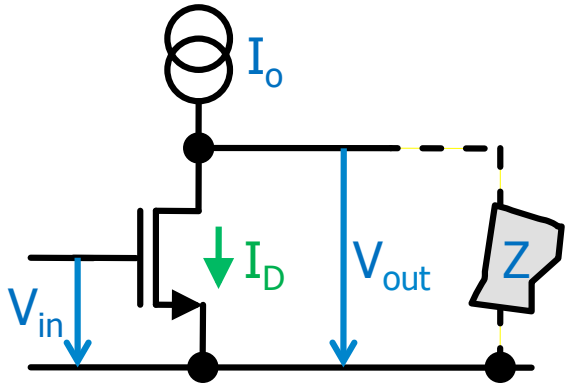
THE GAIN STAGE (COMMON SOURCE AMPLIFIER)

The Gain Stage

- The current in the MOS is set by the (large signal) $V_{GS} = V_{in}$
- We assume for now that this current is coming from an *ideal* voltage source sourcing I_o
- In the operation point, V_{GS} and I_o must 'correspond'!



- When V_{in} raises (above the op. point)
  - I_D increases. It becomes > I_0
  - Current is pulled out of the load
  - V_{out} drops
- When V_{in} drops
  - I_D decreases. It becomes < I_0
  - Current is pushed into the load
  - V_{out} increases

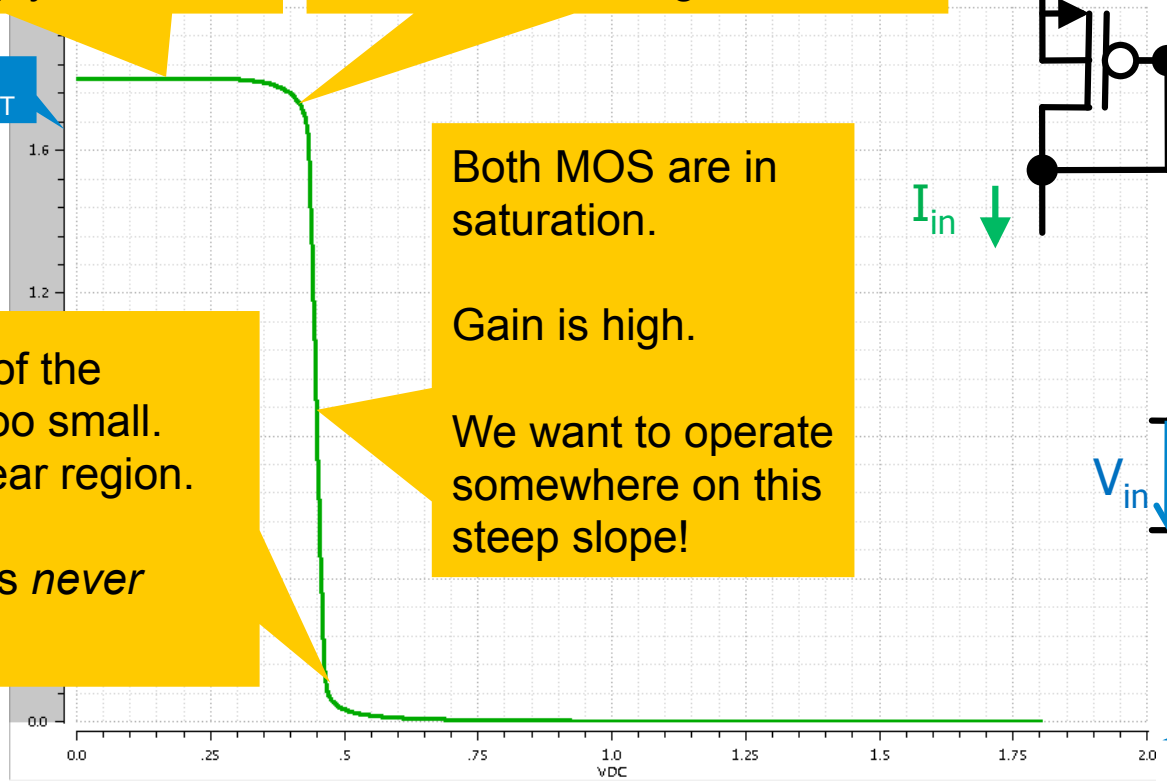
Inverting amplifier

Large Signal Behavior

- Use real current source now (PMOS mirror)
- Observe the 4 main operation regimes:

V_{in} is below NMOS threshold. No current in NMOS. PMOS can pull the output all the way to the positive supply 'VDD'

The NMOS starts to draw current. The PMOS is in the linear region, its output resistance is low, gain is low.

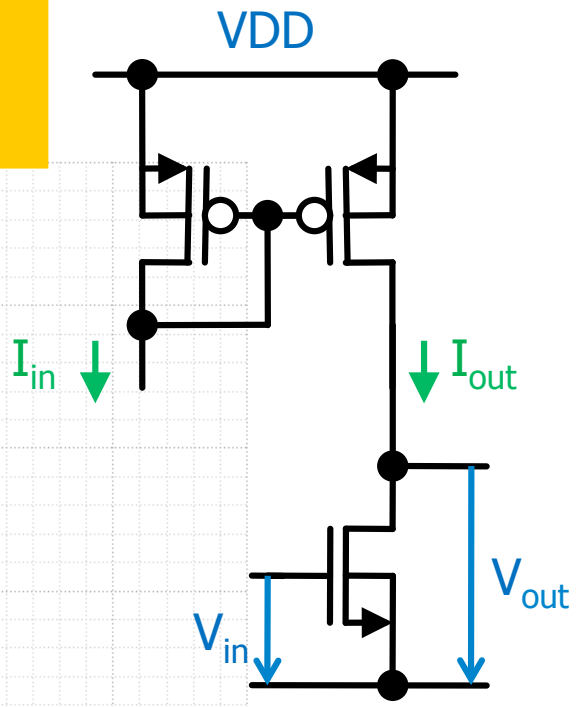


Both MOS are in saturation.

Gain is high.

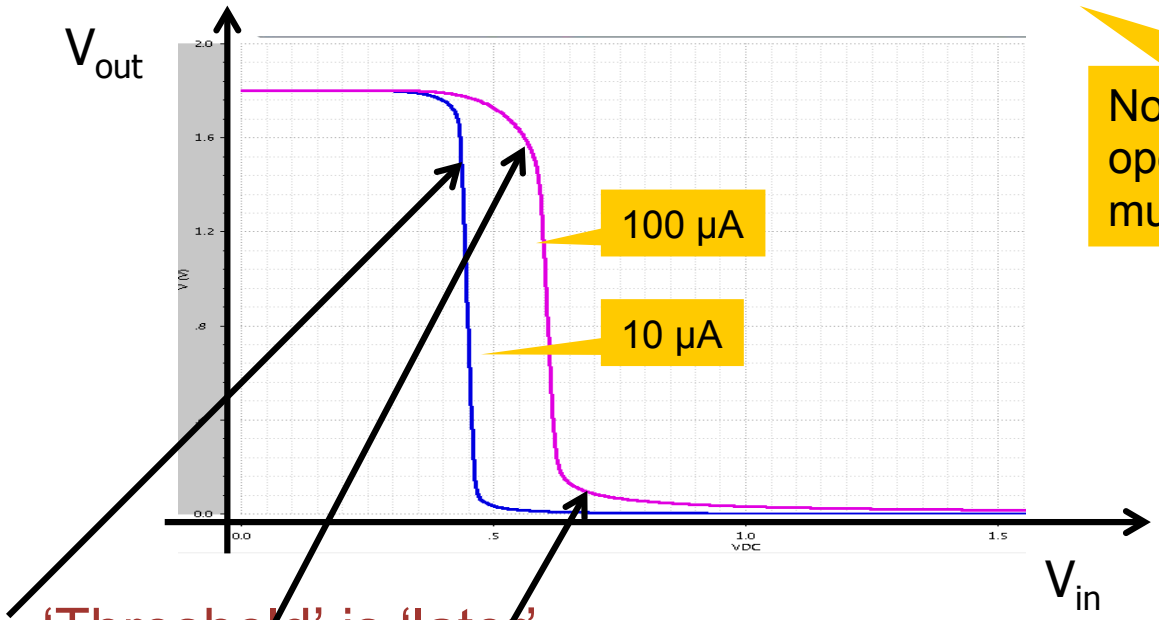
We want to operate somewhere on this steep slope!

The drain voltage of the NMOS becomes too small. It goes into the linear region. Gain drops. Note that $V_{out} = 0$ is *never* reached



Changing the Bias Current

- More Bias Current ('stronger current source')

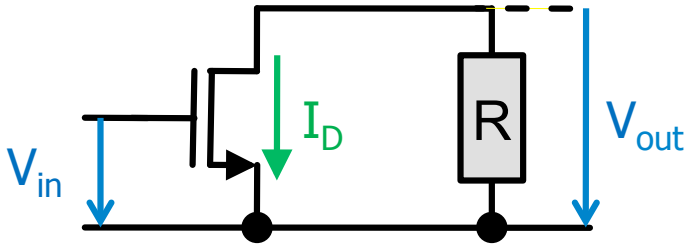


Note that the DC operation point of V_{in} must be adjusted!

- 'Threshold' is 'later'
  - V_{IN} must be higher until I_D reaches 100µA
- 'Round region' is wider
  - **P**MOS is longer in linear region because V_{GS} is higher
- Output does not go so low (all the way to GND)
  - NMOS cannot deliver enough (relative to 100µA) current, it comes into the linear region

Gain of the Gain Stage: Intuitive Way

- When V_{in} changes by a small amount $\Delta V_{in} = v_{in}$, how much does V_{out} change, i.e. what is v_{out}?
  - Note difference in Capital and Small letters: $V_{in} \neq v_{in}$

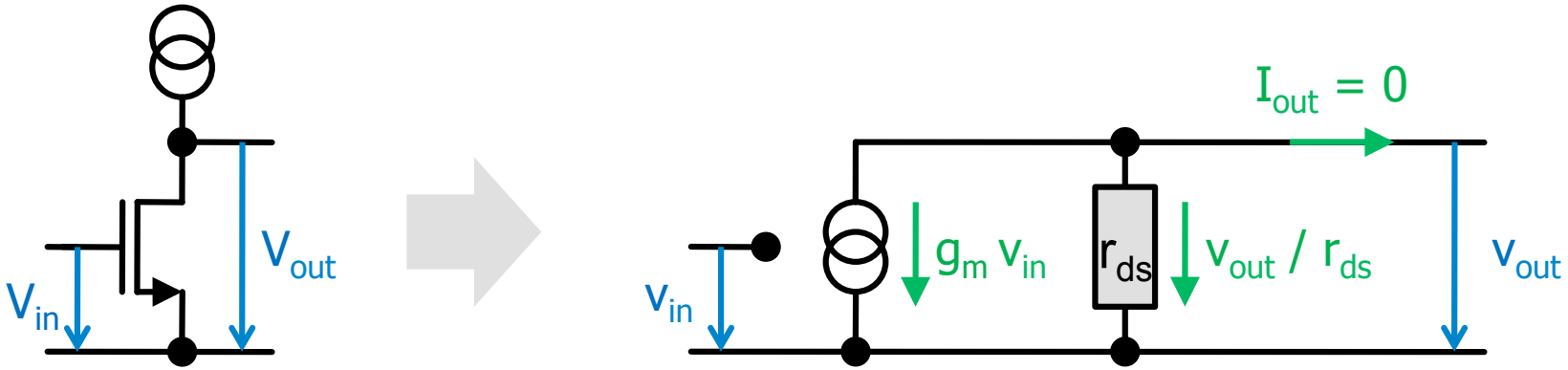


- What happens?
  - v_{in} leads to a change i_D of I_D of $\mathbf{i_D = g_m\ v_{in}}$ (Definition of g_m!)
  - With a resistive load R, this gives a voltage change $\mathbf{v_{out} = R \times i_D}$
  - This change is opposite in direction to v_{in}
  - Therefore: $v_{out} = - R \times g_m \times v_{in}$

$$\text{gain } v = v_{out}/v_{in} = - R \times g_m$$

Gain of the Gain Stage: Small Signal Calculation

- Consider only the MOS
- Replace it by its small signal equivalent:



- Calculation
  - current at output node = 0 (Kirchhoff)
  - therefore: $0 = g_m \times v_{in} + v_{out} / r_{ds}$
  - so that, again

$$v = v_{out}/v_{in} = - g_m \times r_{ds}$$

Numbers

- Typical gains are 10 ... 40
  - they depend on technology, current, transistor size,...

- Therefore: $|v| = g_m r_{ds} = g_m / g_{ds} > 10 >> 1$

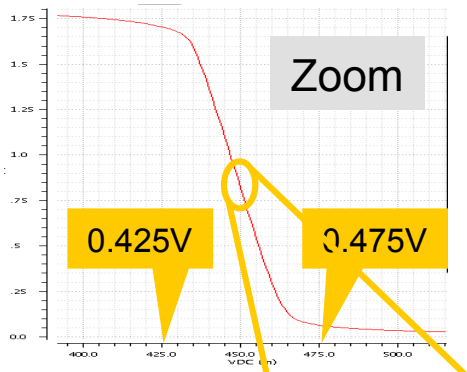
  or $g_m > 10 / r_{ds} = 10\, g_{ds}$

The transconductance g_m of a MOS is usually much larger than the output conductance g_{ds}.

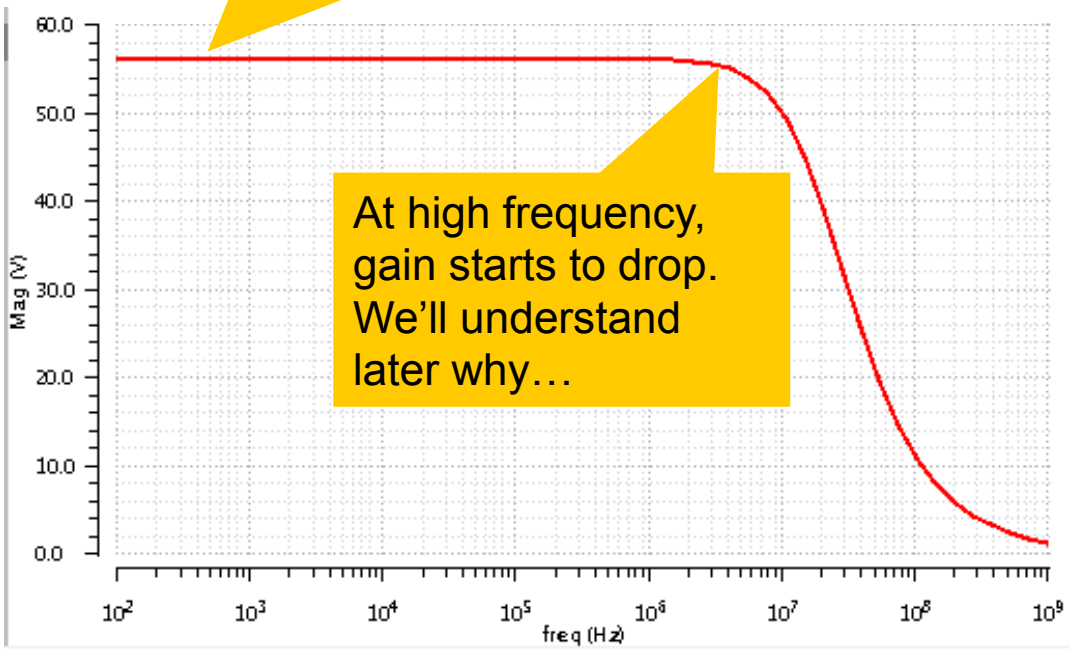
- This can often be used to simplify small signal expressions!

AC Sweep

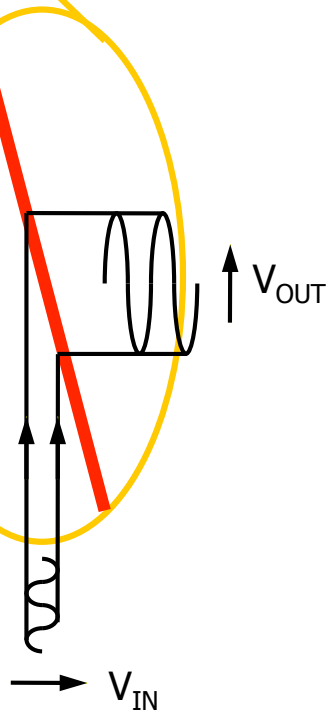
- Chose the DC potential of the input such that we are in the steep part (here: 0.45V):



Here we are in the steep part
Gain = 56

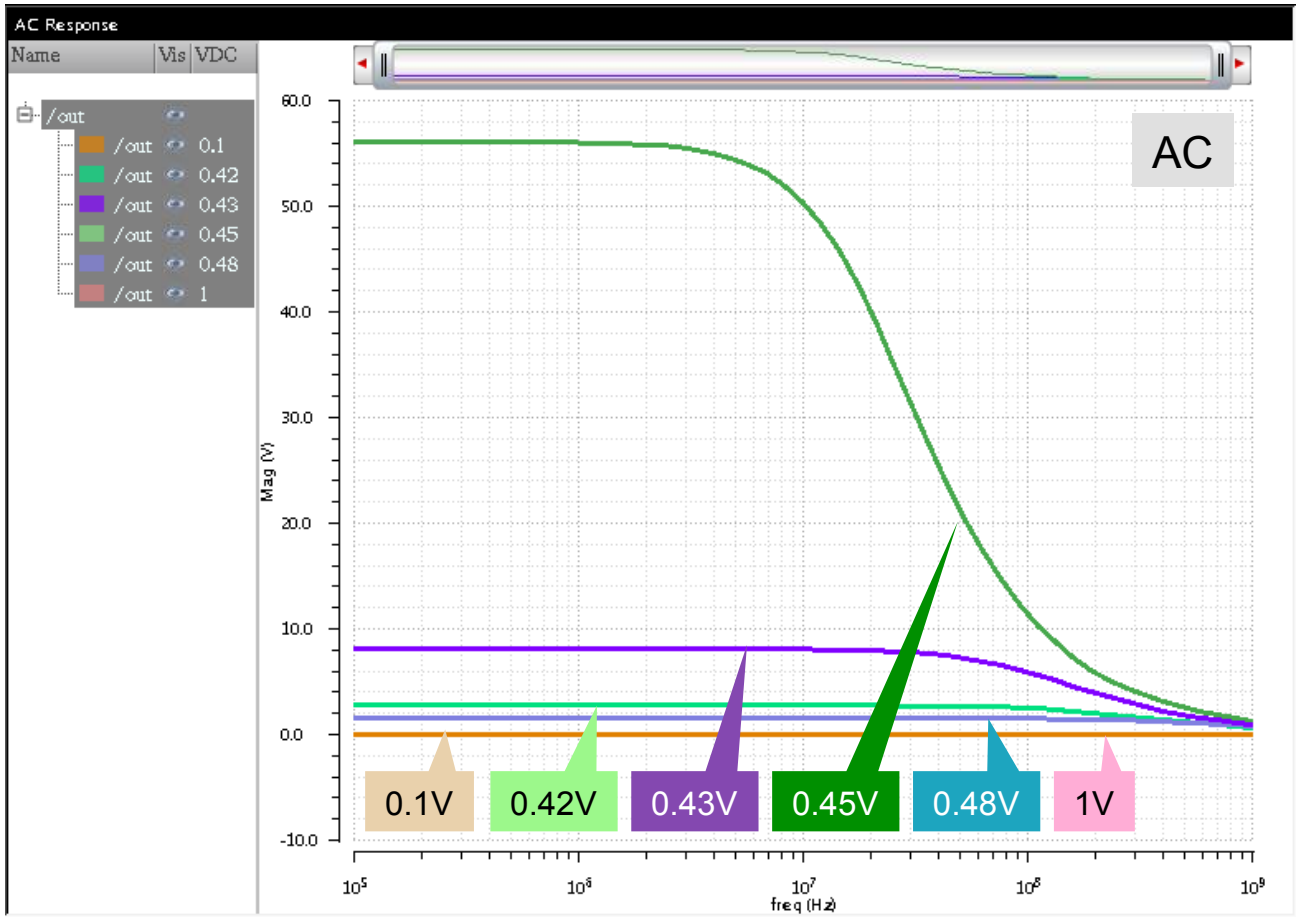


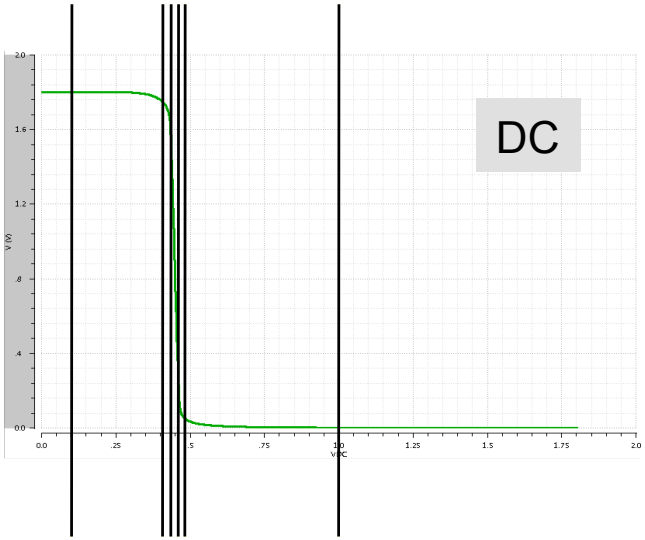
At high frequency, gain starts to drop. We'll understand later why…



Change of Operation Point

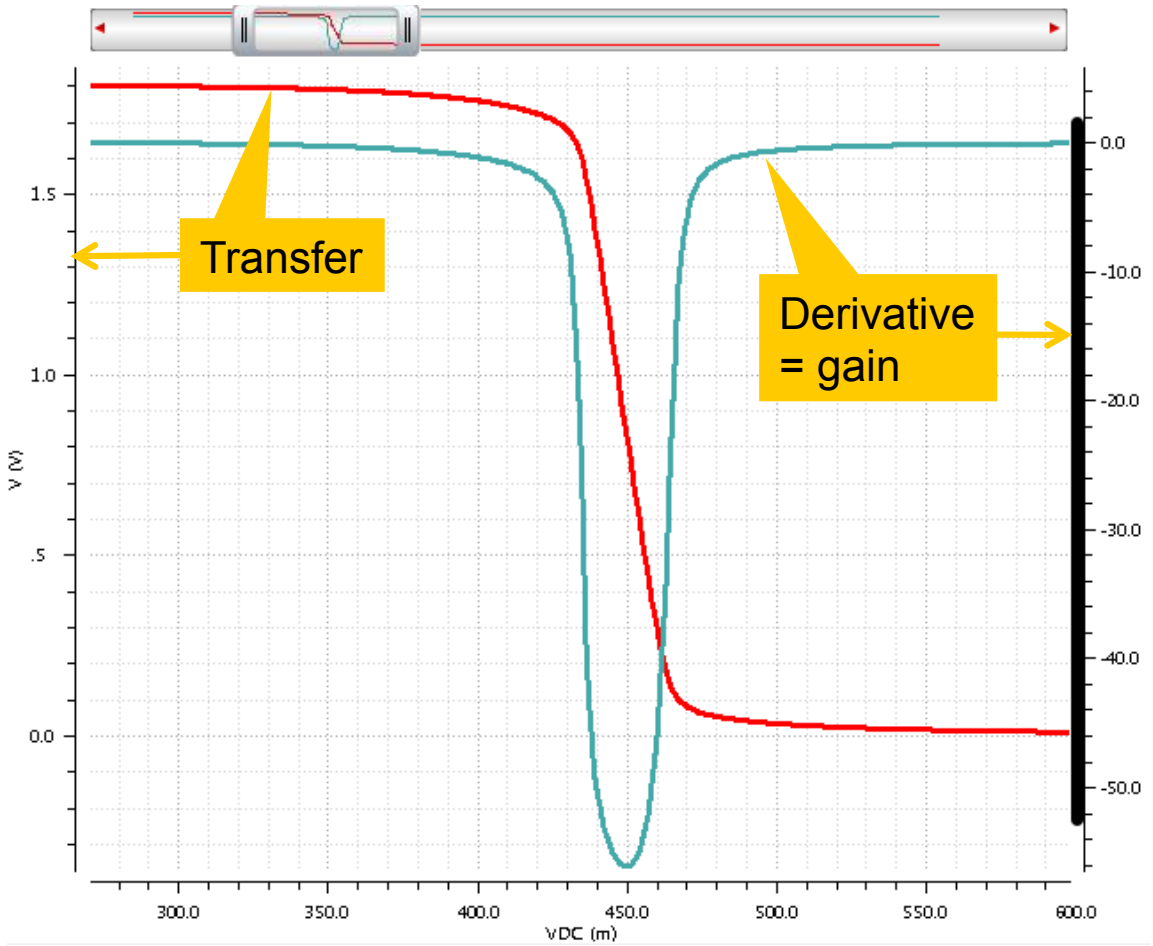
- It the DC potential of V_{IN} is changed, we move to different points of the transfer curve:





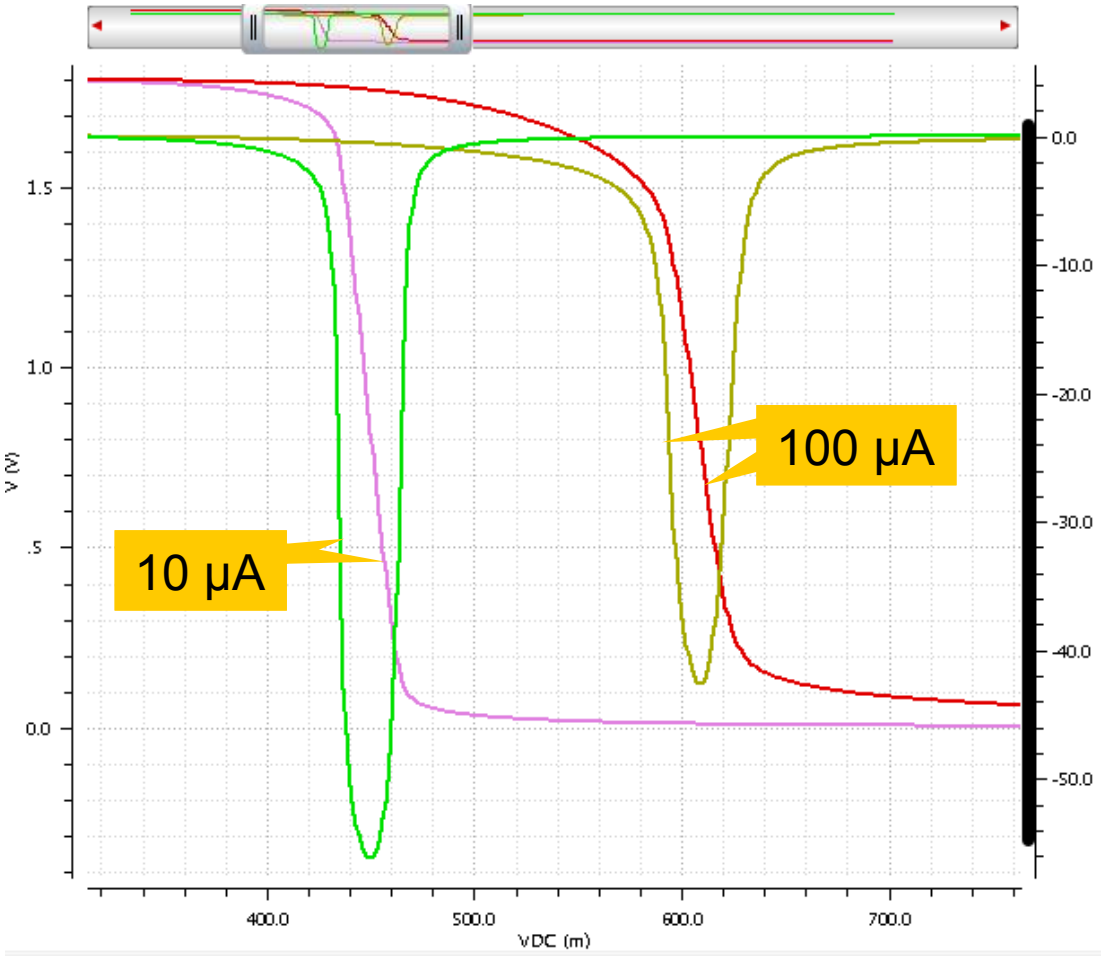
Gain vs. V_{IN}

- Can be obtained by taking derivative of transfer curve



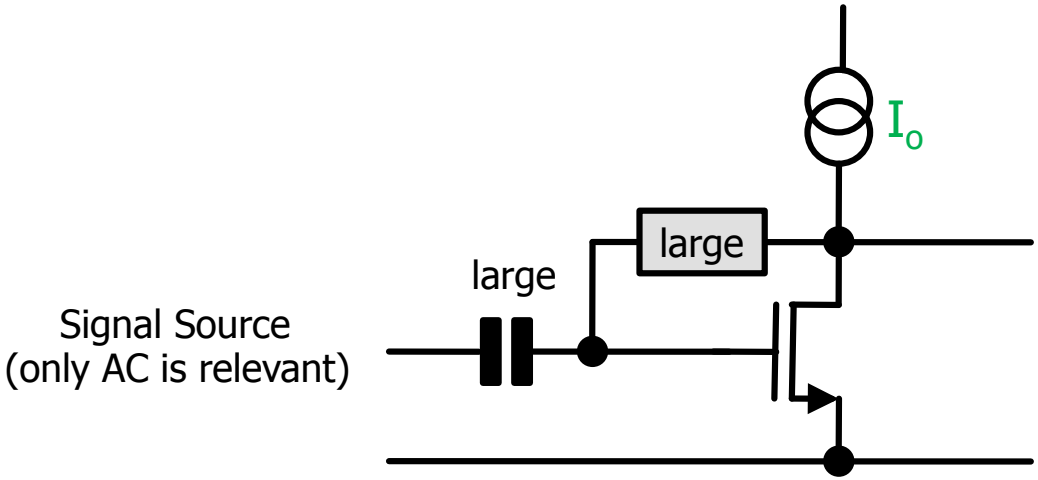
Gain at Different bias Currents

- Position of ‘maximal gain’ *depends on bias current*
- Max. gain is lower for high current



Biasing the Gain Stage

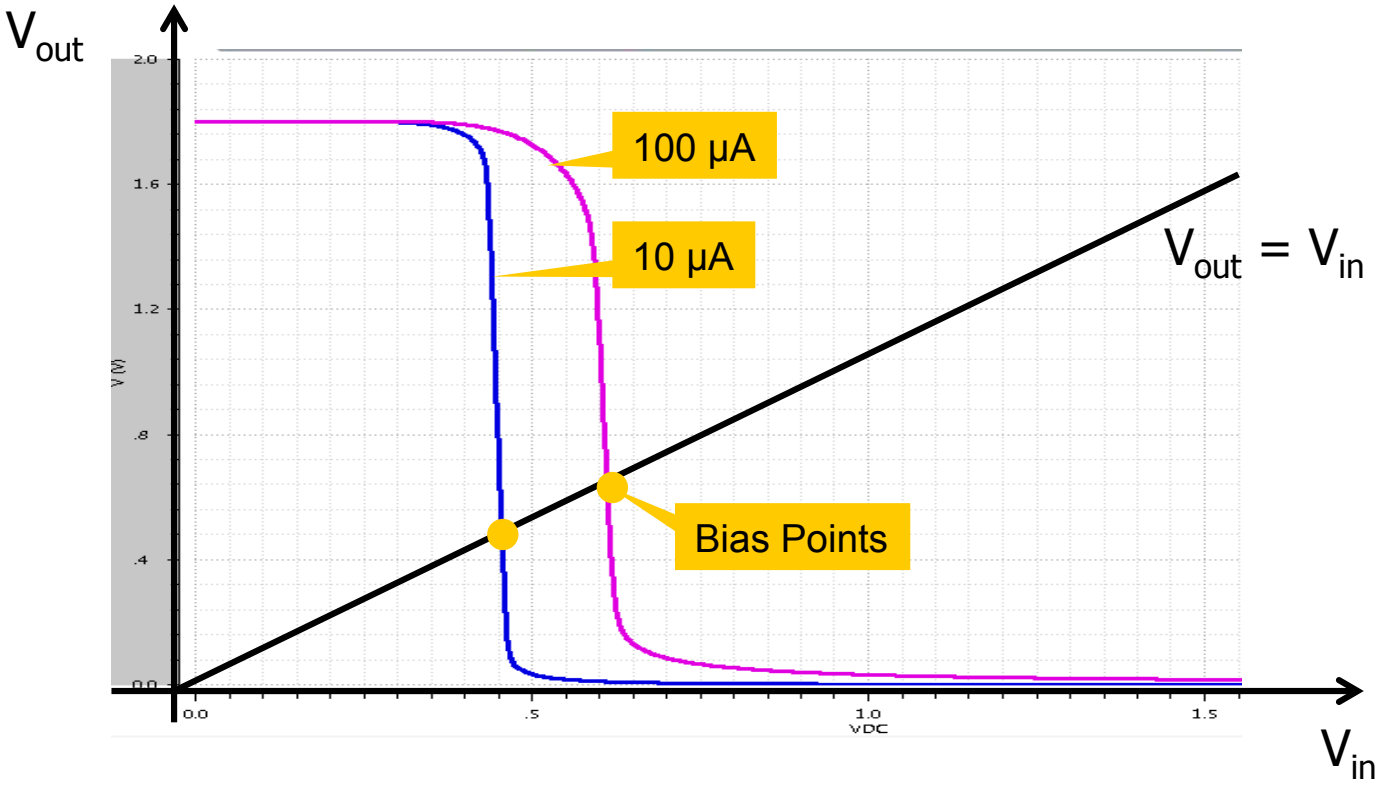
- In practice (& in simulation), V_{GS} and I_0 must 'correspond'
- This can be achieved (for instance) by a 'diode' connection of the MOS
- In simulation: To *let signals pass through*, the connection is done with a very large resistor and the input signal is ac coupled with an ‚infinite' capacitor.



- In practice, other methods can be used…

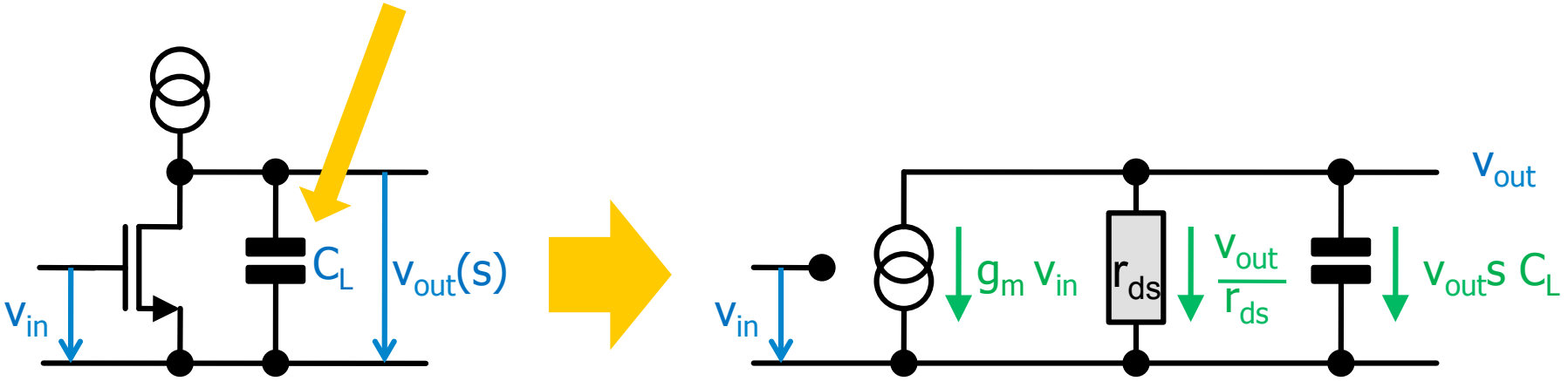
Another View on the Bias Problem

- The resistor forces $V_{out}=V_{in}$
- The operation point is the crossing between the *diagonal* and the *transfer characteristic*
- This is usually a good point (maybe a bit low...)
- This works 'automatically' for changing bias & geometry



Adding a Capacitive Load – 'The Speed'

- With a capacitive load, we have another current path:



- Current sum at output node = 0:
  $0 = g_m\, v_{in} + v_{out} / r_{ds} + s\, C_L\, v_{out}$

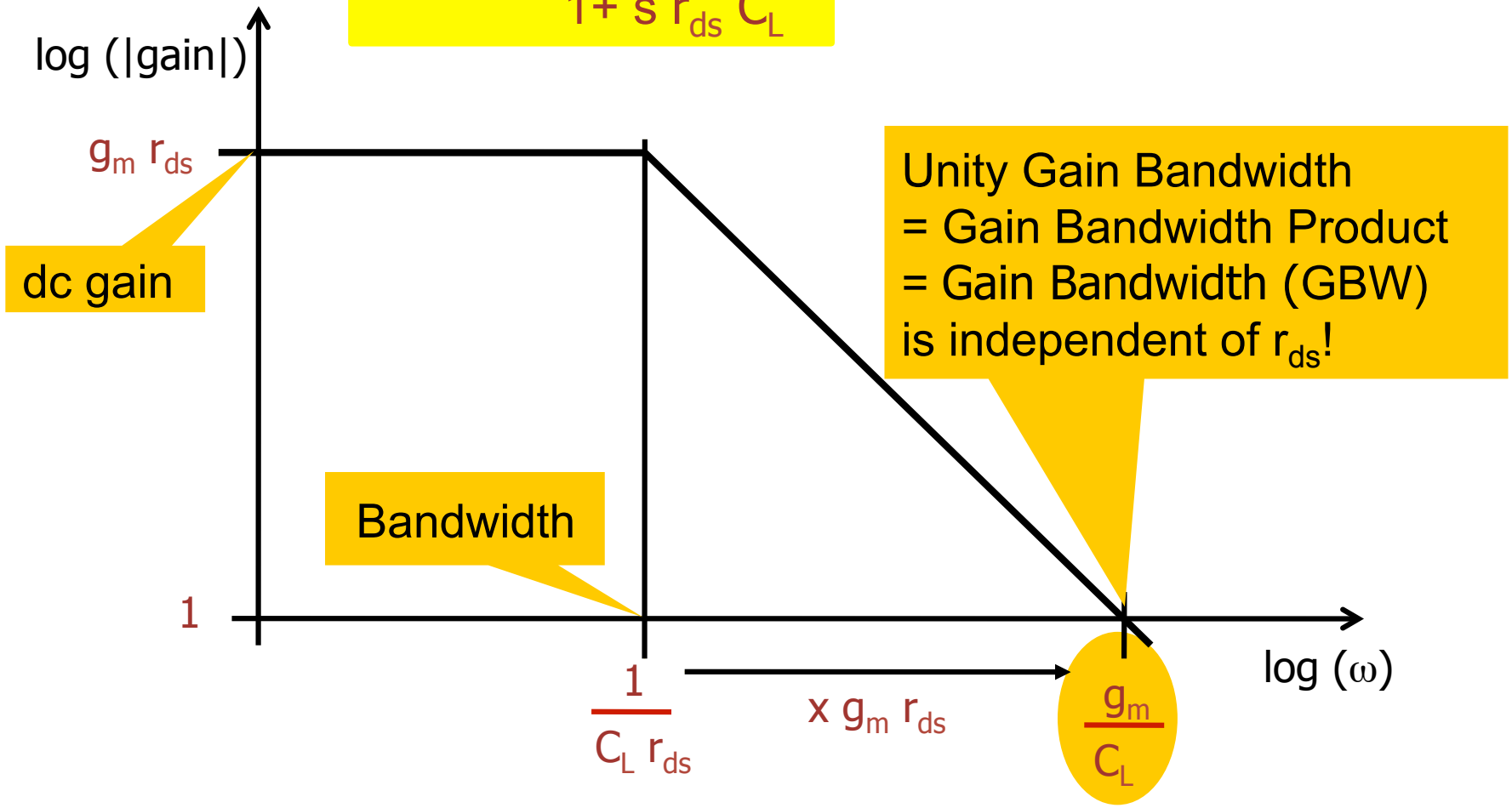
$$v(s) = -\frac{g_m\, r_{ds}}{1 + s\, r_{ds}\, C_L}$$

DC gain (as before)

Low pass behavior
Corner at $1/(r_{ds}\, C_L)$

Bode Plot of the Gain Stage

$$v(s) = -\frac{g_m\, r_{ds}}{1 + s\, r_{ds}\, C_L}$$



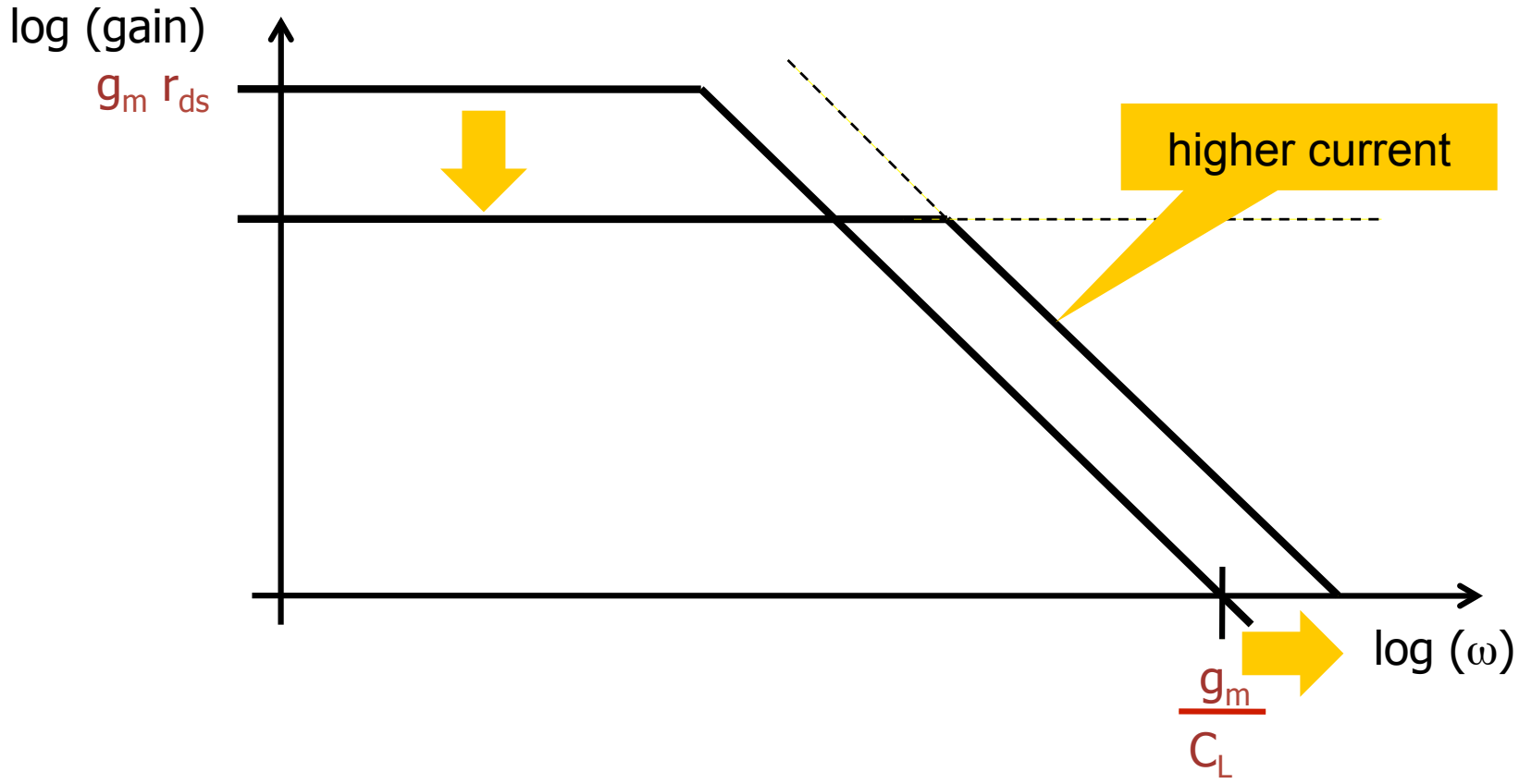
Remember: Gain-Bandwidth-Product

$$GBW = \frac{g_m}{C_L}$$

$$v = -\frac{g_m r_{ds}}{1 + s\, r_{ds} C_L}$$

Bode Plot for two current

- Increasing I_D
  - increases g_m and thus GBW
  - decreases r_{ds} and thus dc gain



Increasing the gain

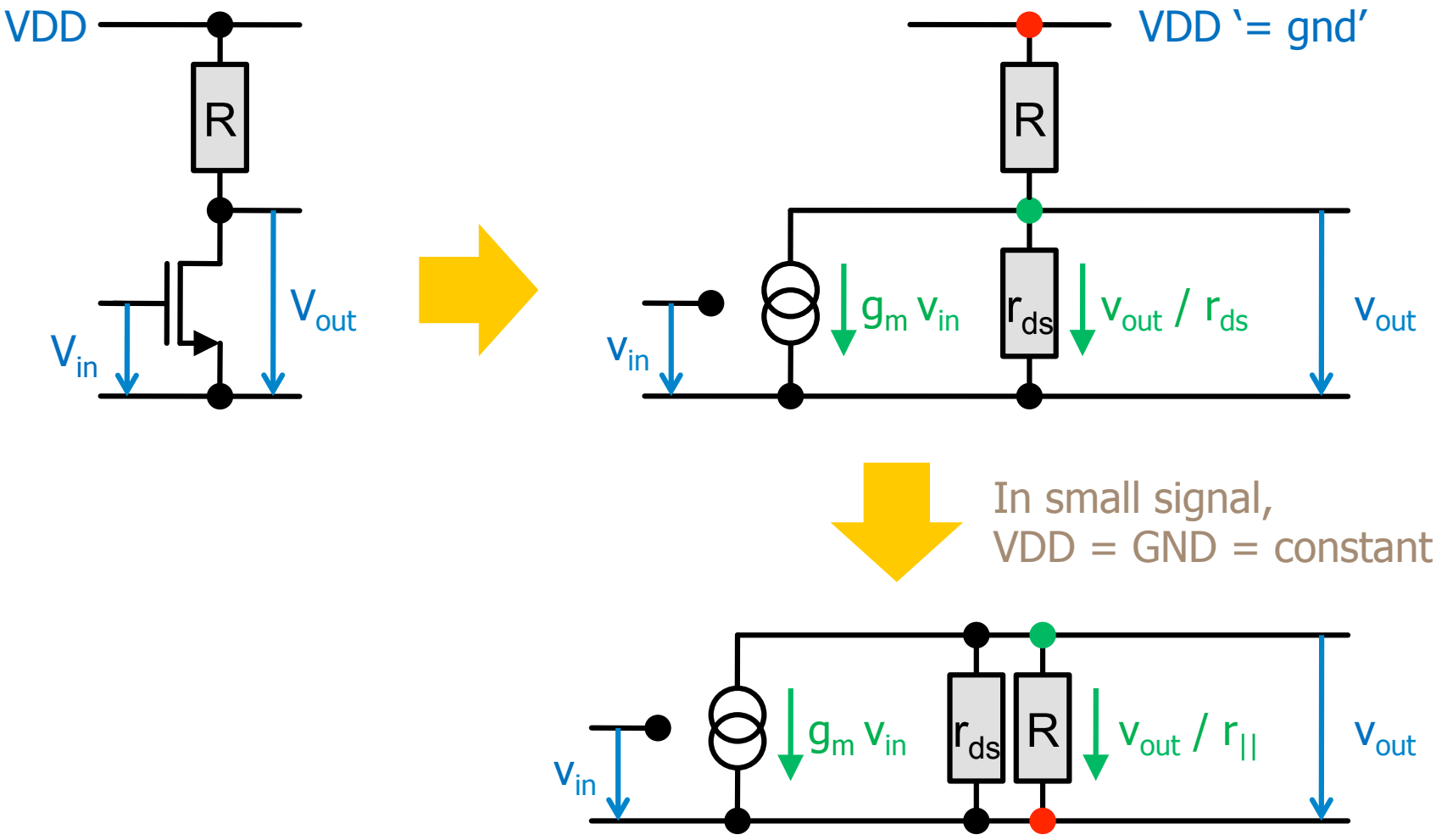
- The gain of a single MOS is $v = g_m r_{ds}$.

- $g_m \sim \mathrm{sqrt}[2 K I_D W/L]$ (strong inversion)
- $r_{ds} \sim L / I_D$

	$I_D \rightarrow 2 I_D$ (strong inv.)	$I_D \rightarrow 2 I_D$ (weak inv.)	$I_D \rightarrow 2 I_D$ (vel. sat.)	$W \rightarrow 2 W$ (s.i.)	$L \rightarrow 2 L$ (s.i.)
g_m	$\rightarrow \sqrt{2}\, g_m$	$\rightarrow 2\, g_m$	$\rightarrow g_m$	$\rightarrow \sqrt{2}\, g_m$	$\rightarrow g_m / \sqrt{2}$
r_{ds}	$\rightarrow r_{ds} / 2$	$\rightarrow r_{ds} / 2$	$\rightarrow r_{ds} / 2$	$\rightarrow r_{ds}$	$\rightarrow 2\, r_{ds}$
v	$\rightarrow v / \sqrt{2}$	$\rightarrow v$	$\rightarrow v / 2$	$\rightarrow \sqrt{2}\, v$	$\rightarrow \sqrt{2}\, v$

- We see:
  - gain is *increased* by *larger* W or L and by *smaller* I_D
  - *gain*-bandwidth only depends on g_m, i.e. mainly on I_D

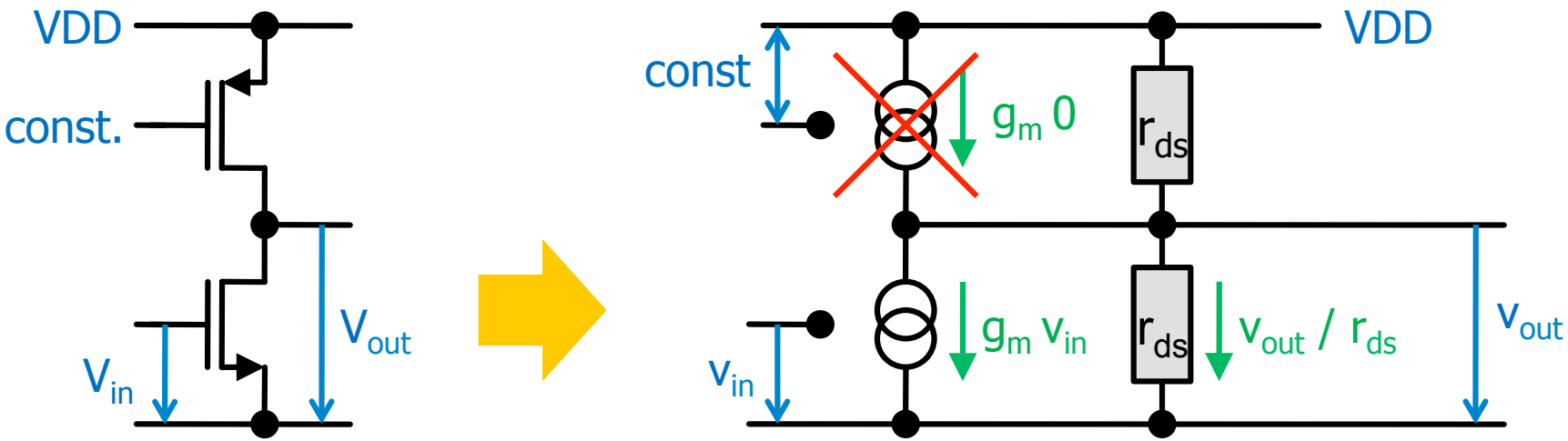
How about a Resistive Load?



→ R and r_{ds} act **in parallel: $v = - g_m \times (r_{ds} \,||\, R)$**

Non-Ideal (PMOS) current source

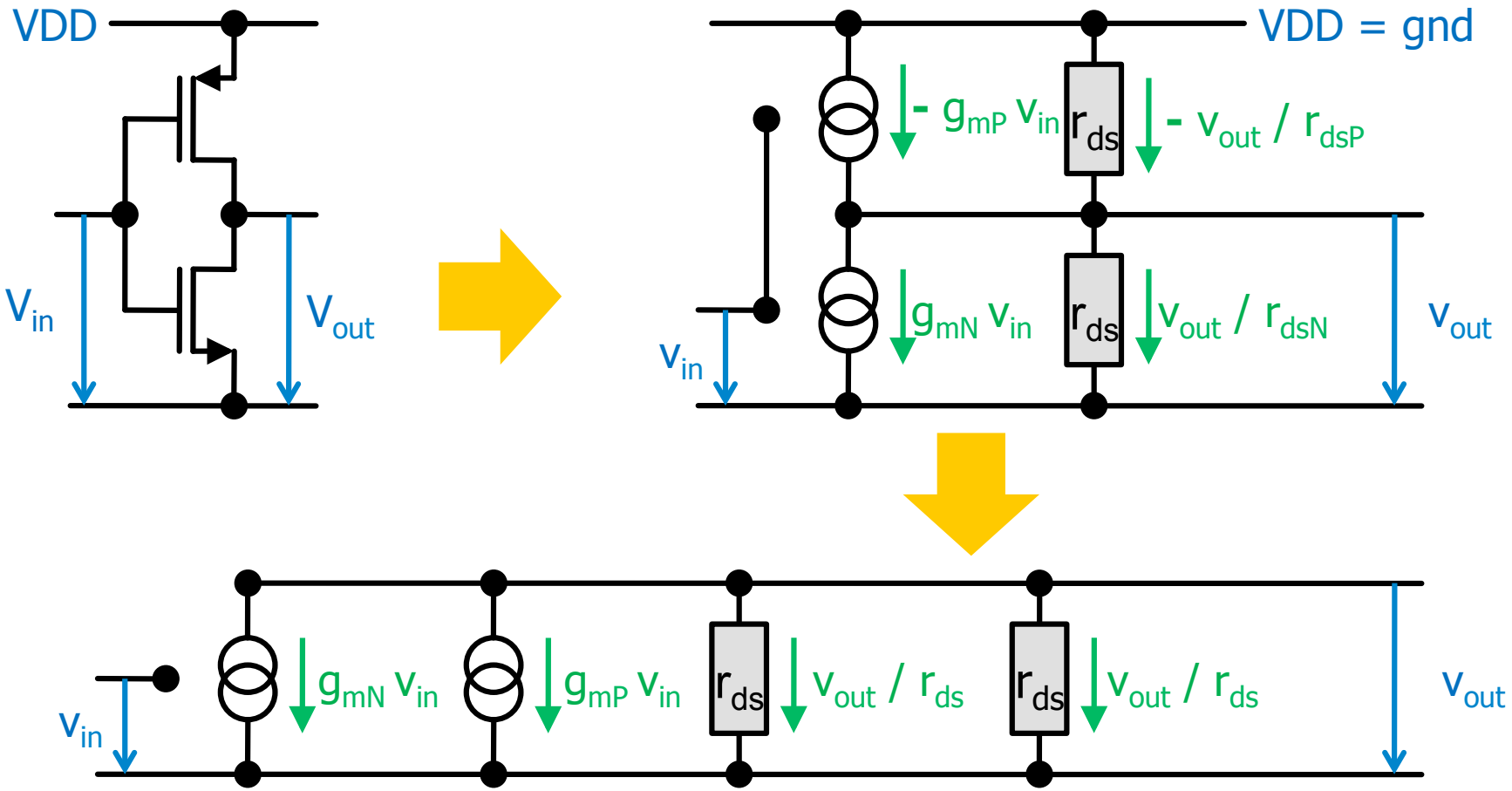
- When a PMOS is used as current source, it ALSO has an output resistance.



- The transconductance part of the PMOS is off (v_{gs} = 0)
- The PMOS behaves just like a pure resistor (but r_{ds} is usually higher when in saturation)

CMOS Inverter

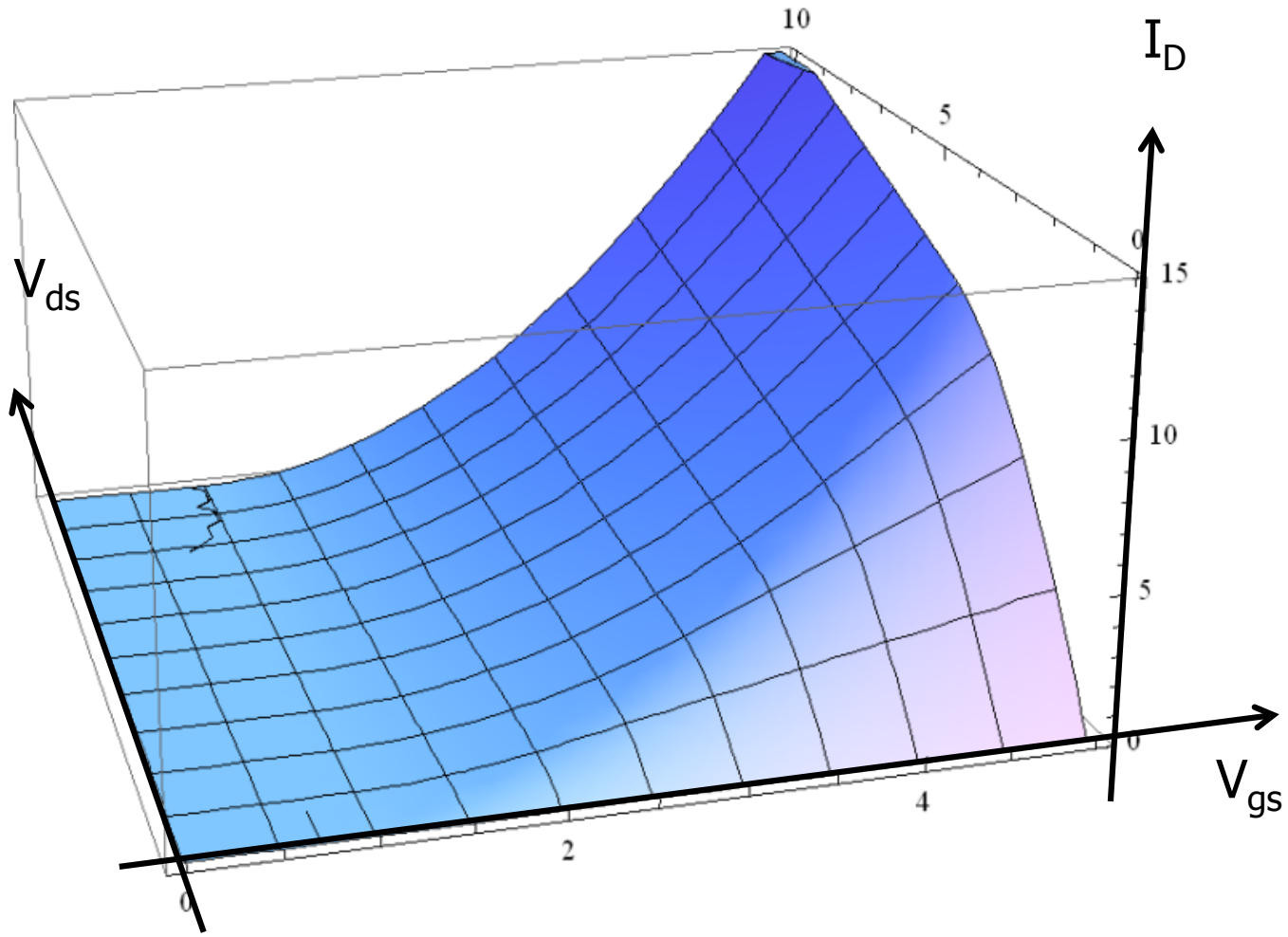
- Now consider a CMOS inverter:



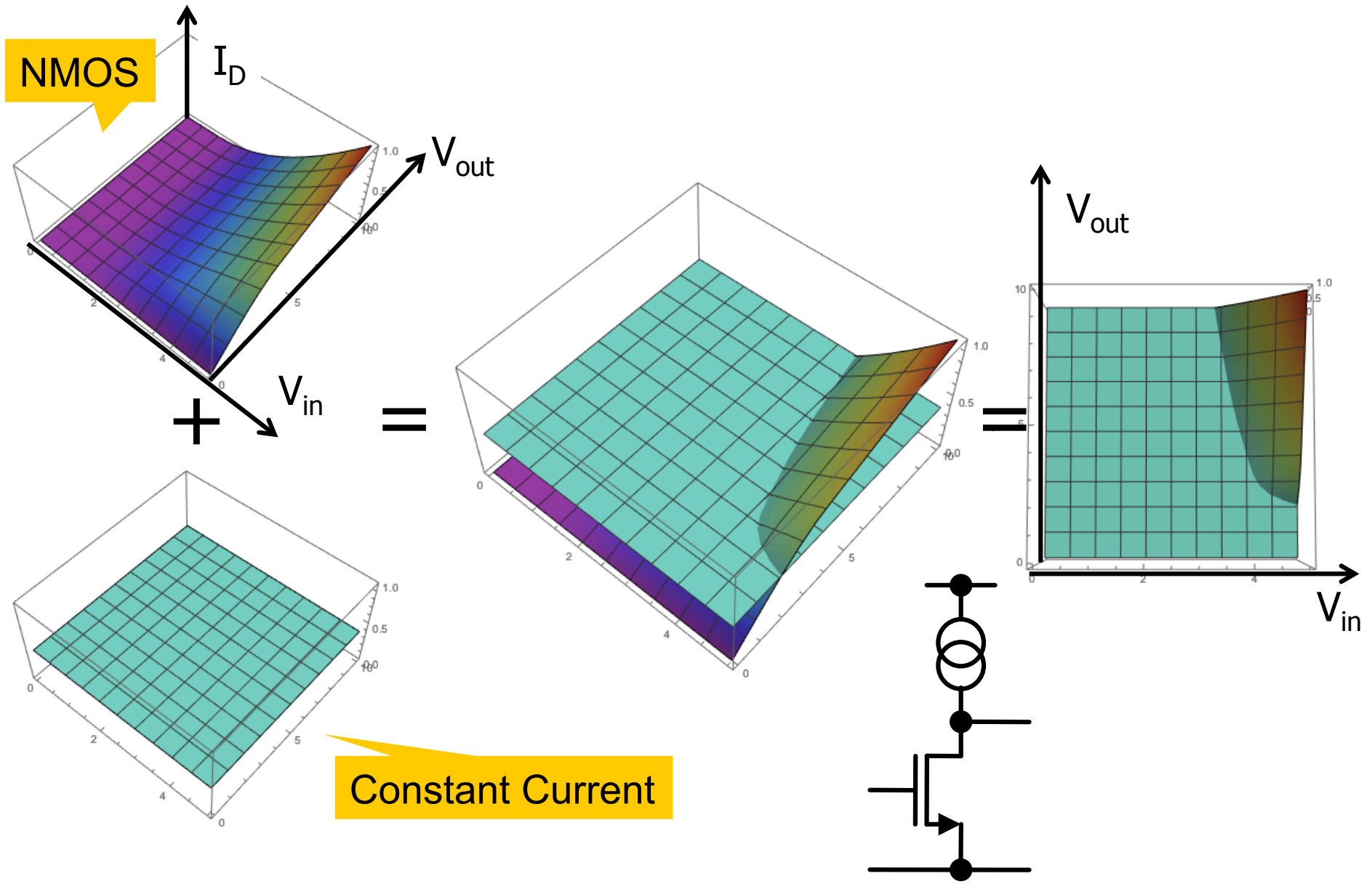
- g_m and r_{ds} of both MOS are in **parallel**

  $\mathbf{v = -(g_{mN} + g_{mP}) \times (r_{dsN} \,||\, r_{dsP})}$

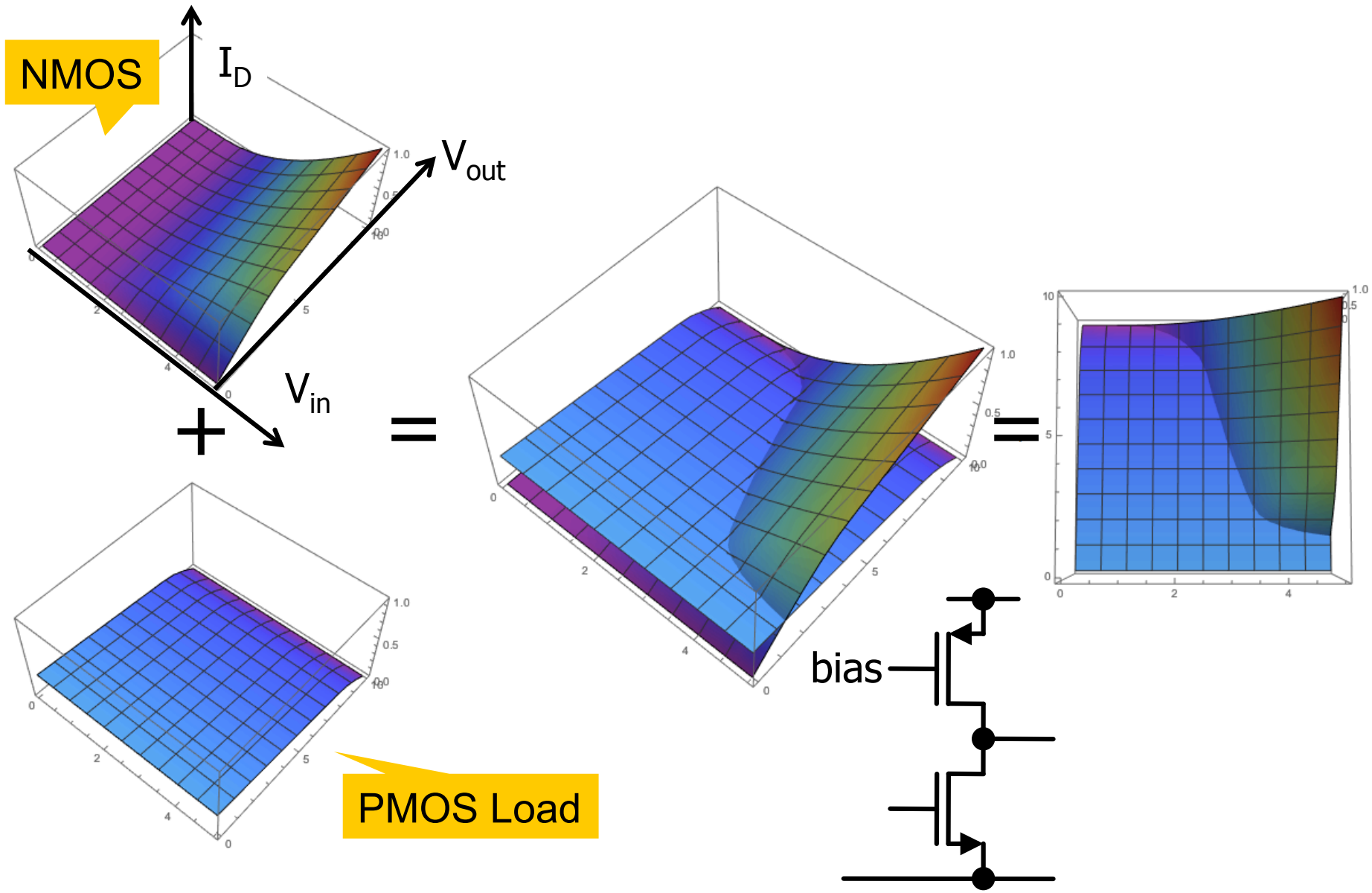
Reminder: Transistor Characteristics



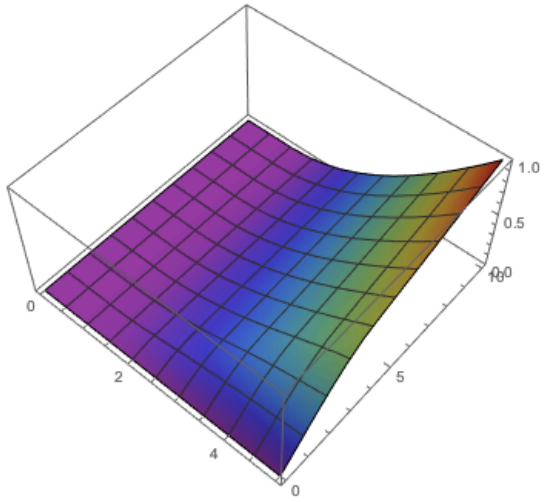
Visualization of Transfer Function: I-Load

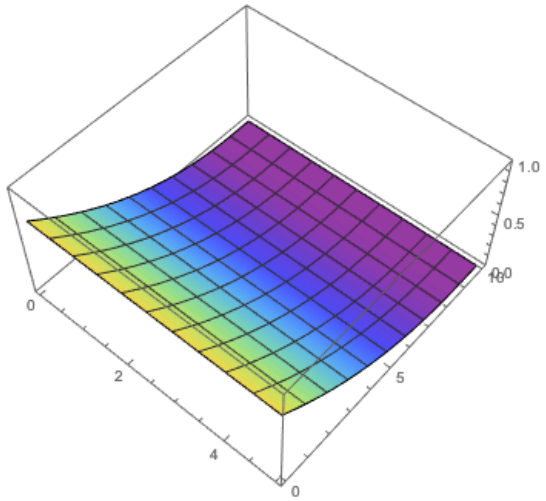


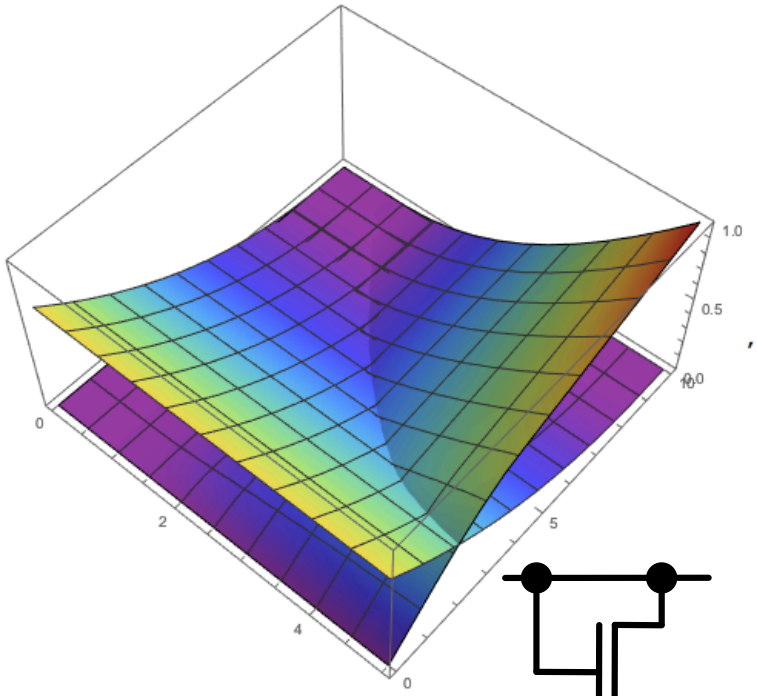
Visualization of Transfer Function: PMOS Load

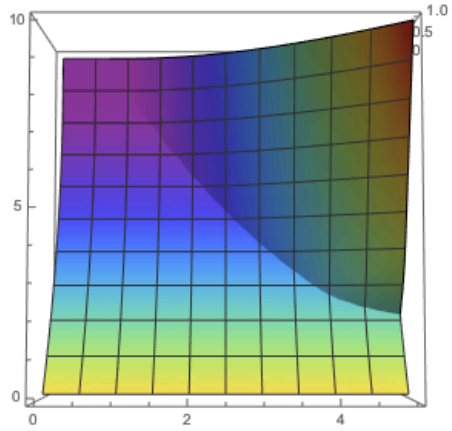


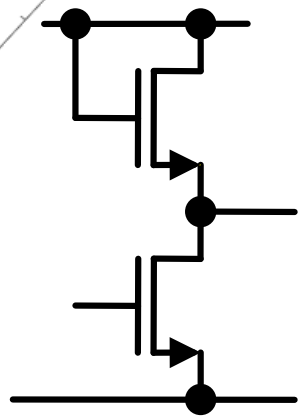
Load = Diode Connected (N)MOS



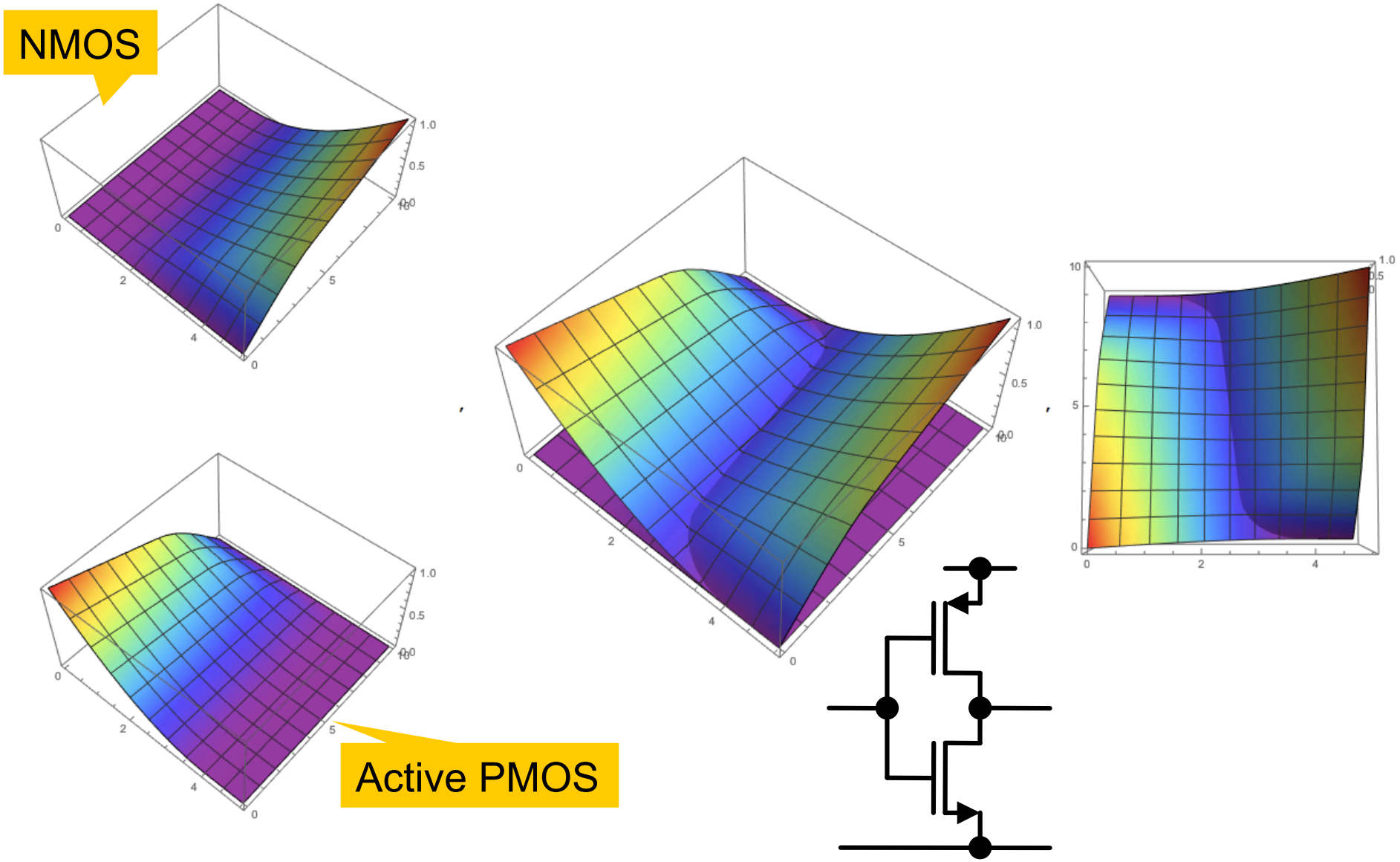






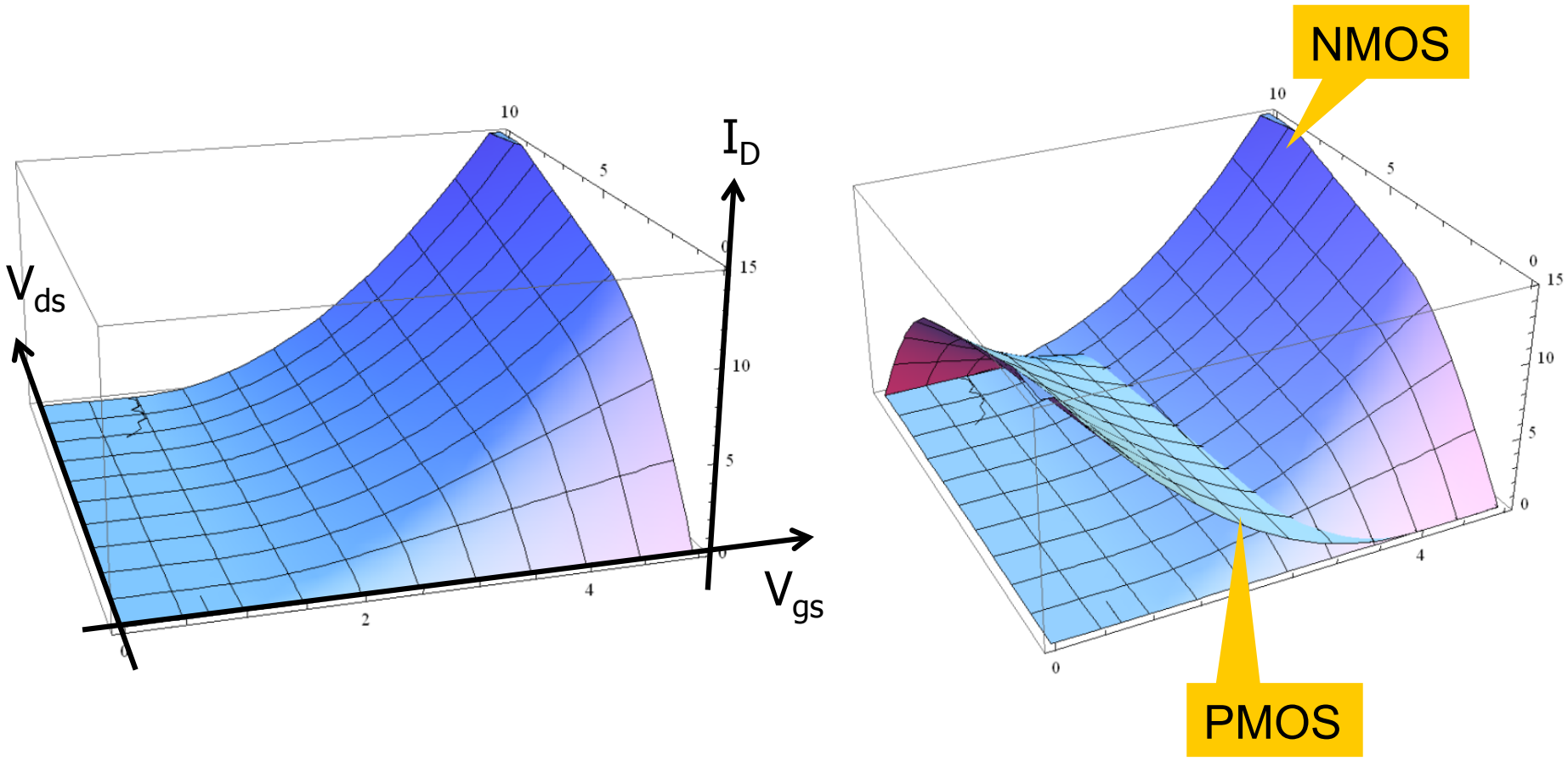


Visualization of Transfer Function: Inverter



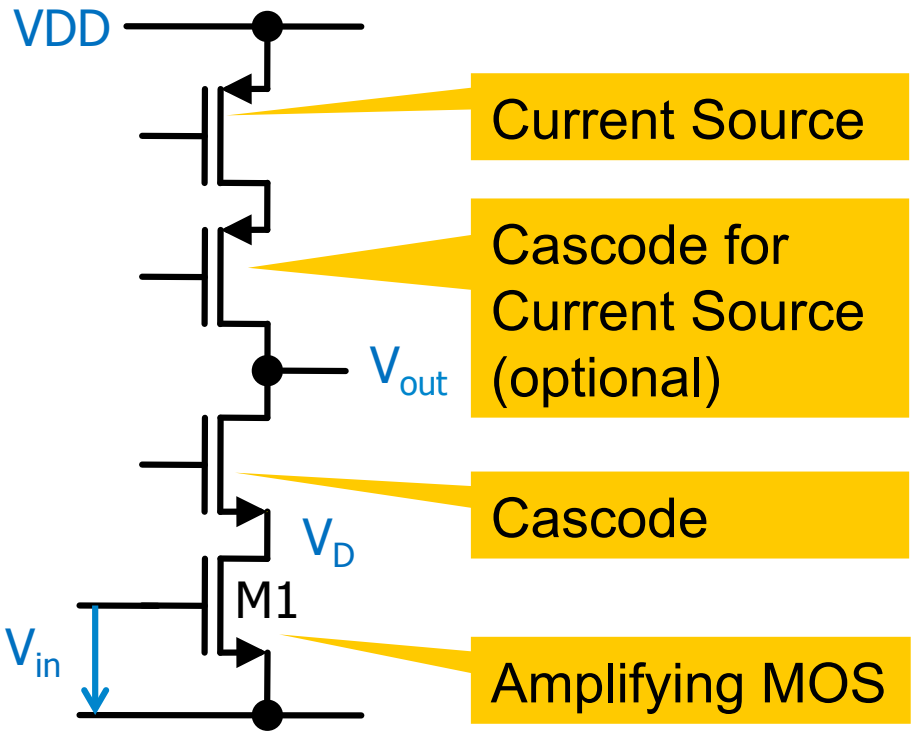
Visualization of Inverter Transfer

- $I_D(V_{gs},V_{ds})$



How to get very high gain ?

- g_m is very much limited by the current
- r_{ds} can be increased by a cascode
- 'Straight' cascode gain stage:



Defines Current

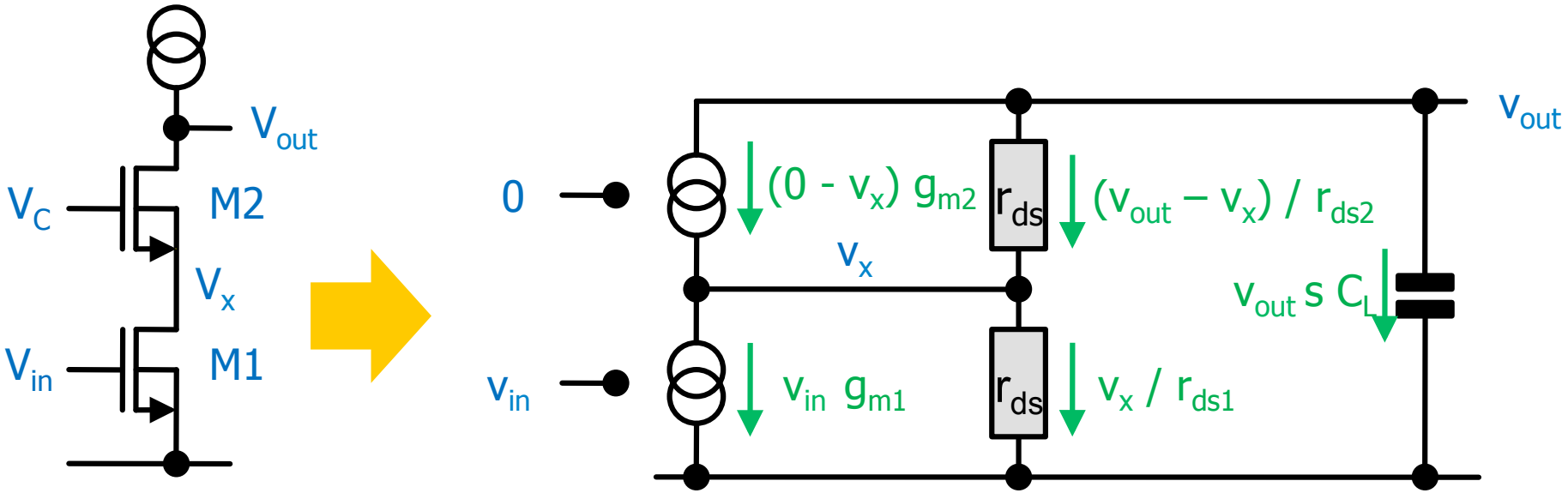
Increase output
Resistance of PMOS

Fix V_D so that changes
In V_{out} do not lead to
current change in M1

Convert input voltage
change to current change

Small Signal Analysis

- Assume bulks are connected to sources (no substrate effect)
  - Not always true in reality when NMOS are used...



- EQ1 (current sum at node v_{out}):

  $-v_x\ g_{m2} + (v_{out}-v_x)/r_{ds2} + v_{out}\ s\ C_L = 0$

- EQ2 (current sum at node v_x):

  $-v_x\ g_{m2} + (v_{out}-v_x)/r_{ds2} = v_{in}\ g_{m1} + v_x/r_{ds1}$

Solution

- $H(s) = -\dfrac{gm1\ rds1\ (1 + gm2\ rds2)}{1 + CL\ (rds1 + rds2 + gm2\ rds1\ rds2)\ s}$

- As usually $g_m\ r_{ds} \gg 1$, the parenthesis can be simplified:

- $H(s) \sim -\dfrac{gm1\ rds1\ gm2\ rds2}{1 + CL\ gm2\ rds1\ rds2\ s}$ (= single pole low pass)

- The *DC gain* is $|H(0)| = g_{m1}\ r_{ds1} \times g_{m2}\ r_{ds2}$

  (i.e. *squared* wrt. a simple gain stage!)

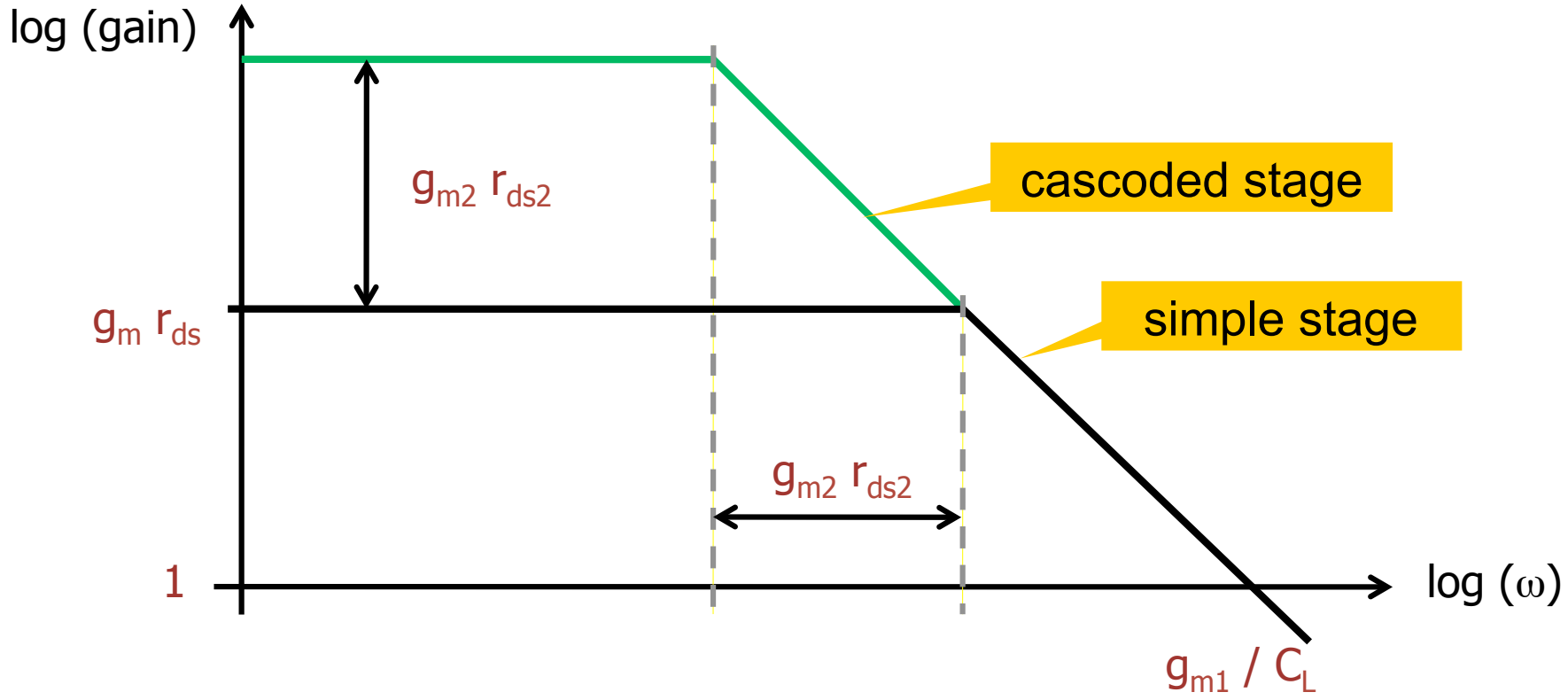
- The bandwidth is $BW = (C_L\ r_{ds1} \times g_{m2}\ r_{ds2})^{-1}$

  (decreased by same factor)

- The unity gain bandwidth is (**same** as simple stage!) $GBW = BW \times |H(0)| = g_{m1}/C_L$

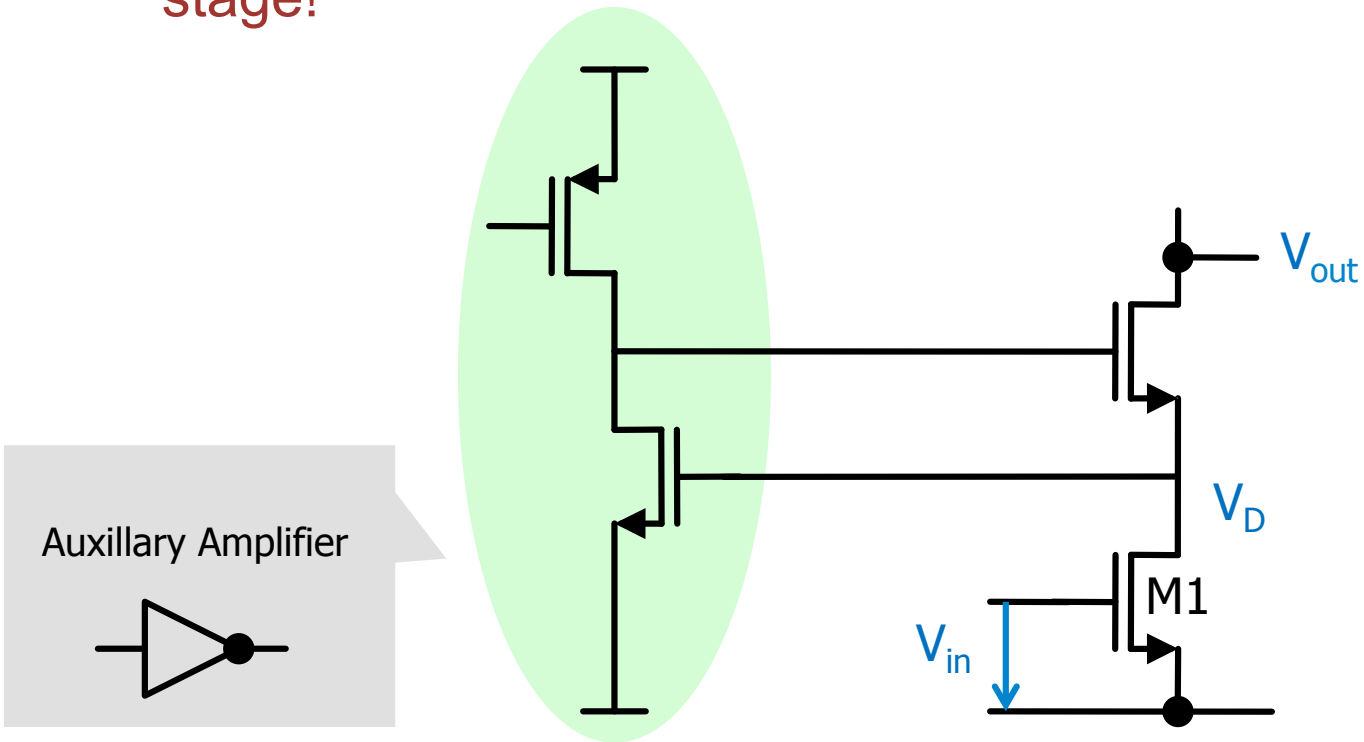
Comparing Simple / Cascoded Gain Stage

- DC gain is increased by the 'gain' $g_m \times r_{ds}$ of the cascode
  - the cascode 'boosts' the output resistance
- The GBW remains unchanged
  - the current generated in M1 must charge C_L. The cascode does not help here...



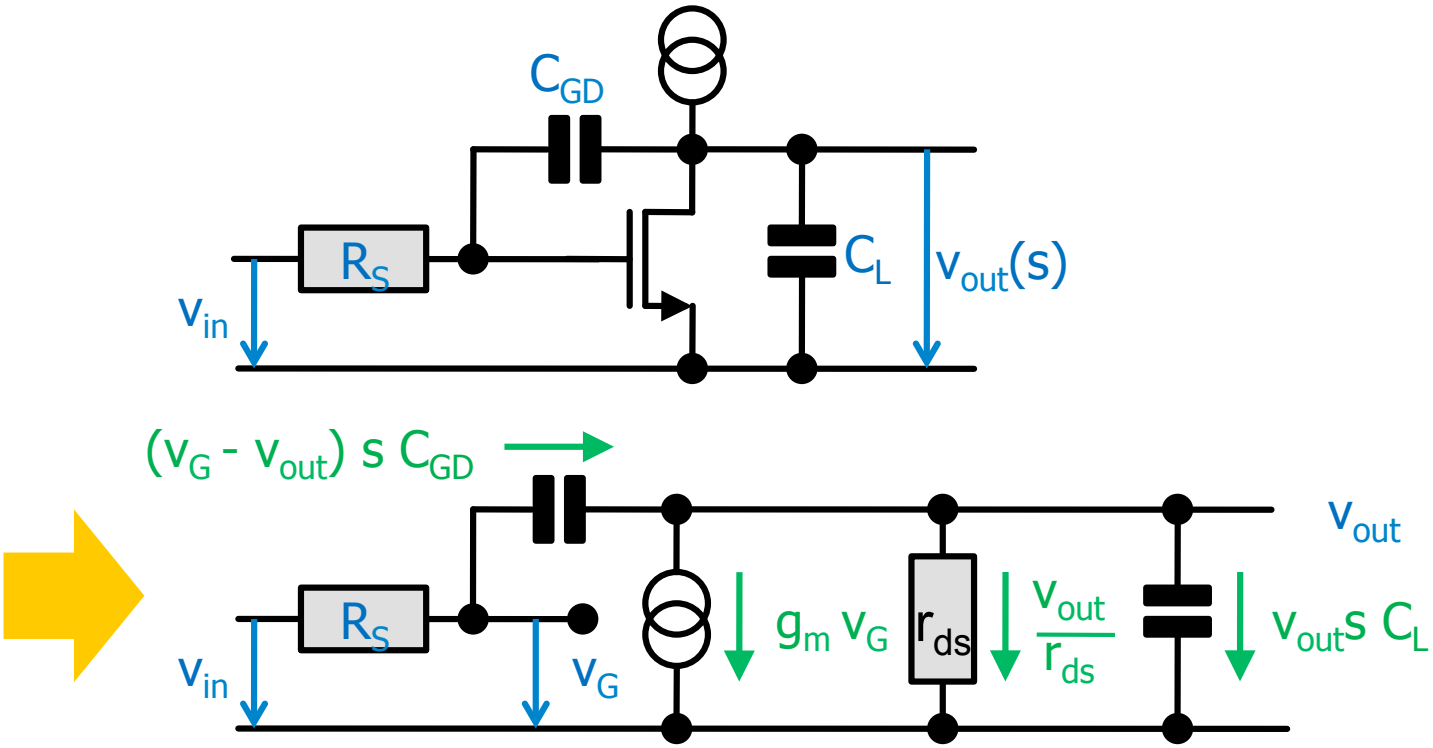
How to get EVEN higher gain ?

- Just like we have done in the 'regulated' mirror, we can use an amplifier to keep the drain of the amplifying MOS at constant potential.
- For the amplifier, we use (again) a simple gain stage…
- With this method, a gain of 10.000 can be reached in one stage!



C_{GD}: Introducing a 'Zero' (Advanced Topic)

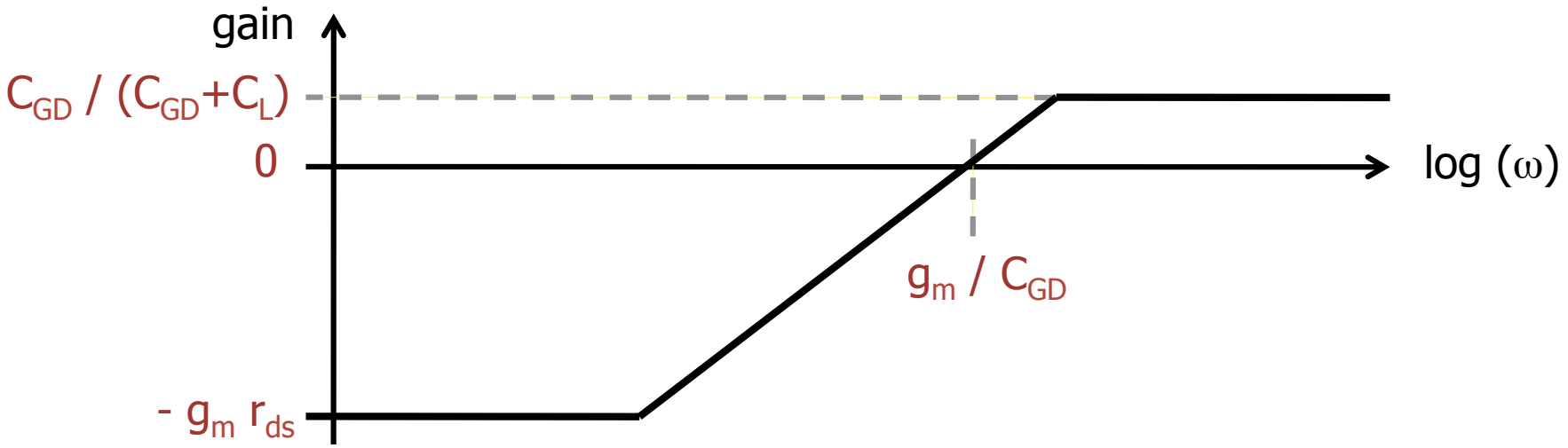
- Consider the effect of the gate-drain capacitance C_{GD}
  - Assume a finite driving impedance of the source R_S:



- $H(s) = \dfrac{-gm\ rds + CGD\ rds\ s}{1 + CL\ rds\ s + CGD\ s\ (rds + RS + gm\ rds\ RS + CL\ rds\ RS\ s)}$

New: We get a Zero - What Happens?

- We have $H(0) = - g_m r_{ds}$ as before.
- For $R_S=0$
  - The input signal propagates directly to the output via C_{GD}.
  - This same phase signal competes with the inverted signal through the MOS.
  - For very large frequencies, C_{GD} 'wins'.
  - We therefore have zero gain at some point
  - At high frequencies, we have a capacitive divider with gain < 1

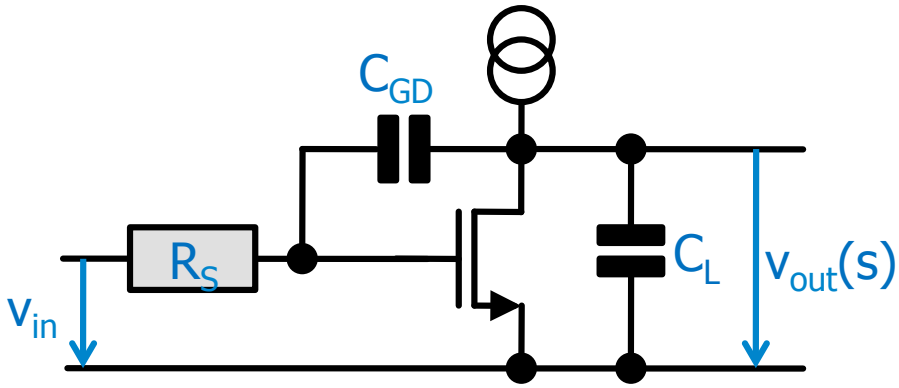


Miller Effect: C_{GD} is bad

- The input impedance of the circuit at DC (s=0) is

$$\frac{1}{CGD\ (1 + gm\ rds)\ RS}$$

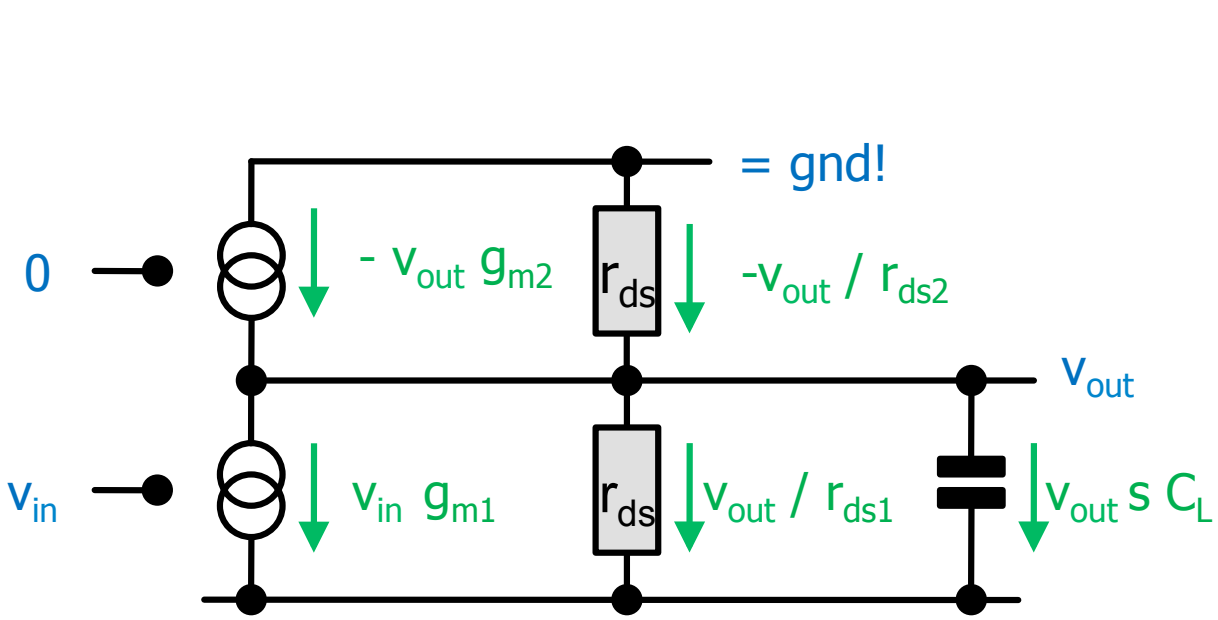
(in addition to C_{GS}, which we have omitted)

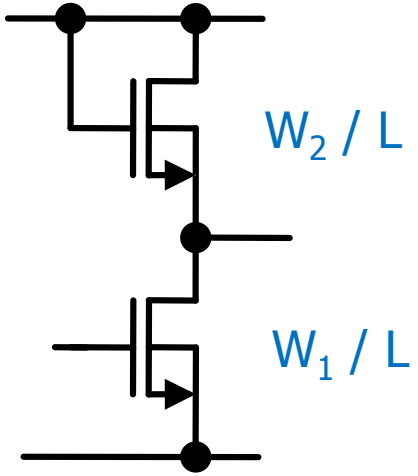


- The Gate-Source cap C_{GD} is AMPLIFIED by the gain of the stage.
- This surprising property occurs because the right side of C_{GD} sees a large signal of inverted polarity.
- This general effect is called the MILLER-EFFECT
- Due to this effect, the small C_{GD} can play an important role.

Check your Understanding:

- What is H(s) of a gain stage with a (NMOS) diode load:



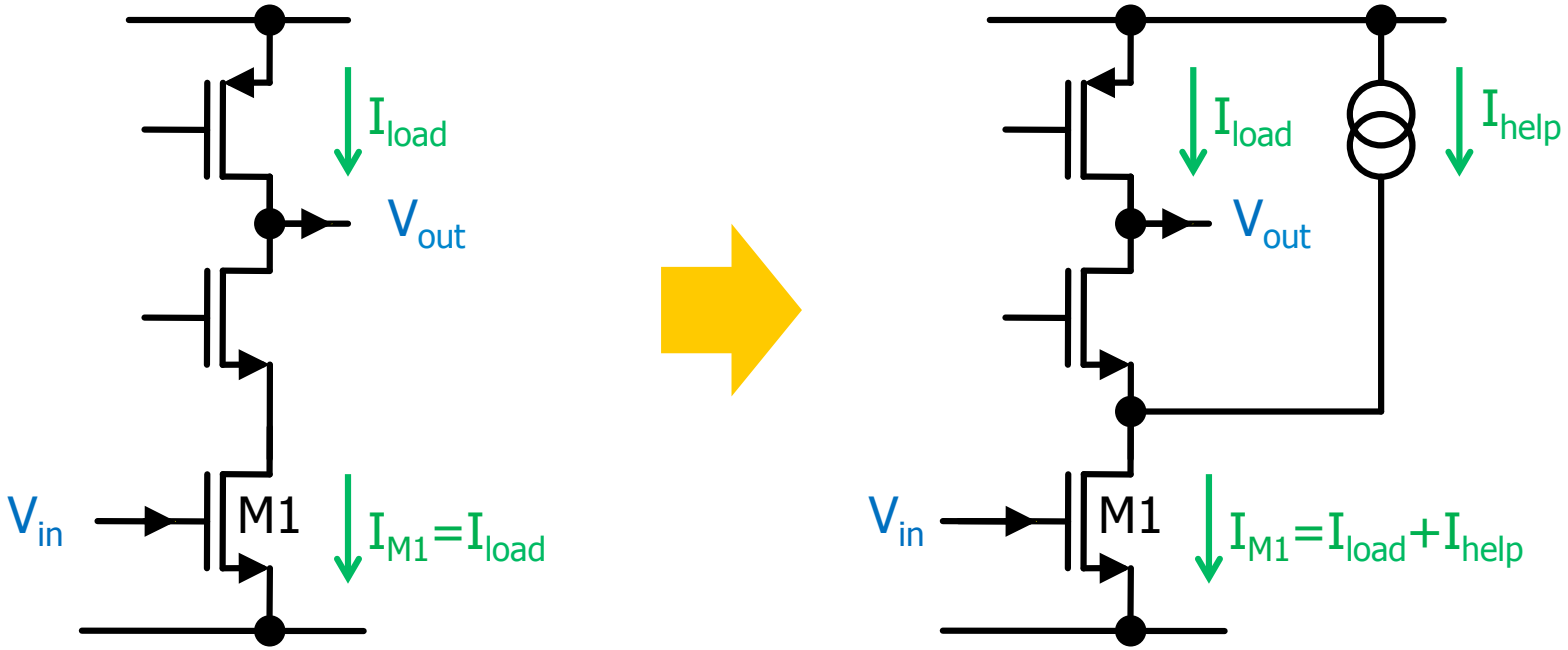


- $H(0) = -\dfrac{gm1\ rds1\ rds2}{rds1 + rds2 + gm2\ rds1\ rds2} \sim -\dfrac{gm1}{gm2}$

- In strong inversion, this is the square root of the W-ratio
  - For instance: for $W_2 / W_1 = 4$, the gain is ~ 2.

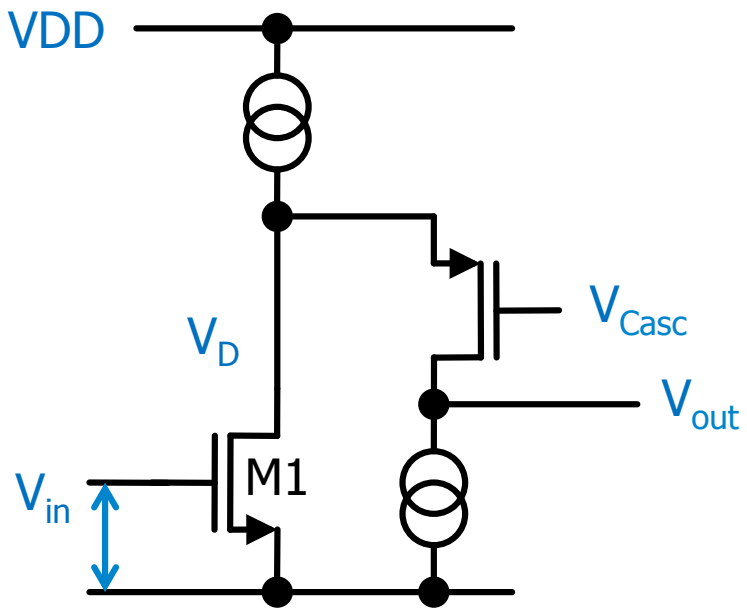
Increasing gain further

- The gain is limited by the output conductance of the load
  - That is proportional to the current in the load
- Can we *reduce* the current in the *load*, keeping the current in the amplifying MOS M1 unchanged (for g_m)?
- Yes: Add an extra current to M1 at the cascode node:



For Experts: The 'folded' cascode

- The 'straight' cascode has some drawbacks
  - many MOS are stacked → dynamic range suffers
  - DC feedback ($v_{out} = v_{in}$) is marginal as v_{out} cannot go very low
- Alternative: use a PMOS to cascode the input NMOS M1:
  - Quite surprising that this works….



  - Current in output branch is smaller than in M1 → r_{out} is higher
- Note: It may *look* like this topology has non-inverting gain…

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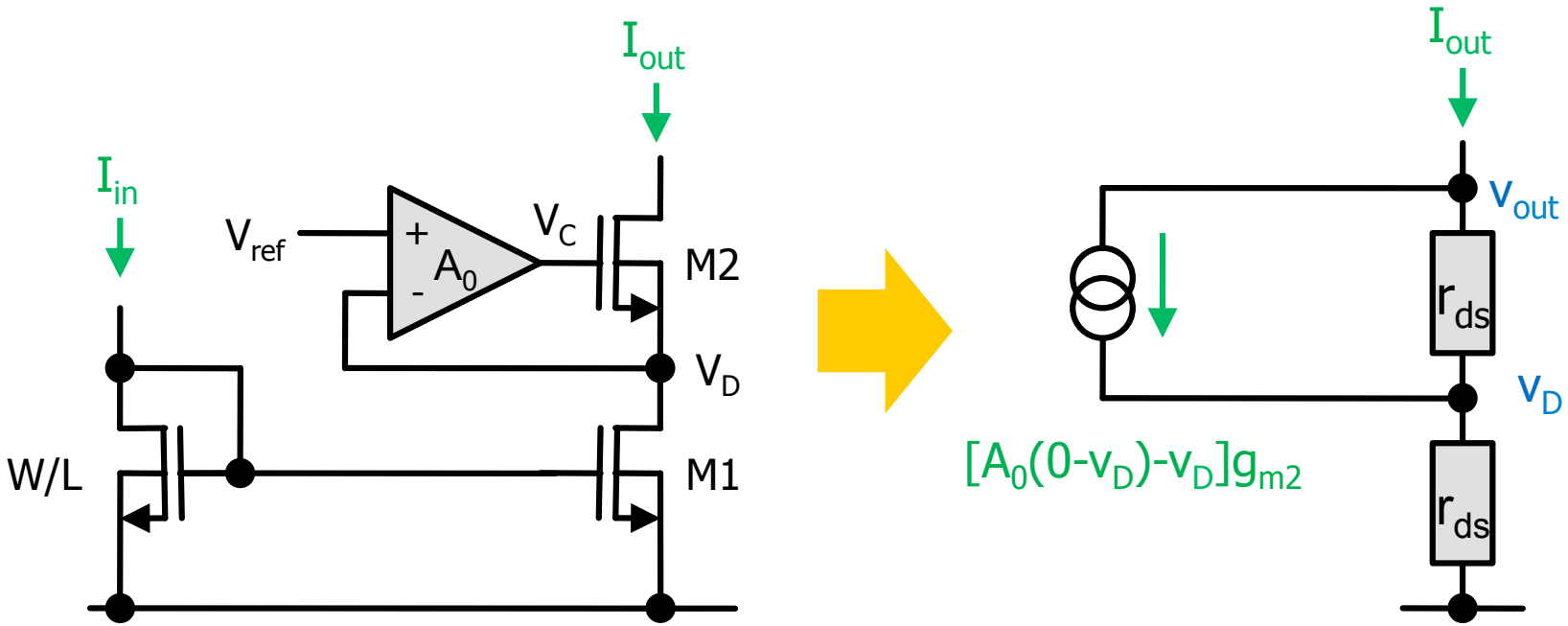
THE CURRENT MIRROR - AGAIN

Active Regulation of the Drain Voltage

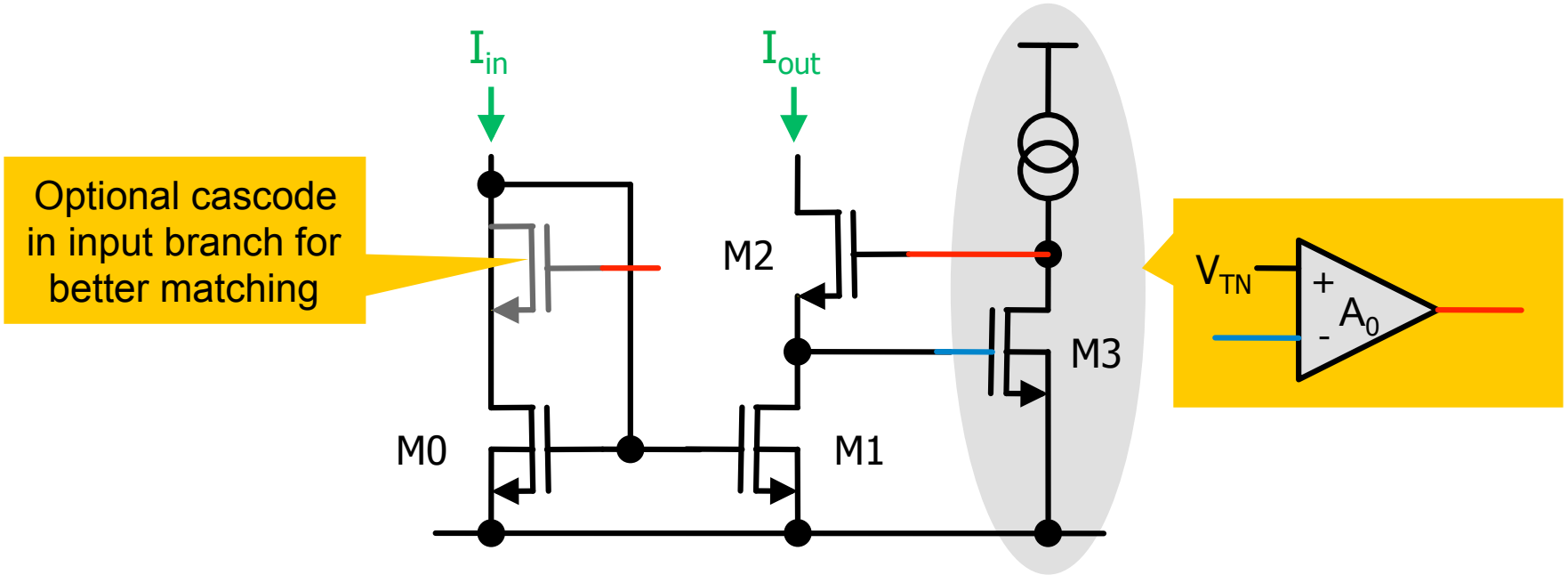
- The following circuit uses an amplifier with gain A_0 to keep V_D constant:
  - V_D is compared to a (fixed) reference V_{ref}.
  - $V_C = A_0 (V_{ref} - V_D)$
- For better *matching*, the input must be cascoded as well..



- r_{out} = rds2 + rds1 (1 + (1 + A0) gm2 rds2)

Practical Realization

- The amplifier can just be a gain stage...
- This gives the ‚regulated current mirror‘:



- Here, $A_0 \sim g_{m3}\, r_{ds3}$, Therefore $r_{out} \sim r_{ds1} \times g_{m2}\, r_{ds2} \times g_{m3}\, r_{ds3}$
- Note:
  - V_{DS} of M1 is ~ V_{TN}, which is higher than needed (wasting dyn.). (Using M3 with lower threshold helps)
  - Matching is *not* good, because $V_{DS0} \neq V_{DS1}$

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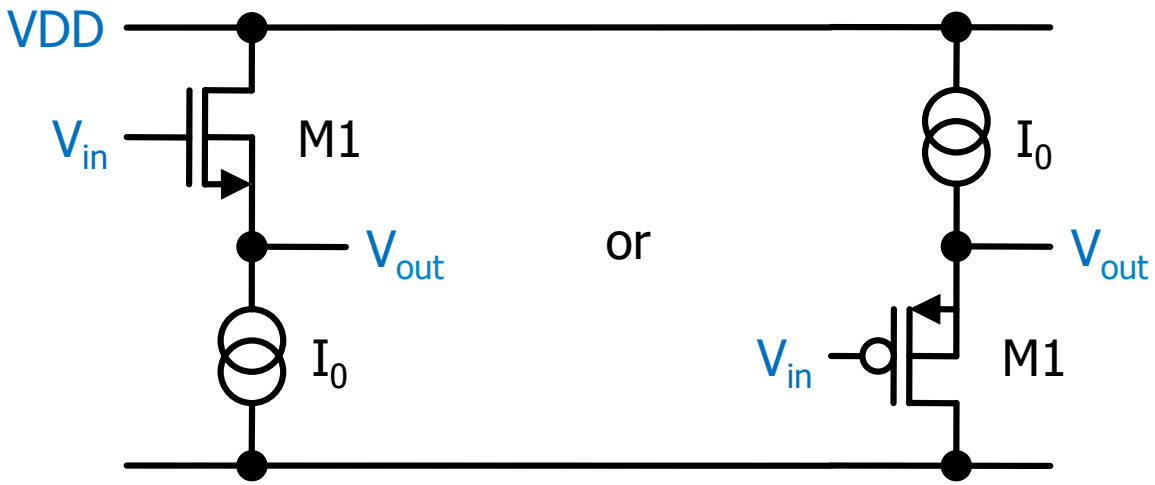
THE SOURCE FOLLOWER

The Source Follower (Common Drain Stage)

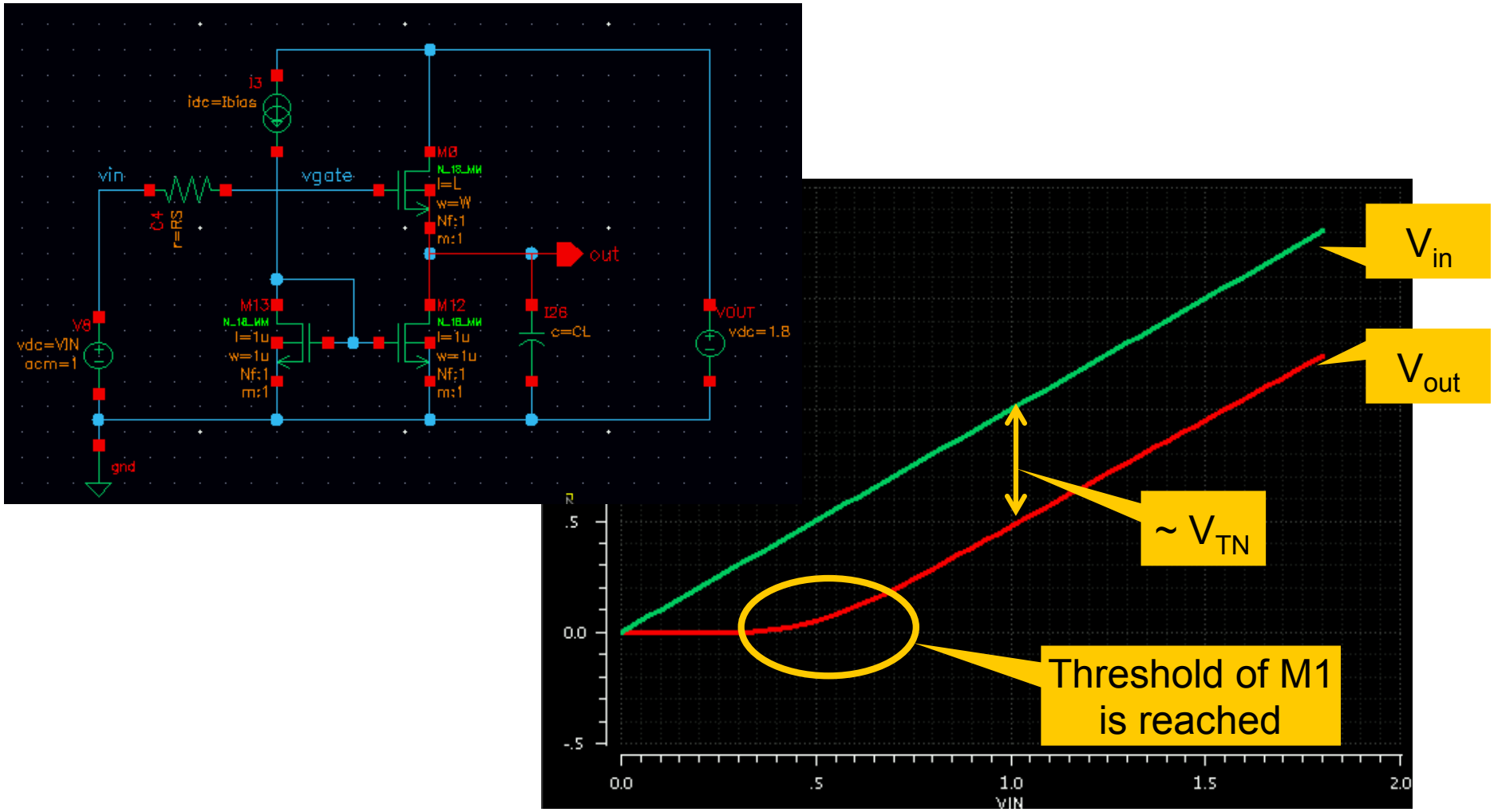
- Current source I_0 pulls a constant current through the MOS
- This fixes V_{GS} of M1 (to V_T + Sqrt(...))
- Therefore, $V_{in} - V_{out} = V_{GS} \sim$ constant

$$V_{out} = V_{in} - \text{constant} \quad \rightarrow \quad v_{out} = v_{in}$$



Simulation

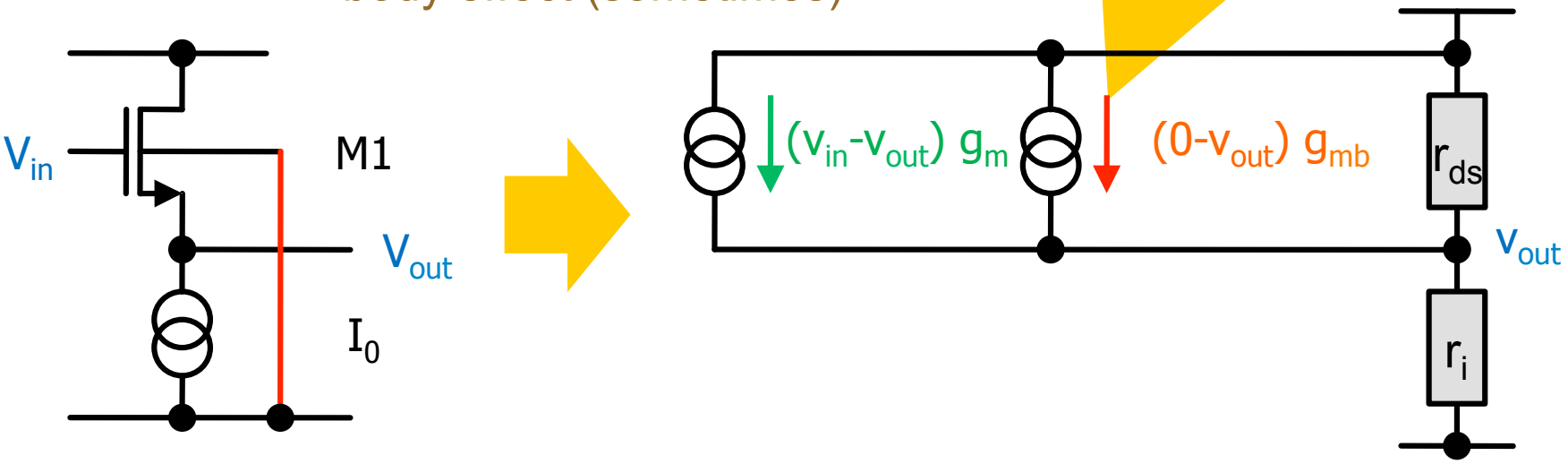
- NMOS Source Follower with NMOS current source:



Real Source Follower (Here with substrate effect)

- In reality, must consider
  - r_{ds} of M1 and current source
  - body effect (sometimes)

body effect (only if body = ground):
$i = v_{BS}\, g_{mb}$



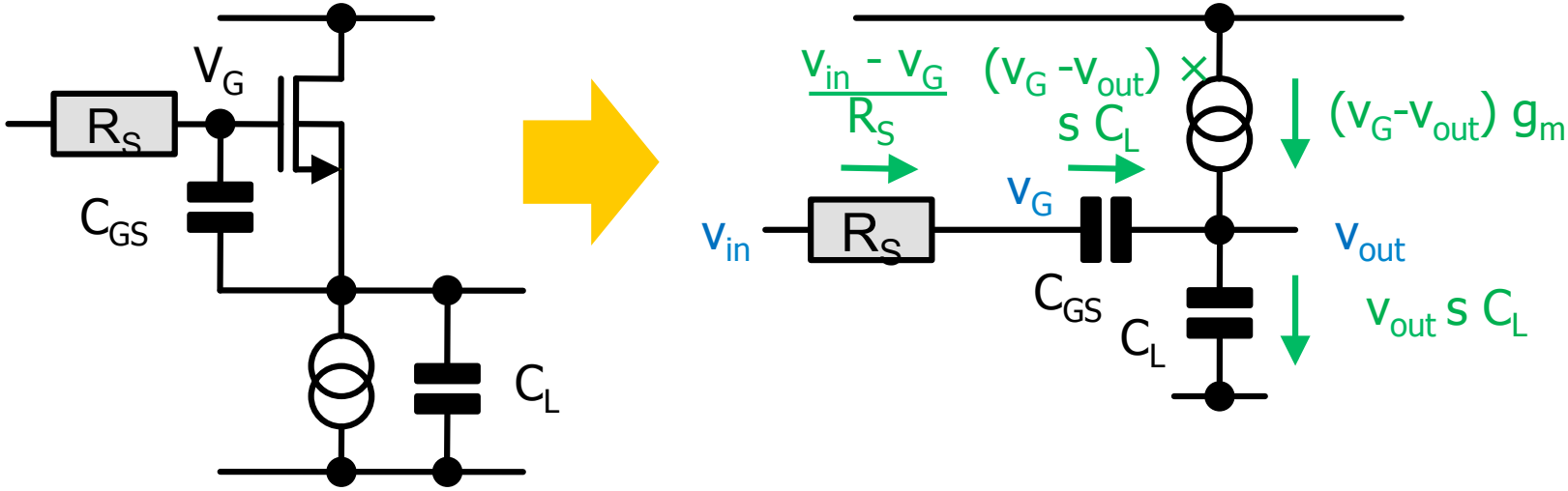
- gain = $\frac{gm\ rds\ ri}{rds + ri + gm\ rds\ ri + gmb\ rds\ ri} = \frac{gm}{gds + gi + gm + gmb} \sim \frac{gm}{gm + gmb}$

  with $g_{ds} = 1 / r_{ds}$, $g_i = 1/r_i$ and $g_{ds} << g_m$...

- Gain is < 1. With $g_{mb} = (n-1)\, g_m$, gain ~ 1/n ~ 0.7

Advanced: Source Follower with finite source imp.

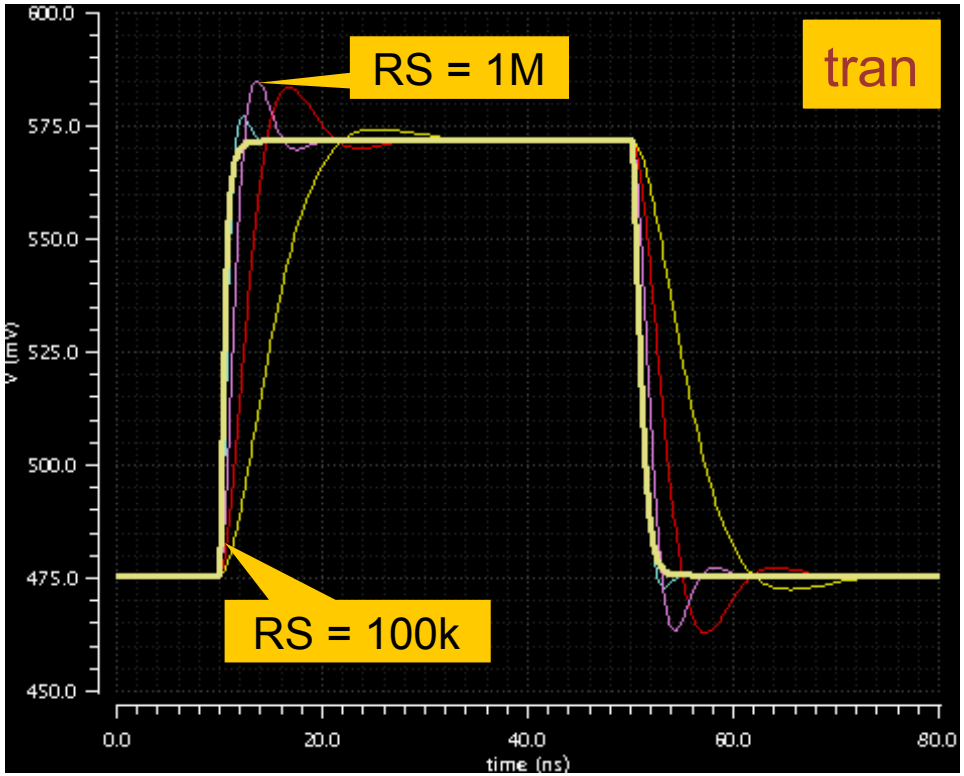
- Study in more detail the case when the SF is driven by a ‚high impedance' source (with output resistance R_S):
  - consider Gate-Source cap. C_{GS} and output cap. C_L
  - neglect output impedances and g_{mb} for simplicity...

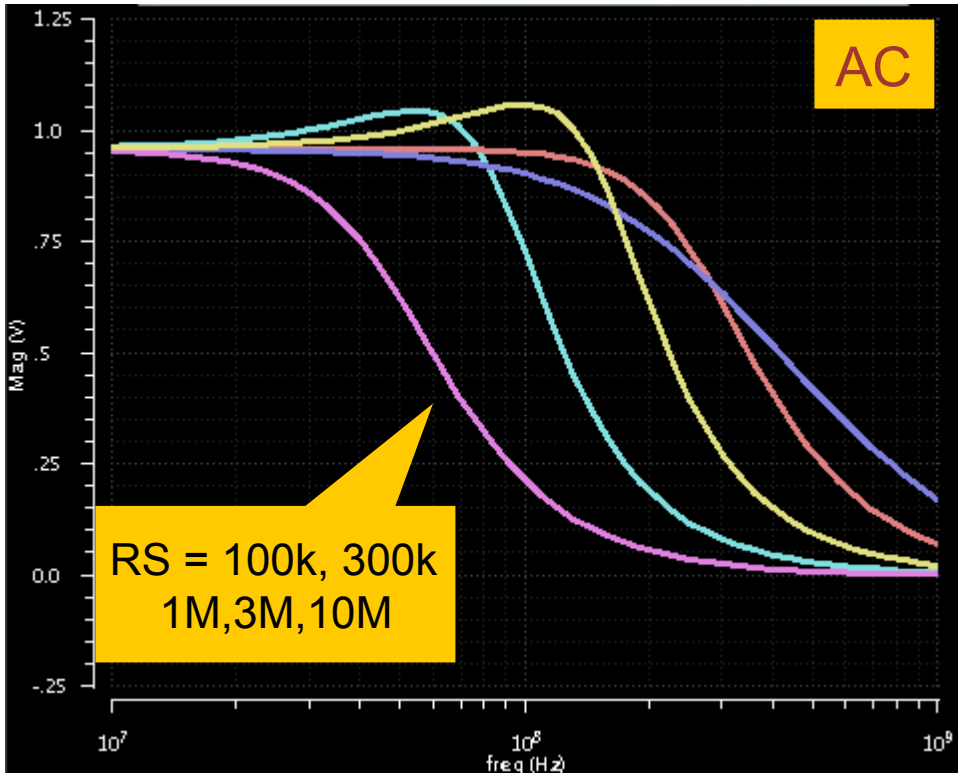


- The transfer function has two poles: $$\frac{gm + Cgs\,s}{gm + s\,(Cgs + CL + Cgs\,CL\,rs\,s)}$$
- There is an *Overshoot* as soon as $R_S > \frac{(Cgs + CL)^2}{4\,Cgs\,CL\,gm}$

Simulation

- W/L = 1µ/0.18µ, C_L = 100fF, I_{bias} = 10µA
- Transient and AC simulation:





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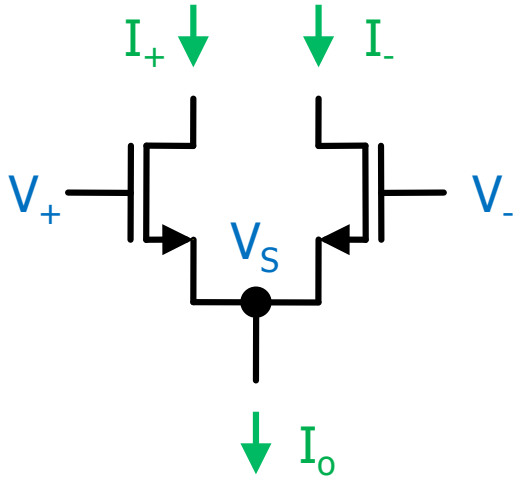
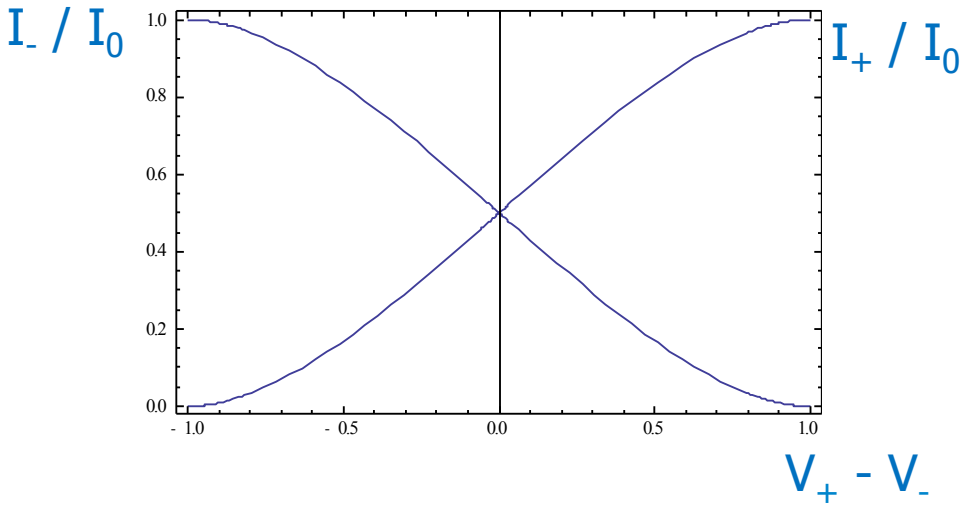
THE DIFFERENTIAL PAIR

The (Differential) Pair

- Very often, the *difference* of voltages must be amplified
- The basic circuit are two MOS with connected sources:

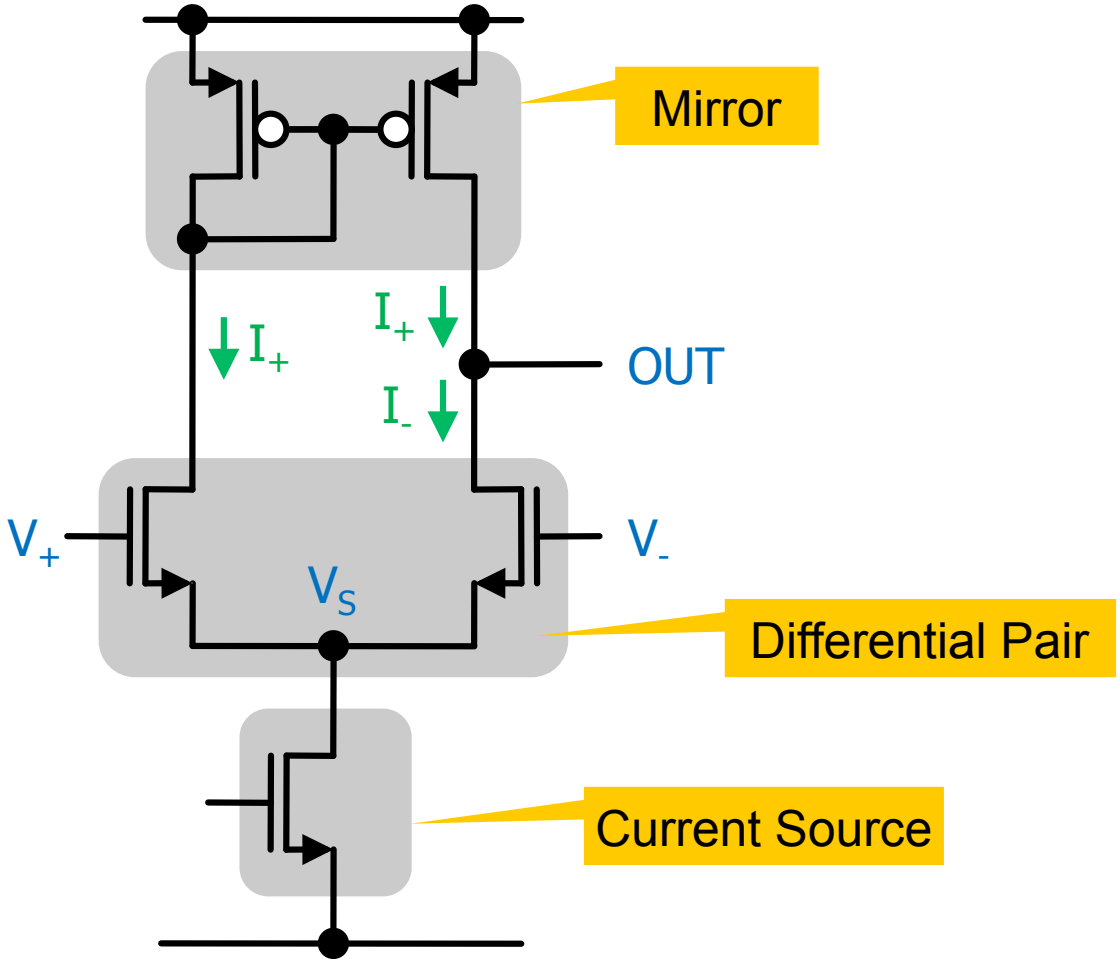




- How does it work?
  - Assume $V_+ > V_-$
  - → V_{GS} of the left MOS is larger than V_{GS} of the right MOS
  - → $I_+ > I_-$
- $V_+ = V_-$ → $I_+ = I_- = I_0 / 2$
- $V_+ \gg V_-$ → $I_+ = I_o$, $I_- = 0$

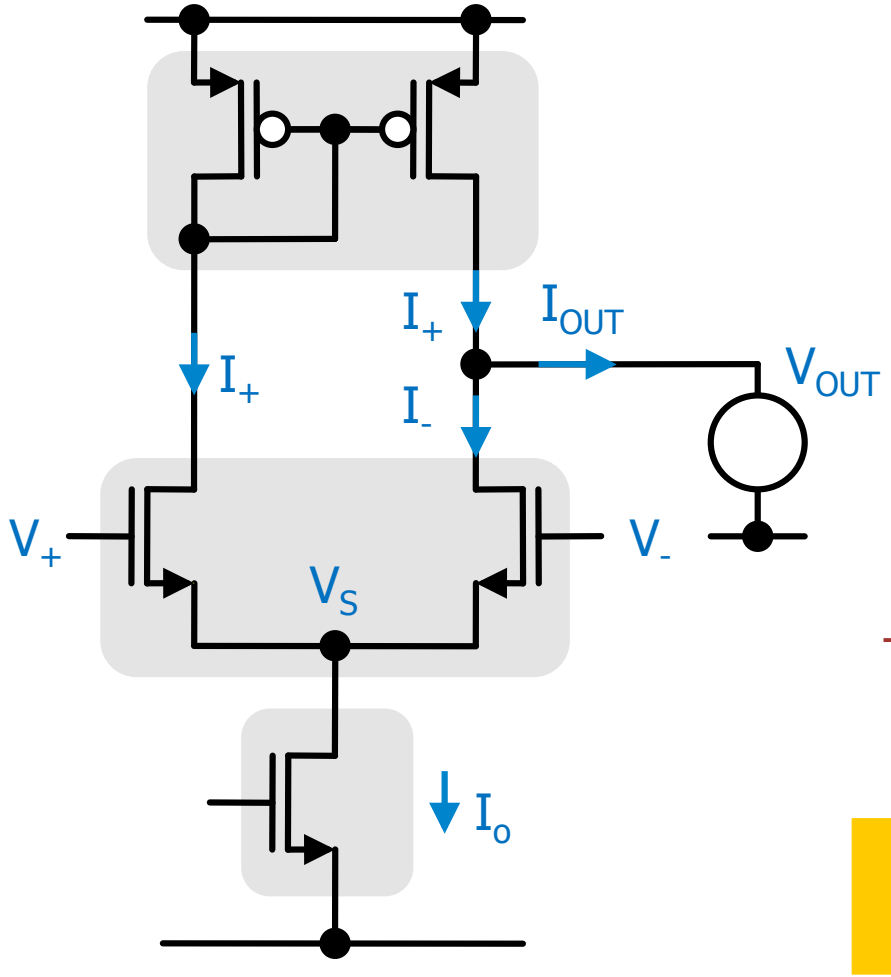
The Differential Amplifier

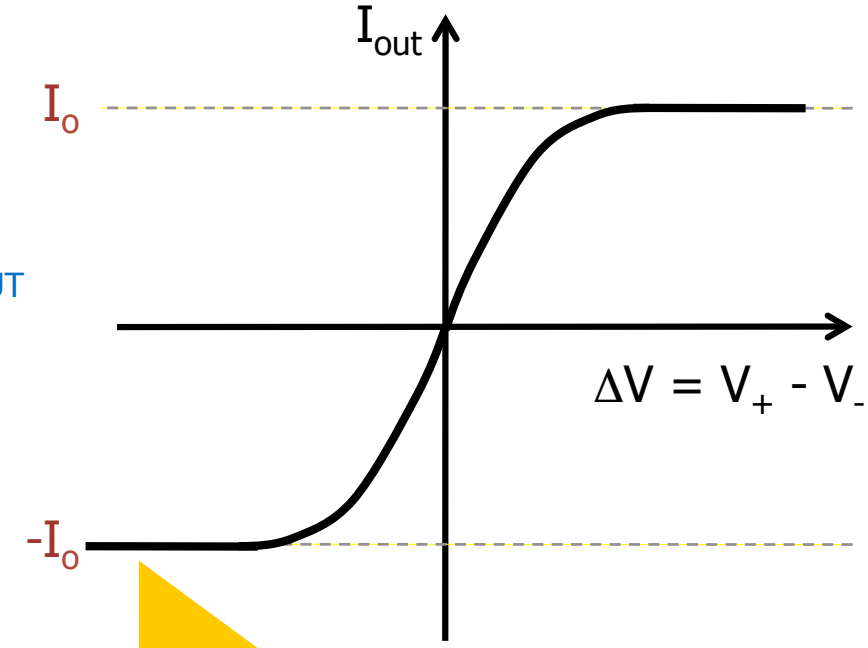
- One current is often mirrored and added to the other:



Output *Current* of the DiffAmp

- If the output voltage is *fixed*, the current is just $I_+ - I_-$
- The circuit is a *Transconductor* (it converts U → I)

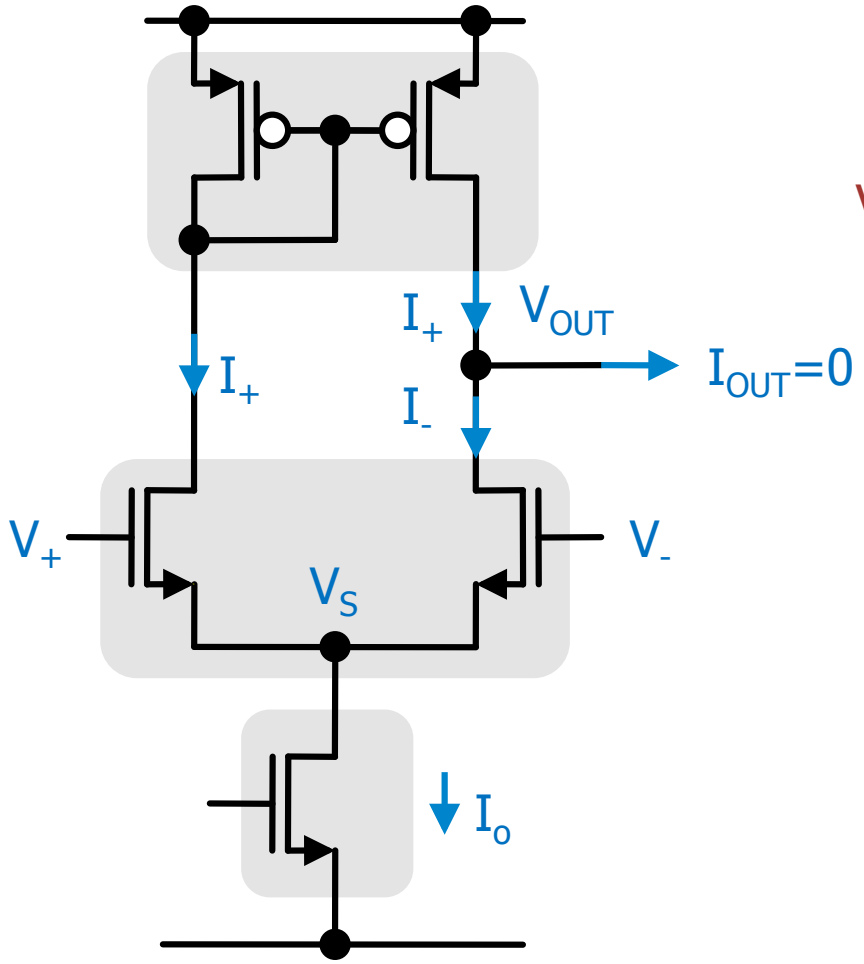


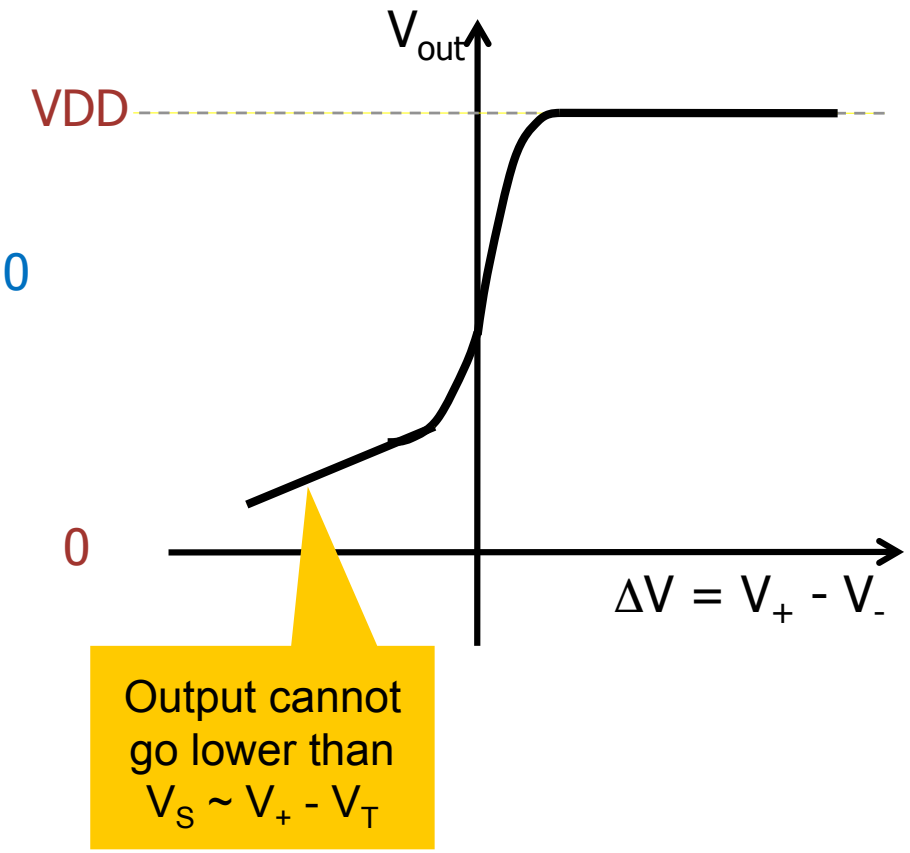


This only works if the V_{OUT} is ‚good'
? What does this mean ?

Output *Voltage* of the DiffAmp

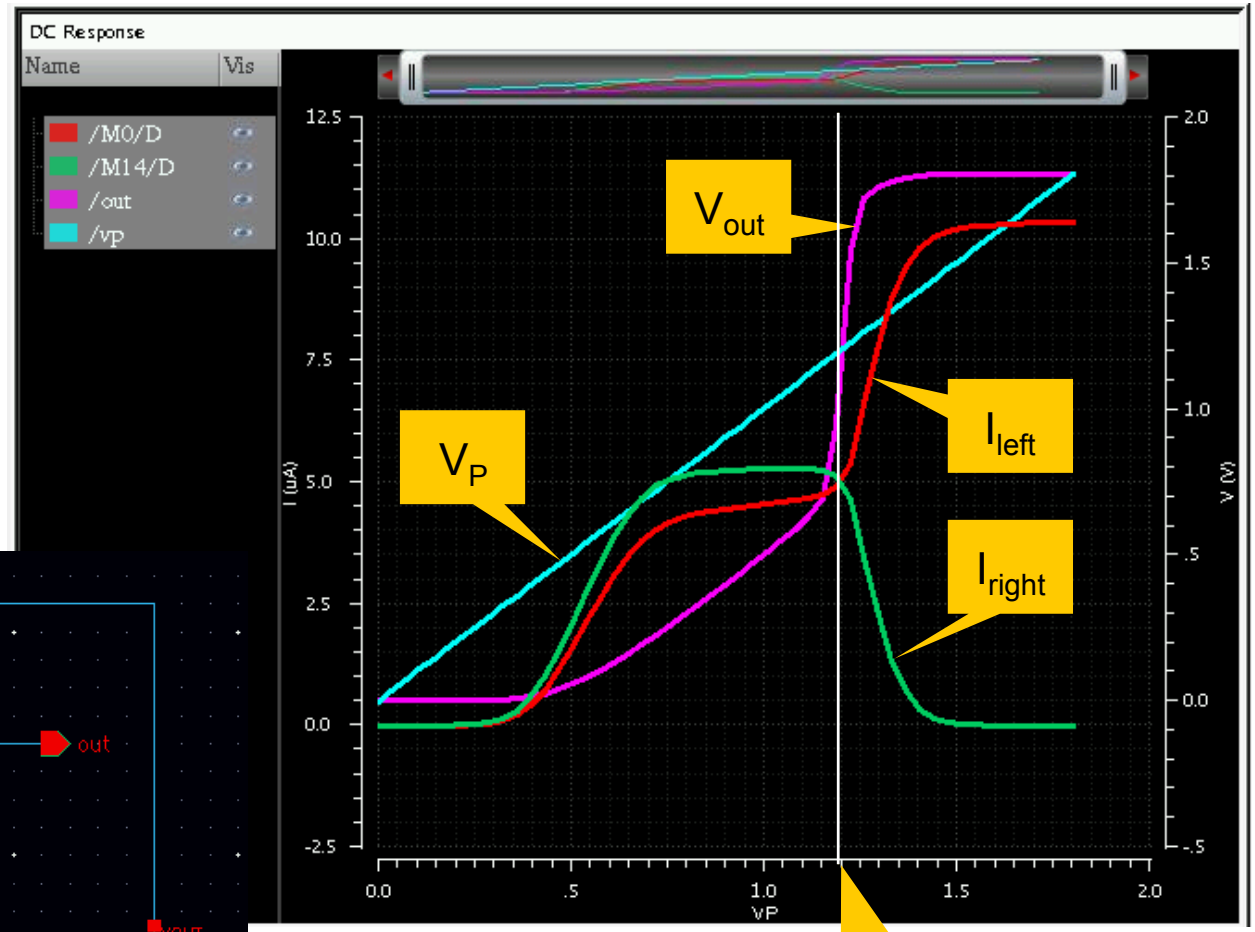
- If the *no current* flows out of the circuit and the output voltage is left free, we have *voltage* gain

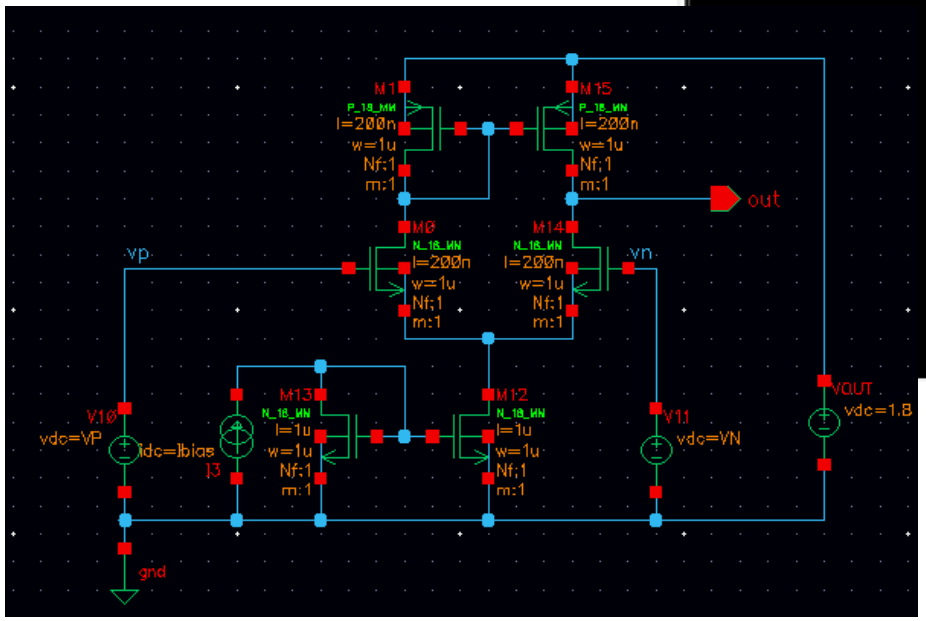




Simulation

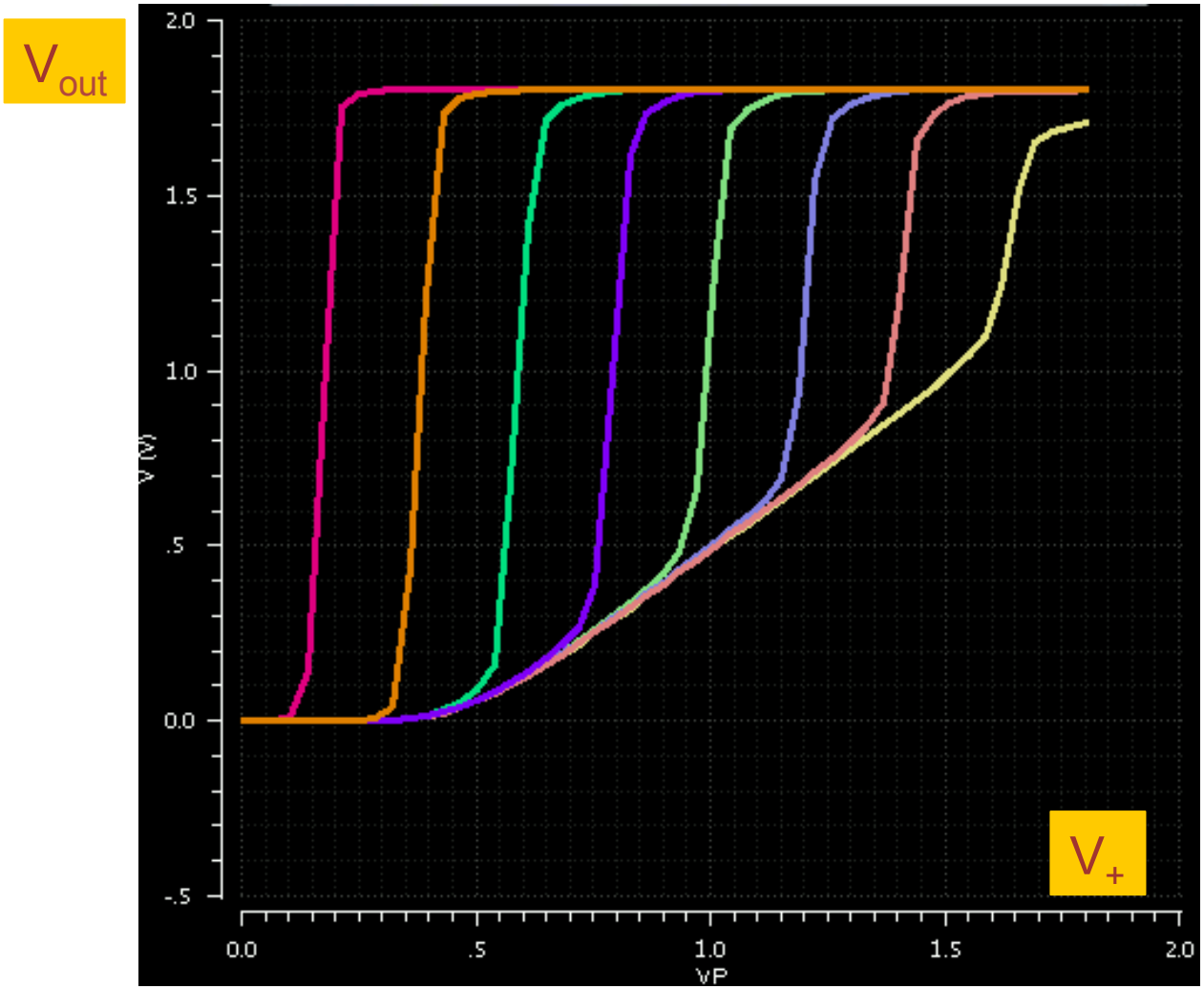
- V_N = 1.2V





Sweeping V-

- V- = 0.2, 0.4,...1.6 V

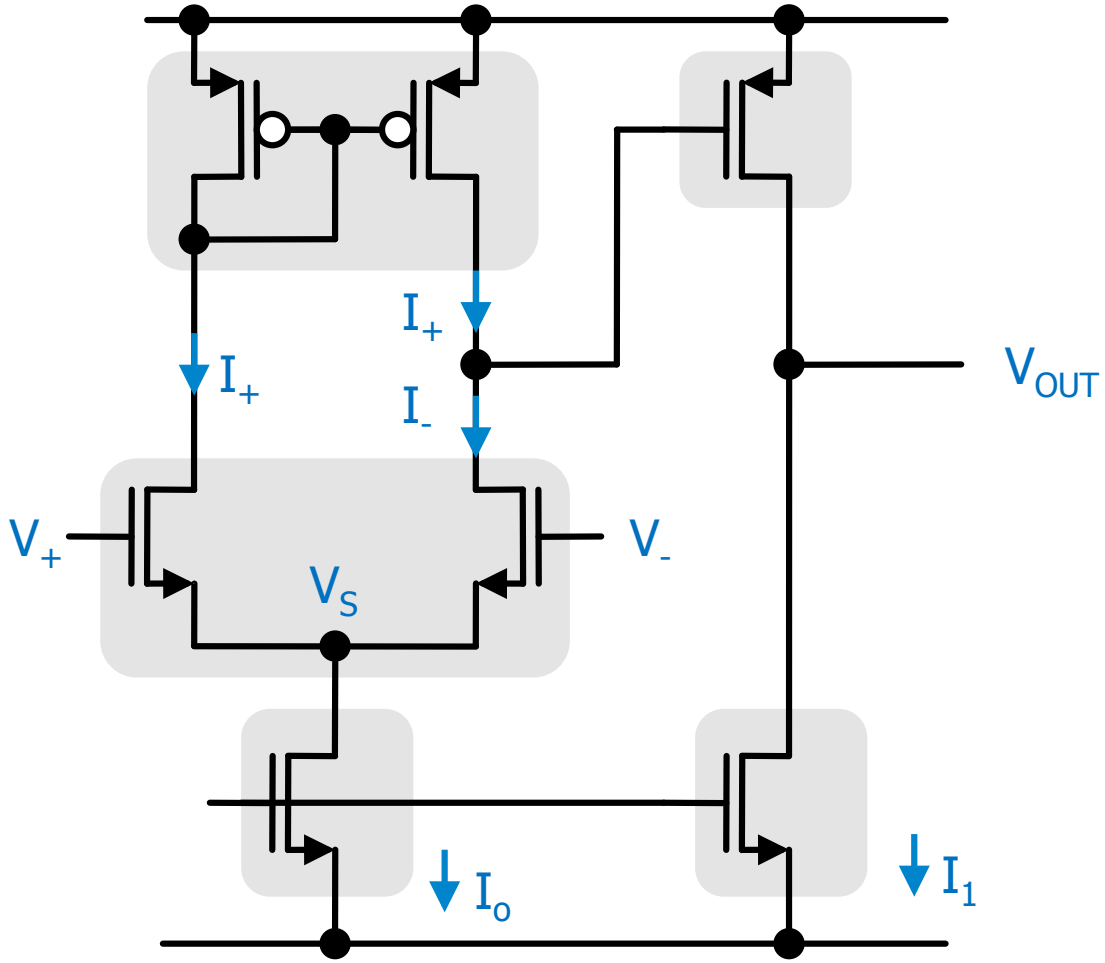


Comments

- Understanding the large signal behaviour for very different V_p,V_n is important, but in practical circuits, feedback is often applied so that $V_p = V_n$.
- Another important property is the *common mode input range*. This is limited by the V_{GS} of the input pair and the compliance of the tail current source: An *NMOS* differential pair *does not work* any more at *low* (common mode) input voltage.
- If the amplifier is loaded with a resistive load, gain drops. Therefore a source follower is often added.
  - Stability in feedback circuits is then more trick. Compensation methods are needed.

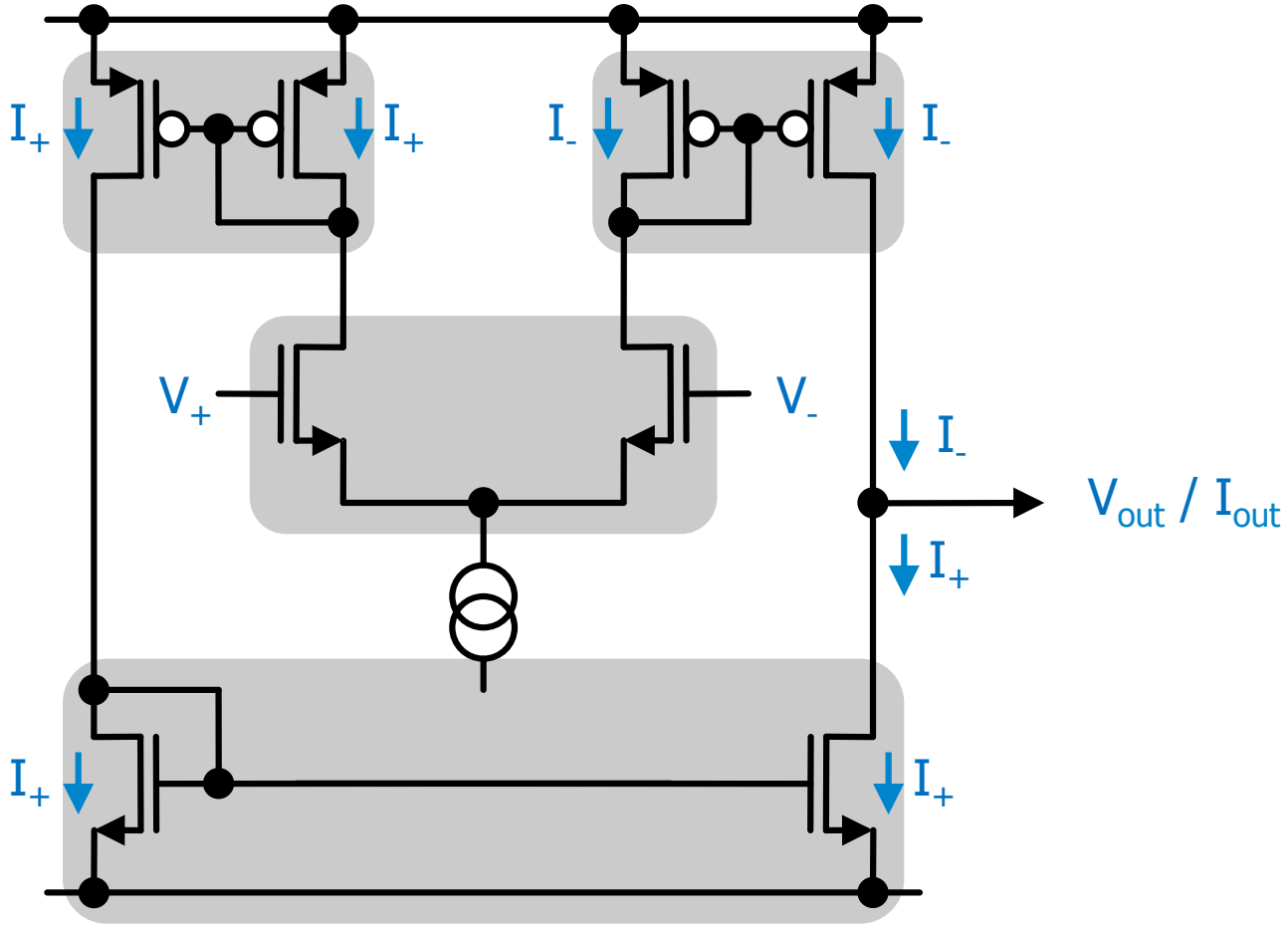
Diff-Amp with Gain Stage

- The differential amplifier is often followed by a gain stage
  - This two-stage design has two ‚main' poles and my need compensation in feedback circuits



Differential Pair + Current Mirror

- The problem of limited output voltage swing for high input common mode can be solved by mirroring the currents:



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SUMMARY

Summary Circuits

- Most important topologies are
  - Current mirror
  - Gain stage
  - Cascode
  - Source Follower
  - Differential Pair
- Their properties depend on
  - Transistor sizes
  - Currents
  - Bias Points
- Better performance can be achieved by extending the topologies
  - Cascodes
  - Current mirrors
  - ...

Summary Circuits

- Circuits must be brought to the correct operation point
- MOS are mostly operated in saturation
  - To gain dynamic range, operate ‘just at the edge of saturation’
- Small signal models give ‘quick’ insight in the ac behaviour
  - They can be used to understand & optimize circuits
- AC analysis gives more insight in the effect of parameter variations on gain, bandwidth, stability
- Transient Analysis checks the large signal behaviour

Summary Circuits

- (DC) Gain can be modified by tricks
- Gain-Bandwidth is fundamentally limited by g_m and C_{load}

Exam Topics

- Basic components, parallel, serial connection, Thevenin
- Transfer functions, Bode Plot, Phase shift
- Diode characteristic, capacitance
- MOS in linear and saturated operation, ideal strong inversion, gm, rds, dependence on geometry & current
- Small signal model
- Current mirror, ratio, output conductance, matching. Also with PMOS!
- Cascode in mirror, benefit, biasing, minimum output voltage
- Gain stage (also with PMOS) with different loads, gain, bandwidth, GBW
- Cascoding of gain stage
- Source Follower (NMOS / PMOS)
- Differential pair