



# Exercise: Starting a Simulation

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# Starting the Simulator

- In an open schematic, start the simulator with
  - Launch → ADE L (top left menu)

The screenshot shows the Virtuoso Analog Design Environment (ADE) interface. The main menu bar includes 'Launch', 'Session', 'Setup', 'Analyses', 'Variables', 'Outputs', and 'Simulation'. The 'Launch' menu is open, showing options for 'ADE L', 'ADE XL', and 'ADE GXL'. The 'Analyses' panel is active, displaying a table with columns for 'Type', 'Enable', and 'Arguments'. The 'Outputs' panel is also visible, showing a table with columns for 'Name/Signal/Expr', 'Value', 'Plot', 'Save', and 'Save Options'. The 'Design Variables' panel is on the left, with a table for 'Name' and 'Value'. The status bar at the bottom indicates 'Status: Ready', 'T=27 C', and 'Simulator: spectre'. Several callouts point to specific features: 'Can set design variables (parameters here)' points to the Design Variables panel; 'List of analysis tasks' points to the Analyses table; 'List of signals to be plotted' points to the Outputs table; 'Select type of simulation' points to the Launch menu; 'Start simulation (regenerate the netlist)' points to the green play button; and 'Plot' points to the plot icon.

Can set design variables (parameters here)

List of analysis tasks

List of signals to be plotted

Select type of simulation

Start simulation (regenerate the netlist)

Plot



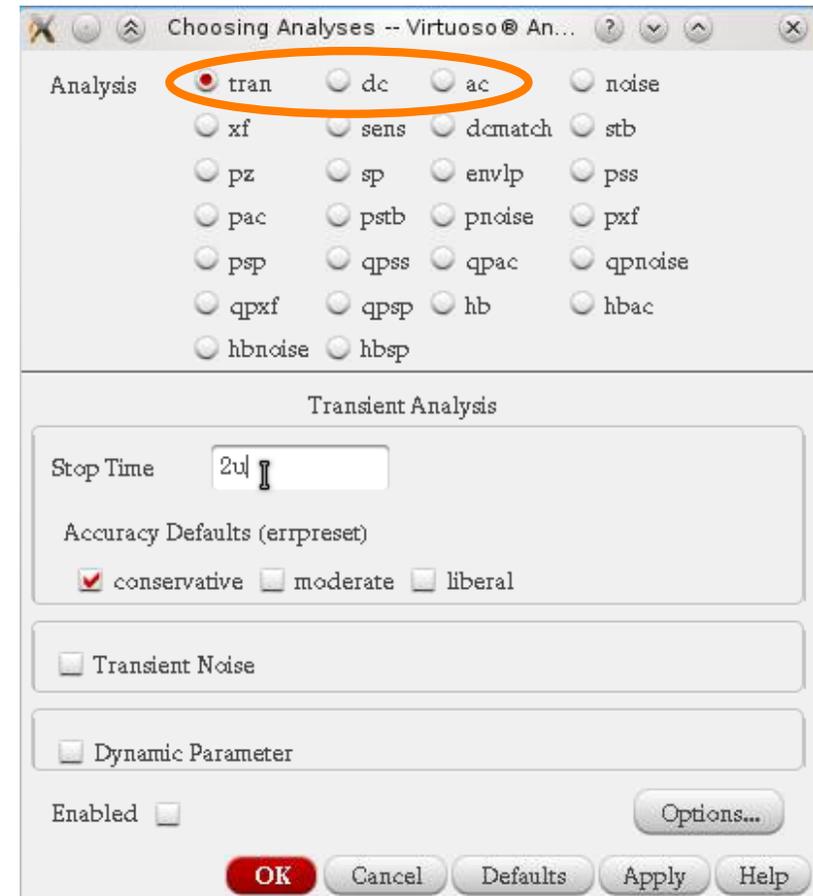
# Select Type of Simulation

- Open the panel
  - By pressing the  button or
  - In **Analyses** → **Choose Menu**

- Choose the analysis you need (we will only use 'tran', 'dc', 'ac')

- Provide the parameters required by the analysis

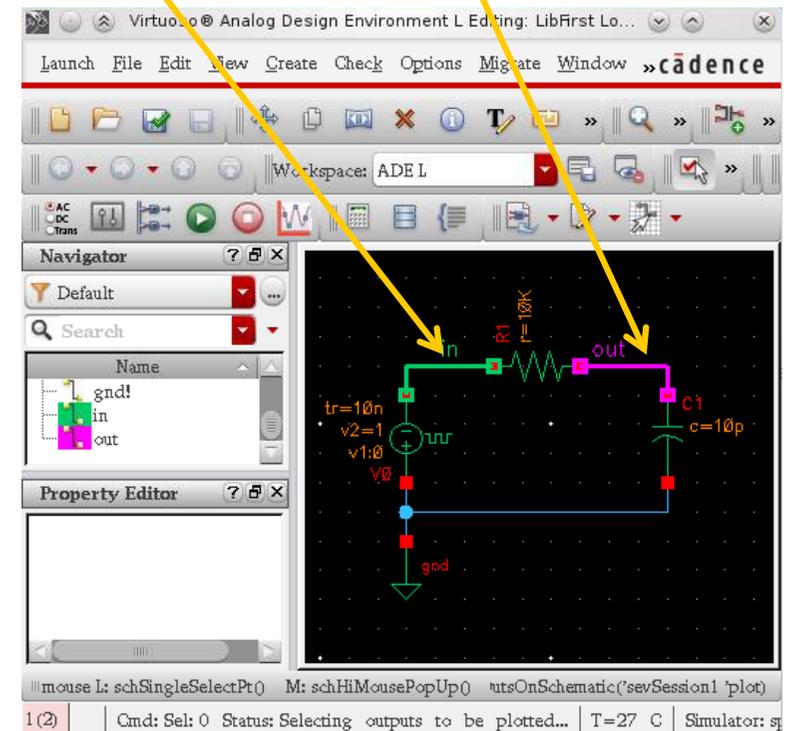
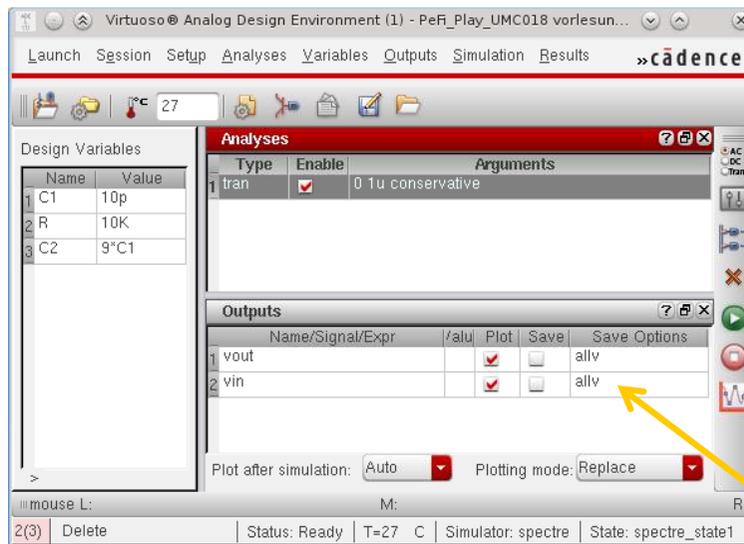
- Press **ok**





# Select Signals to be Plotted

- In simulator window
  - Select Outputs → To be Plotted → Select on Schematic
- Select the **nets** (they are highlighted with different colors) to show **voltages**
- Select **pins** to show **currents**
- End with **ESC** (important!)



- Signals are listed in the lower right panel of the sim. window



# Starting the Simulation

You can disable the automatic display of the log window under Setup → Environment → Automatic output log

- Press  or Simulation → Netlist and Run
- A log file shows up
- If your run fails:
  - Check the log file
  - (Re-open it with Simulation → Output Log)
- Some common reasons for failure:
  - Schematic has been changed, but **not** checked & saved (F8)
  - Device parameters (resistor value..) are missing or wrong
  - Design variables (see later) have not been set
  - Circuit has severe errors (shorts..)
  - ...



```

File Help
cadence

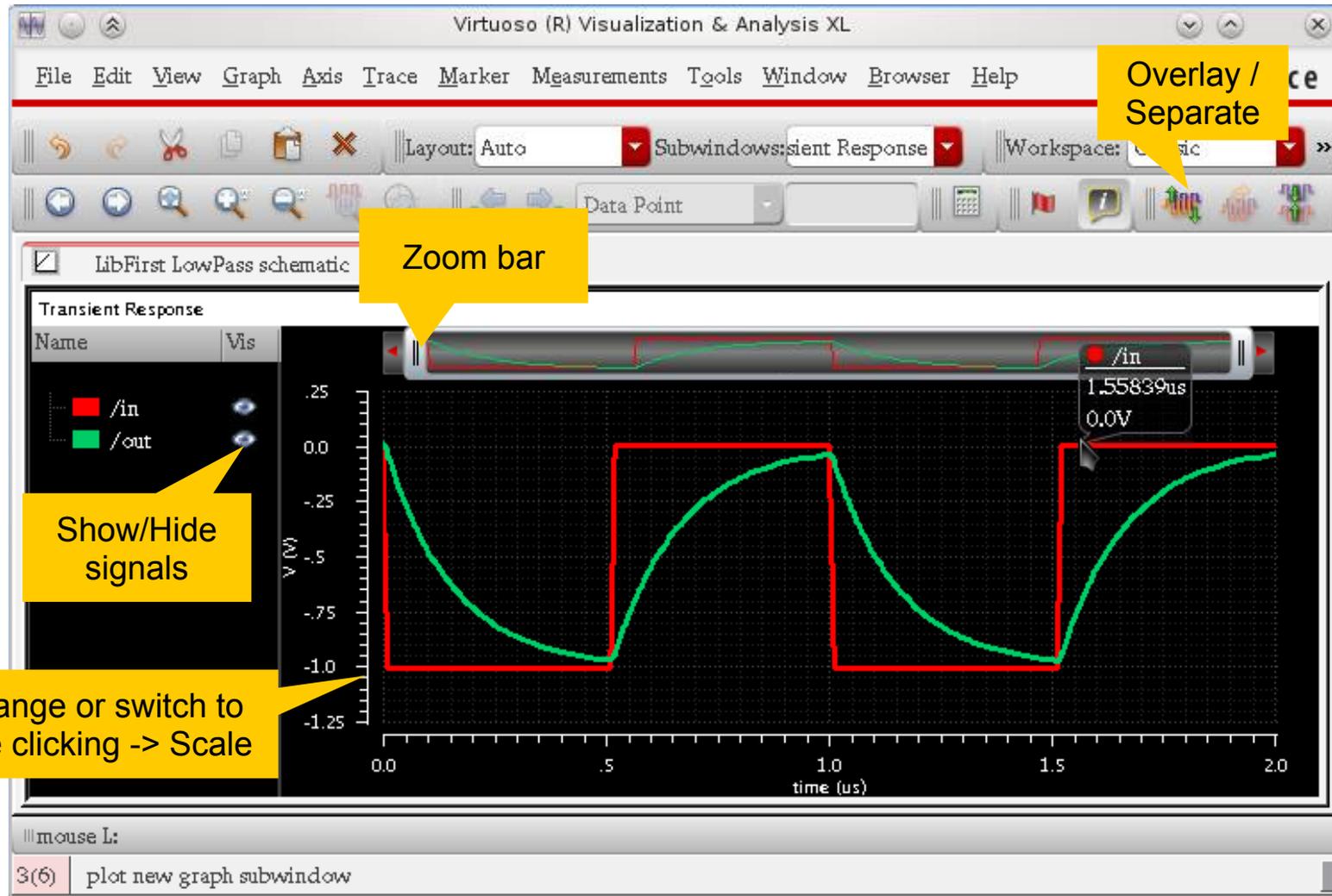
tran: time = 752.4 ns (37.6 %), step = 10.73 ns
tran: time = 854.1 ns (42.7 %), step = 14.58 ns
tran: time = 958.3 ns (47.9 %), step = 19.78 ns
tran: time = 1.055 us (52.7 %), step = 5.961 ns
tran: time = 1.153 us (57.7 %), step = 8.16 ns
tran: time = 1.26 us (63 %), step = 11.35 ns
tran: time = 1.353 us (67.7 %), step = 15 ns
tran: time = 1.46 us (73 %), step = 20 ns
tran: time = 1.555 us (77.8 %), step = 5.728 ns
tran: time = 1.65 us (82.5 %), step = 7.825 ns
tran: time = 1.752 us (87.6 %), step = 10.72 ns
tran: time = 1.854 us (92.7 %), step = 14.56 ns
tran: time = 1.958 us (97.9 %), step = 19.74 ns
Number of accepted tran steps = 268
Initial condition solution time: CPU = 0 s, elapsed = 53
Intrinsic tran analysis time: CPU = 8.001 ms, elapsed
Total time required for tran analysis `tran`: CPU = 12.0
Time accumulated: CPU = 452.028 ms, elapsed = 3.75495 s.
Peak resident memory used = 37.7 Mbytes.

finalTimeOP: writing operating point information to rawfile.
designParamVals: writing netlist parameters to rawfile.
primitives: writing primitives to rawfile.
subckts: writing subcircuits to rawfile.
    
```



# Look at the Results

- The waveform viewer shows all selected signals:

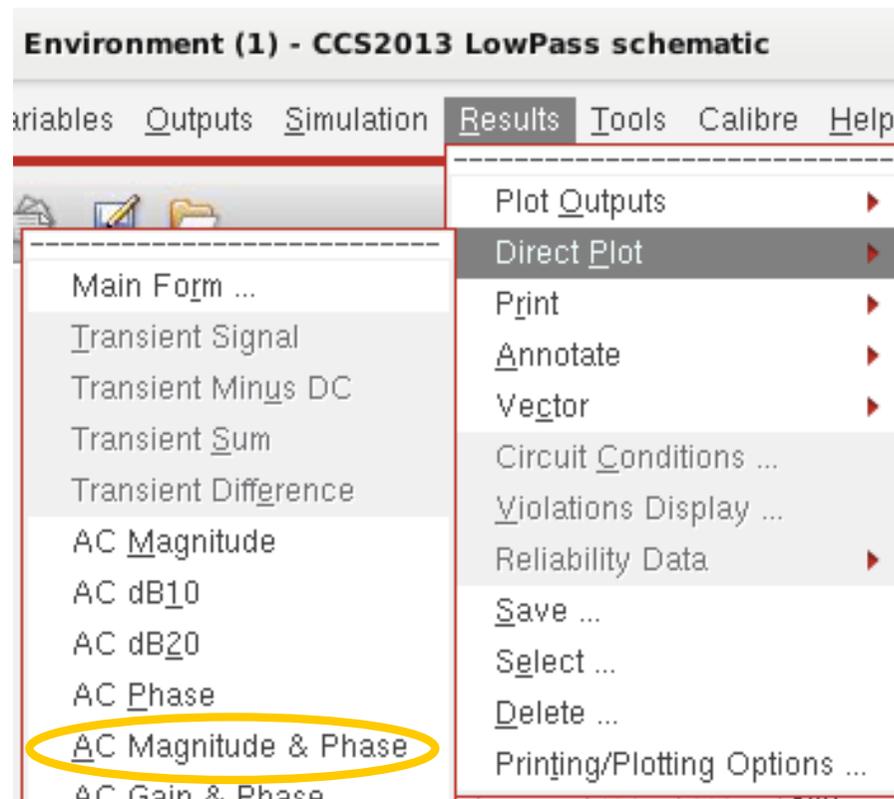


Change axis range or switch to LOG by double clicking -> Scale



# Showing More / Other Signals

- You can also add signals after the simulation using **Results → Direct Plot → ...**
- In this menu, you can select for instance AC Magnitude and Phase
  - As usual, you must then select the net and stop with **ESC**.



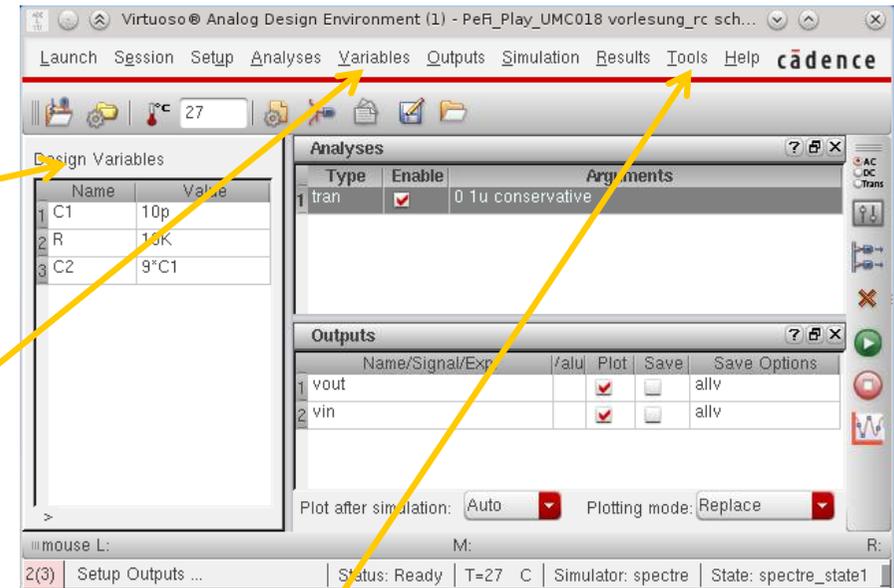


# Adding Design Variables

- You can set parameters to symbolic values ('CF', 'FREQ')
  - These 'design variables' do not need to be 'declared'

- You must then

- Add the 'design variables' by hand in the lower left window or
- Use the **Variables → Copy from CellView** command



- You can then change the Design Variables in the simulation window and just re-run the simulation (**Simulation → Run**) with **no need** to make a new netlist
- You can also run several simulations with varying values in a **Tools → Parametric Analysis**



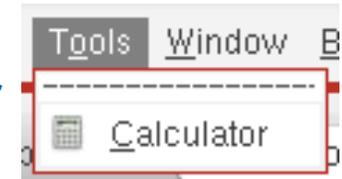
## (Copying Design Variables to the Cellview)

- You can copy the design variables and their values to the cell view with **Variables** → **Copy to Cellview**
  - This helps you to remember the best values..
  
- **Caveat:**
  - If you delete a variable in a schematic component, so that it is not used any more, it may still be 'saved' in the cell view and simulation will complain.  
In such a case you have to delete the variable in the simulation window and copy the new set to the cellview



# The WaveForm Calculator

- For more complex analysis, you can open the Waveform Calculator under **Tools → Calculator**

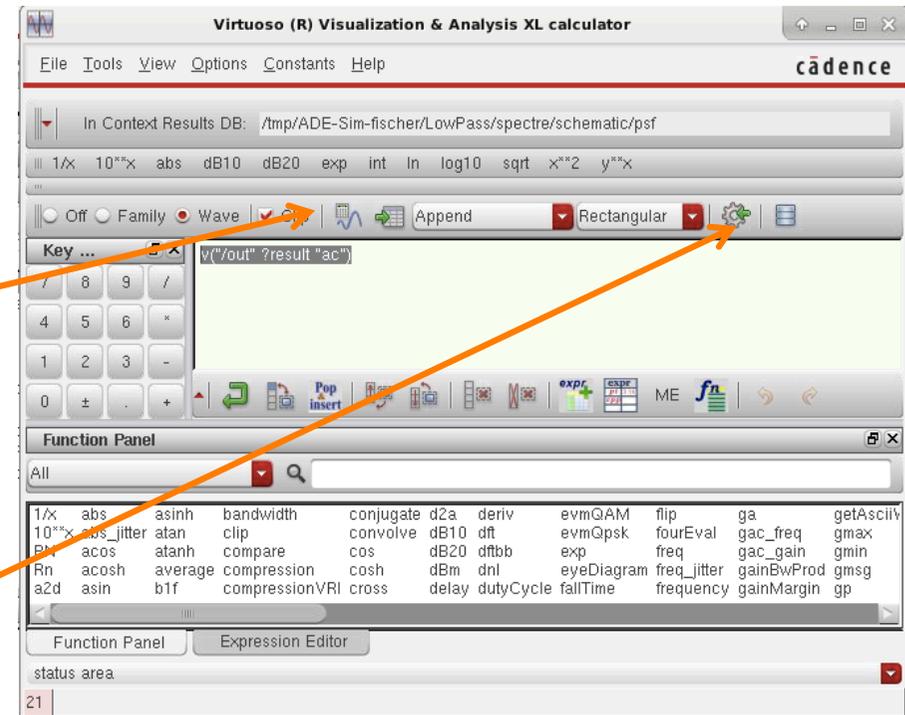


- Best select the wave you want to analyze first

- You can assemble expressions graphically (using RPN)

- Plot the result once or

- Send the expression to the outputs window so that it is evaluated every time you run a new simulation

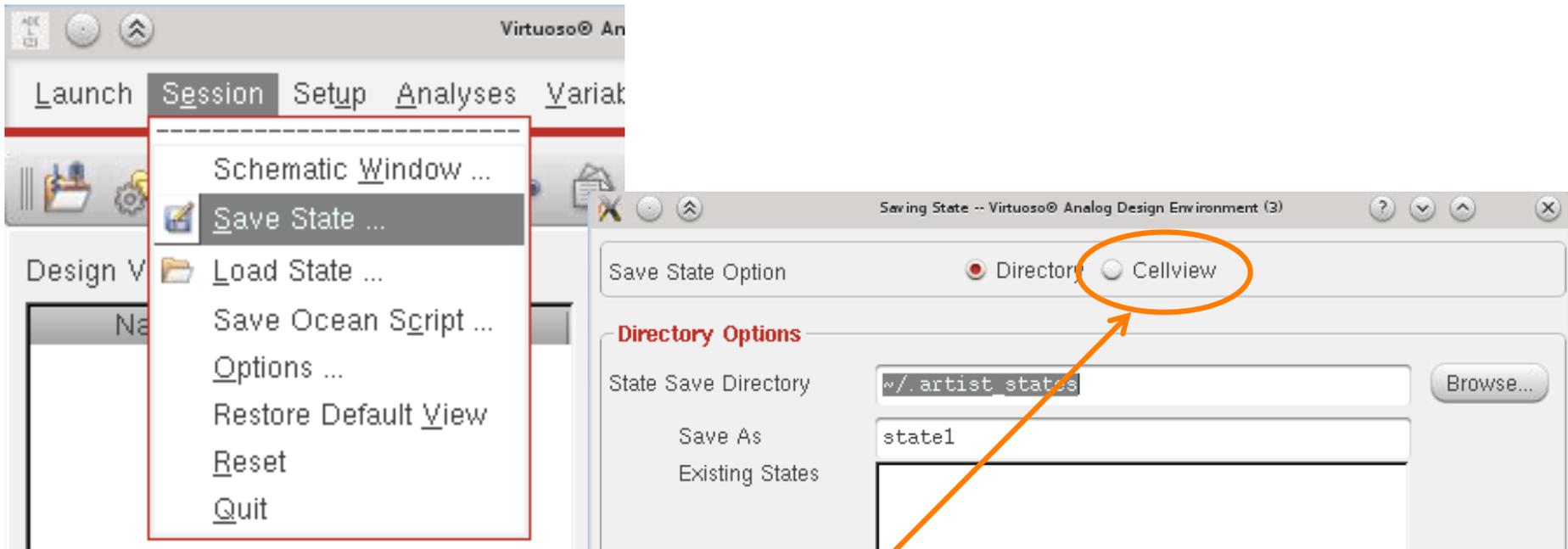


Outputs		
	Name/Signal/Expr	Value Plot
1	out	<input checked="" type="checkbox"/>
2	deriv(v("/out" ?result "ac"))	<input checked="" type="checkbox"/>



# Saving you Simulation Settings

- Before you leave, you can save all settings, results... under **Session** → **Save State**



- You can save to a file or to the cellview (view 'spectre\_state')
  - Better save to the cellview, so that everything is in the library



# EXERCISES



## Exercise 1: High Pass – AC analysis

- Use the HighPass circuit from the previous exercise
  - voltage source, ground,  $R = 1k$ ,  $C=1n$
  - Make sure the voltage source has 'AC Magnitude' set to 1
- Estimate the corner frequency of your circuit
- Chose an AC analysis with frequency span 2-3 orders of magnitude around the corner.
- Plot the Magnitude of the output
- Check that the -3dB point is **exactly** what you calculate!
- Change component values, predict the effect and simulate.
- Make the circuit more complicated (more Rs and Cs)



## Exercise 2: High Pass & Rectangular Pulse

- Now use a rectangular pulse generator (vpulse)
  - Chose the frequency much slower than the RC time
  - How does the output waveform look like ?
  - When has the signal decreased to  $1/e$  of the input step?
  - Is this what you expect from the component values?
- Double the resistor and check what happens!



## Exercise 3: High Pass & Sine Input

- Replace the rectangular generator by a sine wave generator ('vsin')
  - Set the *delay time* and *offset* to 0, the *amplitude* to 1V
  - Calculate the corner frequency (in Hertz!)
  - Check the output for a frequency  $\sim 10$  x lower or  $\sim 10$ x higher than the corner
  - What is the output amplitude *exactly* at the corner frequency?
  - What is the phase shift between input and output at the corner frequency?
  - Try to run a parametric analysis, changing the value of the capacitor (or the resistor)