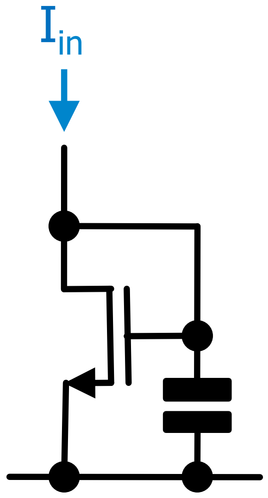
Exercise:
Current Mirrors

Prof. Dr. P. Fischer

Lehrstuhl für Schaltungstechnik und Simulation
Uni Heidelberg

Exercise 1: Dynamic Regulation

- Draw a diode connected NMOS
- Connect a large ‚extra' capacitance to the gate (some pF) with an *initial condition* of 0 V
  - Use a transistor 'n_18_mm' from the UMC library 'UMC_018_CMOS'. Connect bulk and source.
  - Set the initial condition ('IC') in the properties of the capacitor
- Send a small current I_{in} (nA-µA) into the ‚diode'
- Perform a transient simulation

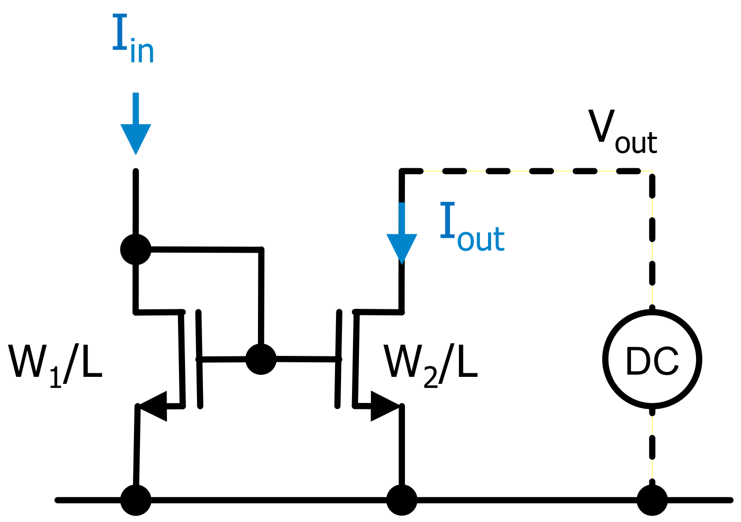


- Observe the Input = Gate = Drain Voltage

- Use different initial conditions (0…1.8V, Parametric sweep!)
- Understand how the equilibrium point is reached!
- Vary I_{in}!

Exercise 2: A First Mirror

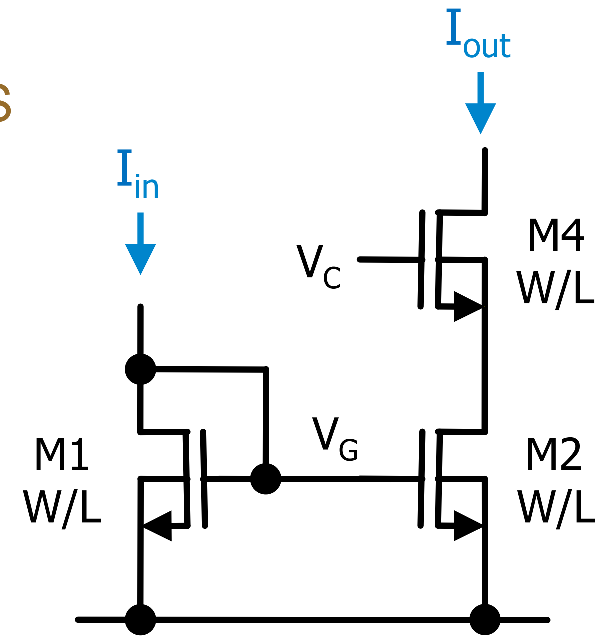
- Draw the following *current mirror*, with $W_1 = W_2 = 1\mu m$. Use for instance $L = 0.5\mu m$ and $I_{in} = 10\mu A$



- Sweep the output voltage V_{out} and observe the current I_{out}.
  - When is $I_{out} = I_{in}$ *exactly*? Why?
  - Try another input current!
  - Change W_2!
- For fixed I_{in}, W_1,W_2, vary L (same in both MOS).
  - Explain what you see!

Exercise 3: A Better Mirror

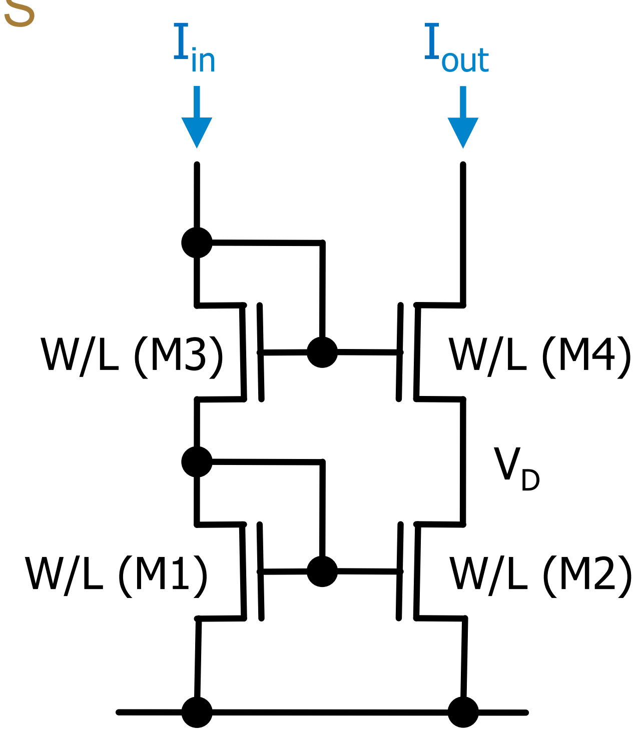
- The output current varies with V_{out} (i.e. the output resistance is not infinite) due to the Early Effect in M2.
- Try the following circuit:
  - Connect bulk and source in all MOS
  - Start with V_C = 1.2V
  - Use I_{in} = 1uA



- Sweep V_{out}
  - How is the output resistance now? (You may simulate the ‚simple' mirror of the previous exercise in parallel for comparison)
- *Calculate* the small signal output resistance!
  - You only need to consider M2 and M4 (because V_G is constant)
- Vary V_C (from 0V to 1.8V) and see what happens
  - What is the 'ideal' V_C ?

Exercise 4: A Mirror with Better Matching

- Unfortunately, the previous circuit does NOT reproduce I_{in} exactly. Why?
- Try this circuit (which does not need V_C and more):
  - Connect bulk and source in each MOS
  - It is called the ‚stacked mirror'

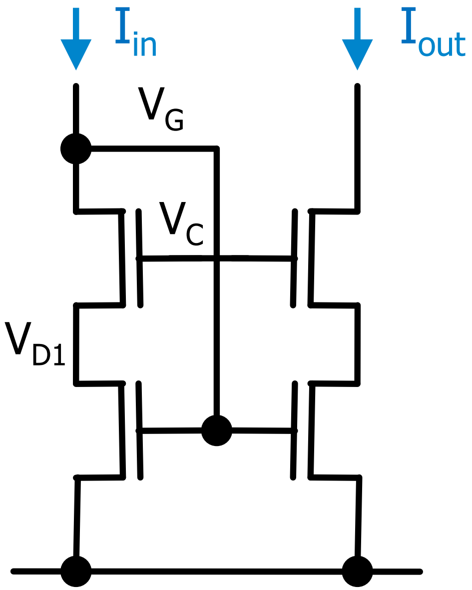


- Sweep V_{out}
  - Do currents match?
  - What is r_{out} ?
  - Where is the saturation ?
- What is the drain voltage V_D of M2? Is that optimal?

Exercise 5: The Low Voltage Mirror

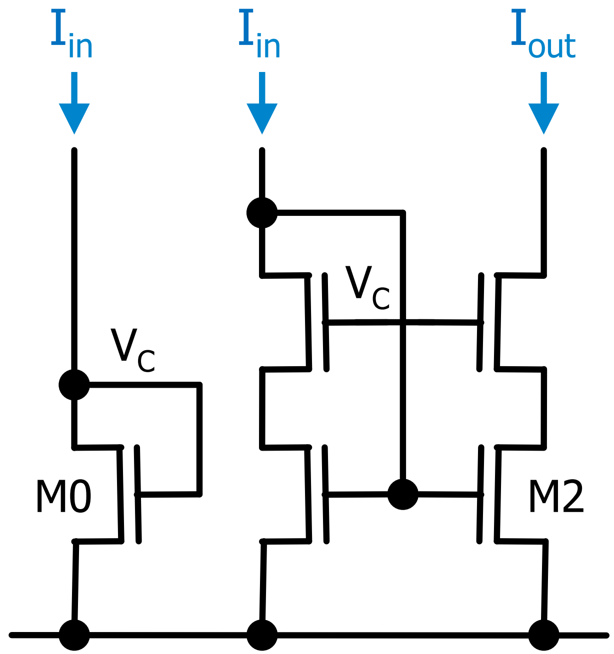
- In the stacked mirror of the previous exercise, the drain voltage V_D of the current source M2 is fixed by the diode connection of M1.
- This is simple, but provides a *too high* voltage (by ~V_T !)

- The following circuit connects the diode differently:
  - Understand that the gate voltage V_G still stabilizes to the 'correct' level!
  - We now need to find V_C
  - Sweep V_C from 0.4 to 1.4V in steps of 0.2V
  - What is a good choice?
  - Why do very low voltages fail (check V_G !)
  - What happens at high voltages? Why? (this is tricky to understand… Look at V_{D1}…)
  - Note that the 'best' V_C depends in I_{in}



Exercise 6: The Low Voltage Mirror

- The required optimal cascode voltage V_C can be generated *automatically* by a diode connected MOS M0 with different geometry than the others:
  $(W/L)_0 = k\ (W/L)_{others}$
- We assume that we have a second input current I_{in} available (boths I_{in}s are equal)



- *Calculate* k so that M2 is just saturated.
  - Use the *large signal* model in strong inversion with no Early effect
- Simulate the circuit

Exercise 7: An *Even* Better Mirror

- The key trick is obviously to keep the drain voltage of M2 very constant irrespective of the output voltage.
- This can be done with an active circuit (with an amplifier):
  - Amp amplifies the difference of the two input voltages by A_0
  - Where is the positive/negative input for table operation?
  - Simulate the circuit. Use a voltage controlled voltage source vcvs from the analogLib for Amp with A_0=1000
- *Calculate* the output resistance!
- This topology is called the *Regulated Mirror*