The pn-Diode

A few Natural Constants

q	1.602×10^{-19} C	elementary charge
k	1.381×10^{-23} J/K	Boltzmann constant
$4kT$	1.657×10^{-20} J	Noise Power density @ 300K
U_T	$= kT/q = 25.9$ mV	Thermal voltage @ 300K
ε_0	8.854×10^{-12} F/m	vacuum susceptibility (Hint: $C = \varepsilon_0$ A/d, 1m x 1m x 1m: ~10pF)

A few Constants for Silicon

- E_g 1.12 eV band gap at 300K
- N_{atom} 5×10^{22} cm^{-3} atom density
- N_i 1.01×10^{10} cm^{-3} intrinsic carrier density at 300K* ('old' value: 1.45)
- μ_e 1400 cm^2/Vs electron mobility (@ low fields)
- μ_h 480 cm^2/Vs hole mobility ($v = \mu E$)
- E_{cit} 1 V/µm critical field where mobility starts to drop

- ε_{Si} 11.9 dielectric constant of silicon
- ε_{SiO2} 3.90 dielectric constant of silicon - dioxide

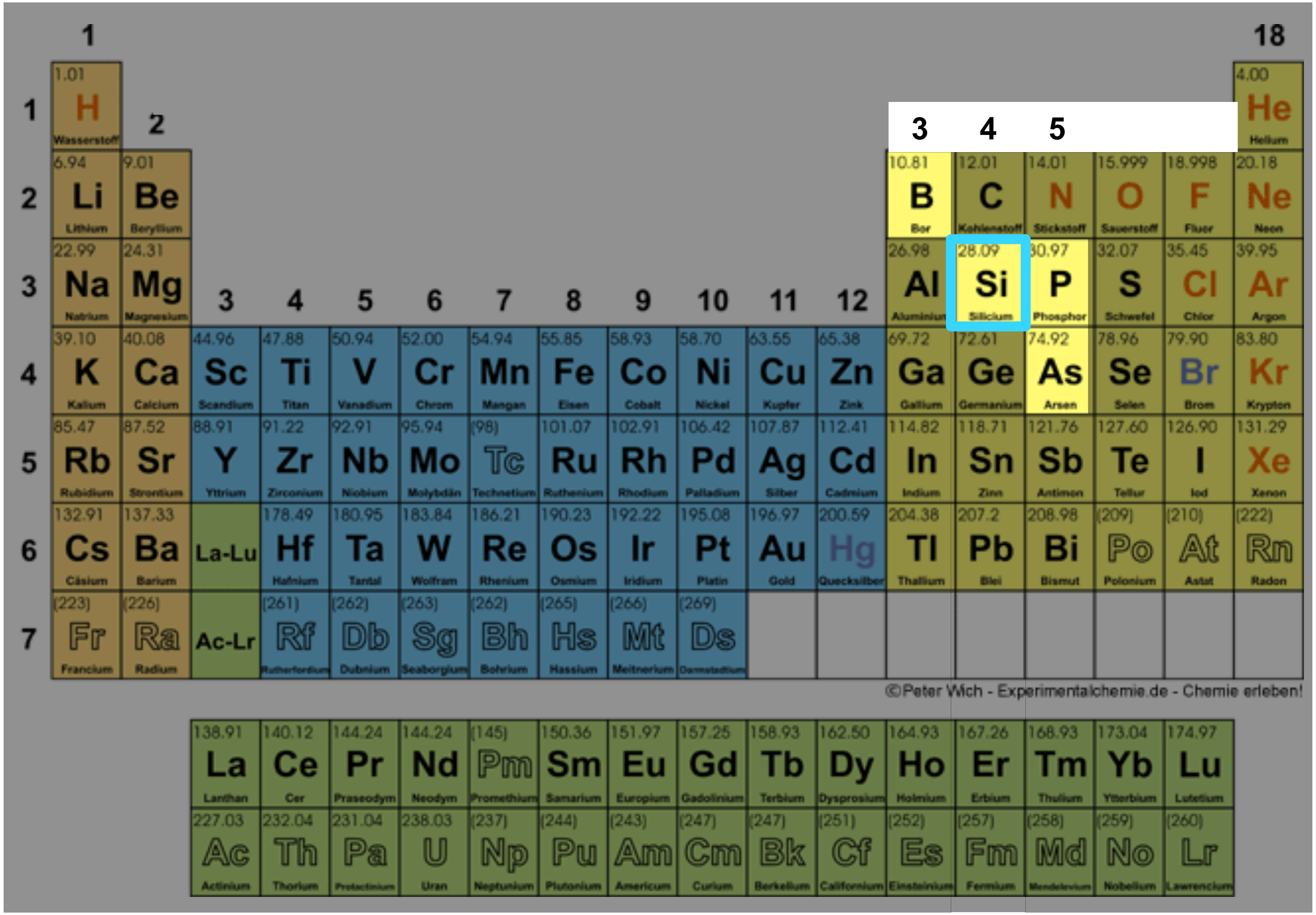
- E_{max} $\sim 3 \times 10^7$ V/m break through field strength

- E_{eh} 3.6 eV Av. Energy required to generate an e-h pair

- ρ 7.87 gcm^{-3} density
- λ 150 W / (mK) thermal conductivity
- α 2.56 $10^{-6}\ K^{-1}$ thermal expansion coefficient (e,g, Al: 23.1)

*Sproul AB, Green MA. Improved value for the silicon intrinsic carrier concentration from 275 to 375 K. Journal of Applied Physics. 1991;70:846-854. Available from: http://link.aip.org/link/?JAP/70/846/1

Silicon


1
18
2
3
4
5
1.01 H
4.00 He
6.94 Li
9.01 Be
10.81 B
12.01 C
14.01 N
15.999 O
18.998 F
20.18 Ne
22.99 Na
24.31 Mg
26.98 Al
28.09 Si
30.97 P
32.07 S
35.45 Cl
39.95 Ar
3 4 5 6 7 8 9 10 11 12
39.10 K
40.08 Ca
44.96 Sc
47.88 Ti
50.94 V
52.00 Cr
54.94 Mn
55.85 Fe
58.93 Co
58.70 Ni
63.55 Cu
65.38 Zn
69.72 Ga
72.61 Ge
74.92 As
78.96 Se
79.90 Br
83.80 Kr
85.47 Rb
87.52 Sr
88.91 Y
91.22 Zr
92.91 Nb
95.94 Mo
(98) Tc
101.07 Ru
102.91 Rh
106.42 Pd
107.87 Ag
112.41 Cd
114.82 In
118.71 Sn
121.76 Sb
127.60 Te
126.90 I
131.29 Xe
132.91 Cs
137.33 Ba
La-Lu
178.49 Hf
180.95 Ta
183.84 W
186.21 Re
190.23 Os
192.22 Ir
195.08 Pt
196.97 Au
200.59 Hg
204.38 Tl
207.2 Pb
208.98 Bi
(209) Po
(210) At
(222) Rn
(223) Fr
(226) Ra
Ac-Lr
(261) Rf
(262) Db
(263) Sg
(262) Bh
(265) Hs
(266) Mt
(269) Ds
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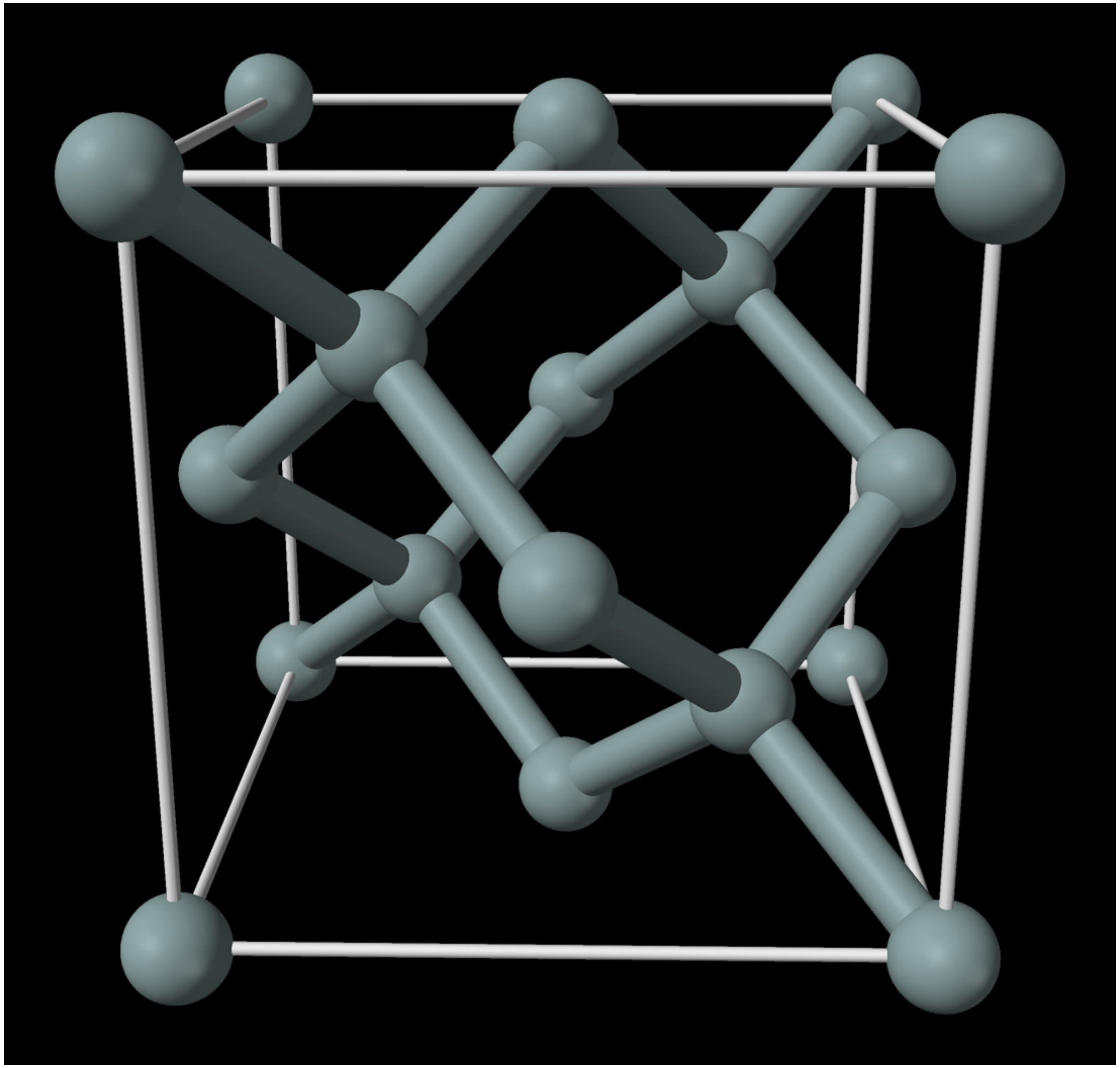
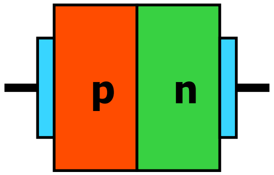
138.91 La
140.12 Ce
144.24 Pr
144.24 Nd
(145) Pm
150.36 Sm
151.97 Eu
157.25 Gd
158.93 Tb
162.50 Dy
164.93 Ho
167.26 Er
168.93 Tm
173.04 Yb
174.97 Lu
227.03 Ac
232.04 Th
231.04 Pa
238.03 U
(237) Np
(244) Pu
(243) Am
(247) Cm
(247) Bk
(251) Cf
(252) Es
(257) Fm
(258) Md
(259) No
(260) Lr

Silicon Crystal



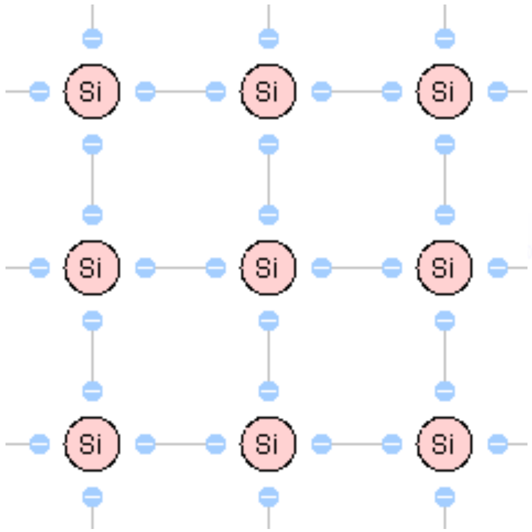
Face centered
Cubic lattice

The Diode (p-n-junction)

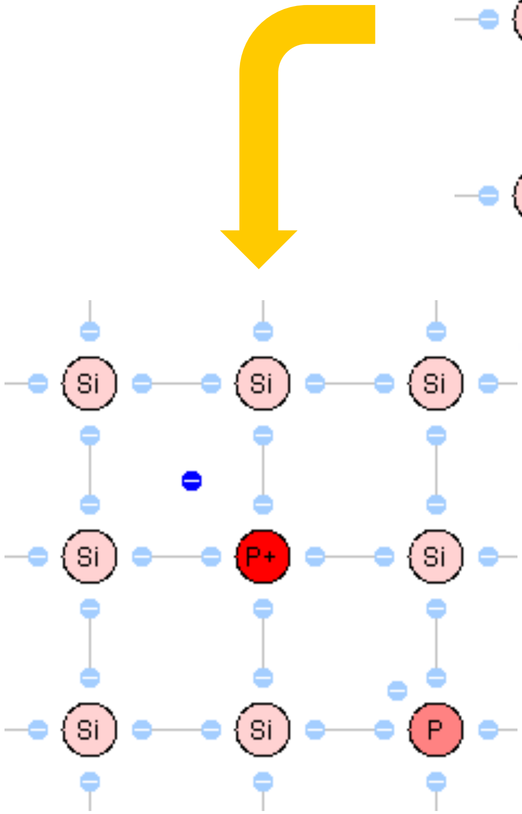


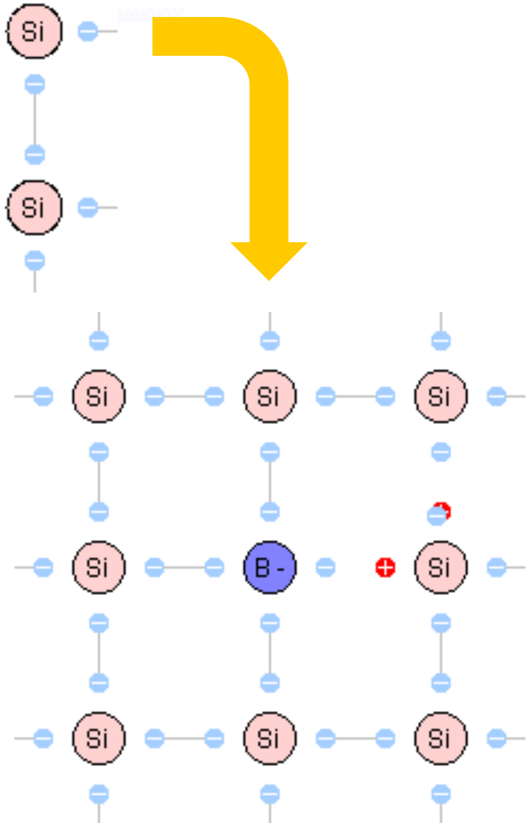
Silicon: Crystal & Doping

Doping with 5-valued DONOR atoms:
- electrons can escape easily
- **N-conductor**
- Remaining donor atoms are **positive**



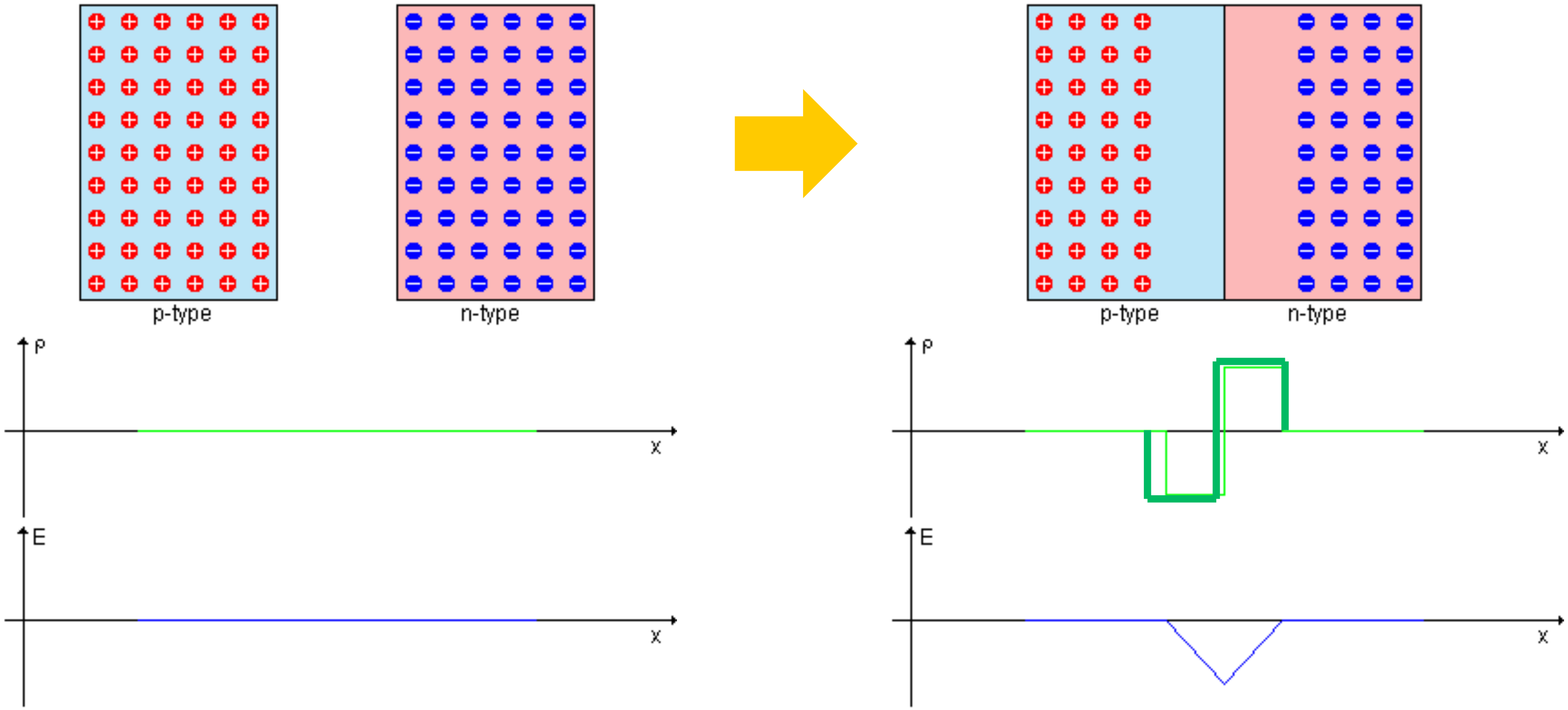
Doping with 3-valued ACCEPTORs:
- electrons jump from atom to atom
- this is like a positive moving charge
- **P-conductor**
- Remaining acceptors are **negative**



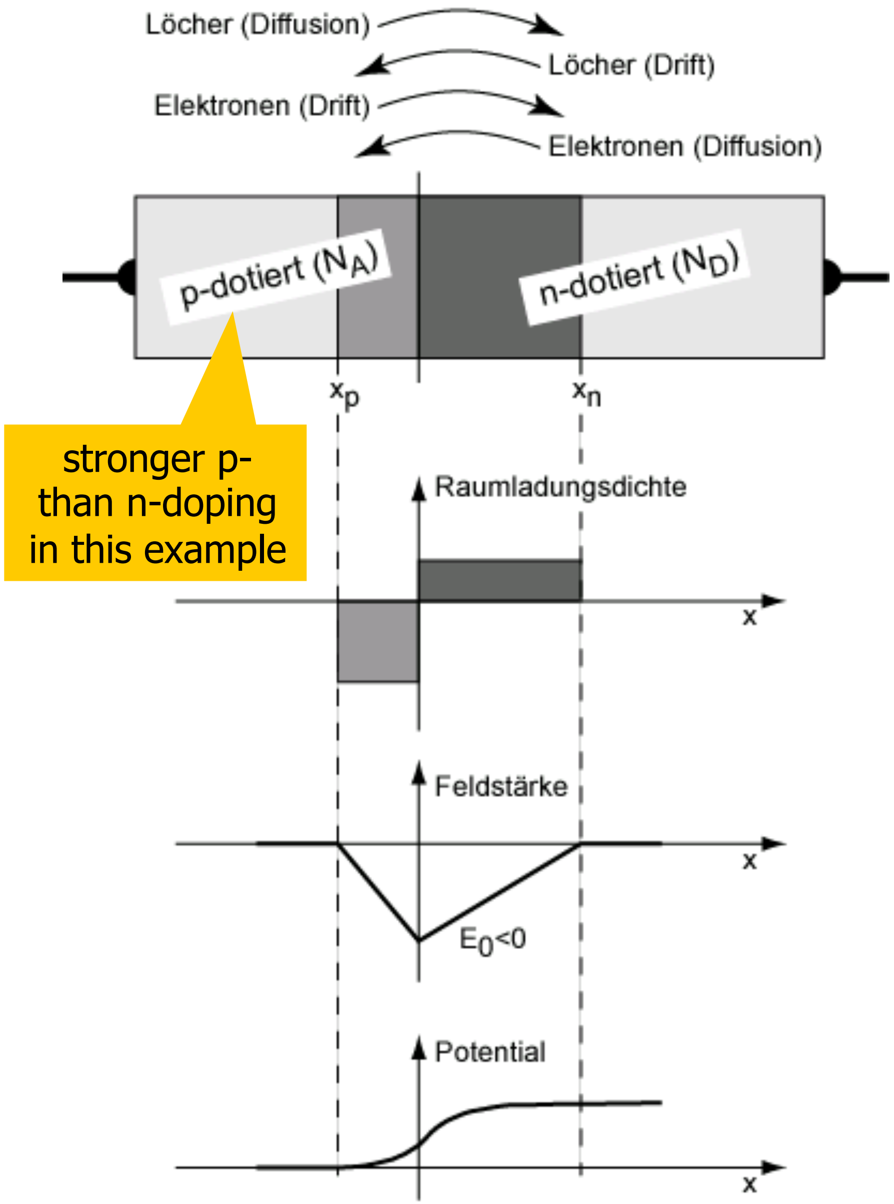


The pn-junction (diode)

- Bringing together a p- and n doped region:
  - A depletion zone with no charge carriers is created
  - There is a space charge
  - -> There is an electric field



Origin of Depletion Layers



- We consider an idealized, 'abrupt' transition between n- and p- region (this is smooth in reality)

- Due to the concentration gradient, electrons diffuse from the n → p region (holes from p → n).
- The carriers compensate and we get depleted regions without mobile carriers

- The fixed, ionized atoms are positively charged in the n-region (negatively in the p-region)
- This leads to an electric field
- The field is associated with a electrostatic potential. This 'built in' potential depends only on doping.
- The field leads to a drift of electrons/holes backwards.
- **The thickness of the depletion region is determined by the equilibrium between drift- and diffusion currents**

- In reality, the depletion zone drops more slowly to zero, but the transition region is small.

Derivation of the Build-In Voltage

- Derivation steps (see extra file on web site for explanations)
  - p(x)= hole density):

$$
\begin{aligned}
j_{Feld}(x) &= -j_{Diff}(x) \\
q\,\mu\,p(x)E(x) &= q\,D\frac{dp(x)}{dx} \\
-\frac{q}{kT}dV(x) &= \frac{dp(x)}{p(x)} \\
-\frac{q}{kT}\int_{V_p}^{V_n} dV(x) &= \int_{p_p}^{p_n}\frac{dp(x)}{p(x)} \\
-\frac{q}{kT}(V_n - V_p) &= \ln\left(\frac{p_n}{p_p}\right) \\
V_{bi} := V_n - V_p &= \frac{kT}{q}\ln\left(\frac{p_p}{p_n}\right)
\end{aligned}
$$

$$
\begin{aligned}
V_{bi} &= \frac{kT}{q}\ln\left(\frac{N_A N_D}{n_i^2}\right) \\
&\approx \left[\log\left(\frac{N_A}{n_i}\right) + \log\left(\frac{N_D}{n_i}\right)\right] \times 60\,\mathrm{mV}
\end{aligned}
$$

V_{bi} is often also called 'Diffusion Voltage'

- kT/q is a quantity which occurs often
- It is called the 'Thermal Voltage'
- It is ~26mV at room temperature

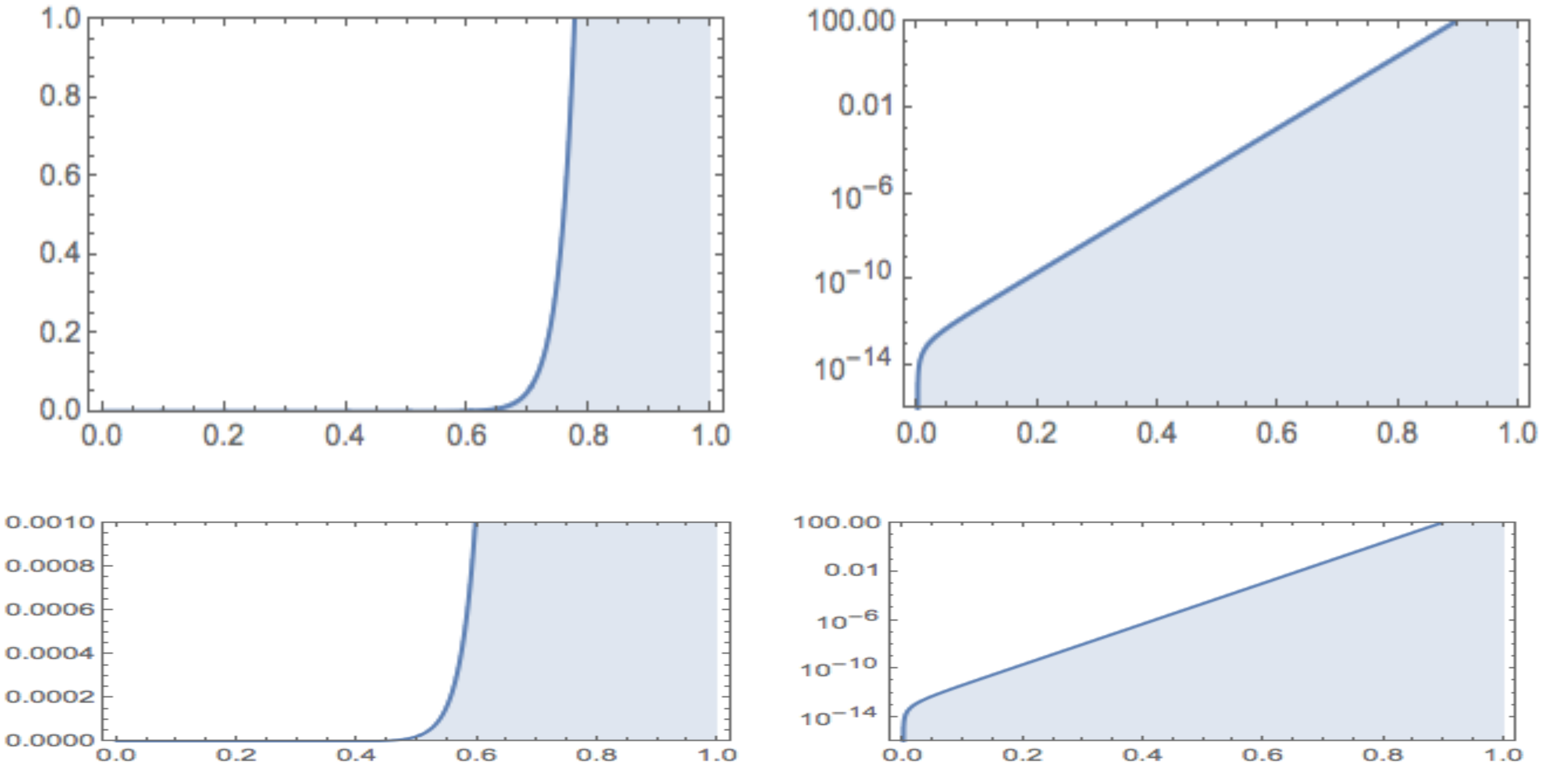
For typical doping concentrations, this is a few 100 mV

Applying an External Voltage

- An external voltage superimposes an additional field and thus *changes the drift contribution*
- The equilibrium *thickness is changed*
- When a positive voltage is applied to the p-side, the overall field is reduced, diffusion becomes stronger and ultimately an increasing current flows
  - To really understand this, solid state physics is required
- It turns out that $I_D = I_S(e^{U_D/U_{TH}} - 1)$
  - Diode current is exponential in a VERY wide range
  - U_D = Diode applied to device (relative to n-Side)
  - I_S = Saturation Current = Device property (mainly just size)
  - U_{TH} = Thermal Voltage = k T / q = 25.9mV @ RT

Diode Forward Current

- For I_S=0.1pA, U_{th} = 25.9 mV
- No magic ‘0.6V’ forward voltage, depends on 'scale'!



Thickness of Depleted Region (See also extra file)

- Charge on both sides must be equal:

$$\begin{aligned} Q_p &= -Q_n \\ A x_p q N_A &= -A x_n q N_D \\ x_p N_A &= -x_n N_D. \end{aligned}$$

- Field at junction:

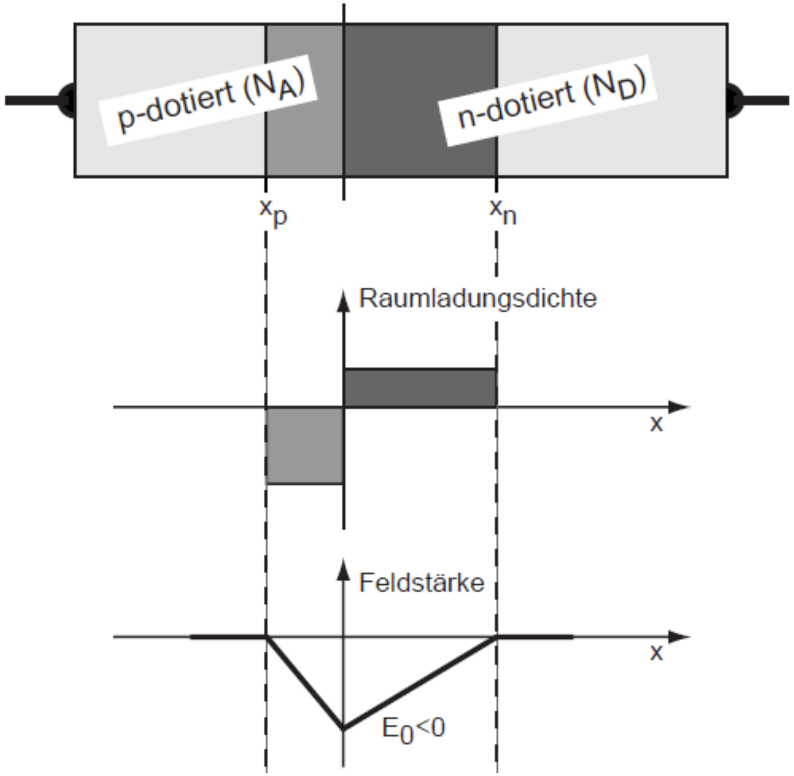
$$E_{max} = \frac{q}{\epsilon} x_p N_A < 0.$$

- Potential = V_{bi}:

$$\Delta V = -\int_{x_p}^{x_n} E(x)dx = -\frac{1}{2}(x_n$$

$$= \frac{q}{2\epsilon}\frac{(N_A+N_D)N_A}{N_D}{x_p}^2$$

$$x_d = \sqrt{\frac{2\epsilon}{q}\frac{N_A+N_D}{N_A N_D}V_{bi}}\sqrt{1-\frac{V_{ext}}{V_{bi}}}$$



Dominated by low doped side! $\sqrt{\frac{2\epsilon}{q}\frac{V_{bi}}{N_D}}$

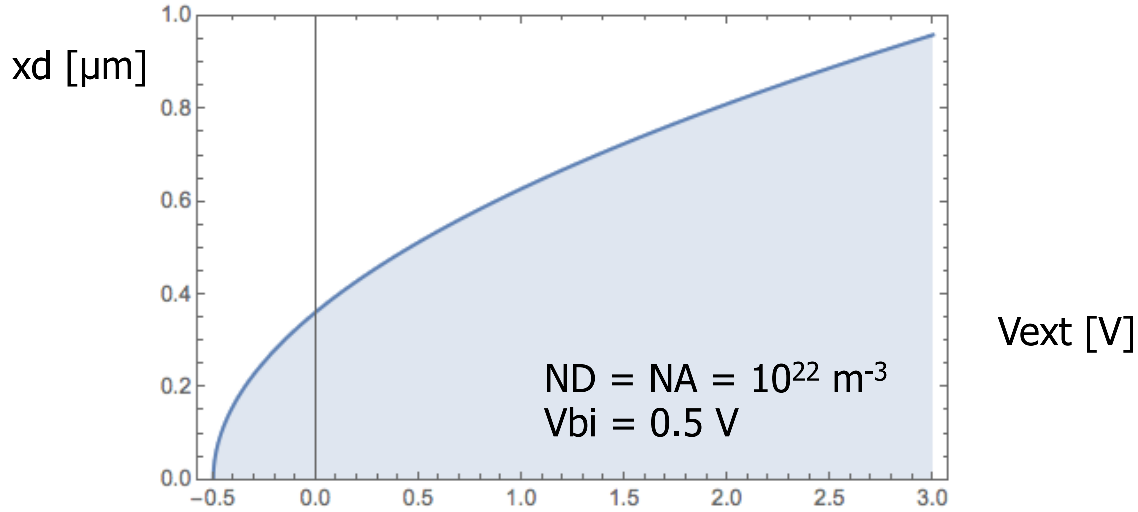
- Note: Depletion is thick for LOW doping

Dependence on External Voltage

- For the considered *abrupt* junction (p changes to n with no transition), we have

$$x_d = \sqrt{\frac{2\epsilon}{q}\frac{N_A+N_D}{N_A N_D}V_{bi}}\sqrt{1-\frac{V_{ext}}{V_{bi}}}$$

  i.e. the thickness of the depletion region increases as the *square root* of the external voltage (for voltages >> Vbi)



- Typical values on chips: < 1 µm

Capacitance

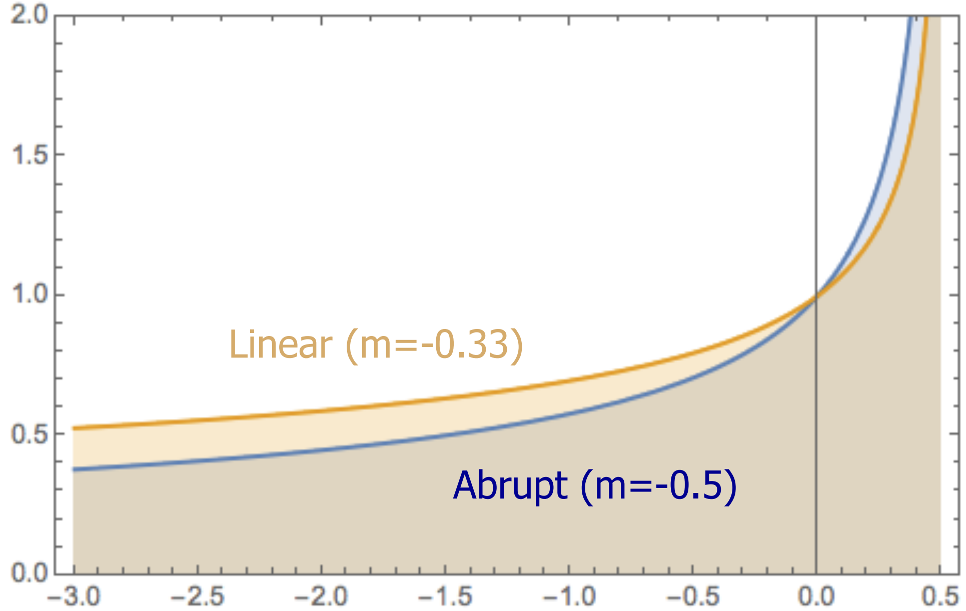
- The depletion region defines a parallel plate capacitor

$$C_j = \epsilon_0 \cdot \epsilon_{Si} \cdot \frac{A}{x_d}$$

$$\frac{C_j}{A} = \underbrace{\sqrt{\frac{q\epsilon_0\epsilon_{Si}}{2}\frac{N_A N_D}{N_A + N_D}\frac{1}{V_{bi}}}}\left(1 - \frac{V_{ext}}{V_{bi}}\right)^{-1/2}$$

$$= C_{j0} \cdot \left(1 - \frac{V_{ext}}{V_{bi}}\right)^{-1/2}$$

Depends on doping profile:
0.5 for abrupt junction
0.33 for linear junction



Diode Summary

- Diode is conducting, when p-region is at positive voltage
- Forward current $I_D = I_S(\exp(V_D/U_T) - 1)$.
  ($U_T = kT/q \sim 26mV$ @ 300K). I increases x 10 every 60mV

- E-Field is largest at the junction
- Potential increases quadratically (in constant doping)

- Depletion region grows towards **low doped side**.
- Growth with √ of applied voltage $\sqrt{\frac{2\epsilon}{q} \frac{V_{bi}}{N_D}}$
- Capacitance decreases

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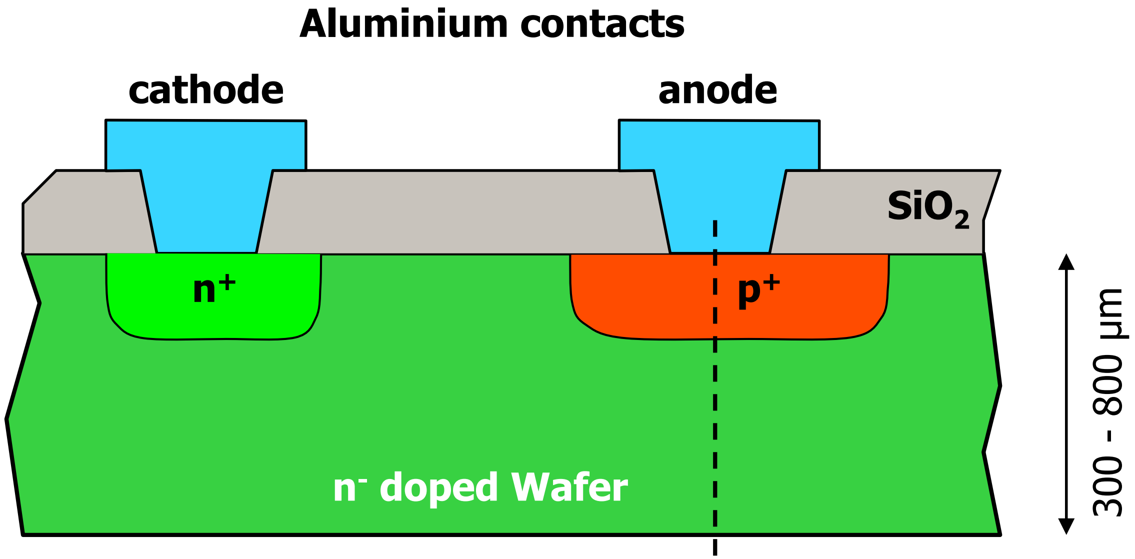
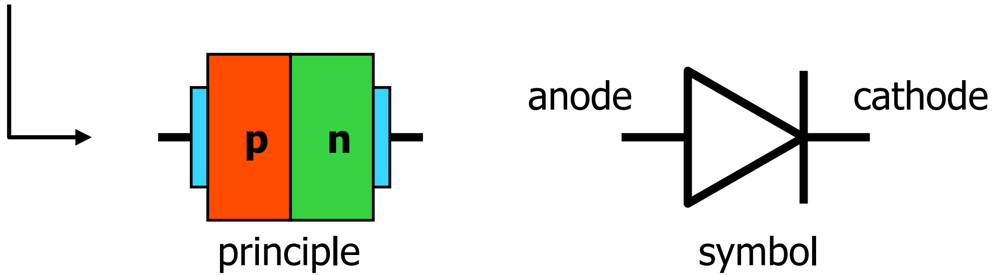
DIODE MODEL

A pn-Diode on a Chip Wafer

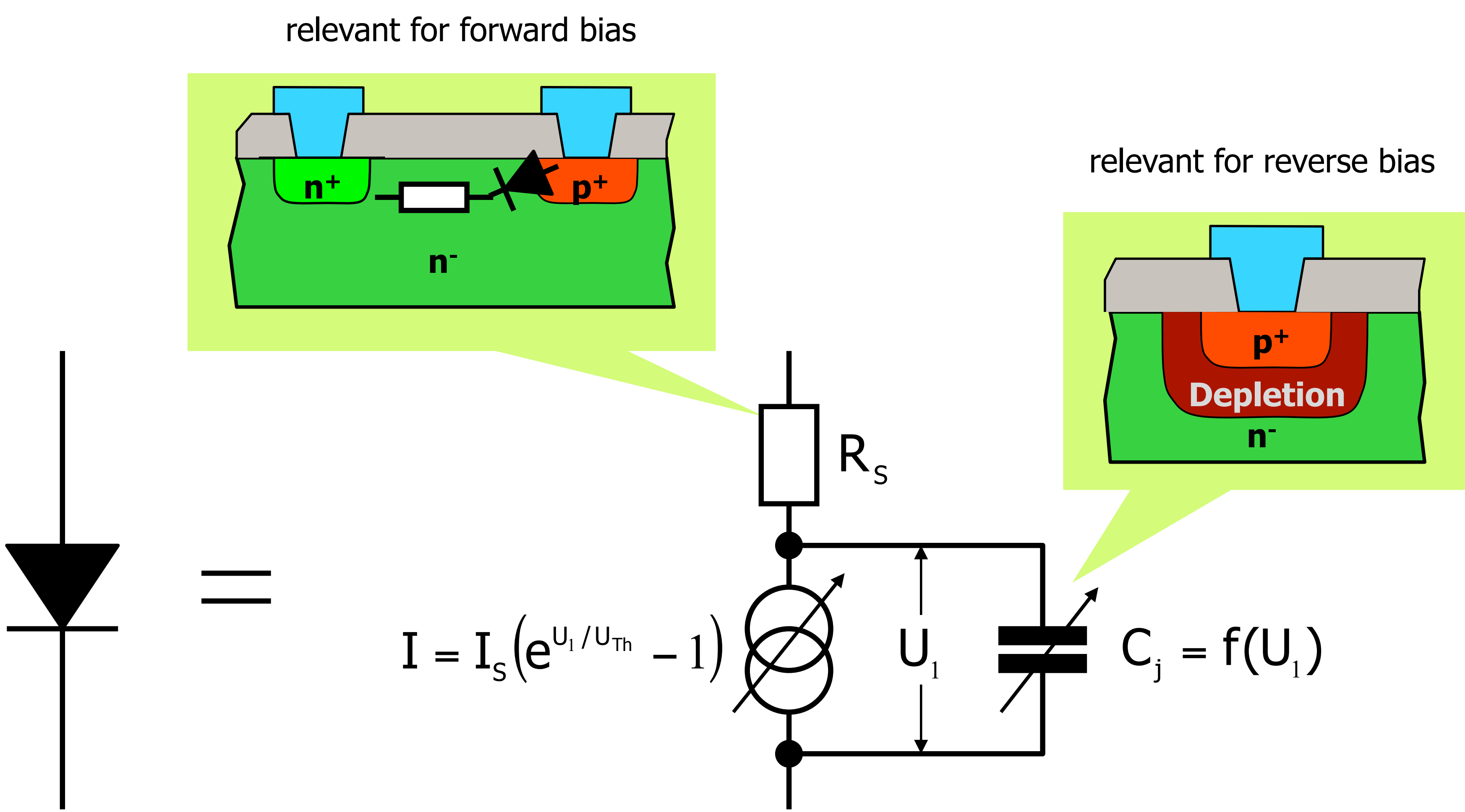
- For instance: n-doped Si 'Wafer' is p-doped at the surface
- EACH pn junction forms a diode



Cross section of an pn-junction on a wafer



Modell of the Diode



Important SPICE Parameters of the Diode

Parameter	Symbol	SPICE Name	Einheit	Default
Sättigungsstrom (Saturation current)	I_S	IS	A	1e-14
Serienwiderstand (Series resistance)	R_S	RS	Ohm	0
Sperrschichtkapazität bei VD=0V (Zero bias junction cap.)	C_{j0}	CJ0	F	0
Exponent in Kapazitätsformel (Grading Koefficient)	m	M	-	0.5
Diffusionsspannnung (Junction Potential)	Φ_0	VJ	V	1
Emissionskoeffizient (Emission Coefficient)	n	N	-	1
Transitzeit (Transit time)	τ_T	TT	s	0

- The values are for a unit size device. They are later multiplied by the diode AREA
- For capacitances, there are often two parameter sets for the AREA of the diode and the (lateral) SIDEWALL. Both contributions are added
- Transit time tells how long it takes for carriers to pass the depletion region.

Simple Small Signal Model

- Determine the slope at the working point:

$$I \approx I_S \cdot e^{U/U_{Th}}$$

$$\frac{\partial I}{\partial U} \approx \frac{1}{U_{Th}} \cdot I_S \cdot e^{U/U_{Th}} = \frac{I}{U_{Th}}$$

$$\Rightarrow R_{eq}(U_0) = \frac{U_{Th}}{I_0}$$