



# Exercise: The MOS Transistor

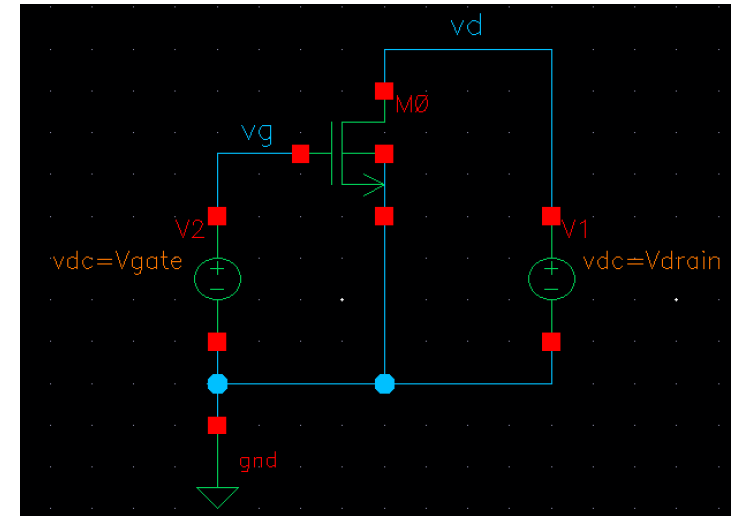
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# Exercise 1: Simple MOS (Level 1 model)

- We want to simulate a MOS with a very simple model (as the formula shown in the lecture)
- Create a schematic which allows you to set  $V_G$  and  $V_D$  of a MOS:
- Use 'nmos4' from 'analogLib'
- Attach the model 'nmossimple' (see diode exercise. Add path!)



- Use the following model:

```
.model nmossimple nmos level=1
+ cox=1e-3 kp=100e-6 lambda=0.1 tox=10e-9 gamma=0.5
vto=0.5
```

- Plot

- $I_D$  for  $V_G=0..2$  V with  $V_D=2$ V (Transfer characteristic)
- $\sqrt{I_D}$  for  $V_G=0..2$  V with  $V_D=2$ V (Sqrt of transfer characteristic)
- $I_D$  for  $V_D=0..2$  V with  $V_G=1$ V (Output characteristic)



## Exercise 2: Output Resistance

- Sweep  $I_D$  for  $V_D=0..2$  V with  $V_G=1V, 1.5V, 2V$
- What are the slopes at high drain voltages ?
- Do they correspond to what you expect ?



## Exercise 3: A real MOS

- Now use the model 'nmos' provided in the file **MOSLib.lib** on the course web site (this MOS should be operated below 2V)
- Compare the transfer curves of a 'nmossimple' and 'nmos'
  - Are they both exactly quadratic?
  - What happens at low gate voltages (below threshold)?  
Do a logarithmic plot!



## Exercise 4: Sizing the MOS

- Set the properties  $W$  and  $L$  of both types of MOS to  $WL$
- Compare the output characteristics for  $WL=1\mu$  and  $WL=10\mu$  for both MOS
  - Is there a change in output resistance if you change the geometry?



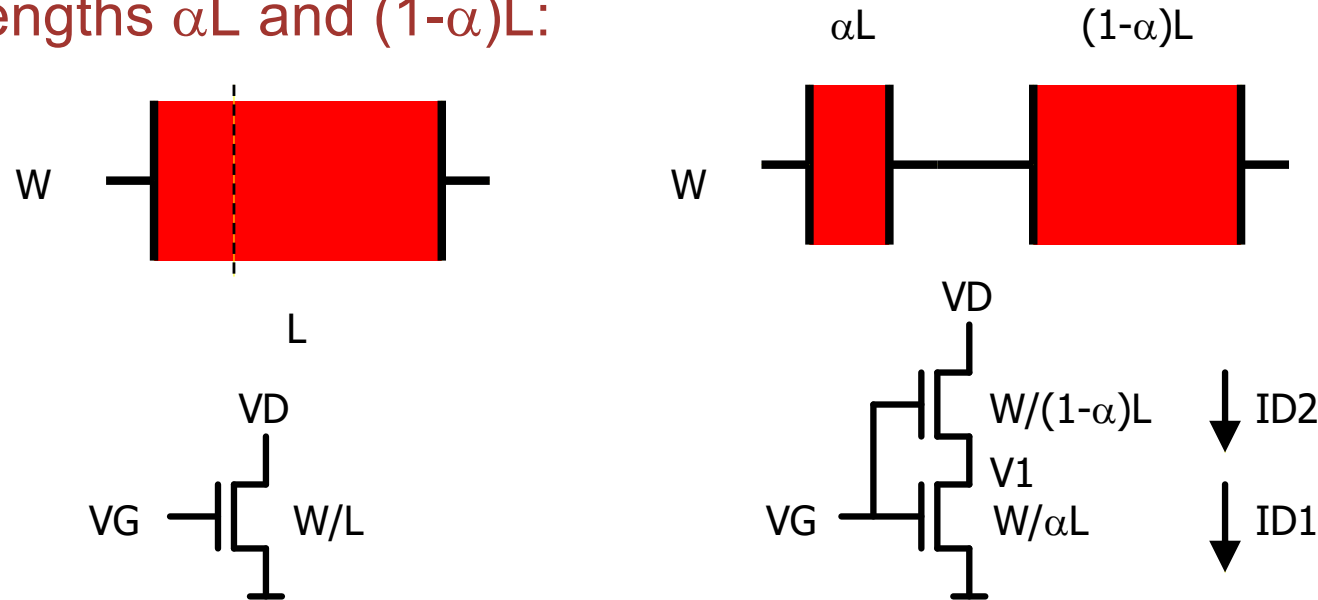
## Exercise 5: PMOS

- Simulate transfer and output characteristic for a PMOS
  - Note that the source of the transistor is now ,on top‘
  - Gate and drain must be negative with respect to source
- Simulate in parallel a NMOS of the same size.
  - Plot the drain current of NMOS and PMOS simultaneously.
  - How big is the difference?
  - Does that fit the model?



## Exercise 6: Formulae match...

- A MOS with width  $W$  and length  $L$  is cut in two devices with lengths  $\alpha L$  and  $(1-\alpha)L$ :



- The series connection must behave as the single device!
- Assume a large  $V_D$ . In which regimes do the 2 MOS operate (lin. / sat.?). Write down the formulae for  $ID_1$  and  $ID_2$
- The currents must be equal. Find  $\alpha$ . Then find  $ID_1$  ( $=ID_2$ )
- Is this the current of the single MOS?
- How large is  $V_1$  for  $\alpha=5/9$  ?