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Exercise:
The MOS Transistor

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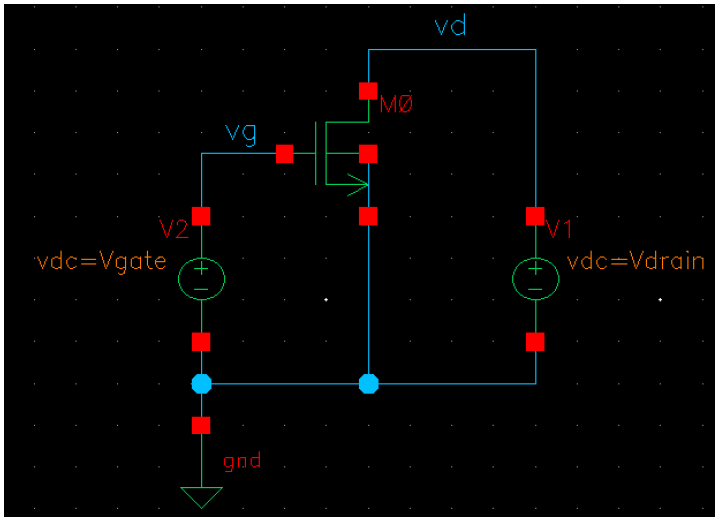
Exercise 1: Simple MOS (Level 1 model)

- We want to simulate a MOS with a very simple model (as the formula shown in the lecture)
- Create a schematic which allows you to set V_G and V_D of a MOS:
- Use ‘nmos4’ from ‘analogLib’
- Attach the model ‘nmossimple’ (see diode exercise. Add path!)

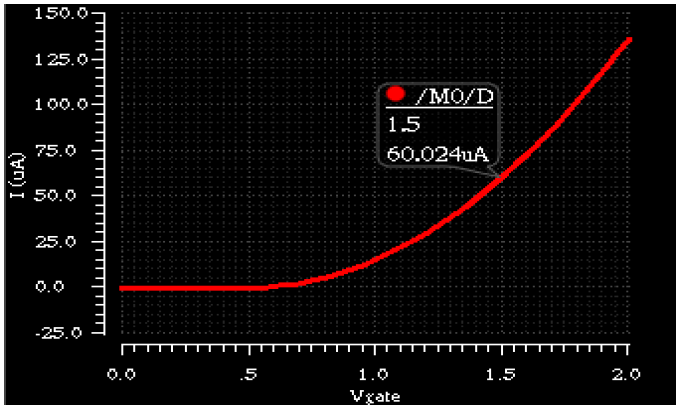


- Use the following model:

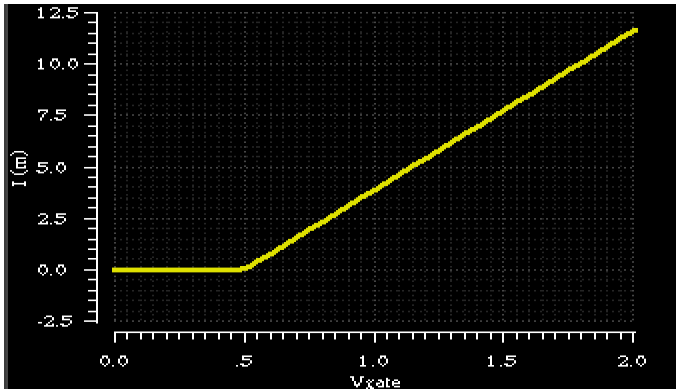
```
.model nmossimple nmos level=1
+ cox=1e-3 kp=100e-6 lambda=0.1 tox=10e-9 gamma=0.5
vto=0.5
```

- Plot
  - I_D for V_G=0..2 V with V_D=2V (Transfer characteristic)
  - $\sqrt{I_D}$ for V_G=0..2 V with V_D=2V (Sqrt of transfer characteristic)
  - I_D for V_D=0..2 V with V_G=1V (Output characteristic)

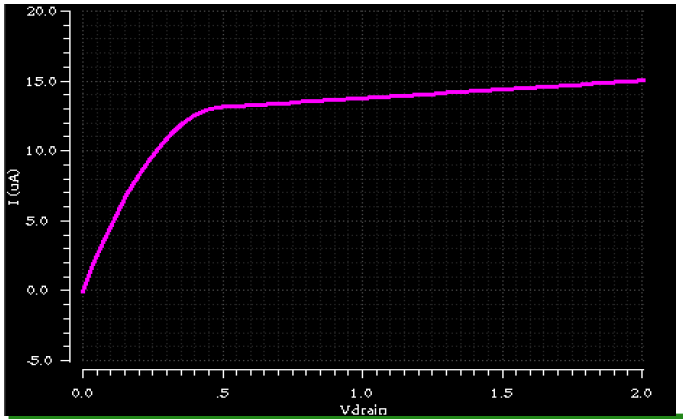
Solution 1



- Transfer (linear y scale)
  - Current at V_G=1.5V is
    I_D=K/2 $(V_G-V_T)^2(1+\lambda V_D)$
    = 50 × 1 × (1+0.1 × 2) µA
    = 50 × 1.2 µA = 60 µA



- Sqrt(..) plot shows exact quadratic behaviour ('level 1 model')



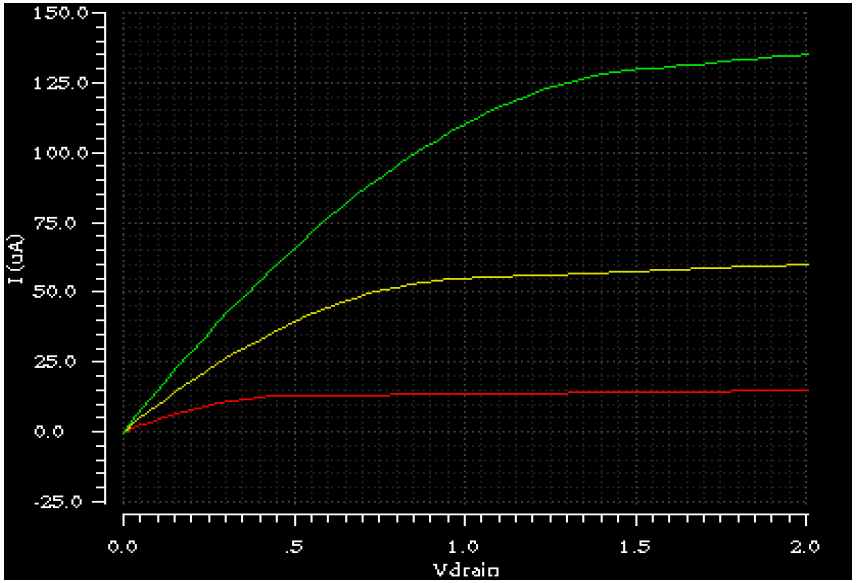
- Output Char. shows Early effect
  - Current at kink is
    I_D=K/2 $(V_G-V_T)^2(1+\lambda V_D)$
    = 50 × 0.5^2 × (1+0.1×0.5) µA
    = 12.5 × (1.05) µA

Exercise 2: Output Resistance

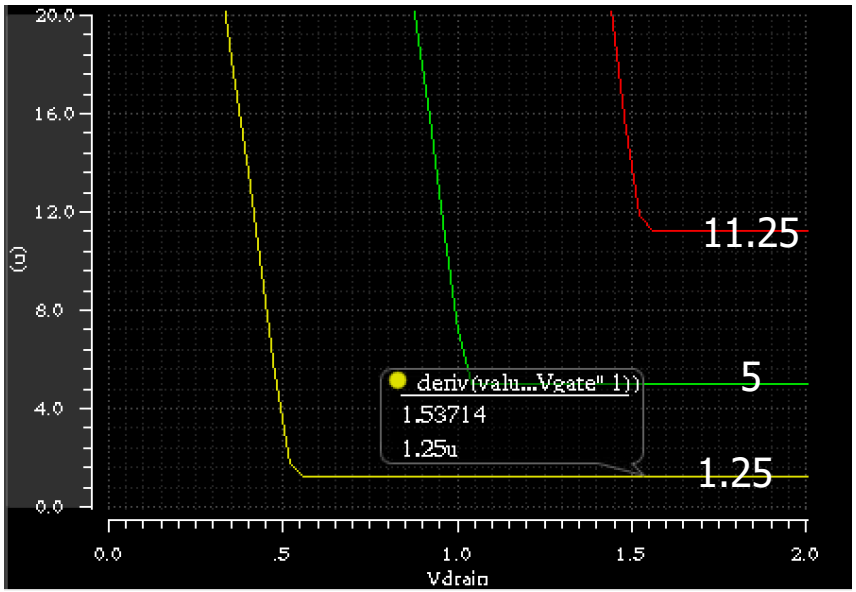
- Sweep I_D for V_D=0..2 V with V_G=1V, 1.5V, 2V

- What are the slopes at high drain voltages ?
- Do they correspond to what you expect ?

Solution 2



- Saturation point increases
- Current increases

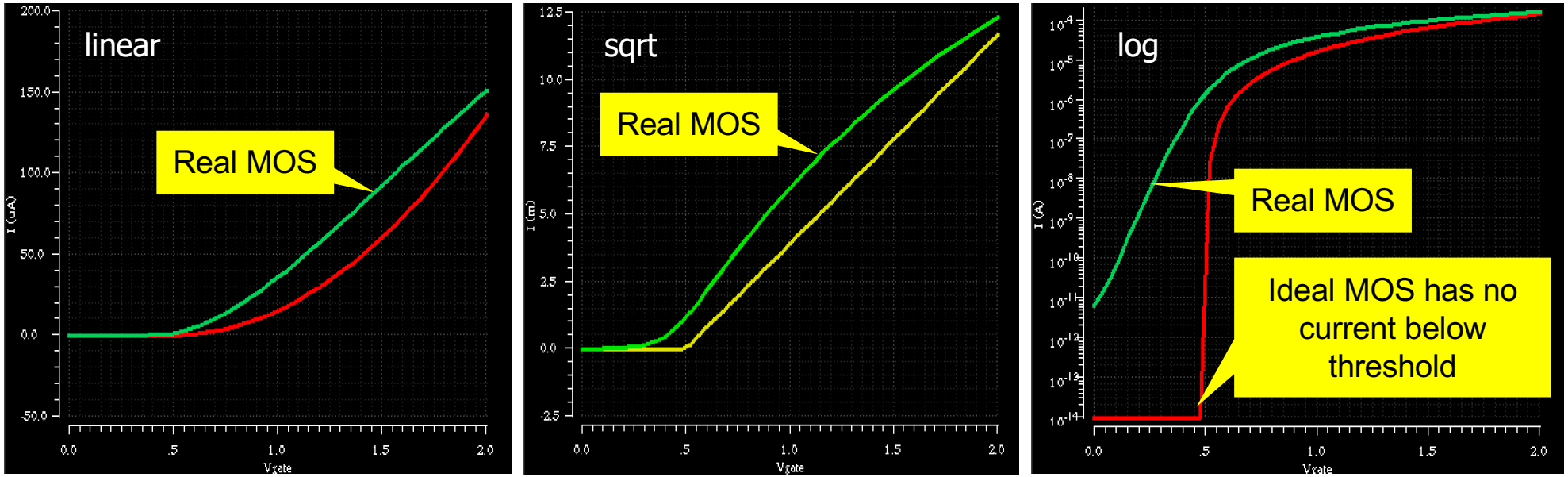


- $I_D = K/2\ (V_G-V_T)^2(1+\lambda\ V_D)$
- $dI_D/dV_D = \lambda\ K/2\ (V_G-V_T)^2$
  $= 0.1 \times 50 \times (0.5/1/1.5)^2$
  $= 5 \times (0.25/1/2.25)$
  $= 1.25/5/11.25$
  as simulated!

Exercise 3: A real MOS

- Now use the model ‘nmos’ provided in the file **`MOSLib.lib`** in moodle (this MOS should be operated below 2V)
- Compare the transfer curves of a ‘nmossimple’ and ‘nmos’
  - Are they both exactly quadratic?
  - What happens at low gate voltages (below threshold)? Do a logarithmic plot!

Solution 3:

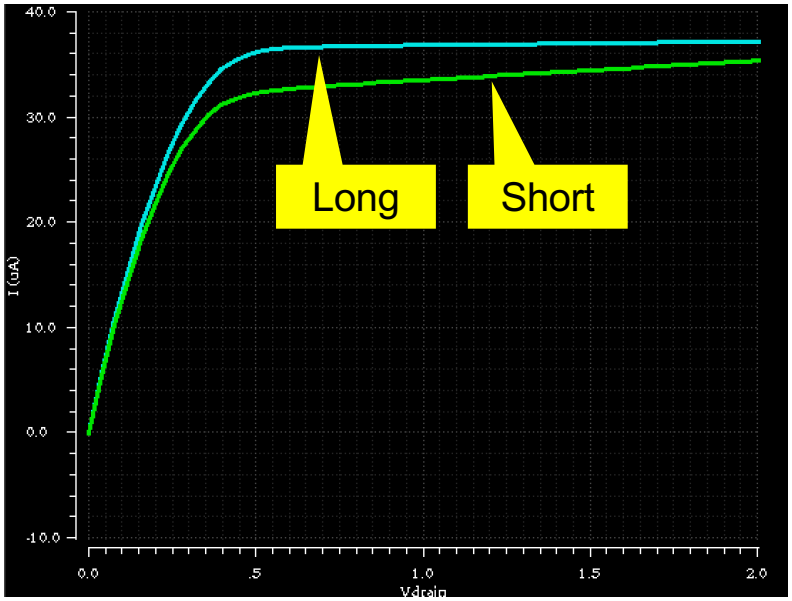


- Real MOS is not quadratic
  - Velocity saturation at high Gate voltages
  - Current >0 in weak inversion (below threshold)

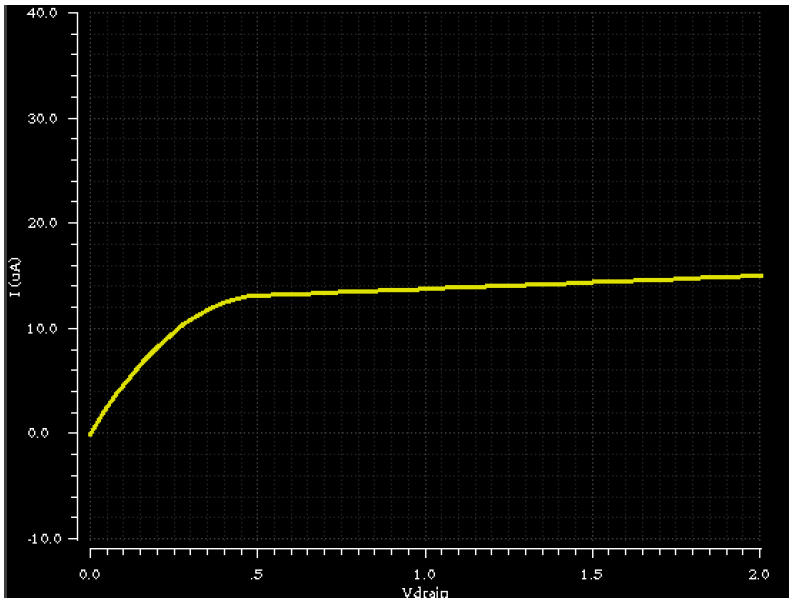
Exercise 4: Sizing the MOS

- Set the properties W and L of both types of MOS to WL
- Compare the output characteristics for WL=1u and WL=10u for both MOS
  - Is there a change in output resistance if you change the geometry?

Solution 4:



- For the real MOS, the output resistance increases, when L is increased



- For the ‘nmossimple’ , there is NO difference (both curves are the same). This model is clearly too simplistic!

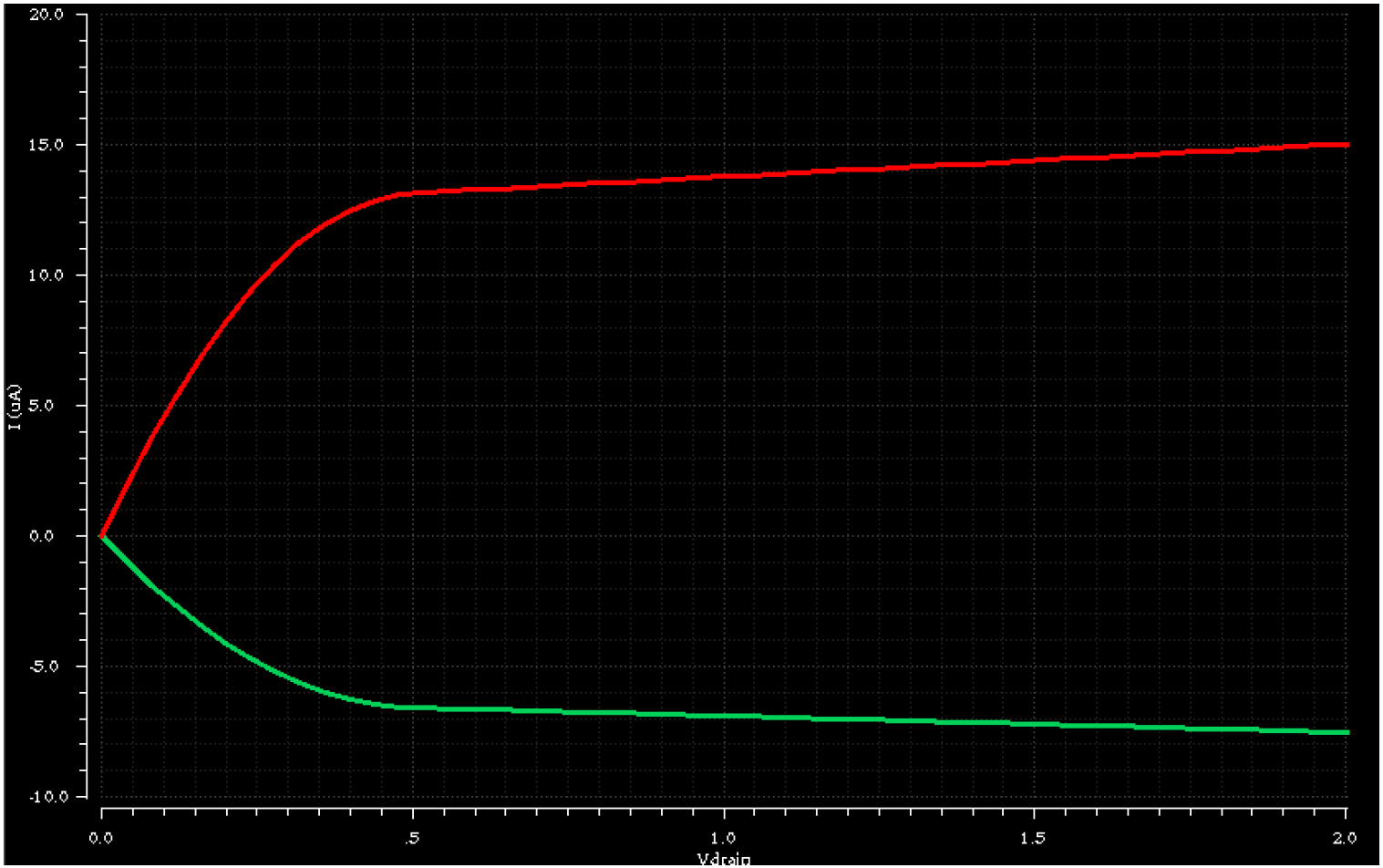
Exercise 5: PMOS

- Simulate transfer and output characteristic for a PMOS
  - Note that the source of the transistor is now ‚on top'
  - Gate and drain must be negative with respect to source

- Simulate in parallel a NMOS of the same size.
  - Plot the drain current of NMOS and PMOS simultaneously.
  - How big is the difference?
  - Does that fit the model?

Solution 5

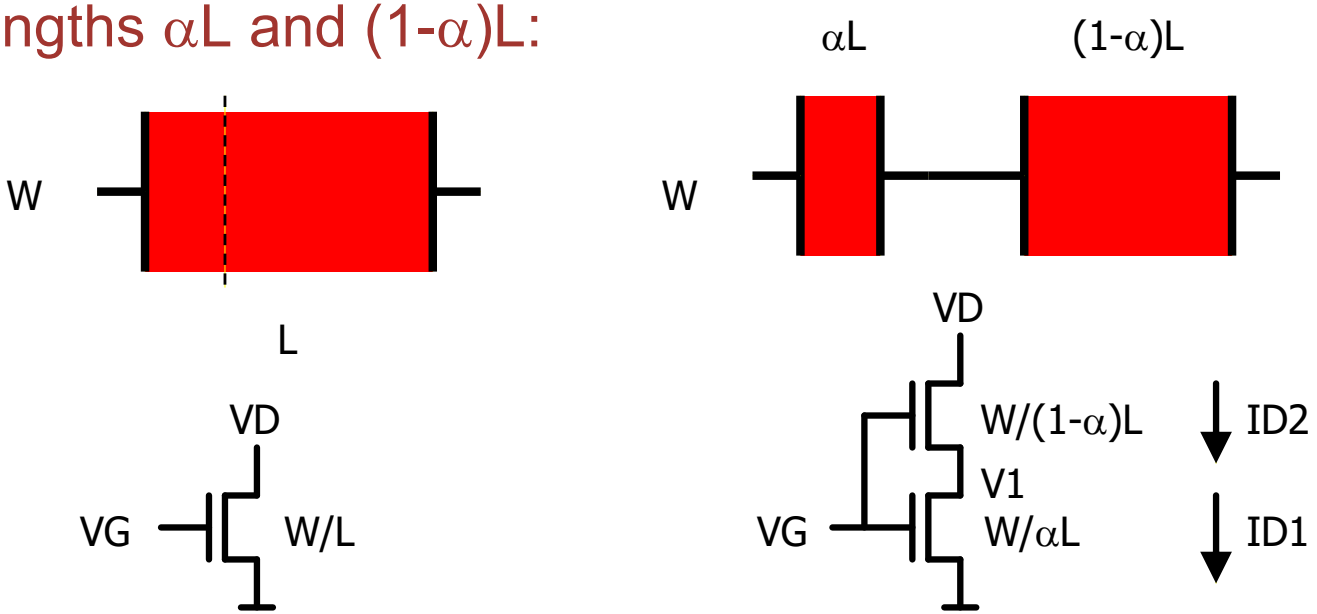
- Here for simple models:



- Ratio is exactly 3, the ratio of the kp parameters

Exercise 6: Formulae match…

- A MOS with width W and length L is cut in two devices with lengths αL and (1-α)L:



- The series connection must behave as the single device!
- Assume a large VD. In which regimes do the 2 MOS operate (lin. / sat.?). Write down the formulae for ID1 and ID2
- The currents must be equal. Find α. Then find ID1 (=ID2)
- Is this the current of the single MOS?
- How large is V1 for α=5/9 ?

Solution 6:

```
In[63]:= ILin[Vgs_, Vds_] = (Vgs - Vt) Vds - 1/2 Vds^2;
         ISat[Vgs_, Vds_] = 1/2 (Vgs - Vt)^2;

In[91]:= EQ1 = W/(α L) ILin[VG, V1] == W/((1 - α) L) ISat[VG - V1, VD - V1] // Simplify

Out[91]= (W (V1^2 - 2 V1 (VG - Vt) + (VG - Vt)^2 α))/(L (-1 + α) α) == 0

In[67]:= αsol = α /. First@Solve[EQ1, α] (* find α *)

Out[67]= (-V1^2 + 2 V1 VG - 2 V1 Vt)/(VG - Vt)^2

In[69]:= I2 = W/(α L) ILin[VG, V1] /. α -> αsol // Simplify (* Find current *)

Out[69]= (VG - Vt)^2 W/(2 L)

In[71]:= I2 == W/L ISat[VG, VD] // Simplify (* Compare to single MOS *)

Out[71]= True

In[72]:= $Assumptions = VG > Vt;

In[73]:= V1sol = V1 /. First@Solve[EQ1, V1] // Simplify

Out[73]= -(VG - Vt) (-1 + Sqrt[1 - α])

In[74]:= V1sol /. α → 5 / 9

Out[74]= (VG - Vt)/3
```

Exercise 5: Drain Capacitance

- Charge the drain capacitance of the ‘real’ MOS to determine its C(V) curve
  - Set V_G to 0 to turn the drain current off
  - Add a small cap in parallel to define the start voltage 0 V

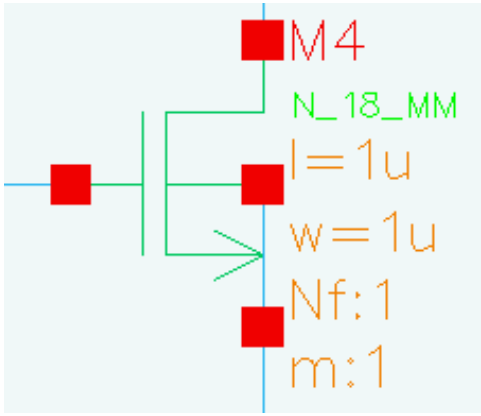
1: Transfer Characteristic & Transconductance

- For an NMOS of W=L=1µm with V_{BS} = 0, keep the drain at 1.8 V and sweep the gate voltage from 0 to 1.8 V. This is the *transfer characteristic* of the MOS.
  - Observe the drain current
  - Plot the square root of the current. Do you find a straight line as expected?
  - Plot the current in log scale. Can you see the sub-threshold region?
  - What is the transconductance at V_{GS} = 1V (make a derivative!)?
- Make a parametric sweep changing W from 0.24µm to 2µm
  - Is the current proportional to W?
- Repeat this for a L-sweep (start with 180nm)

- Plot the transfer curve for two different values of V_{BS}, for instance 0 V and -2 V

Exercise 1: NMOS in Linear Region

- Use an *NMOS* transistor of type N_18_MM from library UMC_18_CMOS with W=L=1µm
- Connect
  - source and bulk to ground
  - the gate to 2 V



- Sweep V_{DS} from -0.1V to 0.1 V and observe the current
- Extract the resistivity of the channel
- Double W *or* L and simulate & extract again.
  - Are the results as expected ? Compare W=L=1µ and W=L=2µ!
- Now sweep the *gate* voltage from 0.6 V to 2 V. Explain!
- Now sweep the *drain* voltage from 0V to 1V. Verify the saturation point for a few gate voltages.
- What happens if you sweep the drain voltage from -1V on?

Exercise 3: Output Characteristic, Saturation

- Now plot the output characteristic, i.e. I_D as a function of V_{DS} for a fixed V_{GS} (for instance V_{GS} = 1.0 V)
  - Can you see the linear region and the saturated region?
- Extract the output resistance for instance for V_{GS}=1.8V and V_{DS}=1.8V (derivative!).
- Plot the output characteristic for V_{GS} =0..1.8V in 0.2V steps
  - Observe how the current changes
  - Observe how the saturation voltage changes
  - Observe how the output resistance changes (Early voltage ?)

- Now use two NMOS with different W (for instance 0.5µm and 2µm).
  - Search for gate voltages so that the currents for a given V_{DS} (for instance for 1.8 V) are similar.
  - Compare the output characteristics & saturation voltages