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Exercise:
Current Mirrors

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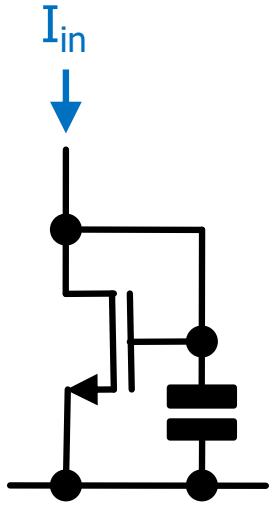
Exercise 1: Dynamic Regulation

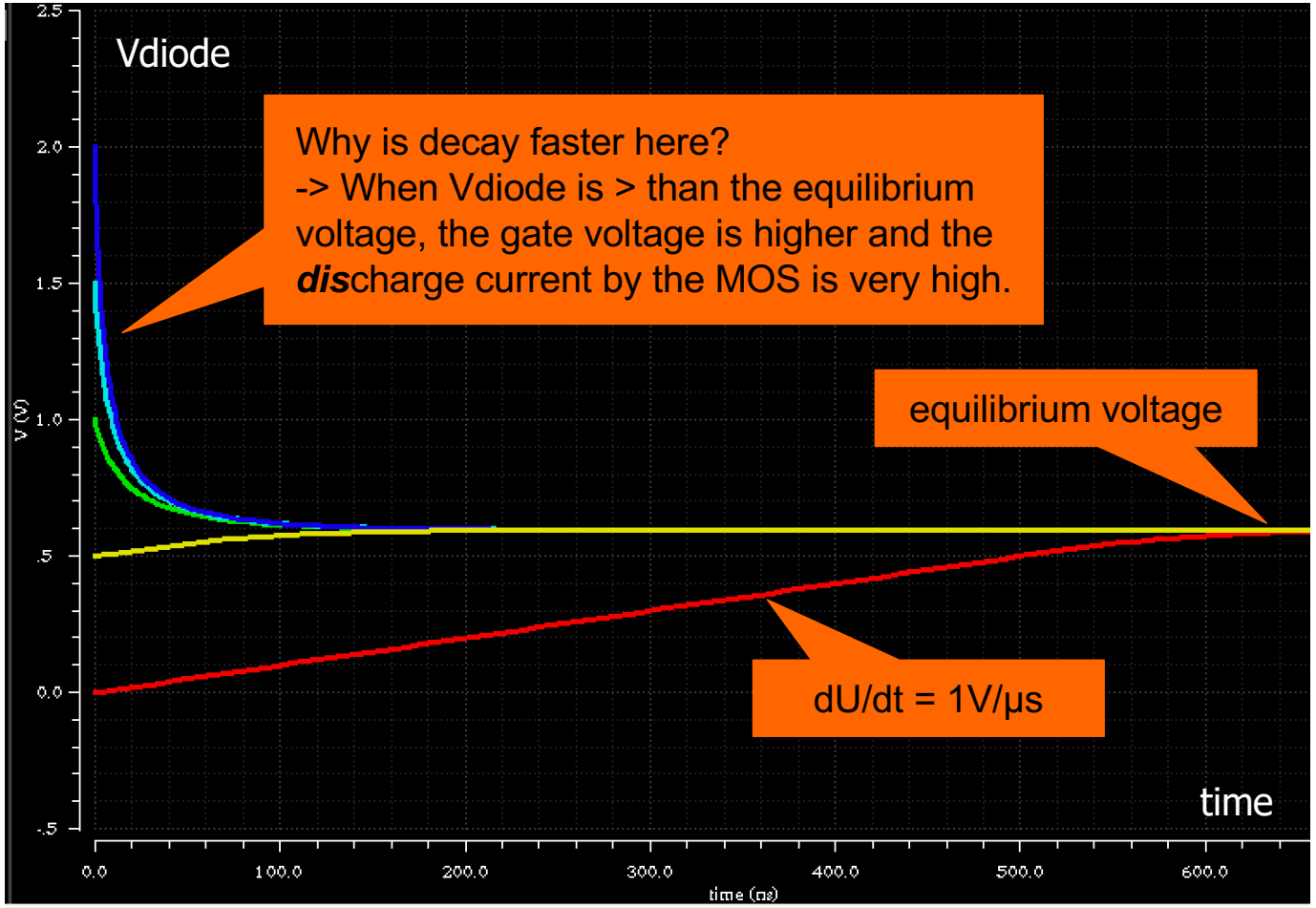
- Draw a diode connected NMOS
- Connect a large ‚extra' capacitance to the gate (say, 1 pF) with an *initial condition* of 0 V
  - Use a 'simple' MOS model
  - Set the initial condition ('IC') in the properties of the capacitor
- Send a small current I_{in} (1 µA) into the ‚diode'
- Perform a transient simulation
  - Estimate / Calculate a reasonable max. time!
- Observe the Input = Gate = Drain Voltage



- Use different initial conditions (0…1.8V, Parametric sweep!)
- Understand how the equilibrium point is reached!
- Vary I_{in}!

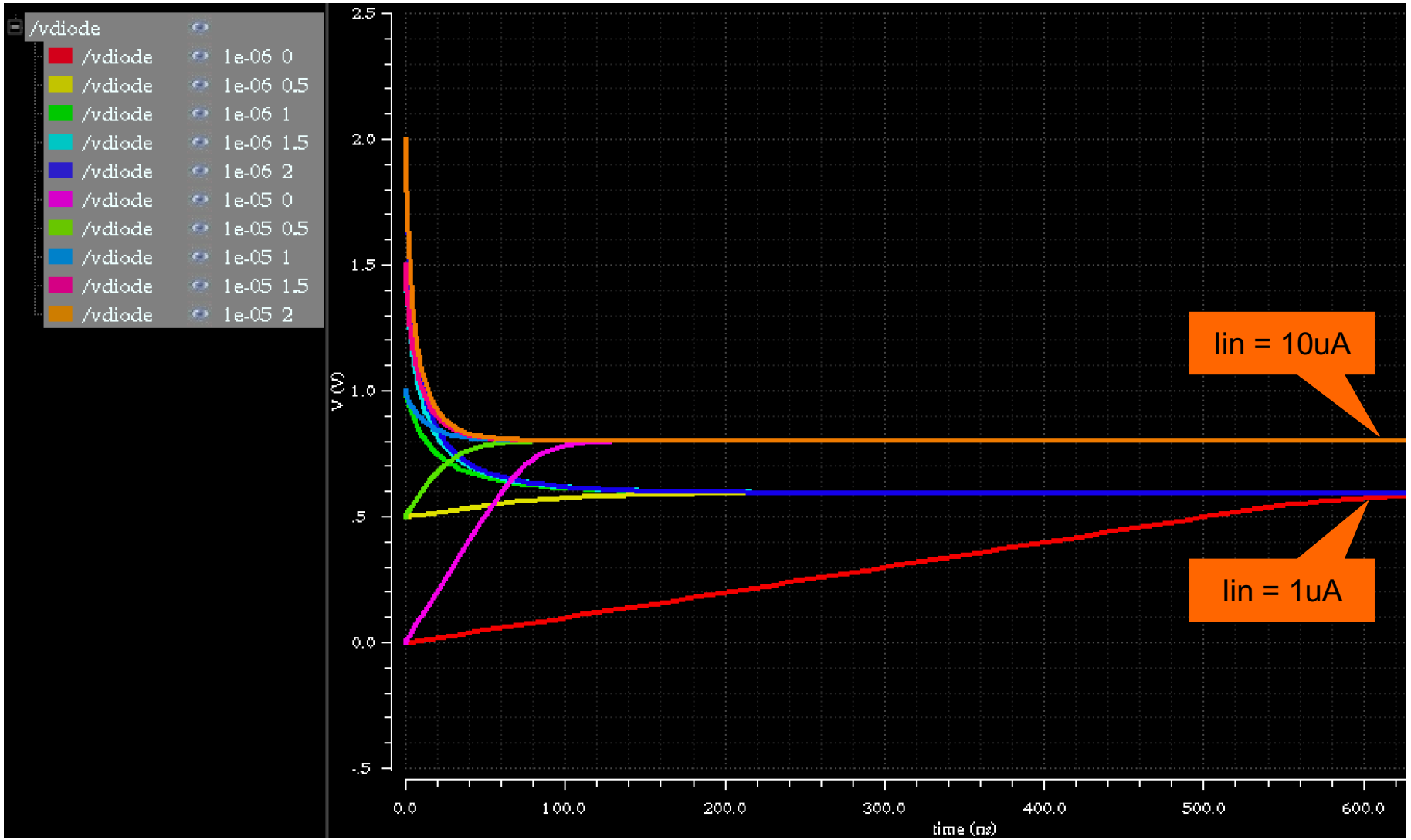
Solution 1

- The ramping slope us dU/dt = I/C = 1u/1p=1M (V/s), or 1V / µs -> simulate 1 µs



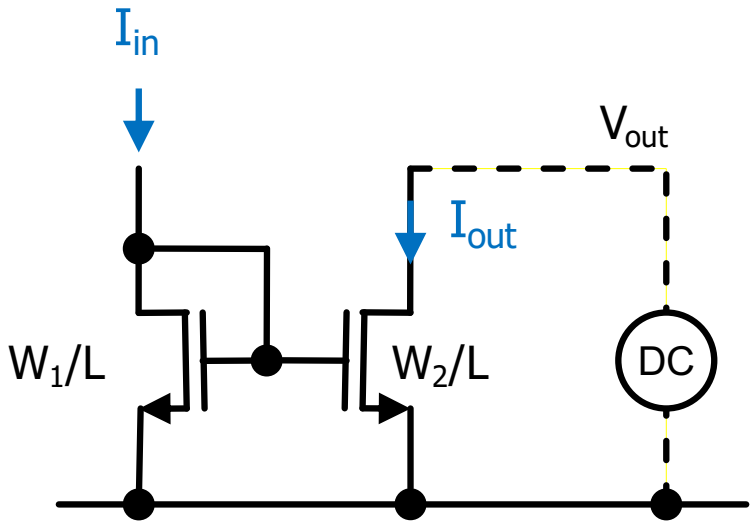
Solution 1

- When Iin is changed, the gate settles to another voltage:



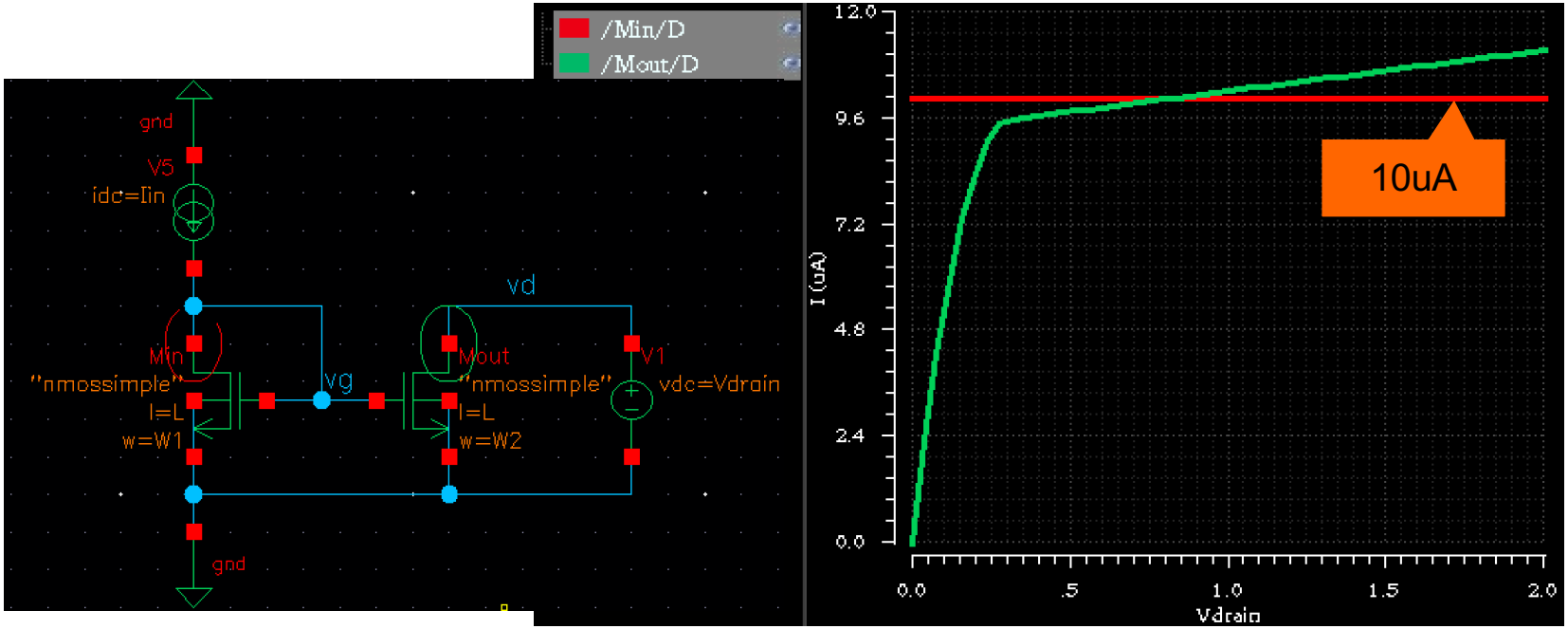
Exercise 2: A First Mirror

- Draw the following *current mirror*, with $W_1 = W_2 = 1\mu m$. Use for instance $L = 0.5\mu m$ and $I_{in} = 10\mu A$



- Sweep the output voltage V_{out} and observe the current I_{out}.
  - When is $I_{out} = I_{in}$ *exactly*? Why?
  - Try another input current!
  - Change W_2!
- For fixed I_{in}, W_1,W_2, vary L (same in both MOS).
  - Explain what you see!

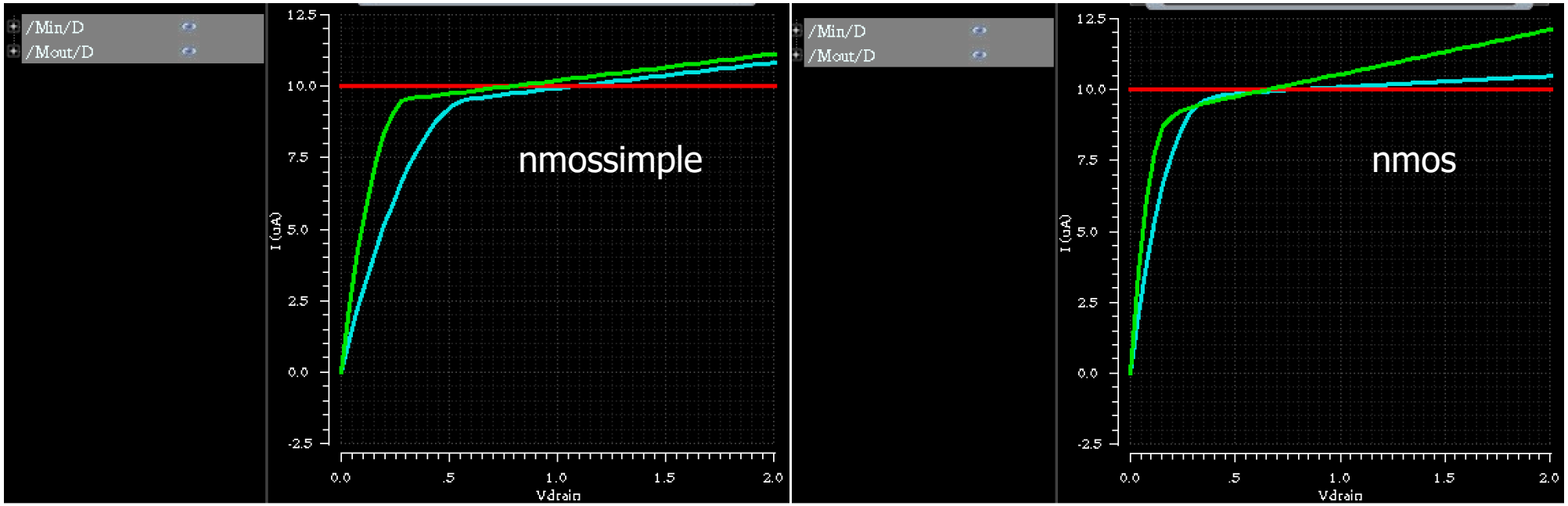
Solution 2



- Currents are equal when Drain voltages are equal, i.e. when Vout = Vg (this depends on Iin)
- When W2 is increased, current scales up

Solution 2

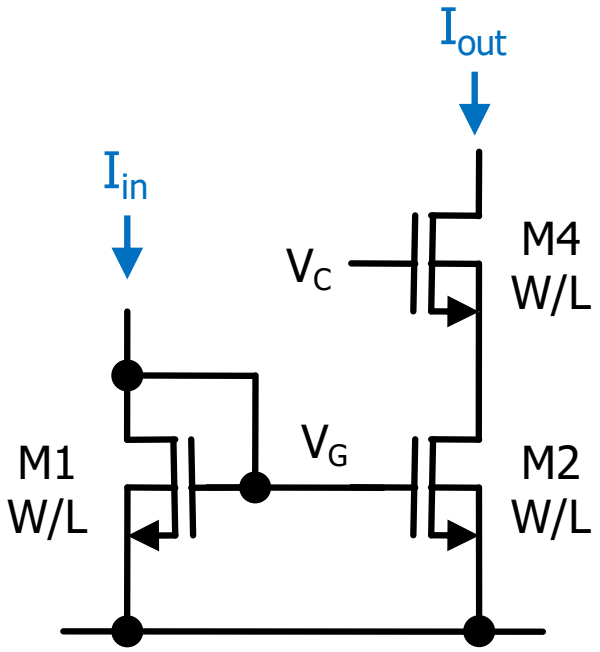
- When varying L with nmossimple, we get (left):



- The saturation point changes, as expected, but not the slope: The simple model does not take L into account!
- Using model ‘nmos’, we see the increase in output resistance with longer L (right)

Exercise 3: A Better Mirror

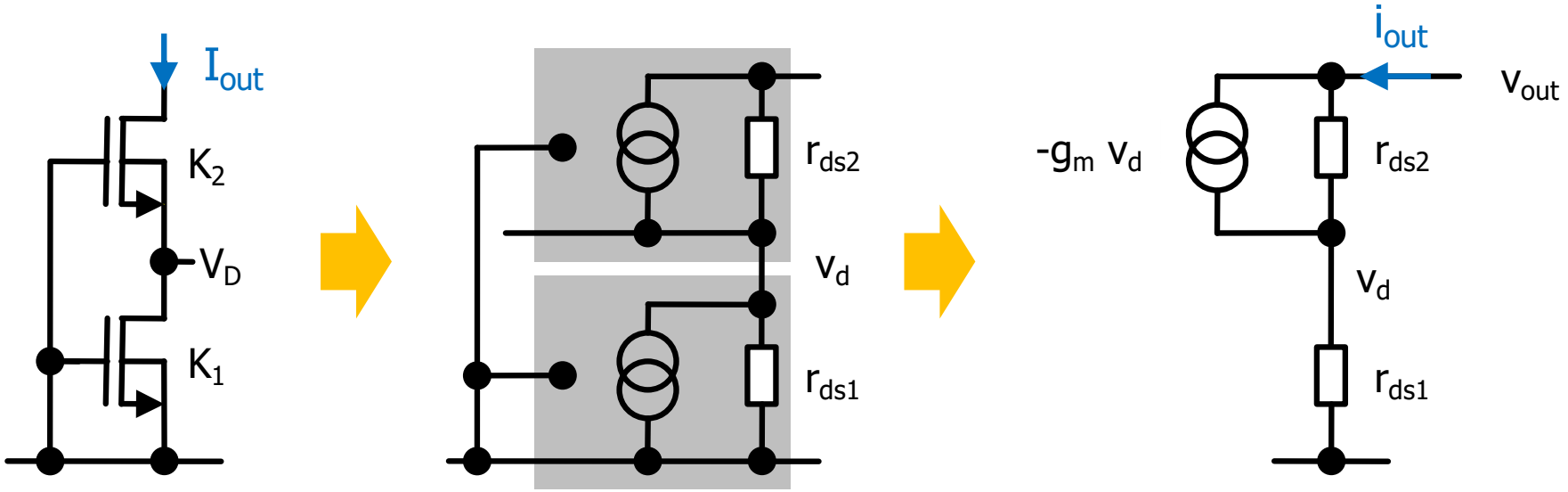
- The output current varies with V_{out} (i.e. the output resistance is not infinite) due to the Early Effect in M2.
- Try the following circuit:
  - Connect bulk and source in all MOS
  - Start with V_C = 1.2V
  - Use I_{in} = 1uA
- Sweep V_{out}
  - How is the output resistance now? (You may simulate the ‚simple' mirror of the previous exercise in parallel for comparison)



- *Calculate* the small signal output resistance!
  - You only need to consider M2 and M4 (because V_G is constant)
- Vary V_C (from 0V to 1.8V) and see what happens
  - What is the 'ideal' V_C ?

Solution 3: Output Resistance of Cascode Mirror

- Small signal analysis (for simulation, see lecture slides)
  - We only need to consider the output part
  - Fixed voltages are equivalent to ground
  - Current source of M1 delivers no current (V_{GS} = fix)

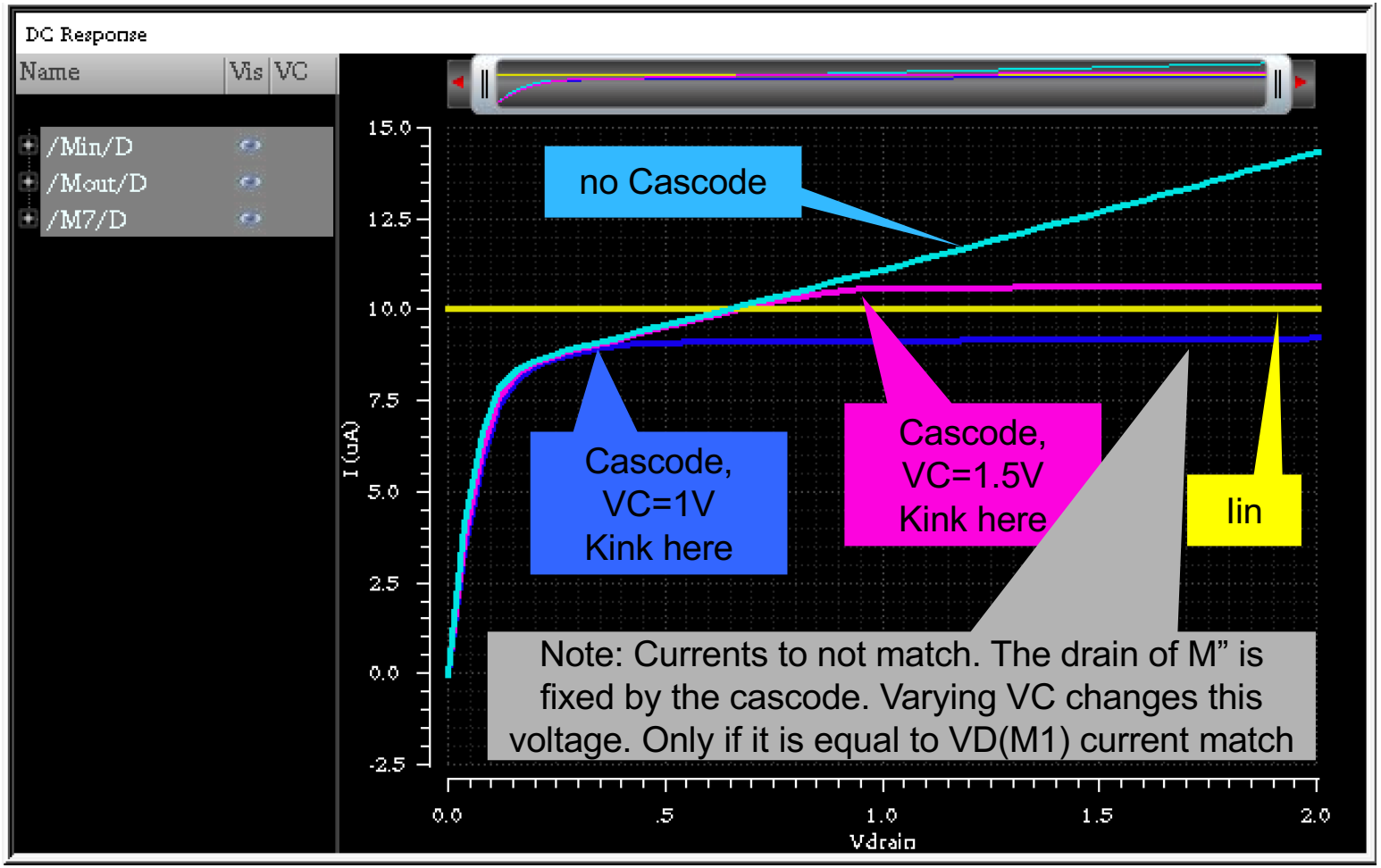


- Current sum at middle node:
  - $i_{out} = (v_{out} - v_d)/r_{ds2} - g_{m2}\, v_d = v_d / r_{ds1}$

$\rightarrow r_{out} = r_{ds1} + r_{ds2} + g_{m2}\, r_{ds1}\, r_{ds2} \rightarrow$ $r_{out} \cong r_{ds1} \times (g_{m2}\, r_{ds2})$

Solution 3: Simulation

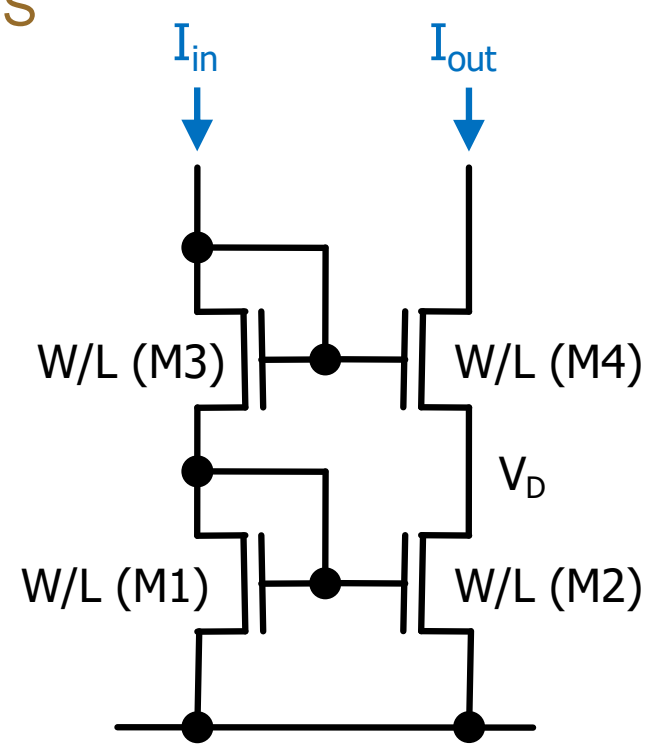
- nmos model, All W/L = 1u/0.3u



- VC is 'ideal' if the onset of cascode action (the kink) is just above the saturation voltage of M2

Exercise 4: A Mirror with Better Matching

- Unfortunately, the previous circuit does NOT reproduce I_{in} exactly. Why?
- Try this circuit (which does not need V_C and more):
  - Connect bulk and source in each MOS
  - It is called the ‚stacked mirror'

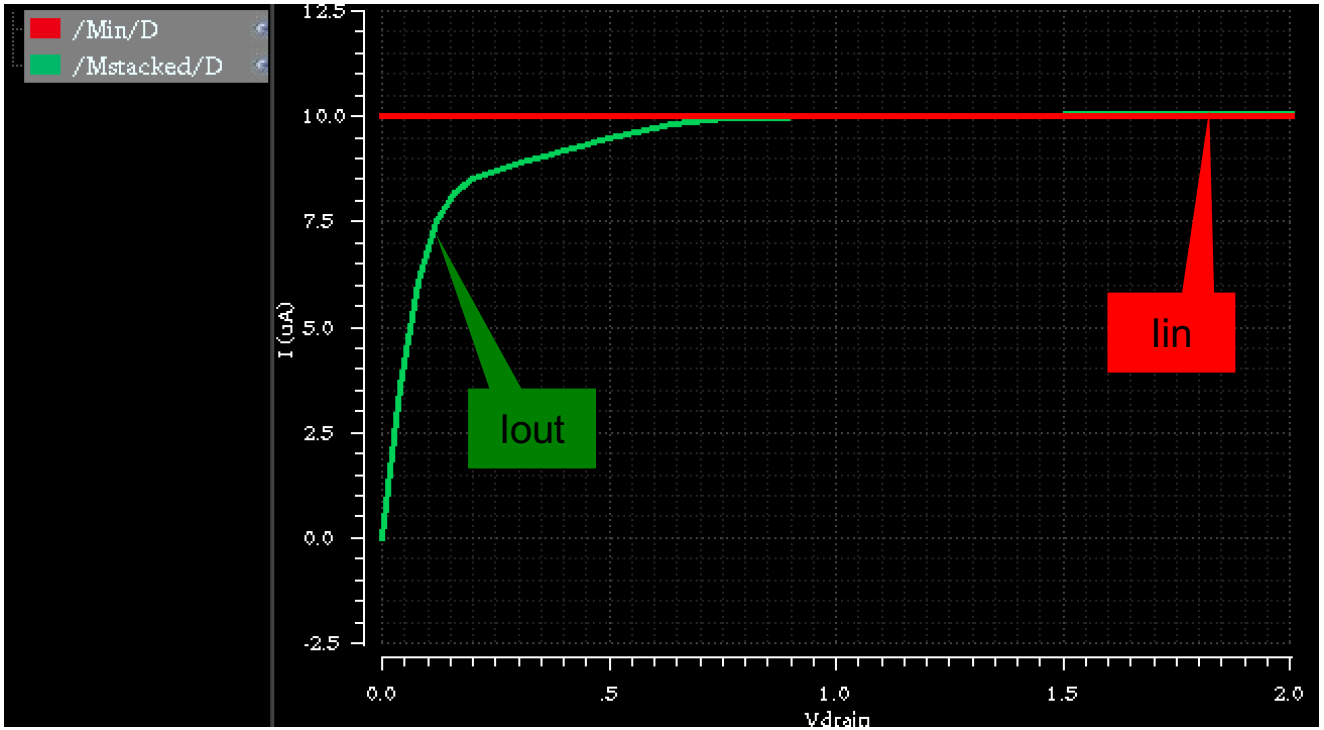


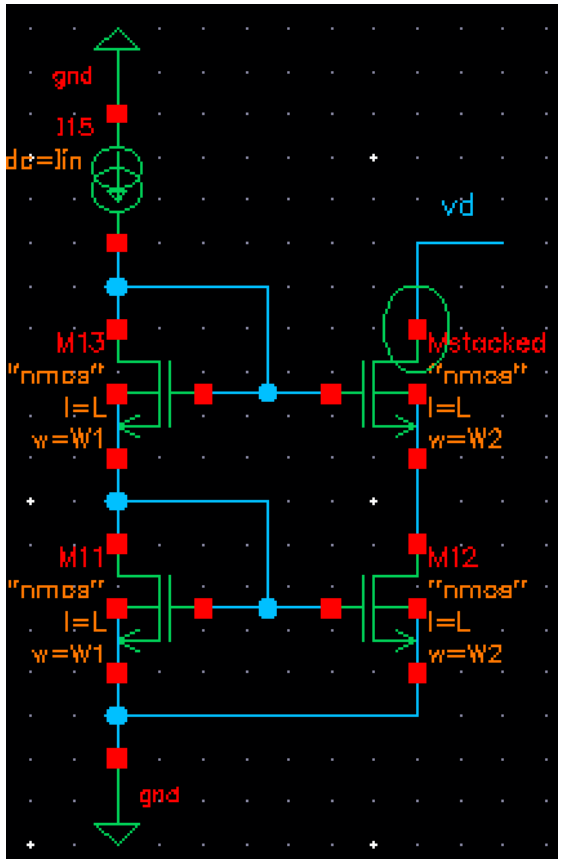
- Sweep V_{out}
  - Do currents match?
  - What is r_{out} ?
  - Where is the saturation ?

- What is the drain voltage V_D of M2? Is that optimal?

Solution 4

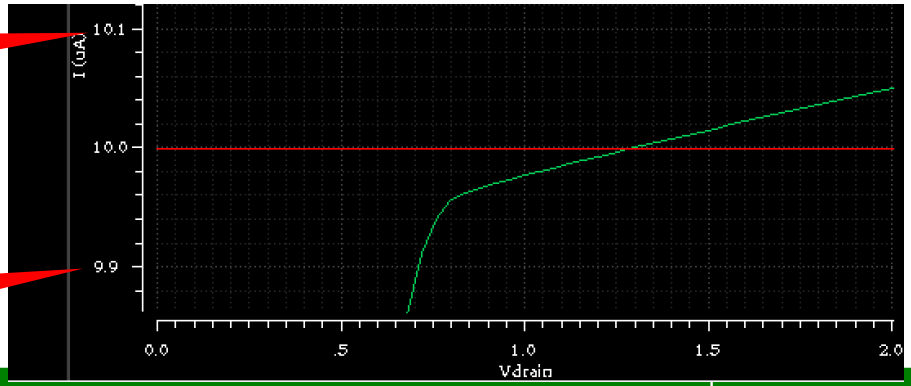
- Very nice current match, but ‘kink’ at too high voltage





10.1uA = I0 + 1%

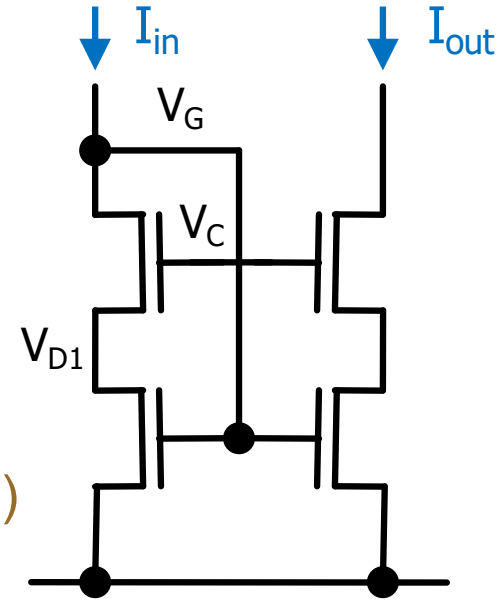
9.9uA = I0 - 1%



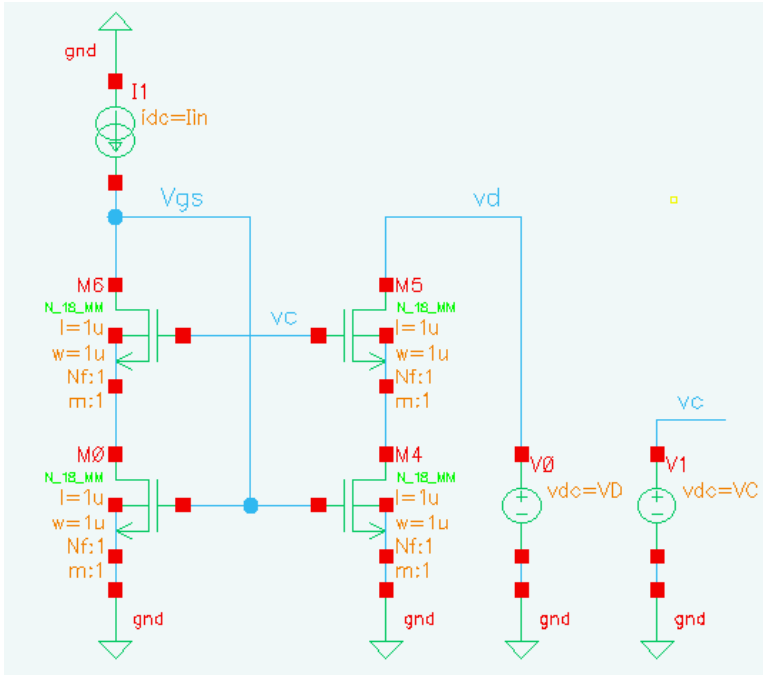
Exercise 5: The Low Voltage Mirror

- In the stacked mirror of the previous exercise, the drain voltage V_D of the current source M2 is fixed by the diode connection of M1.
- This is simple, but provides a *too high* voltage (by ~V_T !)

- The following circuit connects the diode differently:
  - Understand that the gate voltage V_G still stabilizes to the 'correct' level!
  - We now need to find V_C
  - Sweep V_C from 0.4 to 1.4V in steps of 0.2V
  - What is a good choice?
  - Why do very low voltages fail (check V_G !)
  - What happens at high voltages? Why? (this is tricky to understand… Look at V_{D1}…)
  - Note that the 'best' V_C depends in I_{in}



Solution 5: Results



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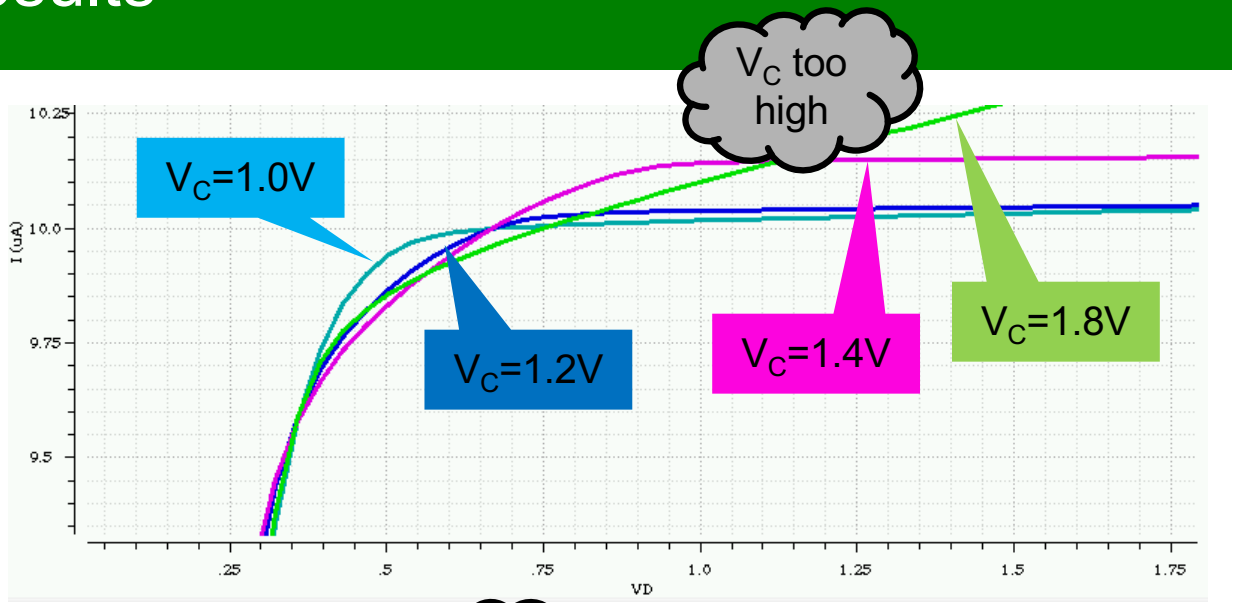
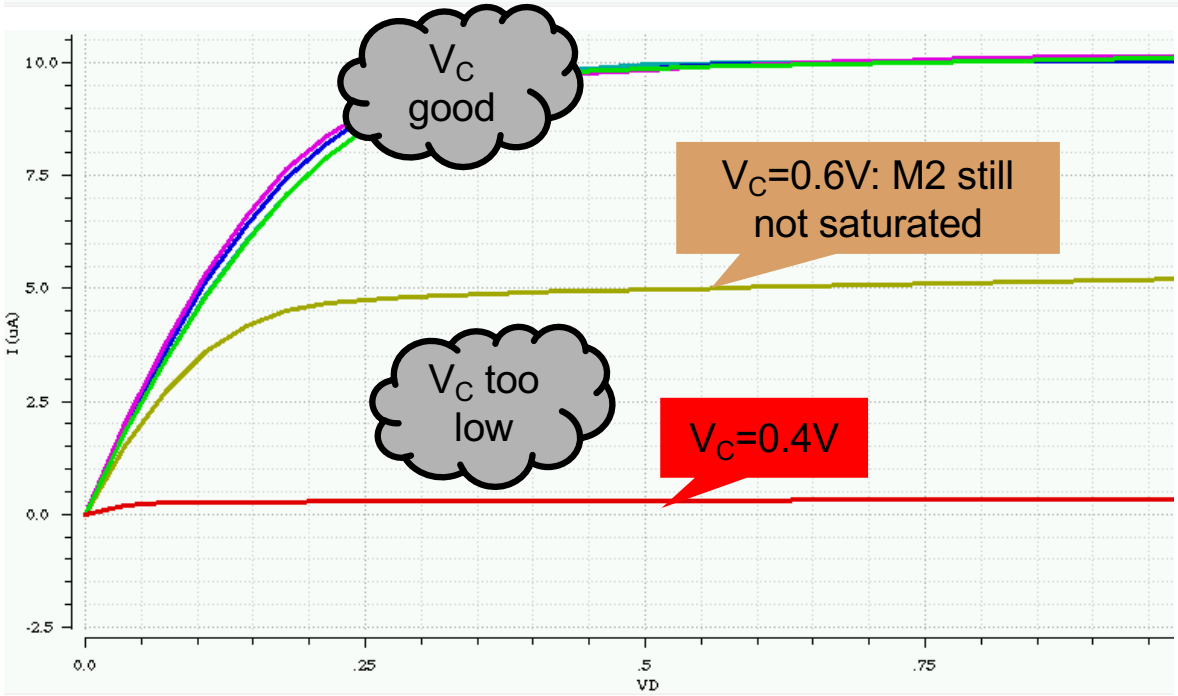
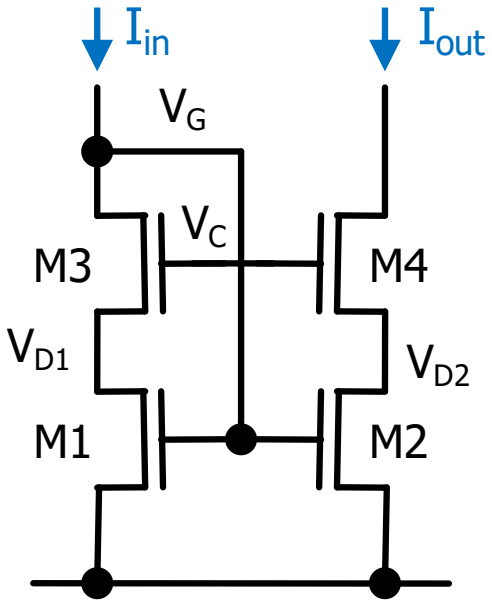




Exercise 5: Explanations (for experts)

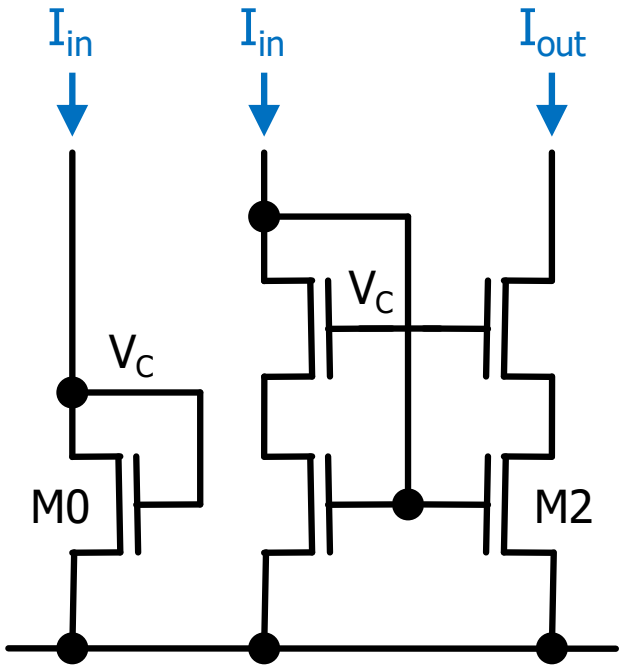
- Low V_C:
  - V_{D1} is very low
    → M1 is in linear region
    → current is low
    → V_G must be very (too) high to conduct requested current
- High V_C:
  - V_C pulls V_{D1} up
  - V_G is fixed, therefore V_{DS} of **M3** is small, M3 is in linear region
    → $V_{D1} \sim V_G$
    → Cascode M4 also in linear mode, does not work properly



- Optimal V_C:
  - M1 should *just* be saturated. This is then also optimal for M2

Exercise 6: The Low Voltage Mirror

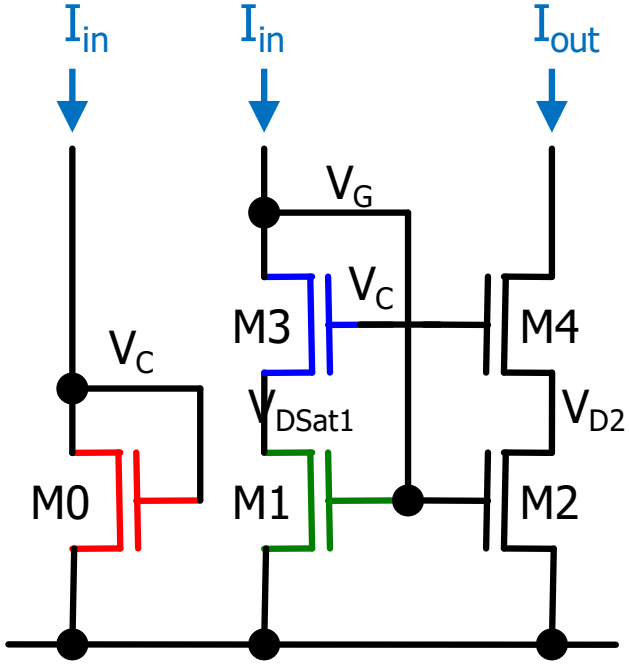
- The required optimal cascode voltage V_C can be generated *automatically* by a diode connected MOS M0 with different geometry than the others:
  $(W/L)_0 = k\ (W/L)_{others}$
- We assume that we have a second input current I_{in} available (boths I_{in}s are equal)



- *Calculate* k so that M2 is just saturated.
  - Use the *large signal* model in strong inversion with no Early effect
- Simulate the circuit

Solution 6

- We use $I_D = \beta (V_{GS}-V_T)^2$
- Gate voltage of M1:
  $I_{in} = \beta (V_G-V_T)^2$
  $V_G = V_T + \sqrt{(I_{in} / \beta)}$
- Saturation voltage of M1/M2:
  $V_{DSat1} = V_{GS1}-V_T = \sqrt{(I_{in} / \beta)}$
- Voltage VC (current in M3):
  $I_{in} = \beta (V_C - V_{DSat1} - V_T)^2$
  $= \beta (V_C - V_T - \sqrt{(I_{in} / \beta)})^2$
- $\sqrt{(I_{in} / \beta)} = V_C - V_T - \sqrt{(I_{in} / \beta)}$

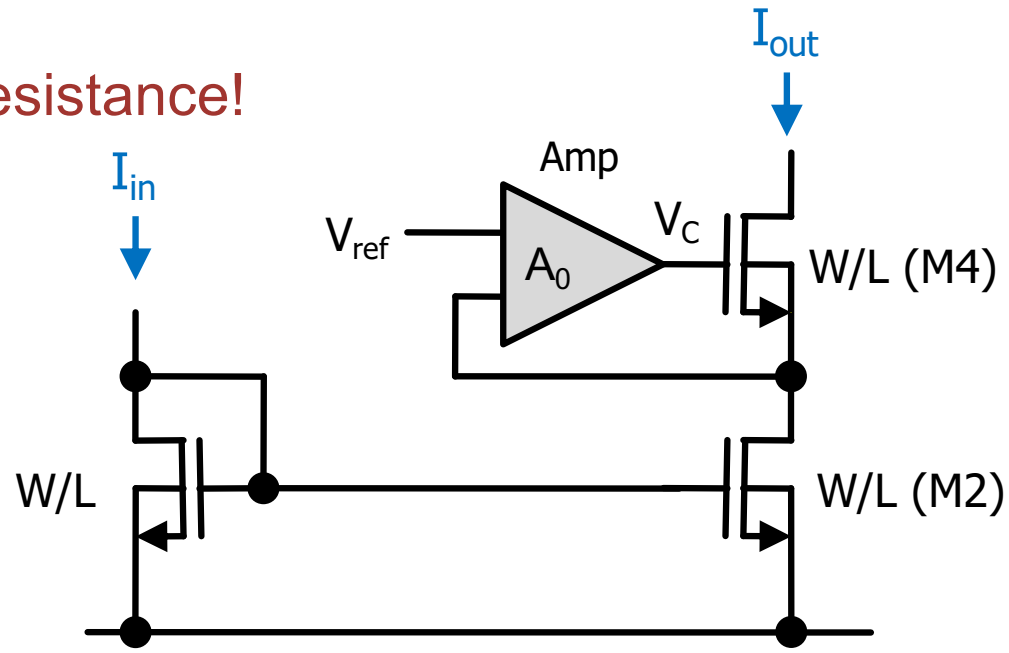


$\beta_0 = \beta / 4$

- Geometry of M0:
  $I_{in} = \beta_0 (V_C-V_T)^2 = \beta_0 (\sqrt{(I_{in} / \beta)} + \sqrt{(I_{in} / \beta)})^2 = \beta_0 4 I_{in} / \beta$

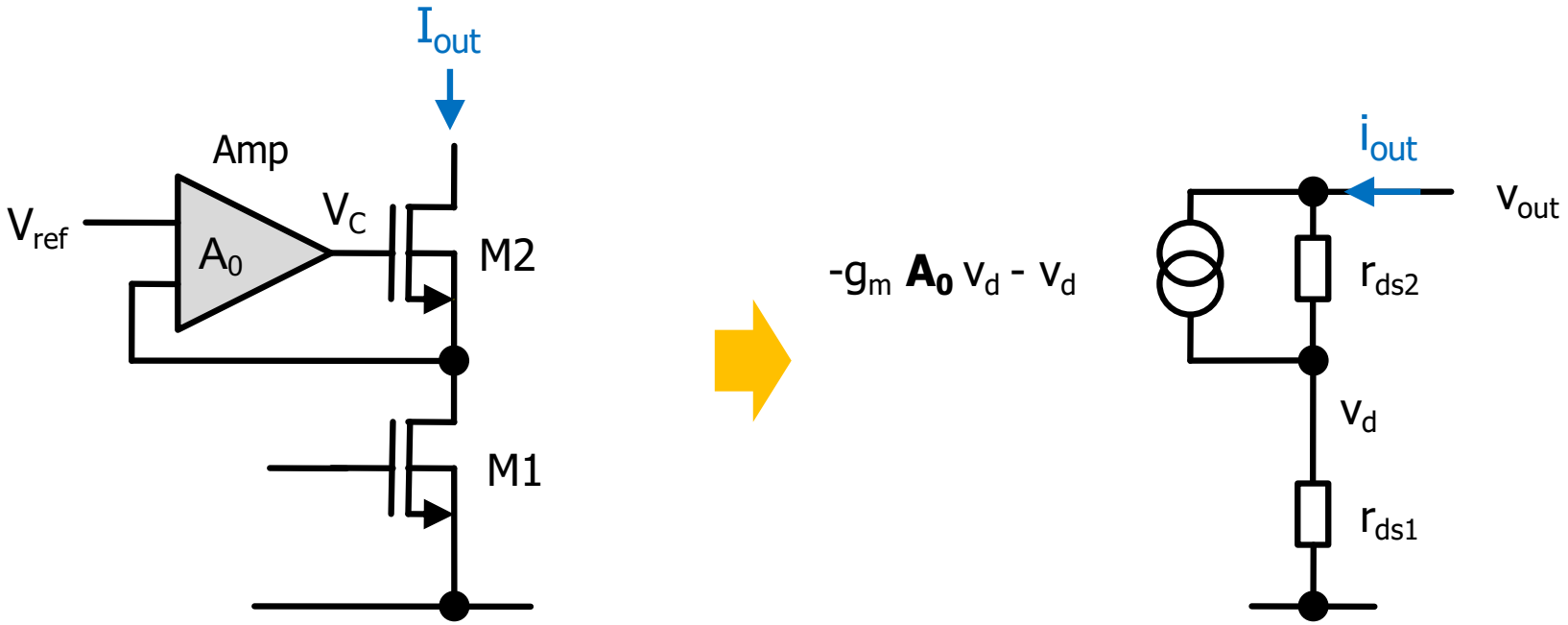
Exercise 7: An *Even* Better Mirror

- The key trick is obviously to keep the drain voltage of M2 very constant irrespective of the output voltage.
- This can be done with an active circuit (with an amplifier):
  - Amp amplifies the difference of the two input voltages by A_0
  - Where is the positive/negative input for stable operation?
  - Simulate the circuit. Use a voltage controlled voltage source vcvs from the analogLib for Amp with A_0=1000
- *Calculate* the output resistance!
- This topology is called the *Regulated Mirror*



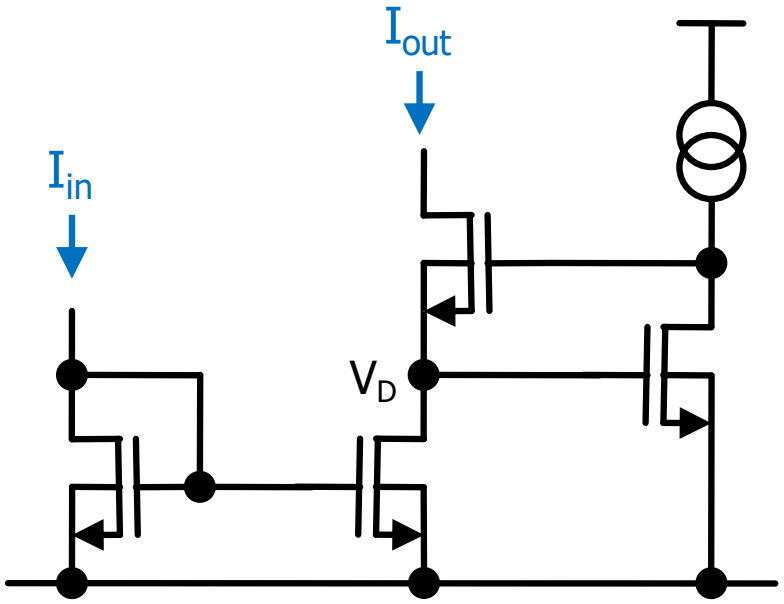
Solution 7: Theory

- Same result as stacked mirror, but with g_m increased by factor A_0



Exercise 8 (Advanced): Implementing the Regulated Mirror

- The amplifier in Ex. 7 can be implemented by a gain stage
- Simulate such a circuit!
- You can use a Spice current source in the regulation amplifier to start with...
- Explain why V_D is not optimal. Can you use a transistor with low threshold?
- You could also cascode in the gain stage...



Solution 7: Practical implementation

- The amplifier in Ex. 7 can be implemented by a gain stage: