



# Exercise: Gain Stage

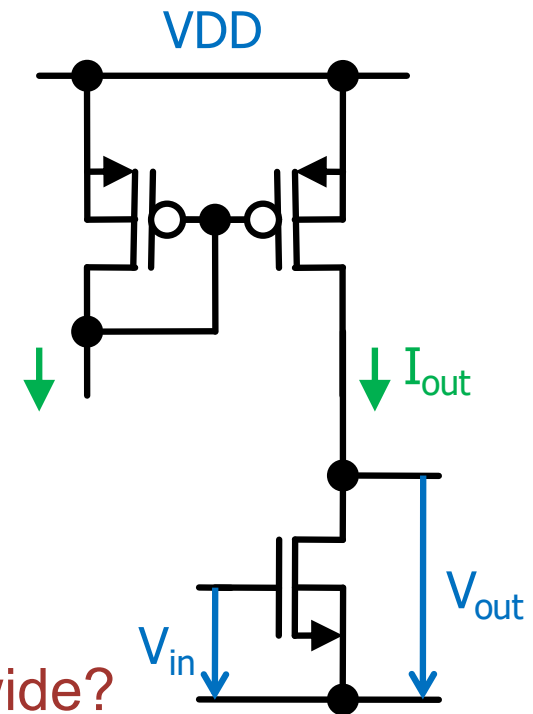
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# 1. Basic Gain Stage

- Implement a NMOS gain stage.
  - Use real transistor models ('nmos', 'pmos')
  - Use a NMOS with  $W/L = 1\mu/0.5\mu$
  - Use a PMOS of  $W/L = 1\mu/1\mu$
  - Bias the PMOS with a *mirror* to  $10\mu\text{A}$
  - Operate at  $V_{DD} = 1.8\text{ V}$
- Sweep  $V_{in}$  and observe  $V_{out}$
- What is the largest gain (derivative!) ?
- Why is the 'upper' part of the curves so wide?
- Change
  - the bias current
  - $W, L$  of the input transistor
 and observe what happens. Explain!  
 Why can't you increase gain more with  $W, L$  changes?
- Can you operate at  $100\mu\text{A}$ ?





## 2. Operation point

- Use the trick explained in the lecture to set the operation point
  - Use for instance  $C=1\mu\text{F}$ ,  $R=100\text{M}\Omega$
- Make an AC sweep



## 3. Bandwidth

- Load the gain stage with a capacitor (1 pF)
- Observe the bandwidth
  - best use the 'automatic' operation point
  
- Modify the load capacitor
  - Is bandwidth inversely proportional to  $C_L$ ?
  
- Modify  $I_D$ 
  - Make a Parametric Sweep with 2-3 values (0.1  $\mu$ A, 1  $\mu$ A, 10  $\mu$ A)
  - Do you find what you expect?



## 4. PMOS Amplifier

- Design a PMOS gain stage (with a NMOS current mirror load)



## 5. Cascoded Gain stage

- Set up a cascoded gain stage
  - Use  $W/L = 5\mu / 0.4\mu$  for all 4 MOS
  - Use  $I_{\text{bias}} = 10 \mu\text{A}$
  - **Use a stacked mirror on the PMOS side** (different from demo in lecture!)
  - Use a 'safe' cascode voltage for the NMOS
- Simulate
  - Make a DC sweep. What is the gain ?
  - Try different Cascode voltages
  - Check that  $v_{\text{out}} = v_{\text{in}}$  is a good operation point for AC analysis
- Make an AC sweep with a load of  $C_{\text{load}} = 100\text{fF}$ 
  - What is the gain?
  - Simulate a non-cascoded gain stage in parallel and compare



## 6. The Inverter

- The PMOS 'load' in the gain stage supplies a more or less constant current
- In the CMOS Inverter shown, the PMOS is switched with the input signal, it acts as the NMOS
- Simulate the DC transfer function  $V_{out}(V_{in})$ 
  - For instance  $L_N = L_P = 0.5\mu$ ,  $W_N = 1\mu$ ,  $W_P = 2\mu$
  - What is different from the normal gain stage ?
  - What is the maximum gain ?
- Use a small signal analysis to find the gain

