Exercise:
Gain Stage

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- Implement a NMOS gain stage.
  - Use real transistor models ('nmos','pmos')
  - Use a NMOS with W/L = 1µ/0.5µ
  - Use a PMOS of W/L = 1µ/1µ
  - Bias the PMOS with a *mirror* to 10µA
  - Operate at VDD = 1.8 V
- Sweep V_{in} and observe V_{out}
- What is the largest gain (derivative!) ?
- Why is the 'upper' part of the curves so wide?
- Change
  - the bias current
  - W, L of the input transistor

  and observe what happens. Explain!
  Why can't you increase gain more with W,L changes?
- Can you operate at 100µA?

Solution 1

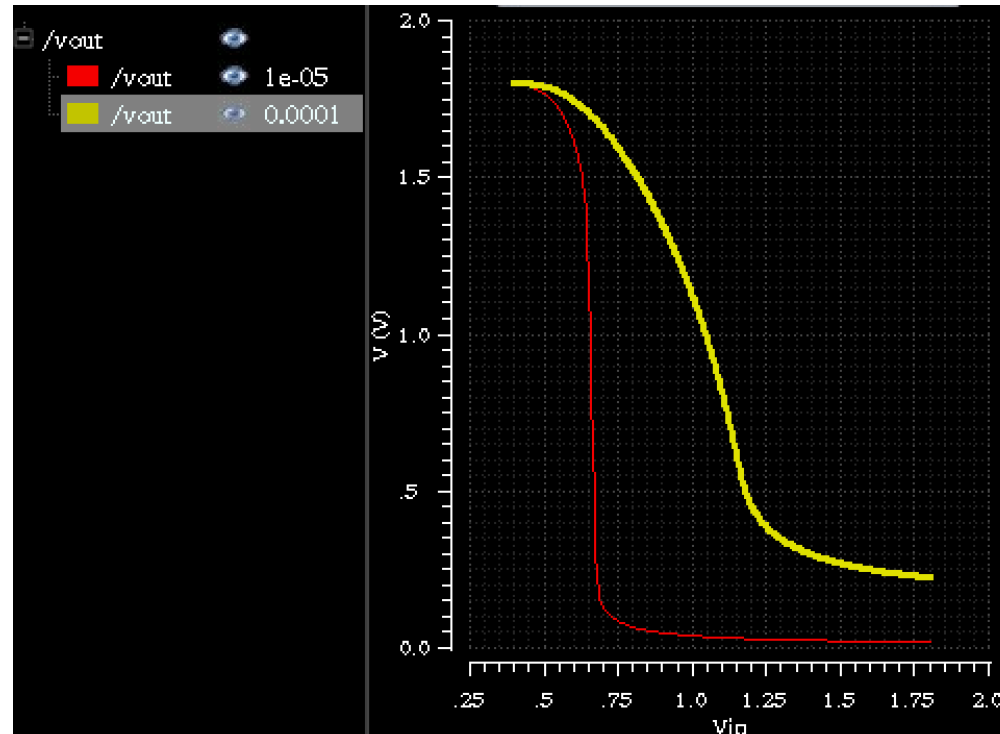- WN=1u, LN=0.5u -> gain ~ -37

- WN=2u -> gain ~ -42
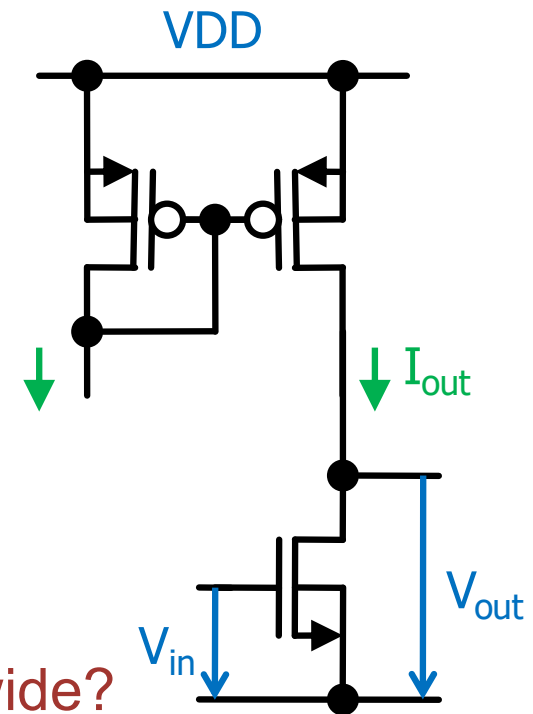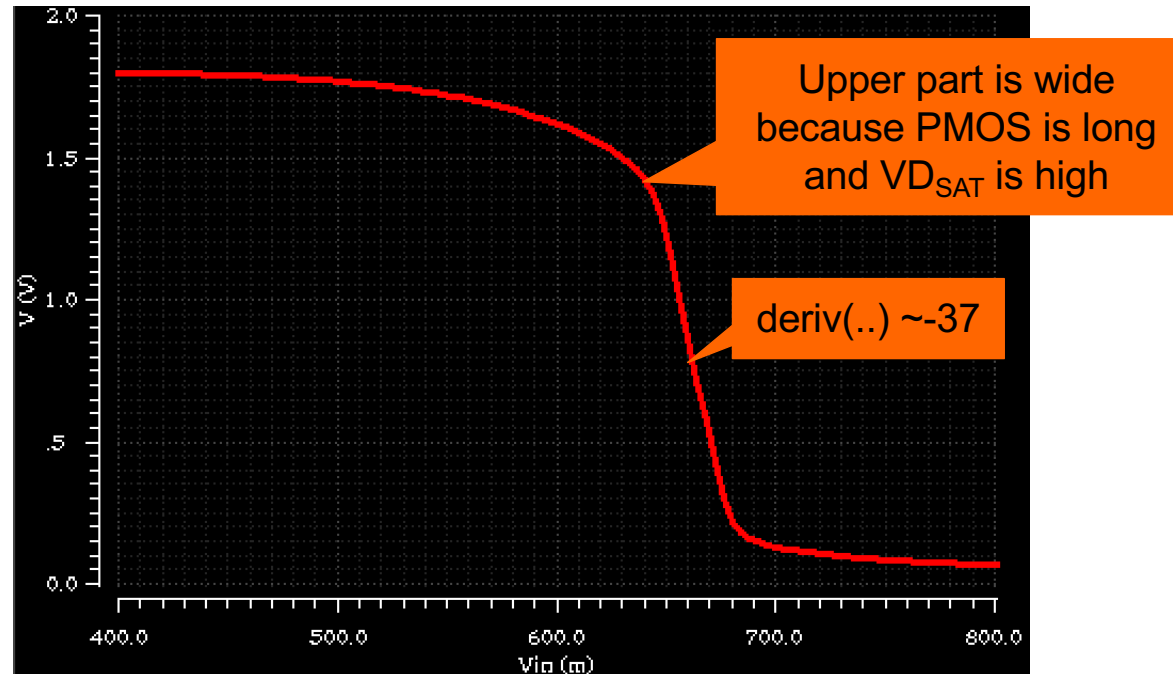
- LN=2u -> gain ~ -31! This is because r_{ds} of the PMOS limits! With an ideal current source, gains are (65/115) for (0.5/2)μ

- At 100uA, the PMOS is nearly always in saturation:

- In order to operate at 100μA, it must be made shorter and/or wider.

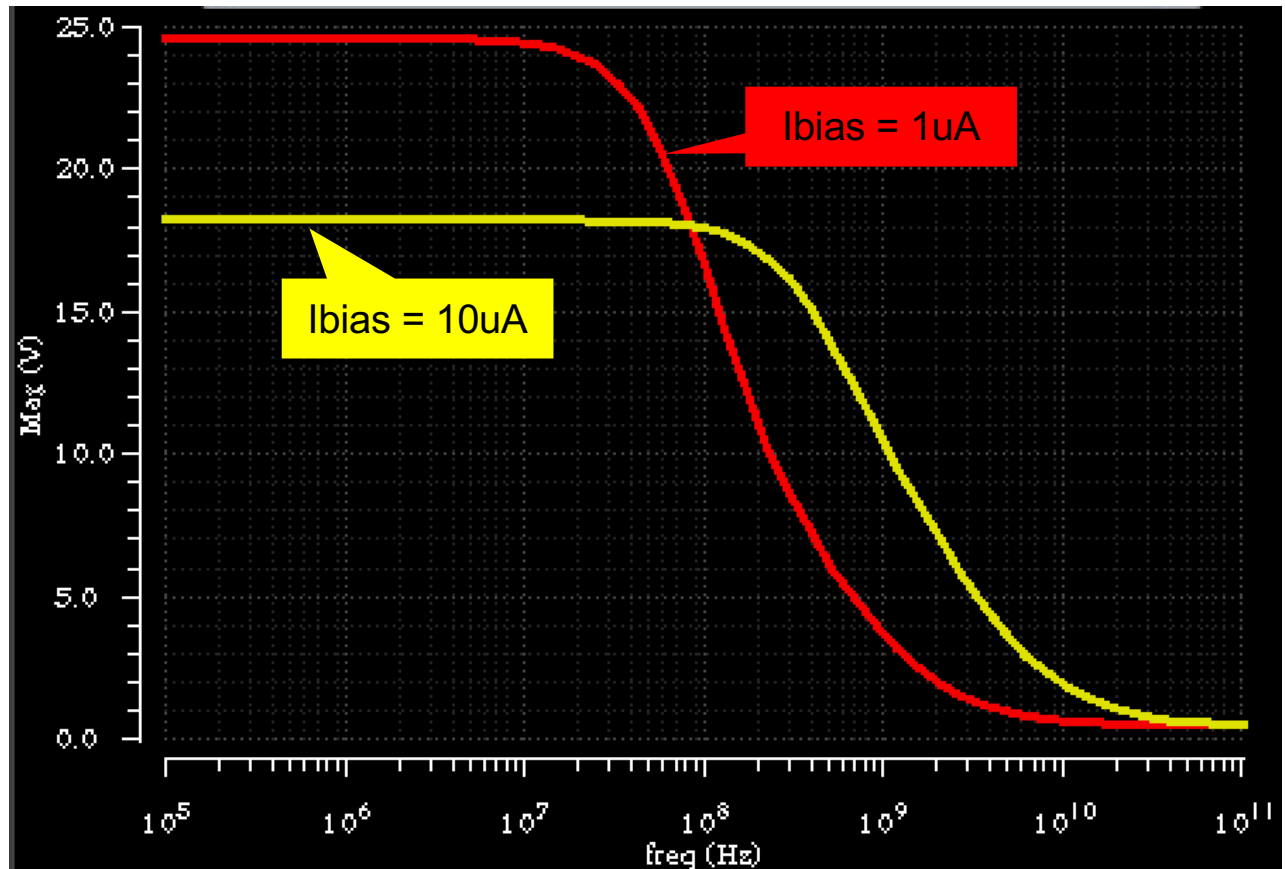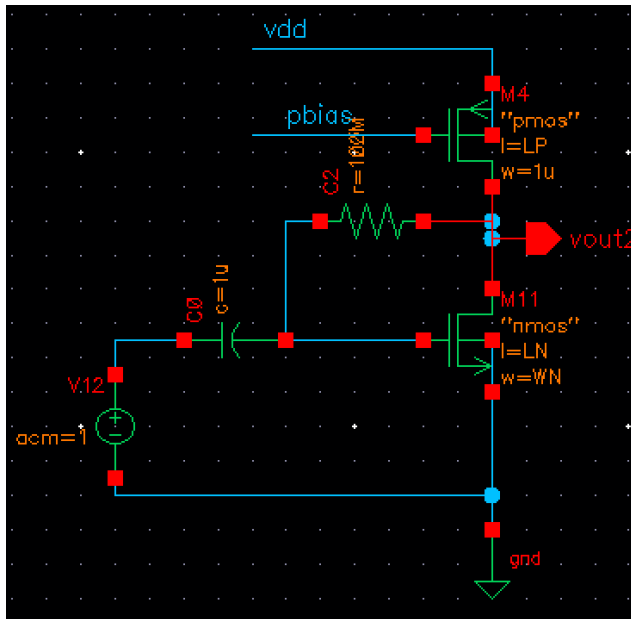- Use the trick explained in the lecture to set the operation point
  - Use for instance C=1uF, R=100MΩ

- Make an AC sweep

- High current -> less gain, but higher bandwidth

- Load the gain stage with a capacitor (1 pF)
- Observe the bandwidth
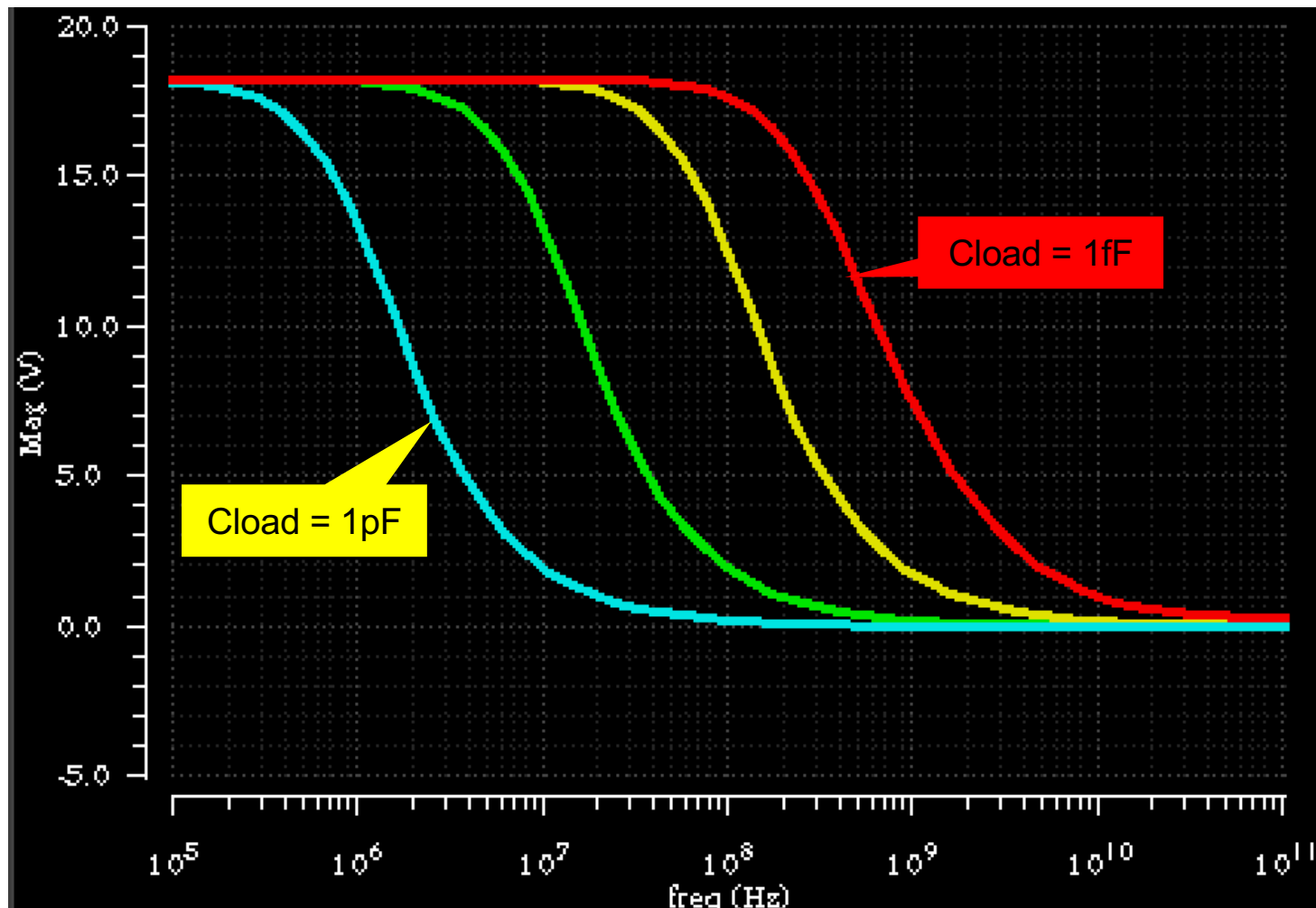 - best use the 'automatic' operation point

- Modify the load capacitor
  - Is bandwidth inversely proportional to C_L?

- Modify I_D
  - Make a Parametric Sweep with 2-3 values (0.1μA, 1μA, 10μA)
  - Do you find what you expect?

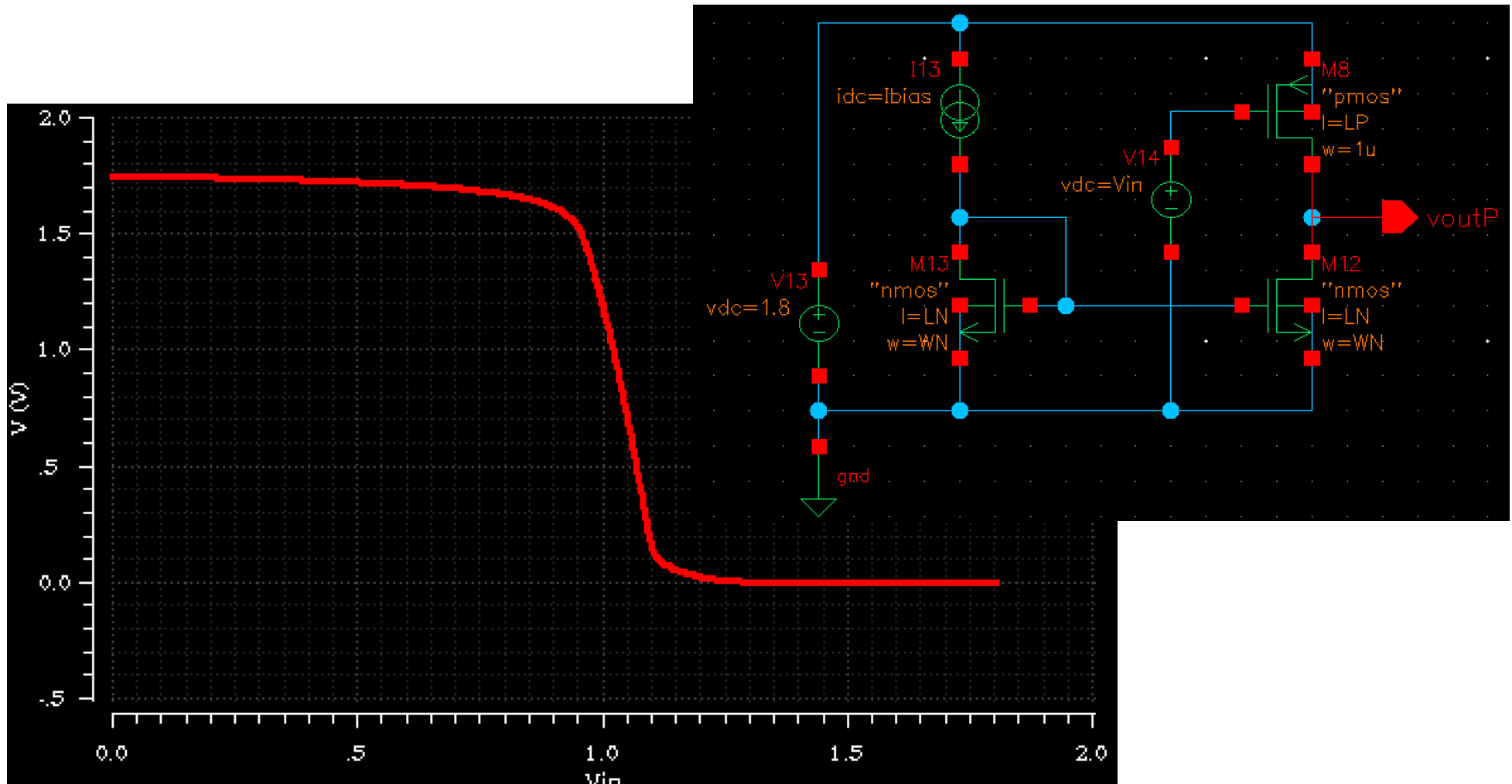- Higher Load cap -> less bandwidth. Proportional.
- For load cap -> 0fF, bandwidth is limited by caps in MOS

- Design a PMOS gain stage (with a NMOS current mirror load)

- Note: In this case, Ground is reached 'exactly' (when the gain PMOS is off) and VDD is only approached.

5. Cascoded Gain stage

- Set up a cascoded gain stage
  - Use W/L = 5µ / 0.4µ for all 4 MOS
  - Use I_{bias} = 10 uA
  - **Use a stacked mirror on the PMOS side** (different from demo in lecture!)
  - Use a 'safe' cascode voltage for the NMOS
- Simulate
  - Make a DC sweep. What is the gain ?
  - Try different Cascode voltages
  - Check that v_{out} = v_{in} is a good operation point for AC analysis

- Make an AC sweep with a load of C_{load} = 100fF
  - What is the gain?
  - Simulate a non-cascoded gain stage in parallel an compare

- Still missing…
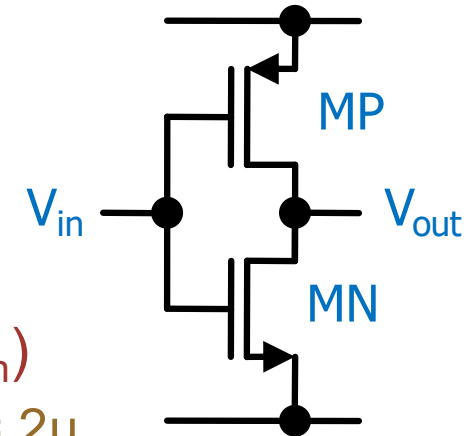
- The PMOS 'load' in the gain stage supplies a more or less constant current

- In the CMOS Inverter shown, the PMOS is switched with the input signal, it acts as the NMOS

- Simulate the DC transfer function $V_{out}(V_{in})$
  - For instance $L_N = L_N = 0.5\mu$, $W_N = 1\mu$, $W_P = 2\mu$
  - What is different from the normal gain stage ?
  - What is the maximum gain ?

- Use a small signal analysis to find the gain

Inverter: Solution

- For gain derivation, see lecture slides.
- The output now reaches gnd and vdd fully
- The current is not constant, it depends on Vin. This is bad!