Exercise:
Thévenin, Resistors, Capacitors

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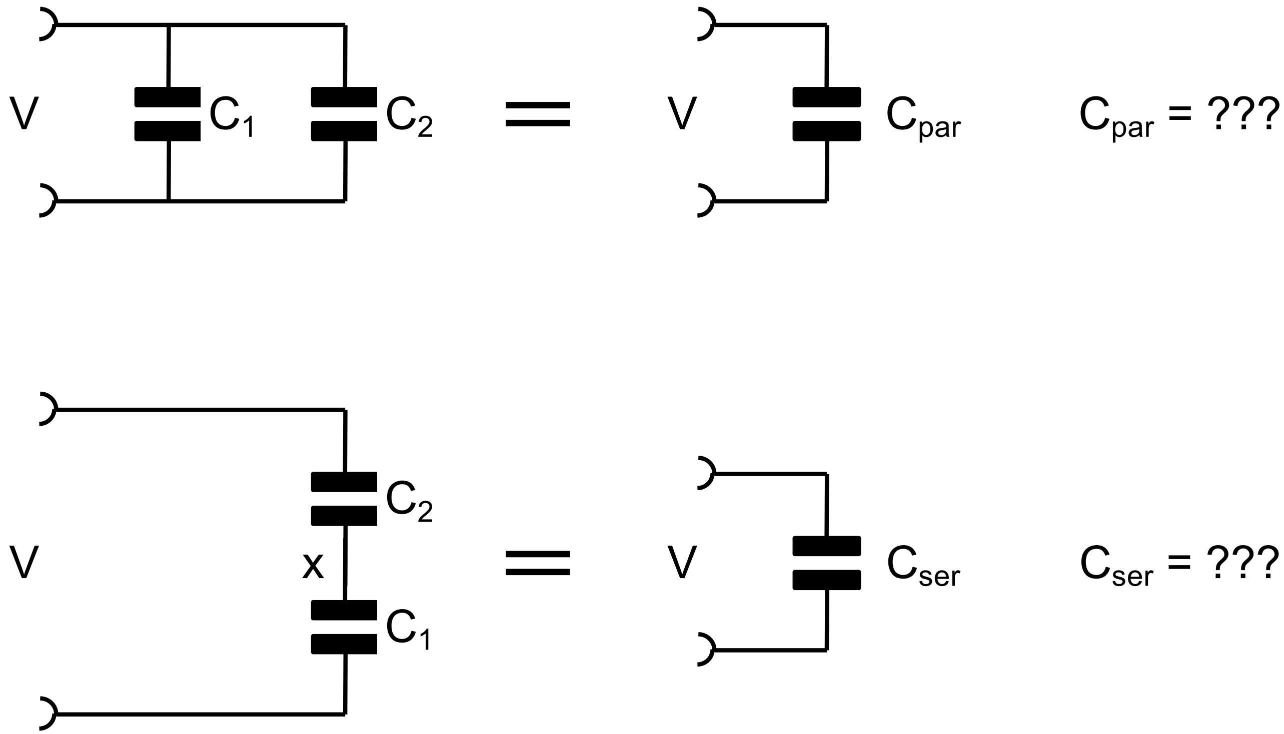
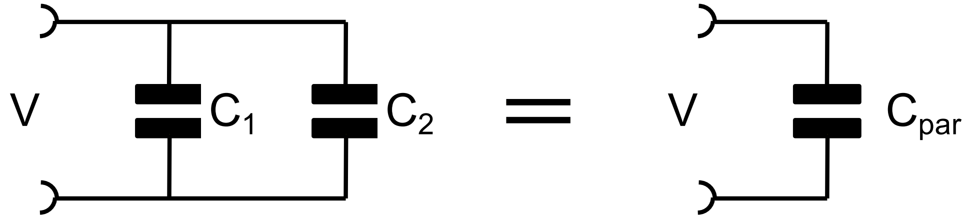
Exercise 1

- Derive the expressions for the series and parallel connection of capacitors
- Use charge conservation (at node x)



Solution 1



$=$

$C_{par} = ???$

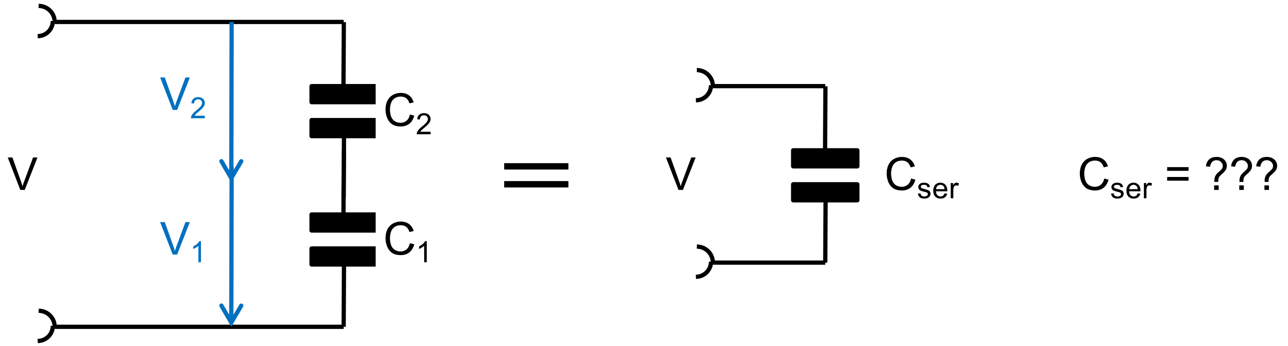
1. Charge conservation:

$V \times C_1 + V \times C_2 = Q_1 + Q_2 = Q_{par} = V \times C_{par} \quad \rightarrow \quad C_1 + C_2 = C_{par}$

2. Kirchhoff & complex impedance:

$V\, sC_1 + V\, sC_2 = i_1 + i_2 = i_{par} = V\, sC_{par} \quad \rightarrow \quad C_1 + C_2 = C_{par}$

Solution 1



1. Charge conservation:

Note: no charge can 'escape' the middle node, so that $Q_1 = Q_2 = Q_{ser}$

$V = V_1 + V_2 = Q_1/C_1 + Q_2/C_2 = Q/C_1 + Q/C_2 = Q/C_{ser}$

$\rightarrow \quad 1/C_1 + 1/C_2 = 1/C_{ser}$

2. Kirchhoff & complex impedance:

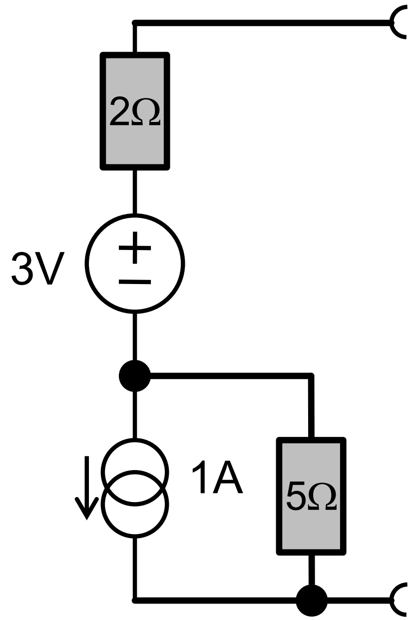
$V_1\, sC_1 = V_2\, sC_2$ and $V_1 + V_2 = V \quad \rightarrow \quad V_1 = V\, C_2 / (C_1+C_2)$

$\rightarrow \quad i_1 = V_1\, sC_1 = V\, s\, C_1C_2 / (C_1+C_2)$

$\rightarrow \quad C_{ser} = i / (Vs) = i_1 / (Vs) = C_1C_2 / (C_1+C_2)$

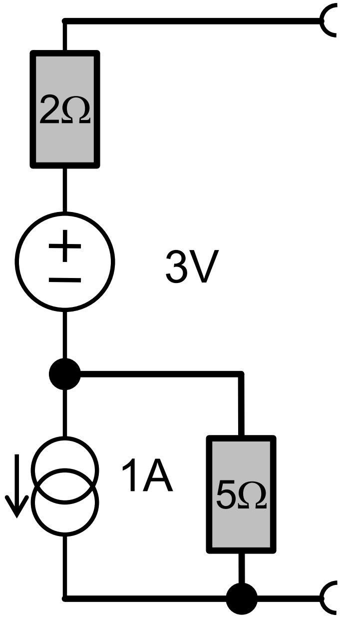
Exercise 2

- Derive the Thévenin Equivalent for the following circuit:



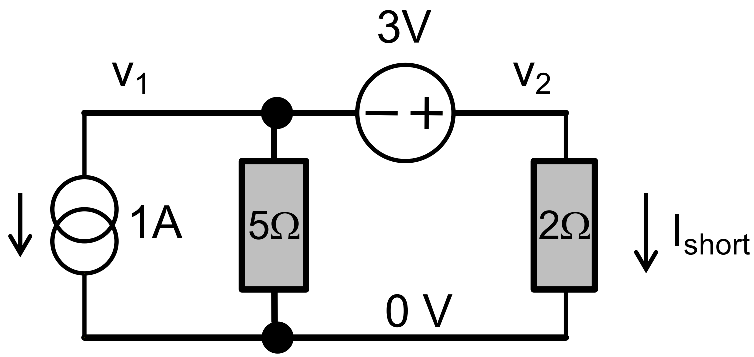
- Try two different methods:
  - Use the Open/Short method with Kirchhoff's rules
  - Convert the I-source part to a voltage source first…

Solution 2 – Kirchhoff



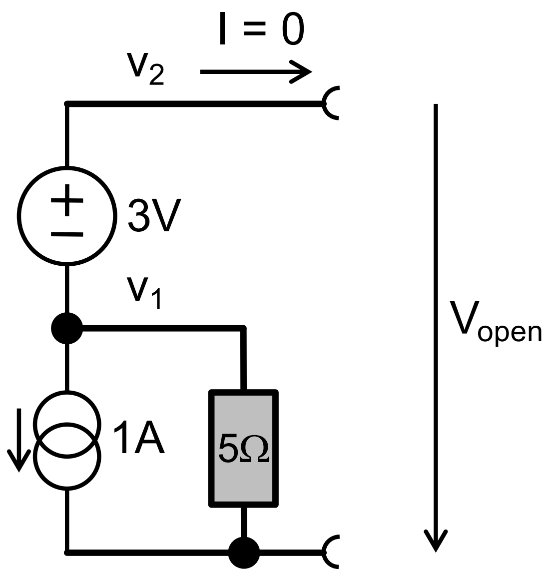
1. Short circuit current:

- EQ1: 1 A + v_1 / 5Ω + v_2 / 2Ω = 0
- EQ2: $v_2 = v_1$ + 3V
- → v_2 = - 4 / 7 V
- → I_{short} = - 2 / 7 A



1. Open circuit voltage:

- EQ1: 1 A + v_1 / 5Ω = 0
- EQ2: $v_2 = v_1$ + 3V
- → v_1 = - 5 V
- → v_2 = V_{open} = - 2 V



- Source: $V_0 = V_{open}$ = - 2 V, $R_V = V_0 / I_{short}$ = 7 Ω

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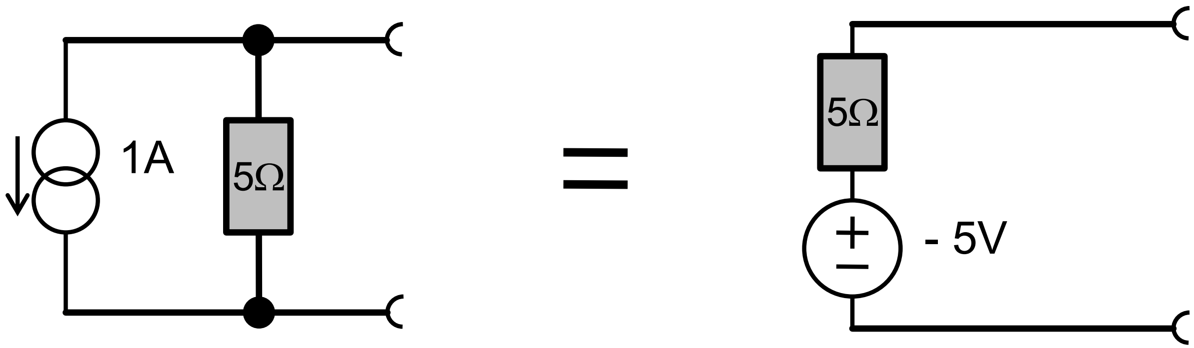
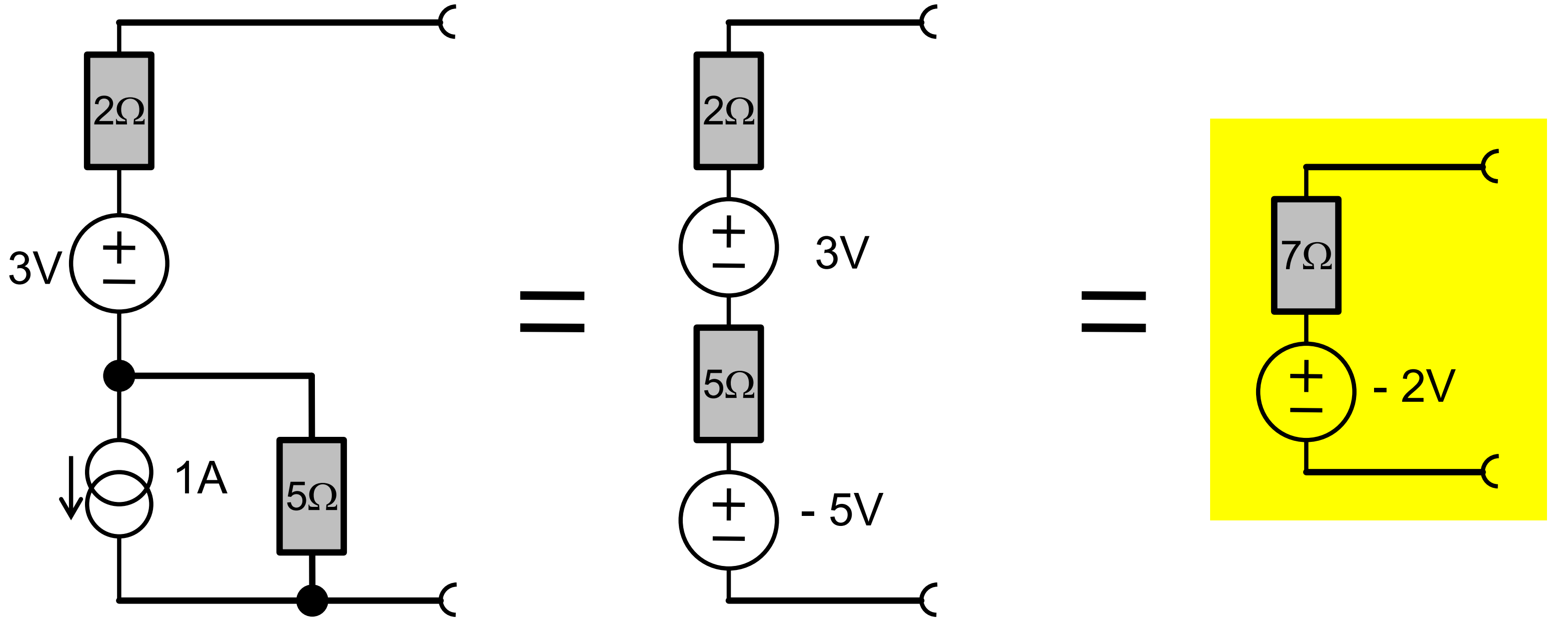
Solution 2 – Thévenin Transformations

1. Convert the current source to a voltage source:



2. Use this in the circuit:



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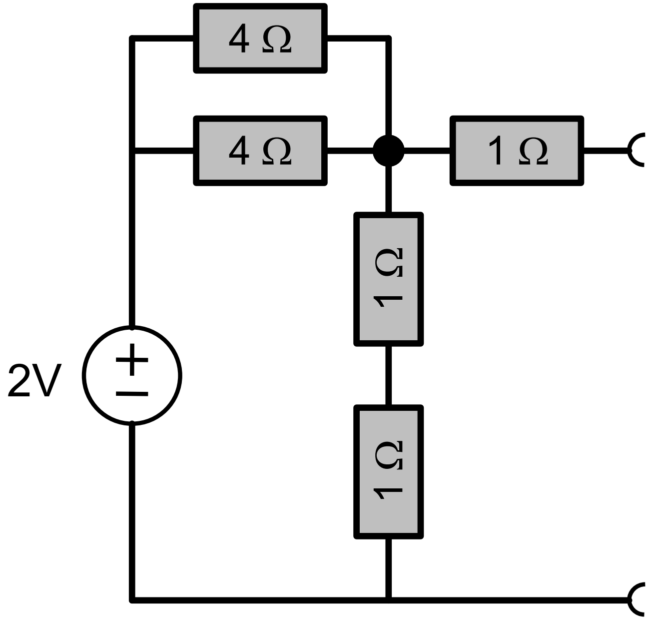
Exercise 3

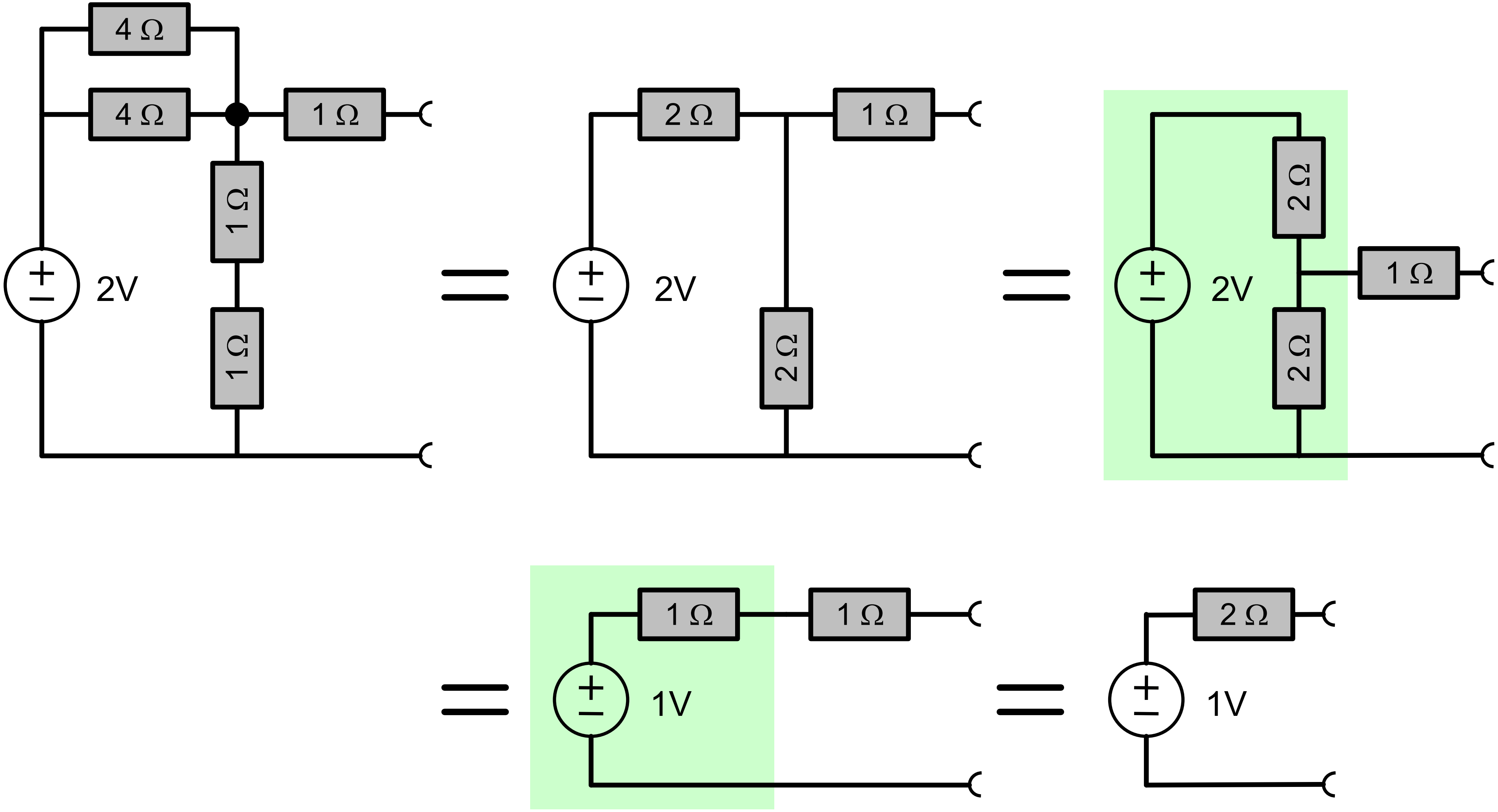
- What is the Thévenin Equivalent of the following circuit?



- Use two methods to find the result:
  - parallel / series connection of resistors and your knowledge about the voltage divider
  - short/open method

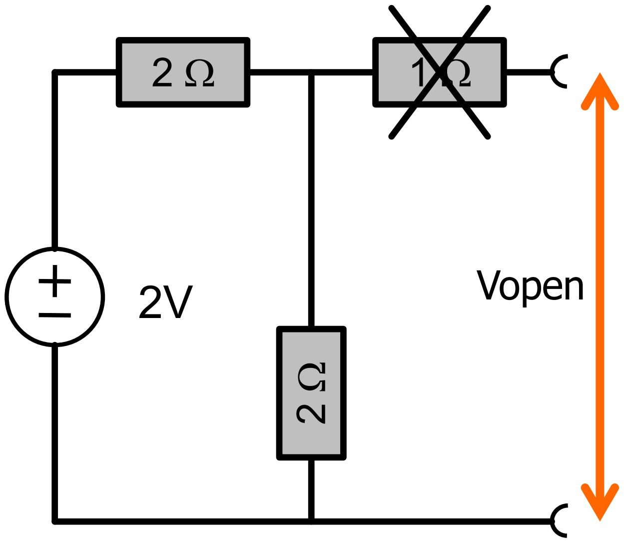
Solution 3

- Parallel-Series Connection, Voltage Divider:

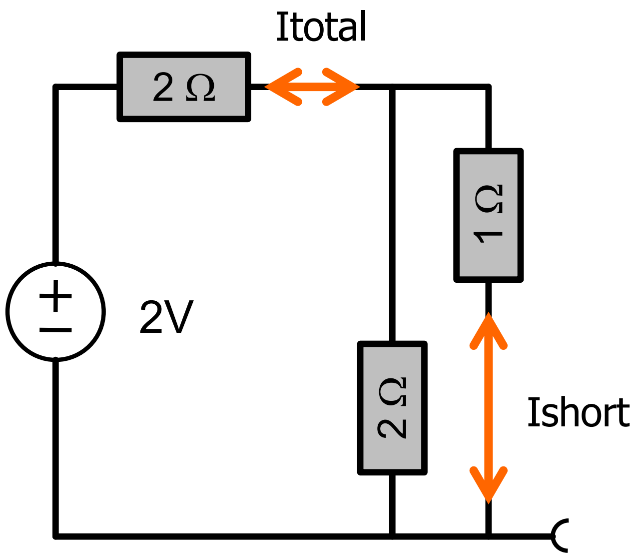


Solution 3

- Open: Vopen = 1V



Short:



Rtotal = 2Ω + 2/3Ω = 8/3 Ω

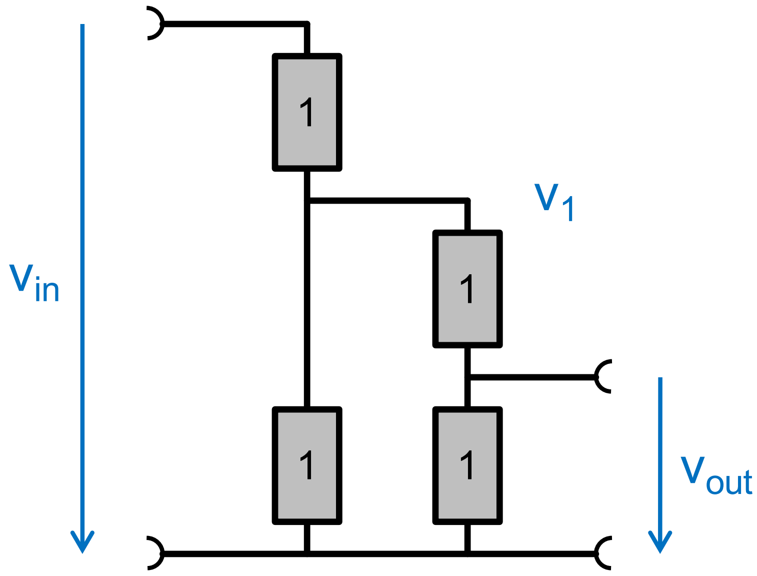
Itotal = 2V / Rtotal = 3/4 A

Ishort = 2/3 Itotal = 1/2 A

Zin = Vopen / Ishort
= 1V / ½ A
= 2 Ω

Exercise 4

- What is the ‘gain’ (attenuation) of the following voltage divider (all resistors have 1 Ohm):



- Try 3 different methods:
  - Your knowledge of parallel / serial connection of resistors
  - Kirchhoff’s law
  - Use your knowledge about the Thévenin equivalent of a voltage divider

Solution 4

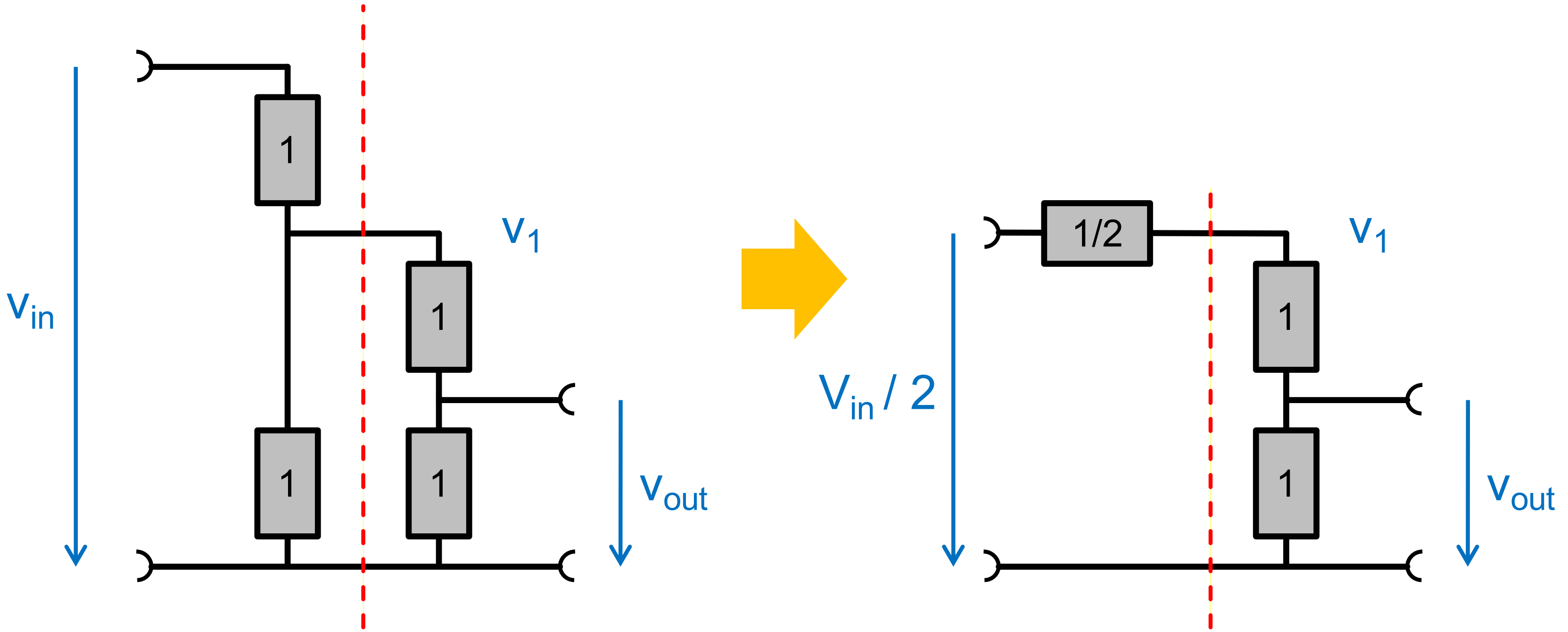
1. 'By hand':
   - The lower part is a *parallel* connection of 1Ω and 2Ω.
     This gives $(1/1\Omega + 1/2\Omega)^{-1} = 2/3\ \Omega$.
   - So we have at node v_1 a voltage divider with 1Ω and 2/3 Ω.
     The voltage at v_1 is $(2/3) / (1+2/3)\ v_{in} = 2/5\ v_{in}$
   - The voltage at v_{out} is half of v_1, so $v_{out} = 1/5\ v_{in}$
2. Kirchhoff
   - We have current equations at nodes v_1 and v_{out}:

```
EQv1 = (vin - v1)/1 == v1/1 + (v1 - vout)/1;
EQvout = (v1 - vout)/1 == vout/1;

Eliminate[EQv1 && EQvout, v1]

5 vout == vin

First@Solve[%, vout]

{vout → vin/5}
```

Solution 4

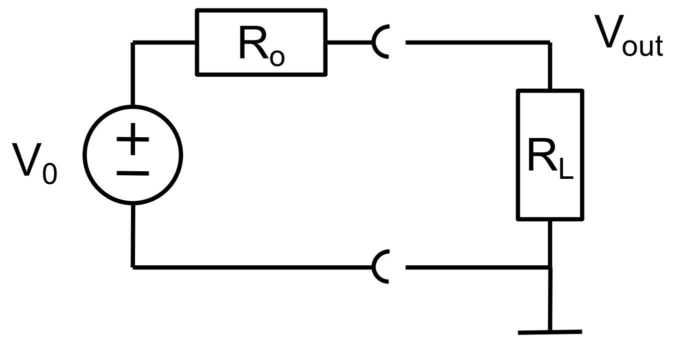
3. Thévenin:

- The first divider (left of the dotted red line) can be replaced by its Thévenin equivalent of a voltage source with $v_{in}/2$ and an outputs resistance of ½ Ω.
- This creates a divider of 1/2.5 of a voltage $v_{in}/2$, so that we get $v_{in}/5$.



Exercise 5

- A voltage source with voltage V_0 and output resistance R_0 is loaded by a resistor R_L:



- What is the output voltage V_{out} ?
- Which current flows in R_L ?
- What power (P = U I) is dissipated in R_L ?
  - Check that noting is dissipated for R_L=0 and $R_L \rightarrow \infty$
- For which value of R_L is the dissipation maximized?
  - What is the dissipation?

Solution 5

In[29]:= $\text{Vout} = \text{V0}\,\dfrac{\text{RL}}{\text{R0} + \text{RL}};$

In[30]:= $\text{Iout} = \dfrac{\text{Vout}}{\text{RL}}$

Out[30]= $\dfrac{\text{V0}}{\text{R0} + \text{RL}}$

In[31]:= Pout = Vout Iout

Out[31]= $\dfrac{\text{RL}\ \text{V0}^2}{(\text{R0} + \text{RL})^2}$

In[38]:= Table[Limit[Pout, RL → x], {x, {0, ∞}}]

Out[38]= {0, 0}

In[39]:= Solve[D[Pout, RL] == 0, RL] // First

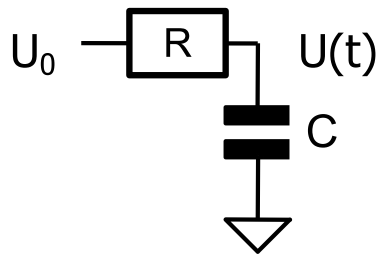
Out[39]= {RL → R0}

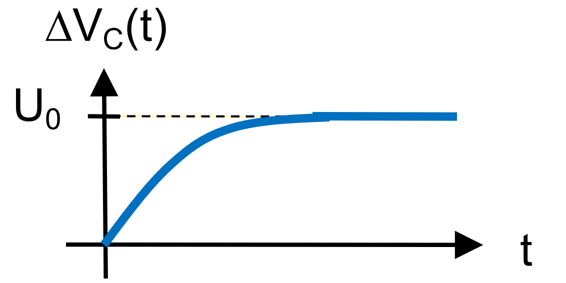
In[40]:= Pout /. %

Out[40]= $\dfrac{\text{V0}^2}{4\ \text{R0}}$

Exercise 6

- We consider charging of a capacitor C though a resistor R to a voltage U_0.





- Show that $U(t) = U_0 - U_0 e^{-\frac{t}{RC}}$ satisfies the differential equation
- Simplify U(t) for small times t<<RC.
- What is the initial slope ?
- Derive this slope directly (assuming U(0) = 0).

Solution 6

- For a capacitor, we have dU/dt = I/C.
  And we have $I = (U_0-U)/R$
  So the DGL is $U'(t) = (U_0-U)/RC$
- The proposed solution $U(t) = U_0-U_0$ Exp(-t/RC) gives
  The left hand side: $U'(t) = U_0/RC$ Exp(-t/RC)
  And the right side: U_0 Exp(-t/RC) / RC, i.e. the same.

- For small x, the Exp(x) is ~ 1+x, therefore
  $U(t) \sim U_0-U_0 (1-t/RC) = t\, U_0/RC$
- The slope is derivative of this, i.e U_0/RC
- This is a charging I/C with an initial current U_0/R

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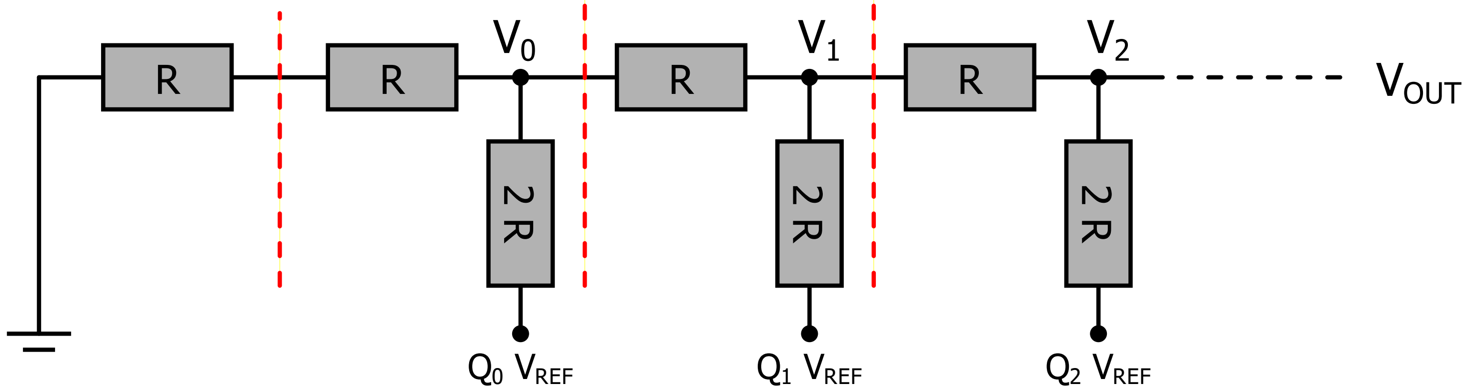
Exercise 7 (new): R-2R DAC

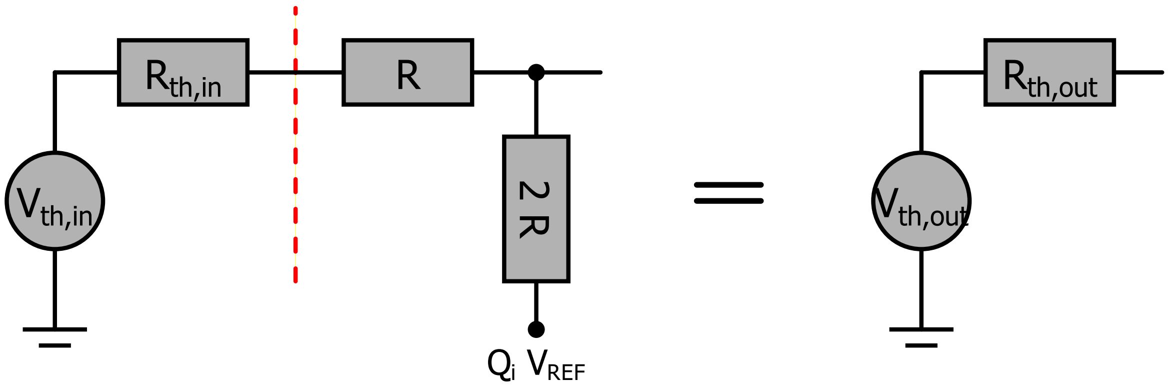
- Digital-Analog-Converters (DACs) convert a digital (normally binary coded) value into a voltage (or current) which is a normally proportional to the digital value.
- A simple circuit is the R-2R DAC:



  - The input voltages at the lower side of the 2R resistors is either 0V or some V_{REF}, depending of the binary bit (Q_0 is the Least Significant Bit, LSB).
- Show that the output voltage of a R-2R DAC with an arbitrary number N of bits is proportional to Q!
  - Hint: Replace the circuit by Thévenin equivalents at the red lines from left to right.

Solution 7

- Assume the left (driving) side of a 'red line' is given by $V_{th,in}$ and $R_{th,in}$:



  - The output resistance is $R_{th,out} = (R_{th,in} + R) \,||\, 2R$.
    For $R_{th,in} = R$, we get again $R_{th,out} = 2R \,||\, 2R = R$!
    Therefore $R_{th} = R$ in all stages.
  - Therefore, $R_{th,in}$ and the serial R add up to 2R and we *always* have a 1:1 divider!: $V_{th,out}$ *is the average of* $V_{th,in}$ *and* $Q\ V_{REF}$
  - With $V_{th,in}$ of the 0-th stage being 0, we get
    V_0 = Average$(0, Q_0 V_{REF}) = Q_0 / 2 \times V_{REF}$
    V_1 = Average$(Q_0 / 2 \times V_{REF} / 2, Q_1 V_{REF}) = (Q_1 / 2 + Q_0 / 4)\, V_{REF}$
    $V_2 = \ldots = (Q_2 / 2 + Q_1 / 4 + Q_0 / 8)\, V_{REF}$
    and so on. This is the desired linear relationship.