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Exercise:
Gain Stage

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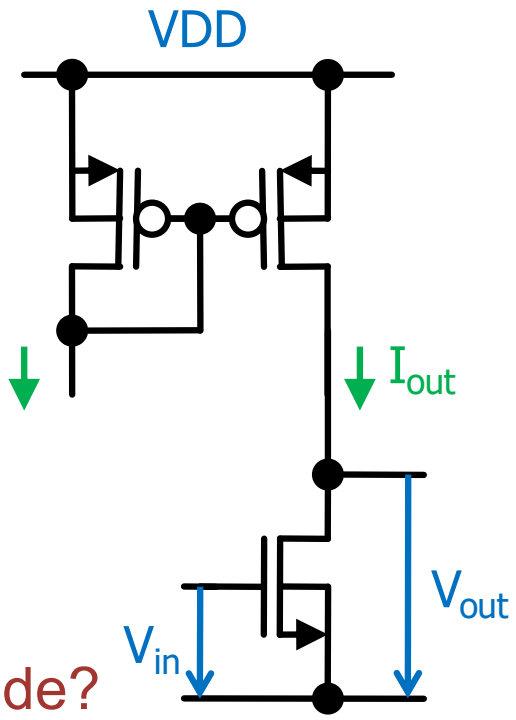
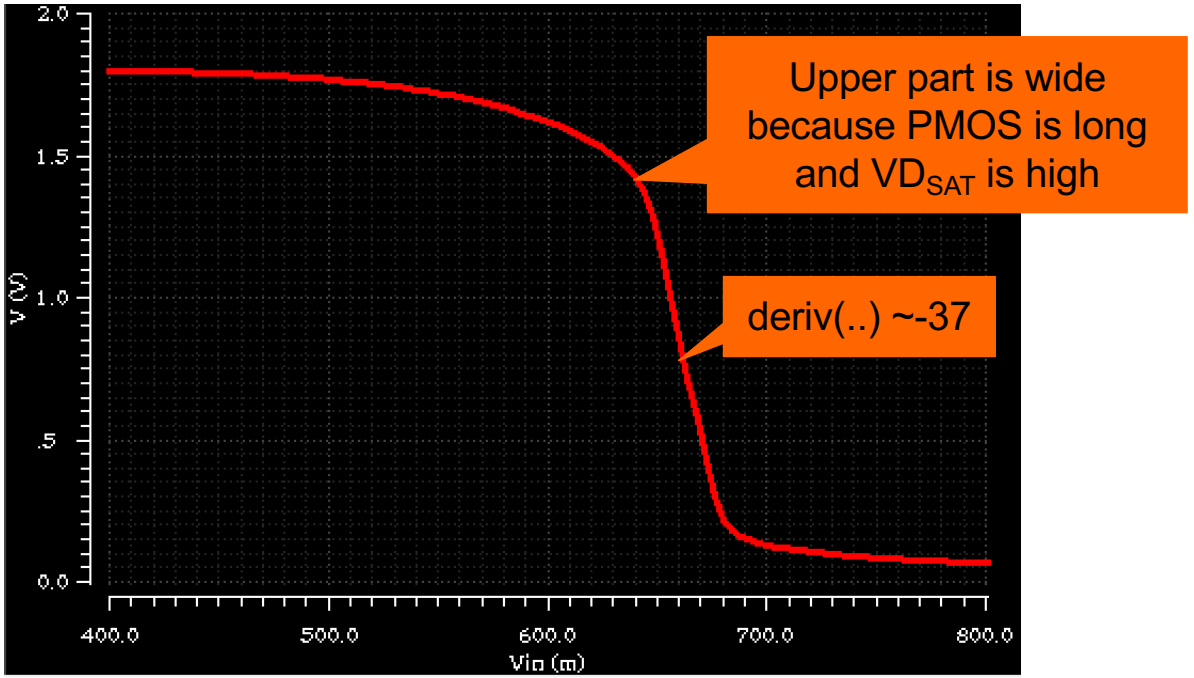
1. Basic Gain Stage

- Implement a NMOS gain stage.
  - Use real transistor models ('nmos','pmos')
  - Use a NMOS with W/L = 1µ/0.5µ
  - Use a PMOS of W/L = 1µ/1µ
  - Bias the PMOS with a *mirror* to 10µA
  - Operate at VDD = 1.8 V
- Sweep V_{in} and observe V_{out}
- What is the largest gain (derivative!) ?
- Why is the 'upper' part of the curves so wide?
- Change
  - the bias current
  - W, L of the input transistor

  and observe what happens. Explain!
  Why can't you increase gain more with W,L changes?
- Can you operate at 100µA?



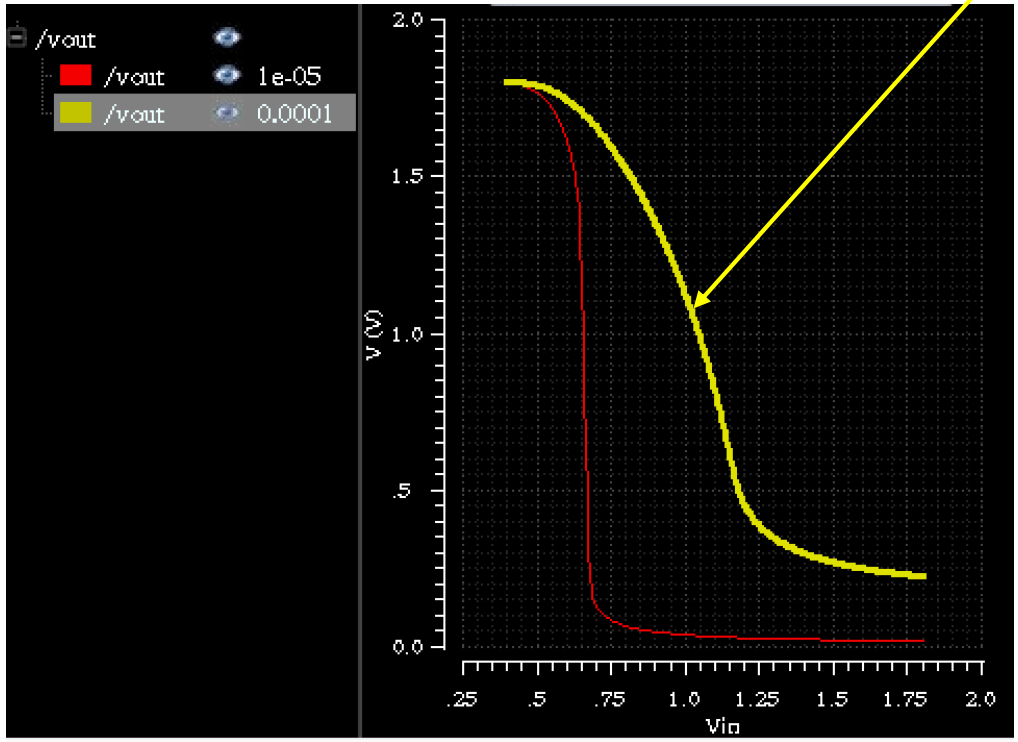
Solution 1



- WN=1u, LN=0.5u -> gain ~ -37
- WN=2u -> gain ~ -42
- LN=2u -> gain ~ -31! This is because r_{ds} of the PMOS limits! With an ideal current source, gains are (65/115) for (0.5/2)µ

Solution 1

- At 100uA, the PMOS is nearly always in the linear region.
- The circuit has too small gain



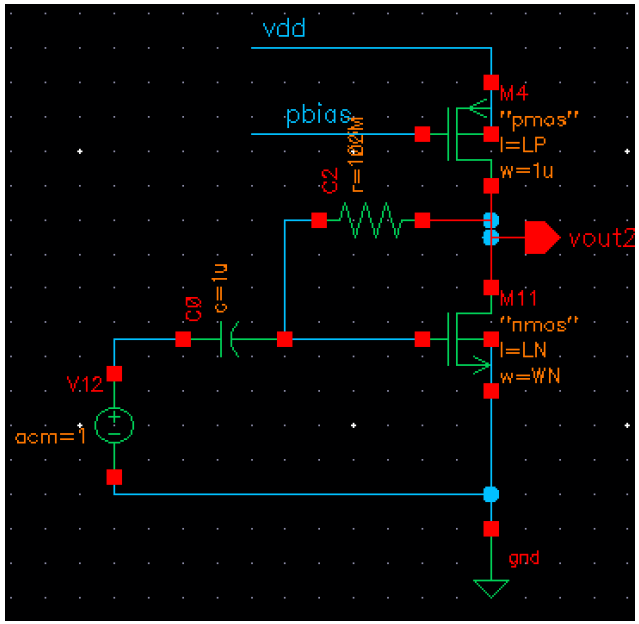
- In order to operate at 100µA, the PMOS must be made shorter and/or wider.

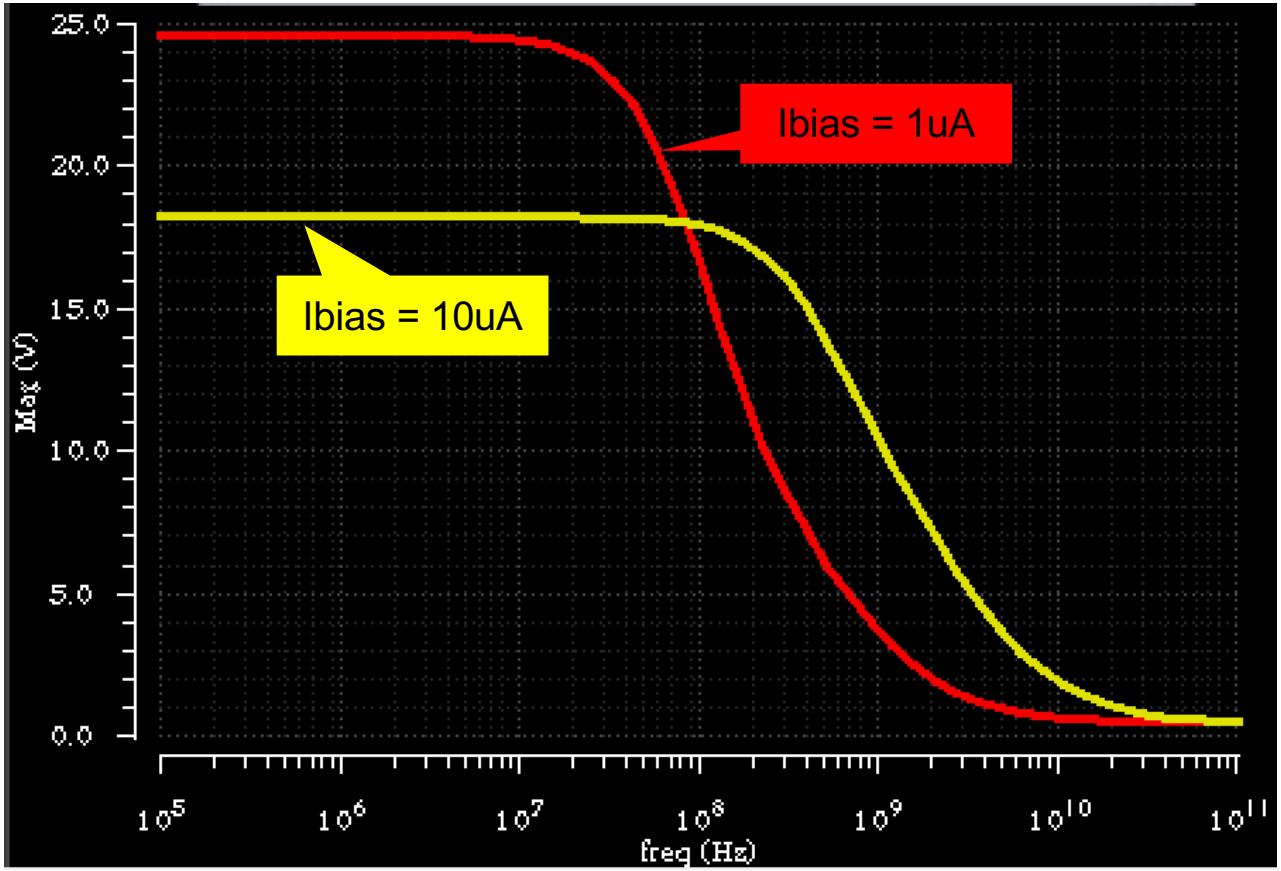
2. Operation point

- Use the trick explained in the lecture to set the operation point
  - Use for instance C=1uF, R=100MΩ
- Make an AC sweep

Solution 2

- Comparing for instance two currents:
- Higher current → less gain, but higher bandwidth



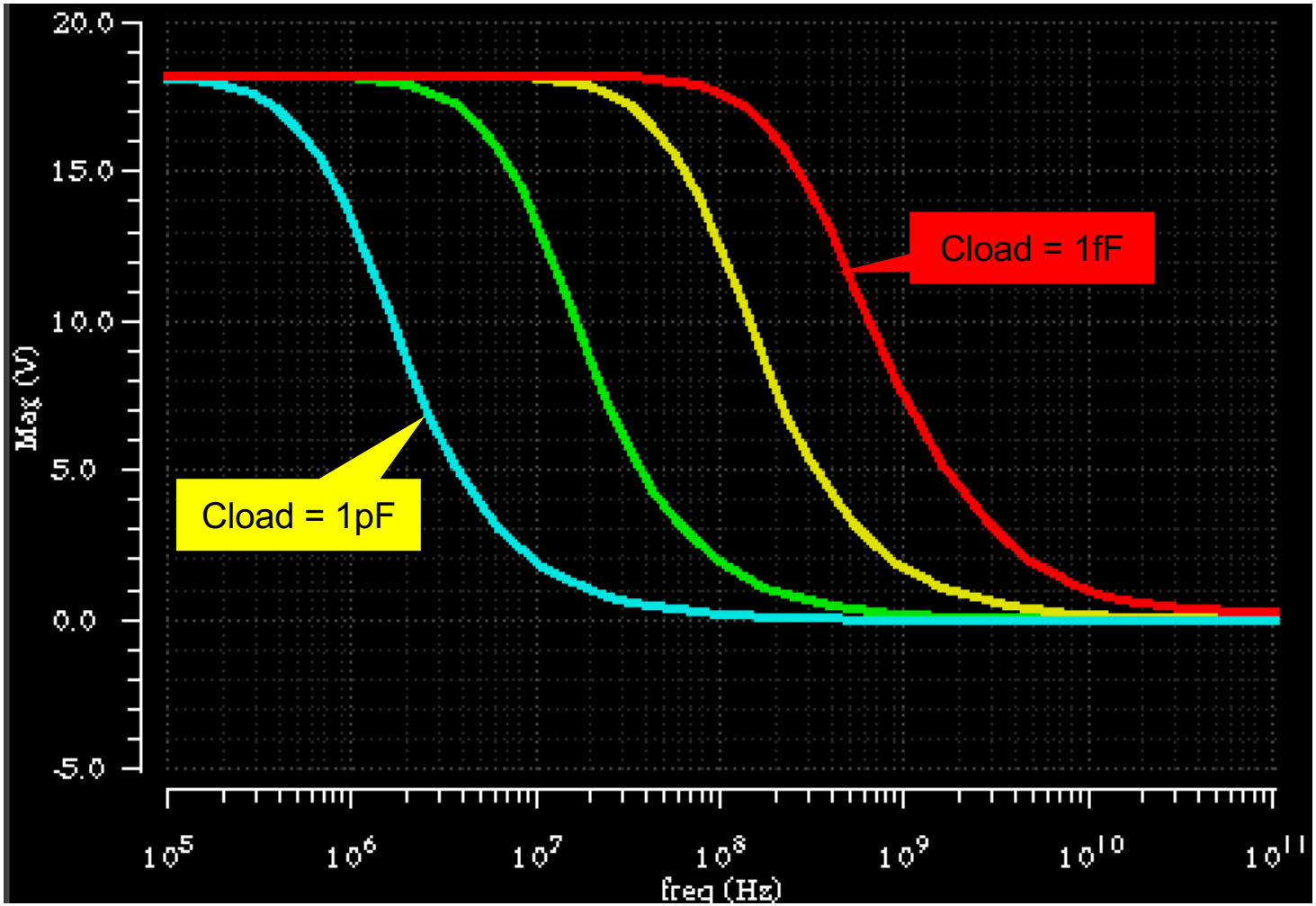


3. Bandwidth

- Load the gain stage with a capacitor (1 pF)
- Observe the bandwidth
  - best use the ‘automatic’ operation point
- Modify the load capacitor
  - Is bandwidth inversely proportional to C_L?
- Modify I_D
  - Make a Parametric Sweep with 2-3 values (0.1µA, 1µA, 10µA)
  - Do you find what you expect?

Solution 3

- Higher Load cap → less bandwidth. Proportional.
- For load cap → 0fF, bandwidth is limited by caps in MOS

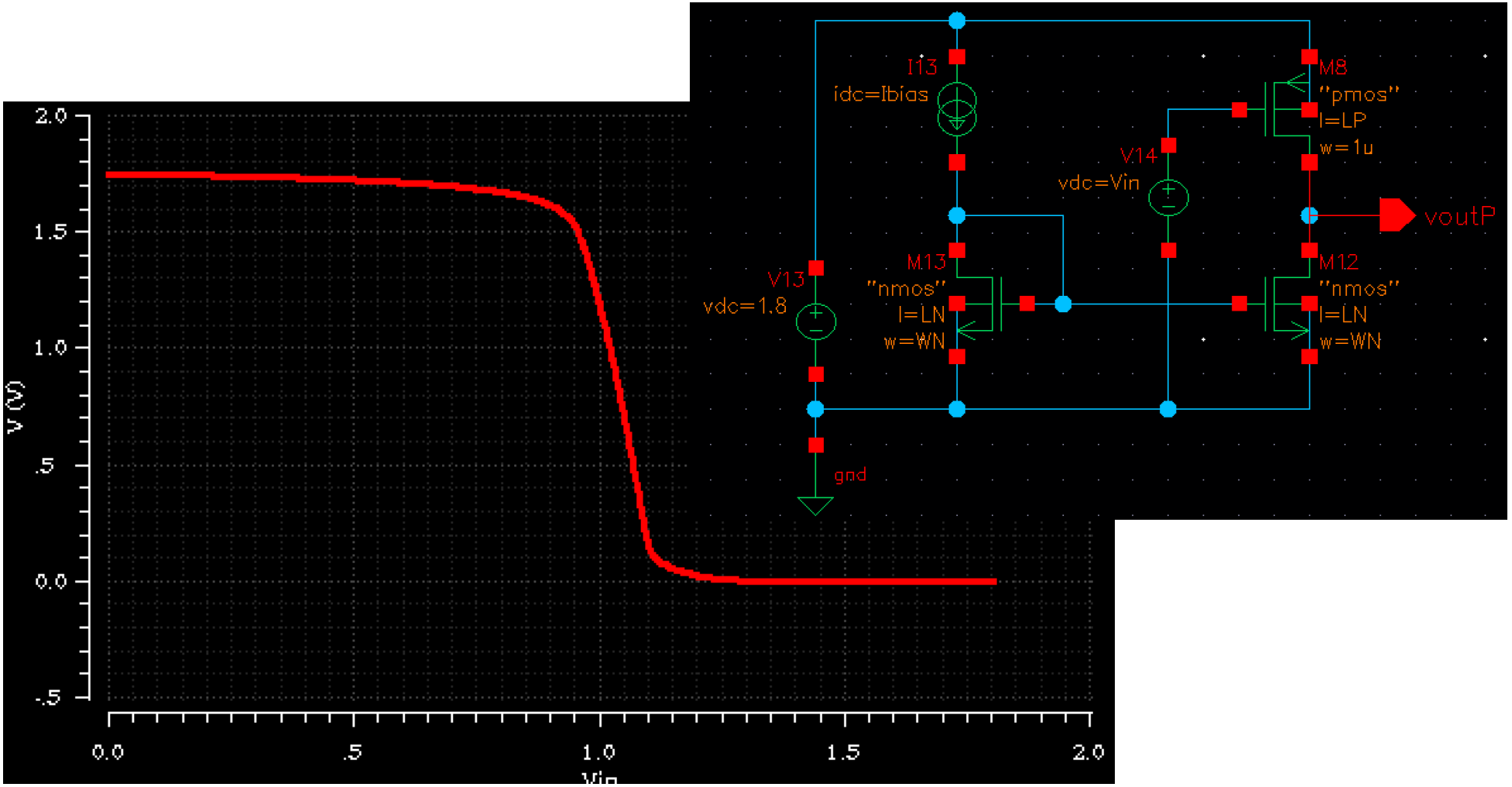


4. PMOS Amplifier

- Design a PMOS gain stage (with a NMOS current mirror load)

Solution 4:

- Note: In this case, Ground is reached ‘exactly’ (when the gain PMOS is off) and VDD is only approached.



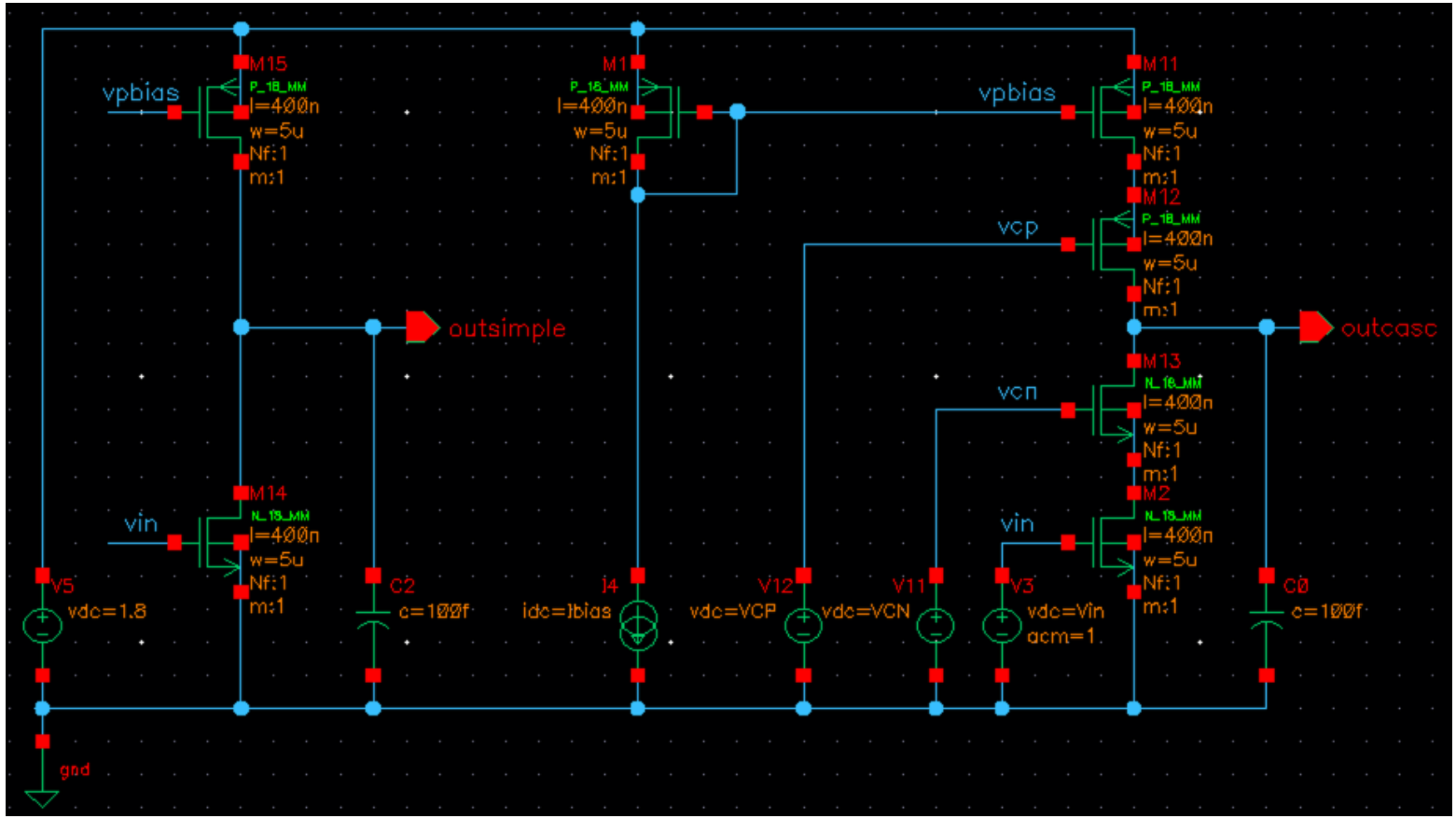
5. Cascoded Gain stage

- Set up a cascoded gain stage with NMOS input
  - Use W/L = 5µ / 0.4µ for all 4 MOS
  - Use I_{bias} = 10 uA
  - Use bias voltage VCN for the NMOS cascode, VCP for the PMOS
  - Chose ‘safe’ VCN, VCP so that the underlying MOS are saturated

- Simulate
  - Make a DC sweep. What is the gain ?
  - Try different VCN / VCP voltages. Observe and explain!
  - Use a stacked mirror generating VCP. Is that ideal?

- Make an AC sweep with a load of C_{load} = 100fF
  - Check that $v_{out} = v_{in}$ is a good operation point for AC analysis
  - Determine the gain with an AC sweep. Is it the same as above?
  - Simulate a non-cascoded gain stage in parallel an compare

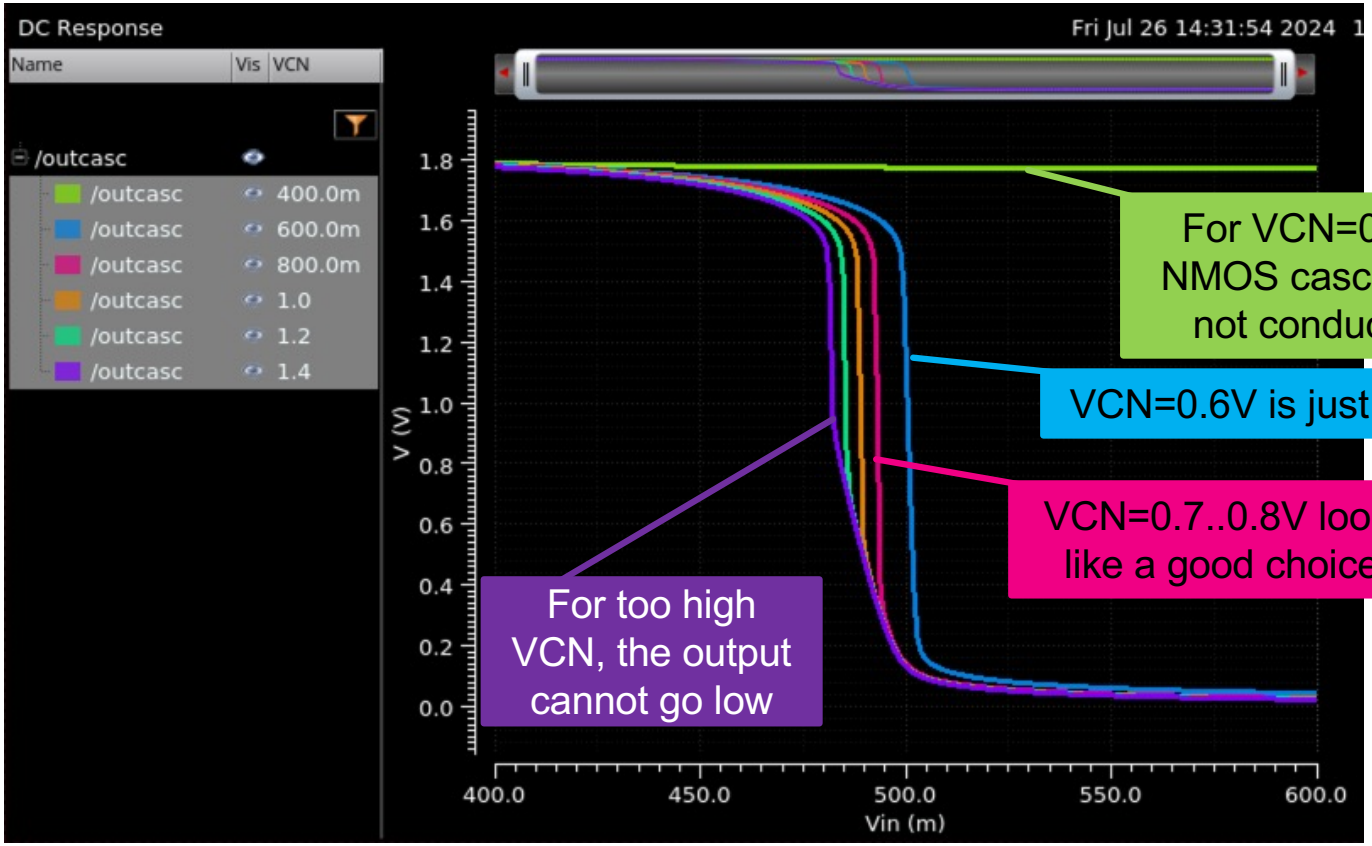
Solution 5: Cascoded NMOS gain stage



- VCN must be high enough so that the input NMOS (M2) is saturated: VCN = Vth,N (of the cascode) + Vdsat (of M2) + Vdsat of the cascode >~0.9V → start with 1V
- Similarly VCP must me >~0.9V below VDD → start with 0.8V

Solution 5: Cascoded NMOS gain stage

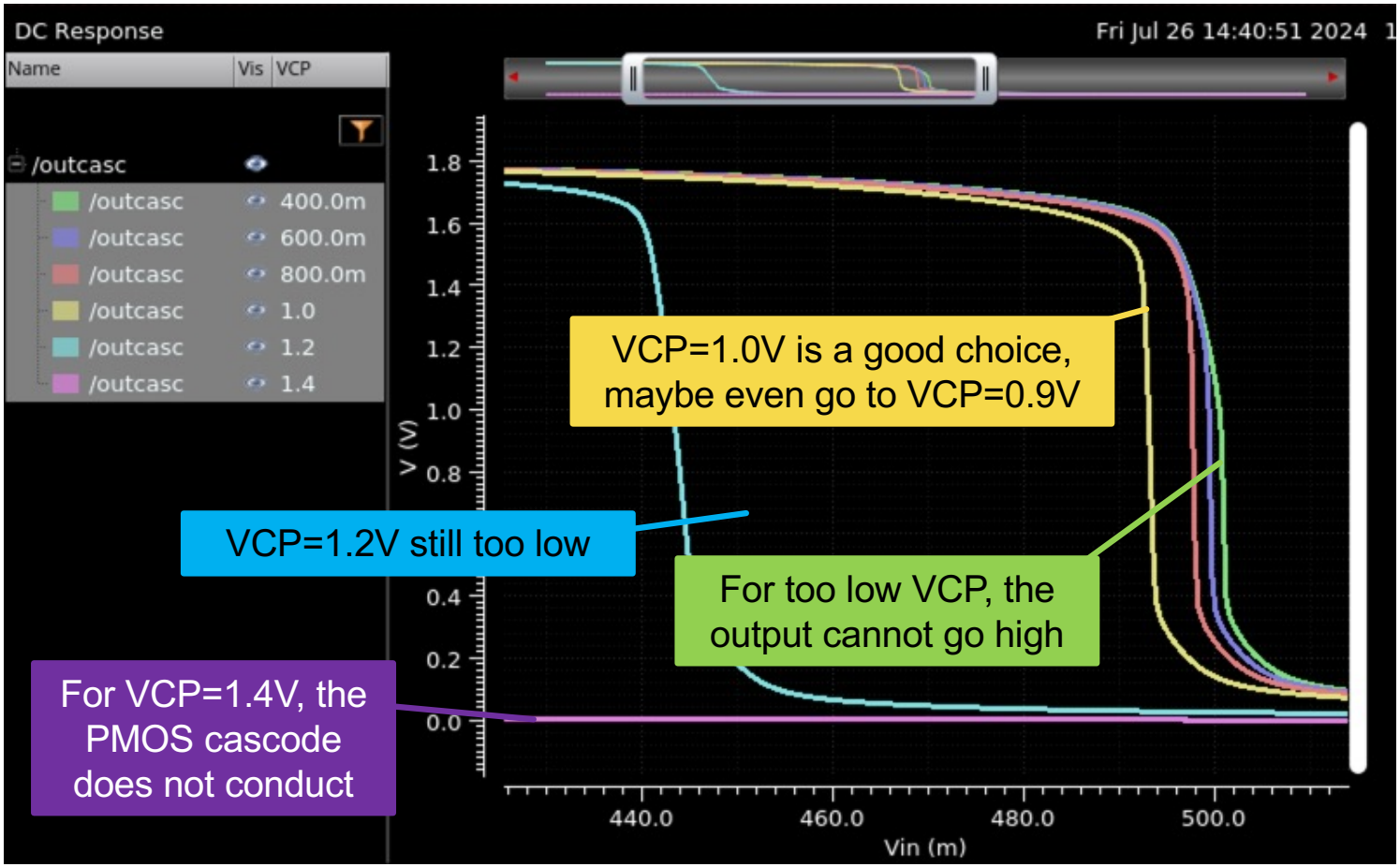
- The switching point is just above the NMOS threshold.
- Trying different VCN (for VCP = 0.8V):



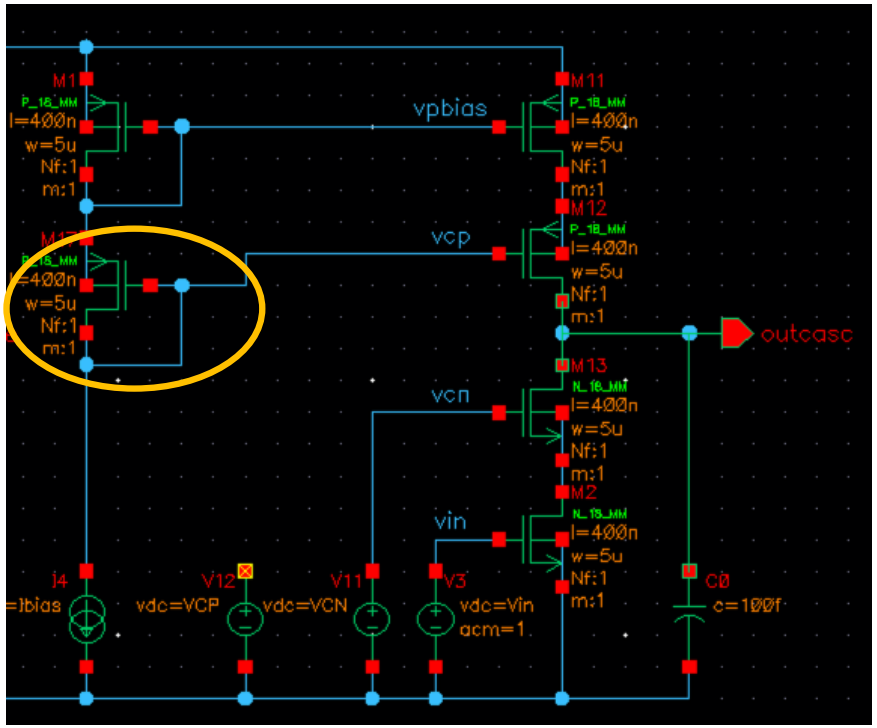
- Note that more headroom is needed for higher currents because V_{dsat} increases!

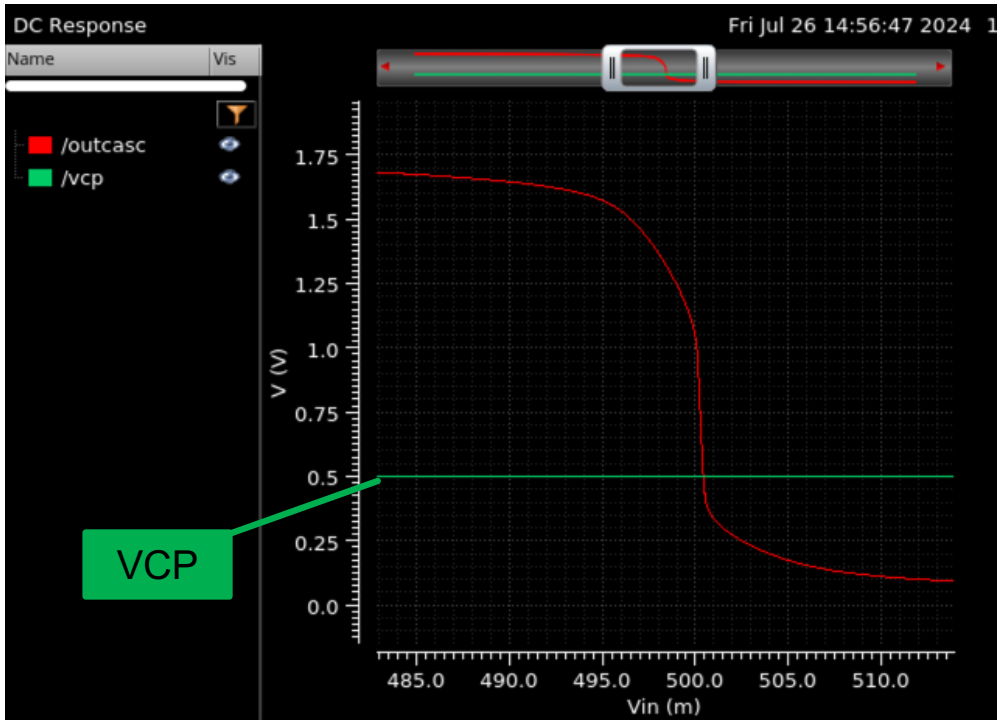
Solution 5: Cascoded NMOS gain stage

- Trying different VCP (for VCN = 0.8V):



Solution 5: Stacked PMOS mirror ?

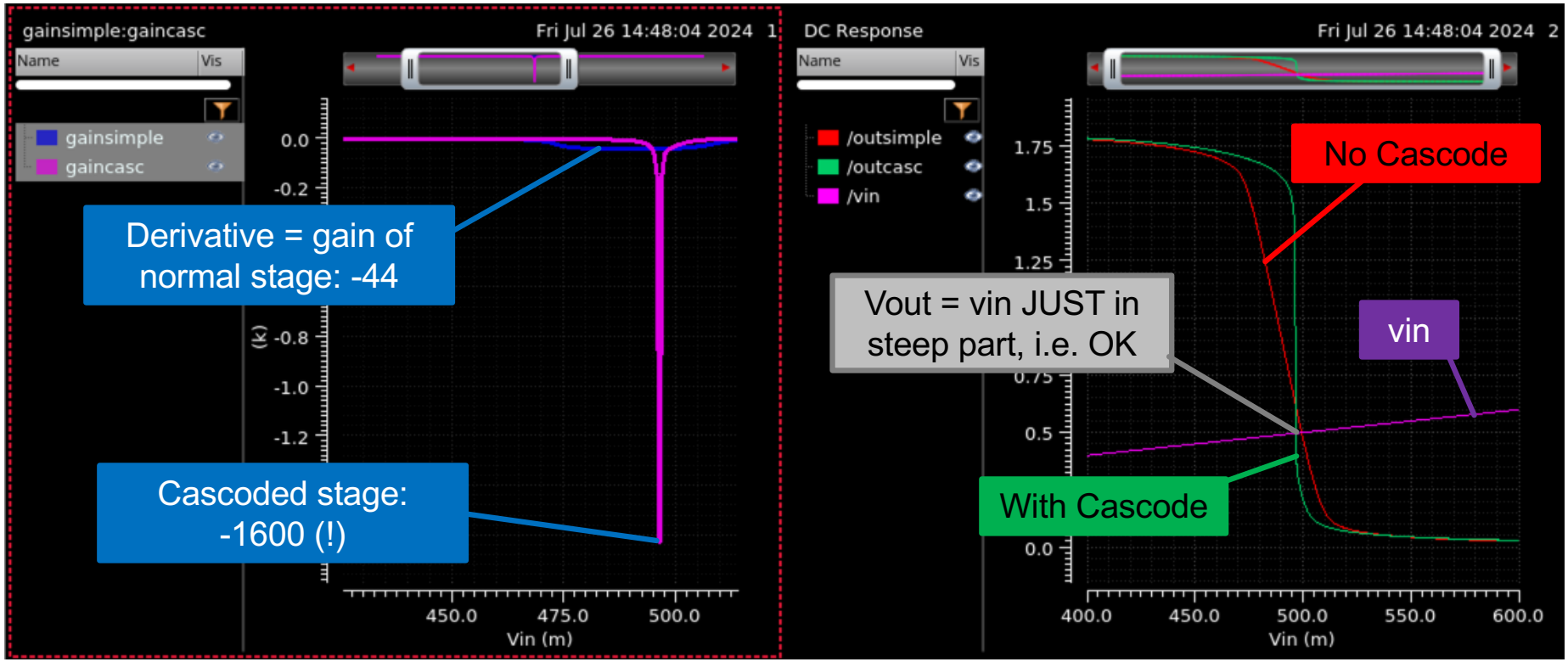




- With stacked PMOS mirror, VCP is only 0.5V
- This is too low. The output cannot go high.
  → The stacked mirror is wasting too much dynamic range!

Solution 5: DC Gain

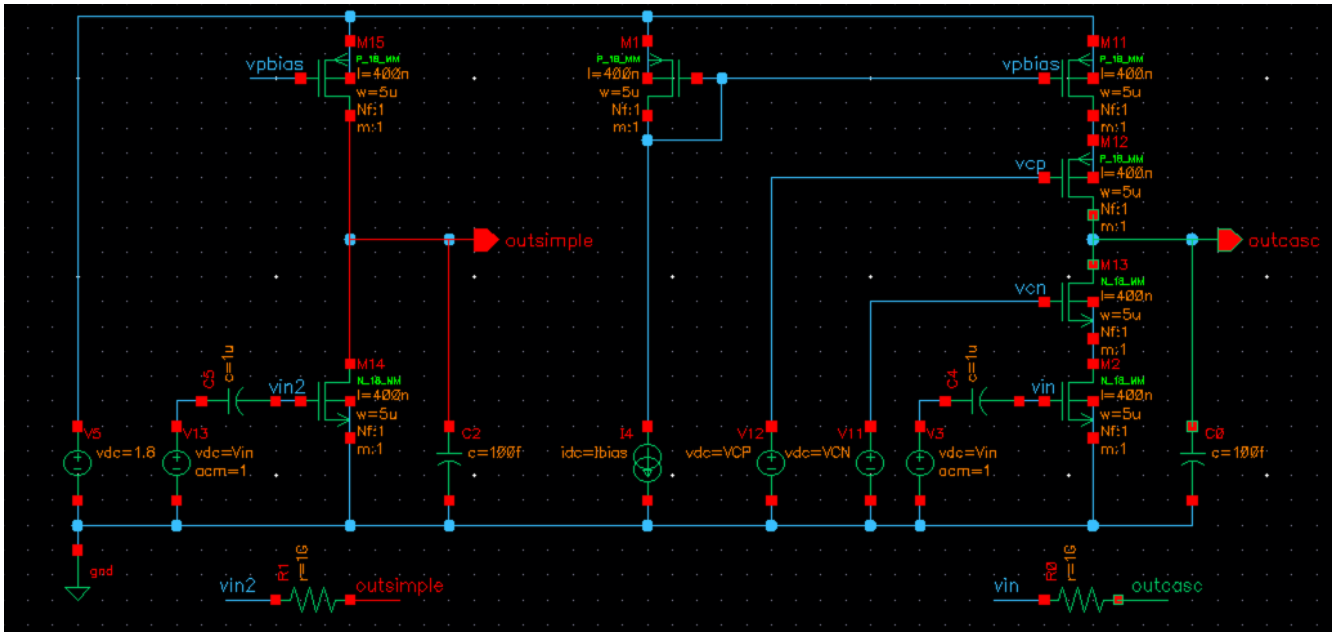
- For VCN=0.8V and VCP=0.9V:



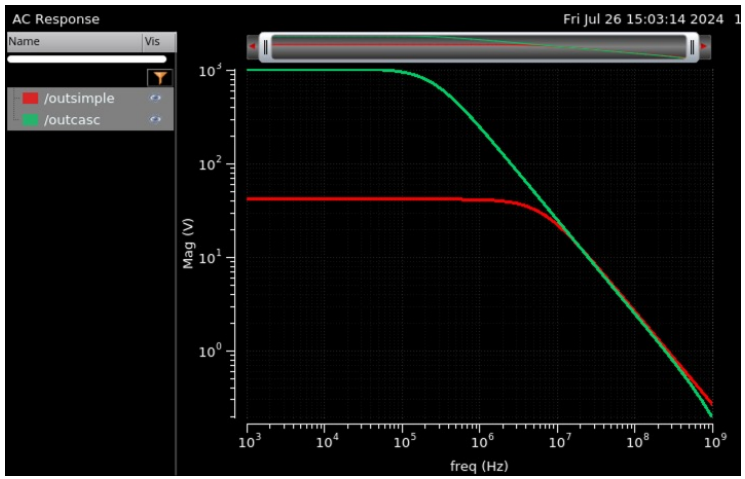
- DC feedback, i.e. vout = vin is just ok for the cascoded stage, because we are still in the steep high-gain part (see right side)

Solution 5: AC gain

- Using DC feedback as in lecture:

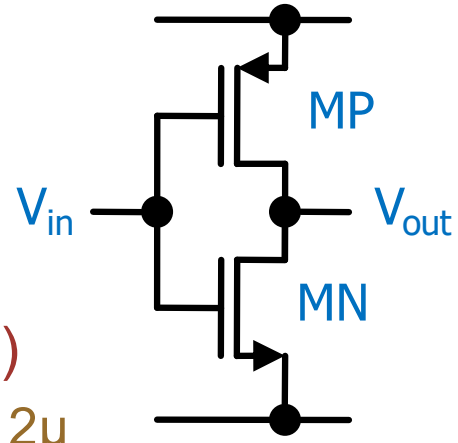


- AC gain is 42 and 1040 (using UMC transistor models)
- Close to DC. Difference is due to operation point.
- GBW is the same!



6. The Inverter

- The PMOS 'load' in the gain stage supplies a more or less constant current
- In the CMOS Inverter shown, the PMOS is switched with the input signal, it acts as the NMOS



- Simulate the DC transfer function $V_{out}(V_{in})$
  - For instance $L_N = L_N = 0.5\mu$, $W_N = 1\mu$, $W_P = 2\mu$
  - What is different from the normal gain stage ?
  - What is the maximum gain ?
- Use a small signal analysis to find the gain

Solution 6: Inverter

- For gain derivation, see lecture slides.
- The output now reaches gnd and vdd fully
- The current is not constant, it depends on Vin. This is bad!