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Exercise:
Source Follower and Differential Amplifier

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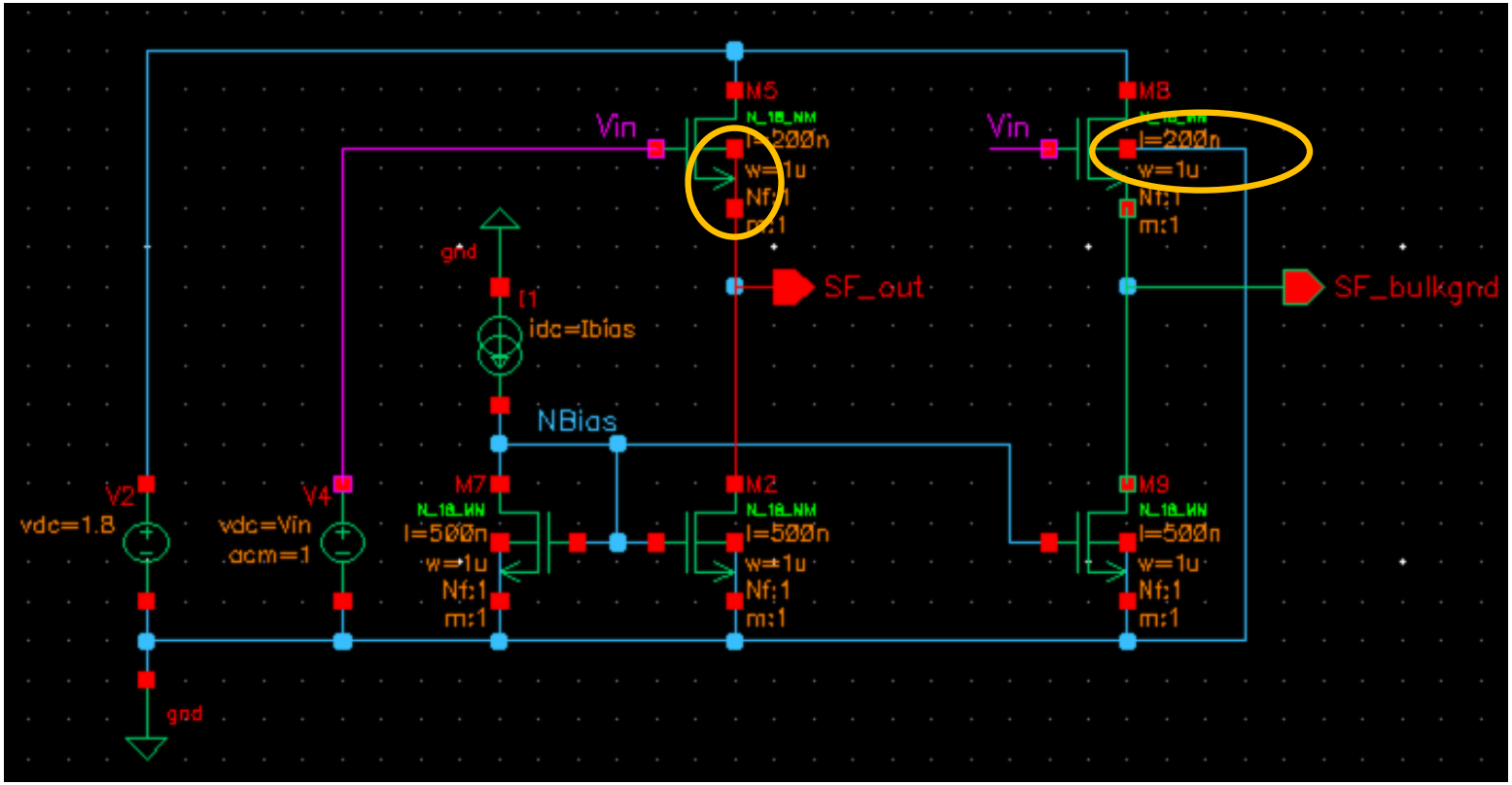
1. NMOS Source Follower

- Implement an NMOS Source follower
  - Use an NMOS with W/L = 1µ / 0.2µ
  - Connect Bulk to Source
  - Use an NMOS mirror with W/L = 1µ / 0.5µ as current source
  - Bias the circuit with 10µA

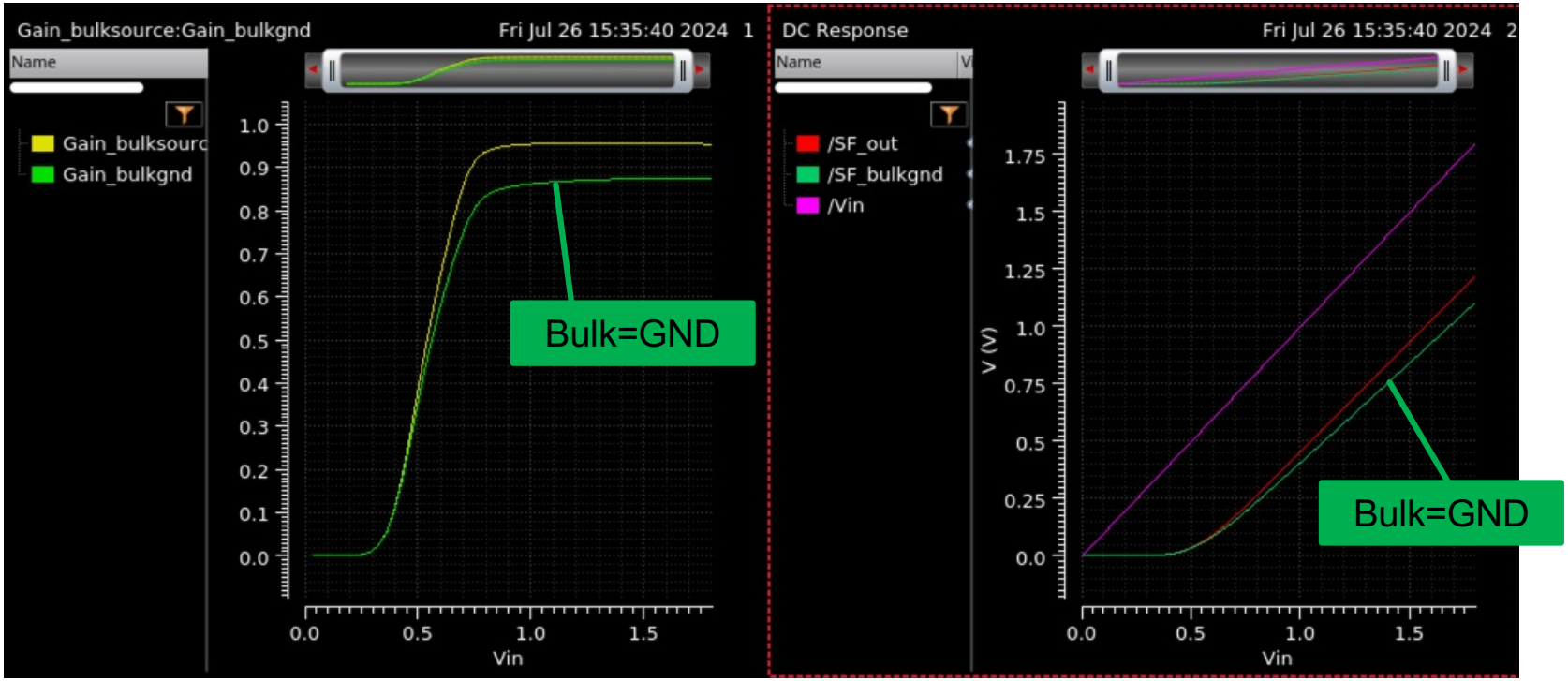
- Perform a DC and a transient analysis
  - What is the gain?
  - What happens for low input voltages? Why?
  - How does the gain change when you connect the bulk of the SF - NMOS to ground?

Solution 1: NMOS Source Follower

- Simulate bulk=source and bulk=GND in parallel:



Solution 1: DC Sweep

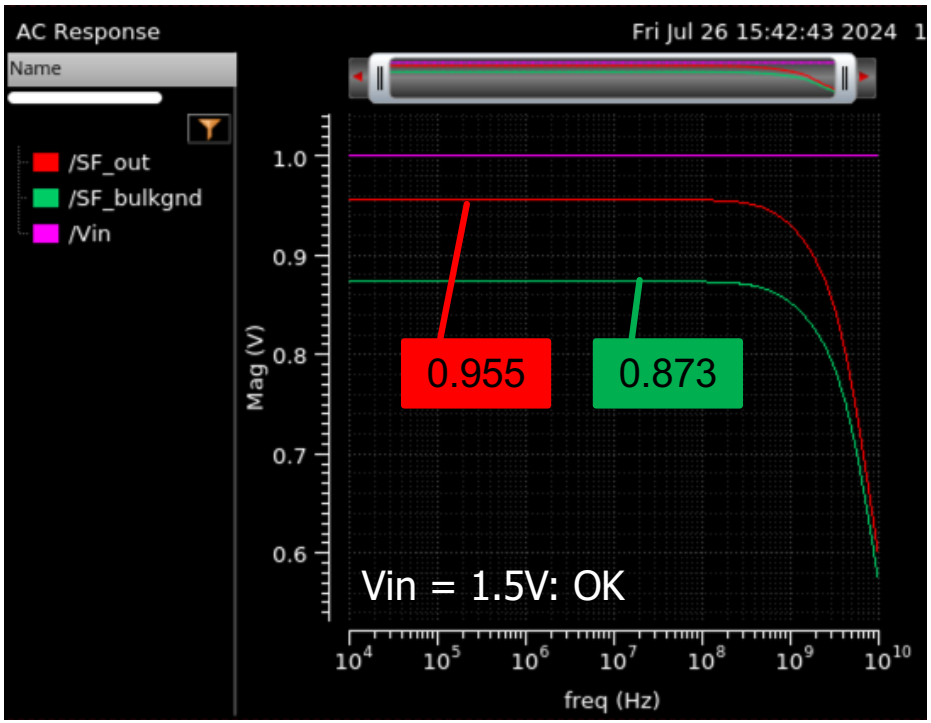


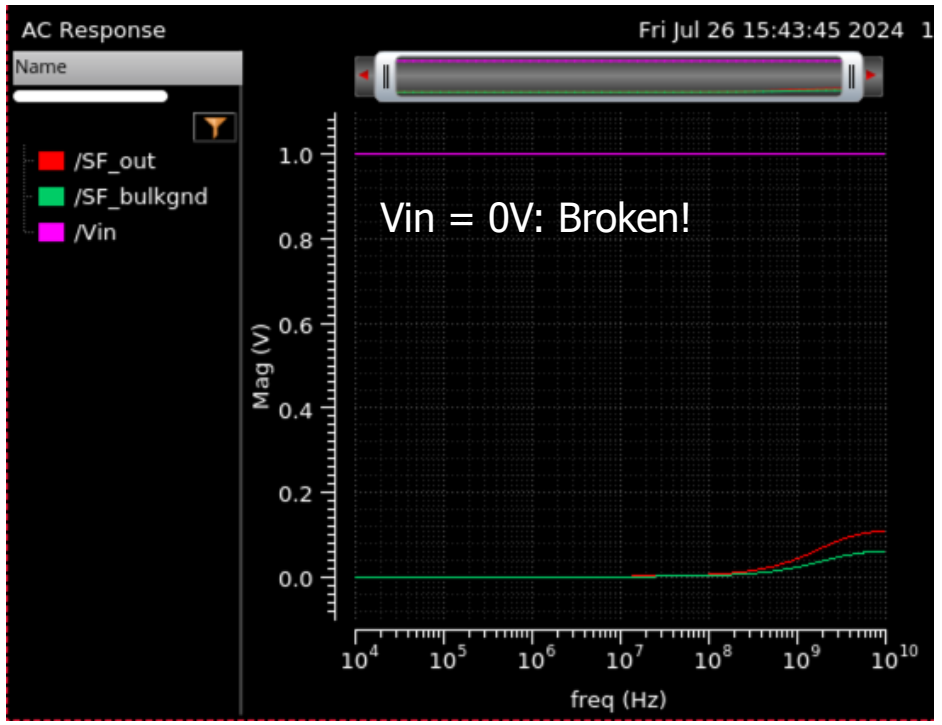
- Gain for bulk=source: ~0.95
- Gain for bulk=GND: ~0.87

- The output is a bit more than Vth below the input.
- Because the output cannot go below gnd, input voltage must be > Vth.

Solution 1: AC Sweep

- Watch out: The operation point must be correct!!!
- Here, the (DC) input voltage must be high enough, so that we do not simulate the AC sweep in the left part of the curve!!!



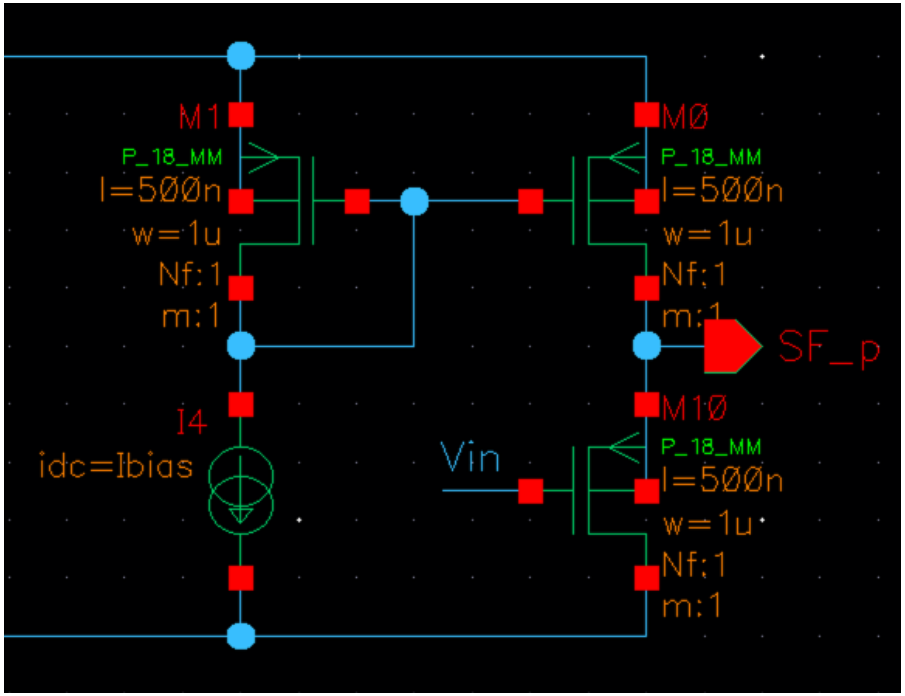


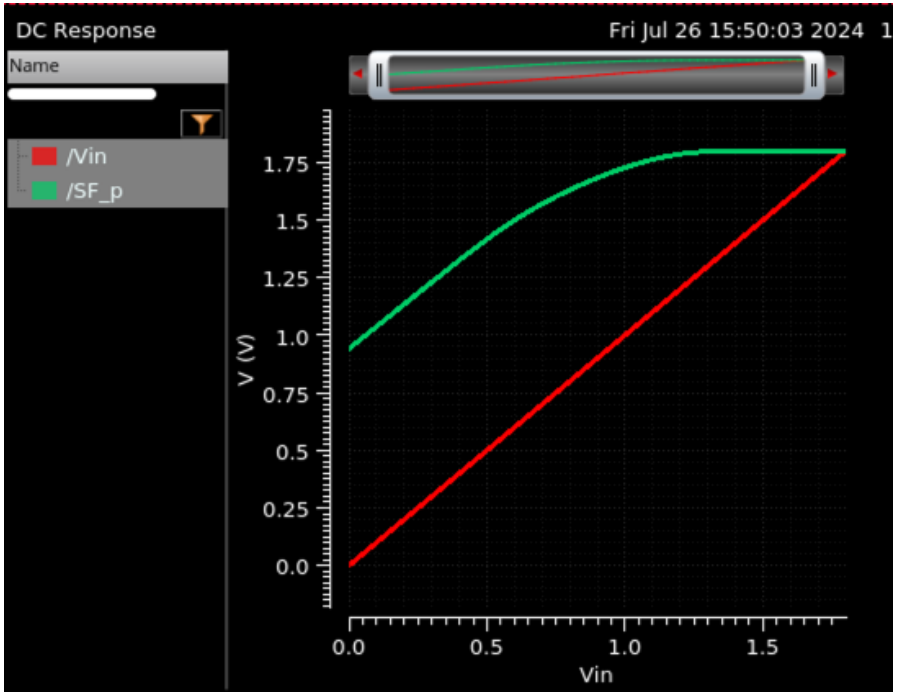
2. *PMOS* Source Follower

- Now draw a ***PMOS*** source follower with the same transistor dimensions & current...

- Which input voltages are now problematic?

Solution 2: PMOS Source Follower





- The output is now *higher* than the input.
- Therefore high input voltages are problematic.
- The voltage difference between input and output is higher than for the NMOS version at same transistor sizes and current. This is because more V_{GS} is required for the same current.

3. (Optional: SF Instability)

- Repeat the situation from the lecture slides:
  - SF driven by a (large) source impedance
  - Added load capacitance
  - Added capacitance between input and output (an exaggerated C_{GS})

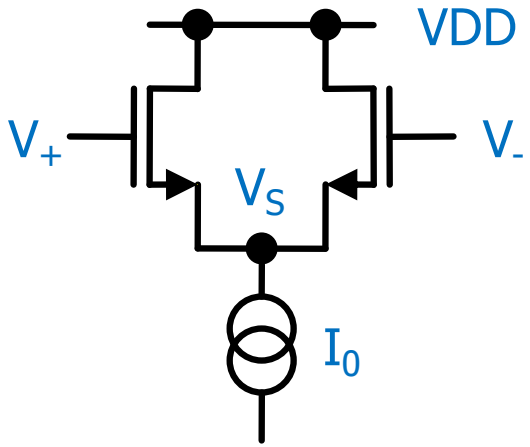
- Observe the overshoot in the transient response for a step input or the increased gain in an AC sweep.

Solution 3

- See lecture slides…

4. Differential pair

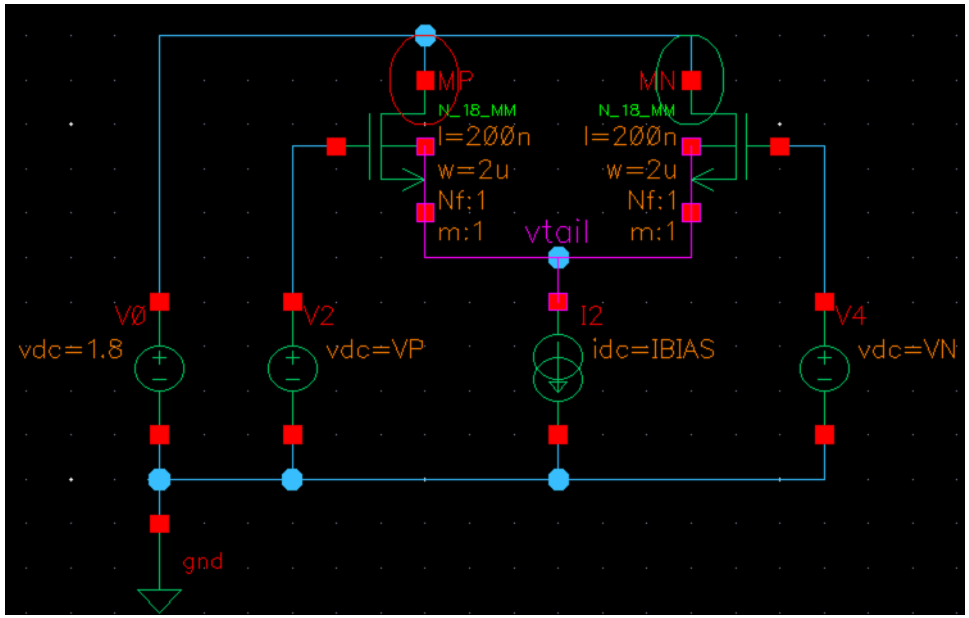
- Draw a differential NMOS pair

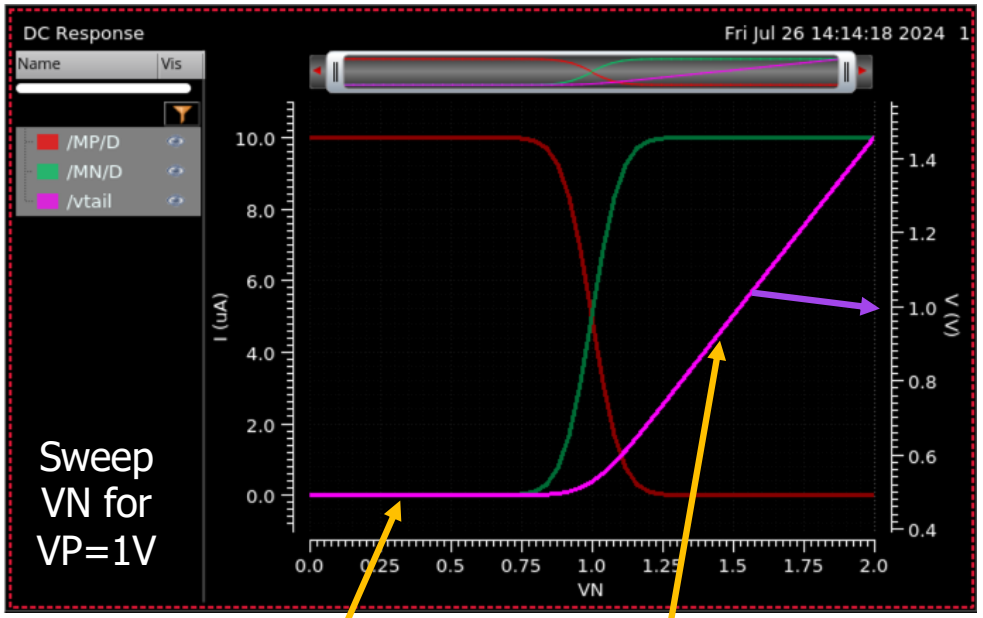


- Set V_- = 1 V and vary V_+ from 0 to VDD = 2 V
  - Observe I_+, I_- and the 'tail' voltage V_S.
  - Explain what you see!

- Change the bias current I_0 or the transistor dimensions.
  - Observe how the switching region changes (i.e. which voltage difference is needed to switch fully). Do you understand?

Solution 4: Switching and tail Voltage

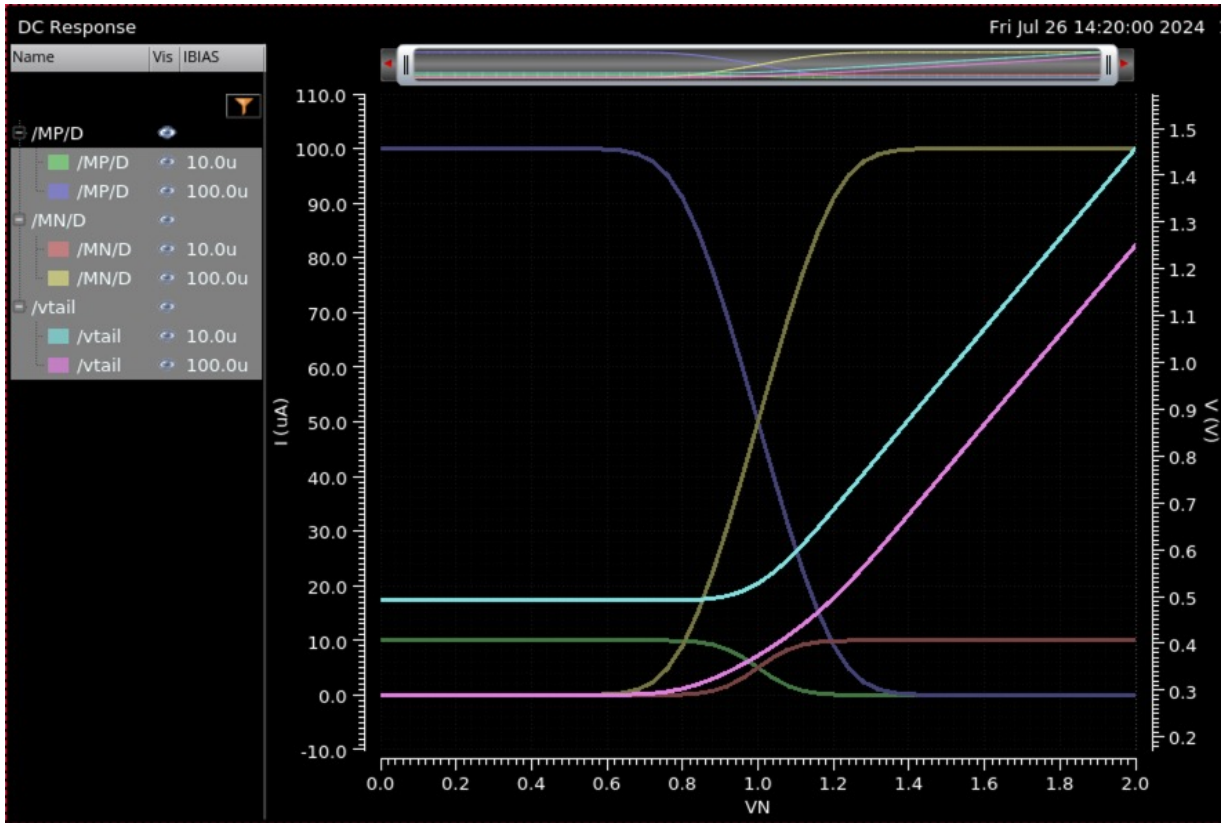




- Current switches in ~200mV
- Vtail is
  - For VN<<VP, all current flows through MP, independent of VN. vtail is a bit more than Vth below VP (here: just below 500mV)
  - For VN>>VP, all current flows through MN. vtail follows the gate voltage of MN, i.e. it is a bit more than Vth below VN

Solution 4: Switching for Higher Current

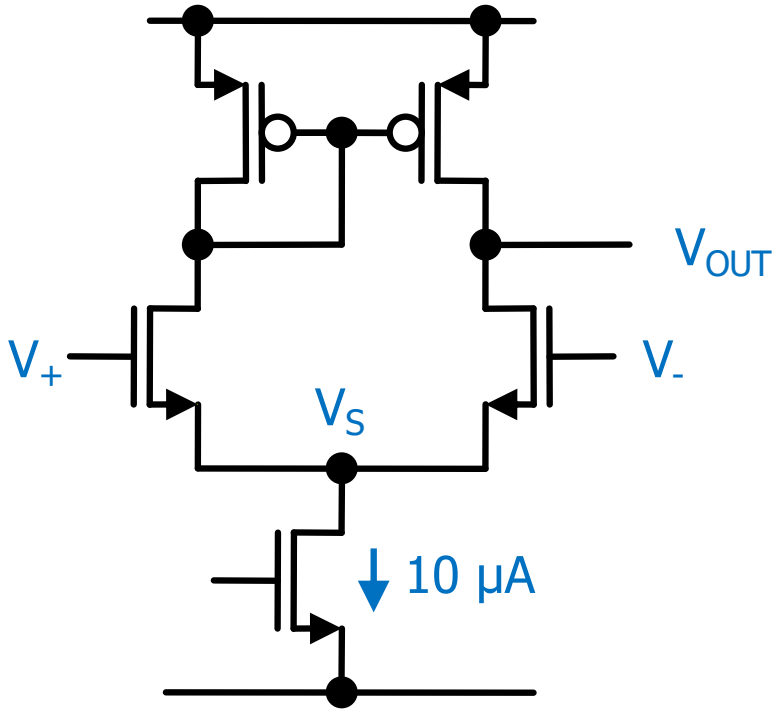
- Comparing I_{bias} = 10/100uA:



- At 100uA, the pair needs more voltage to switch fully.
- vtail is smaller at 100uA because more V_{GS} is needed for more current

5. Differential Amplifier

- Draw a full differential amplifier. Start with all W/L = 1u/0.5u



- Start with V_- = 0.5V
- What is the gain at the switching point?
  - Use a DC sweep. Also try an AC sweep with appropriate bias.
- Check the large signal behavior for different V_-.

Solution 5:

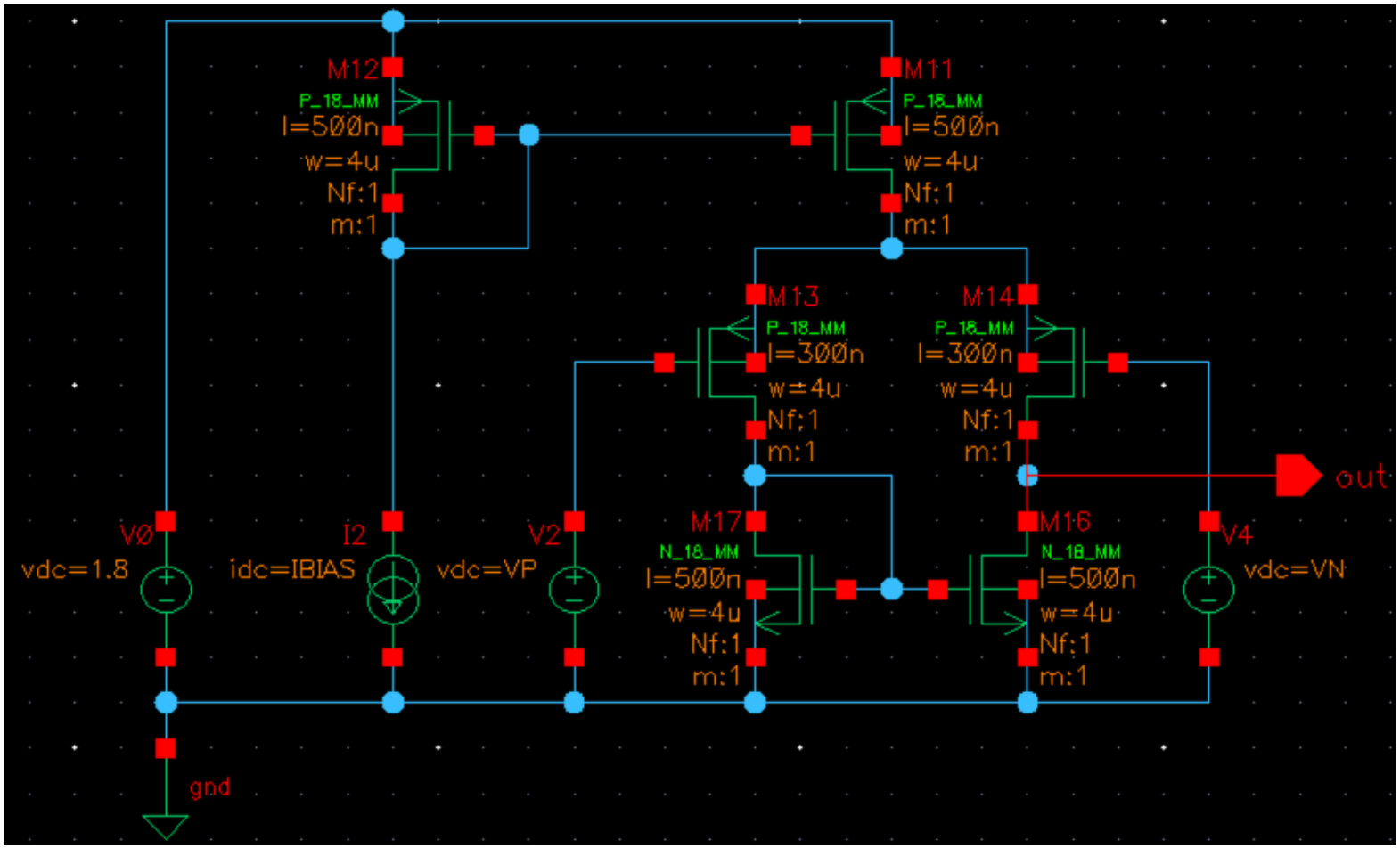
- See lecture slides

6. *PMOS* Differential Amplifier

- This exercise is only useful if you have problems to switch from NMOS to PMOS circuits…

- Draw a full differential amplifier with a PMOS input stage
  - You must also change the other MOSs…

Solution 6: PMOS Differential Amplifier



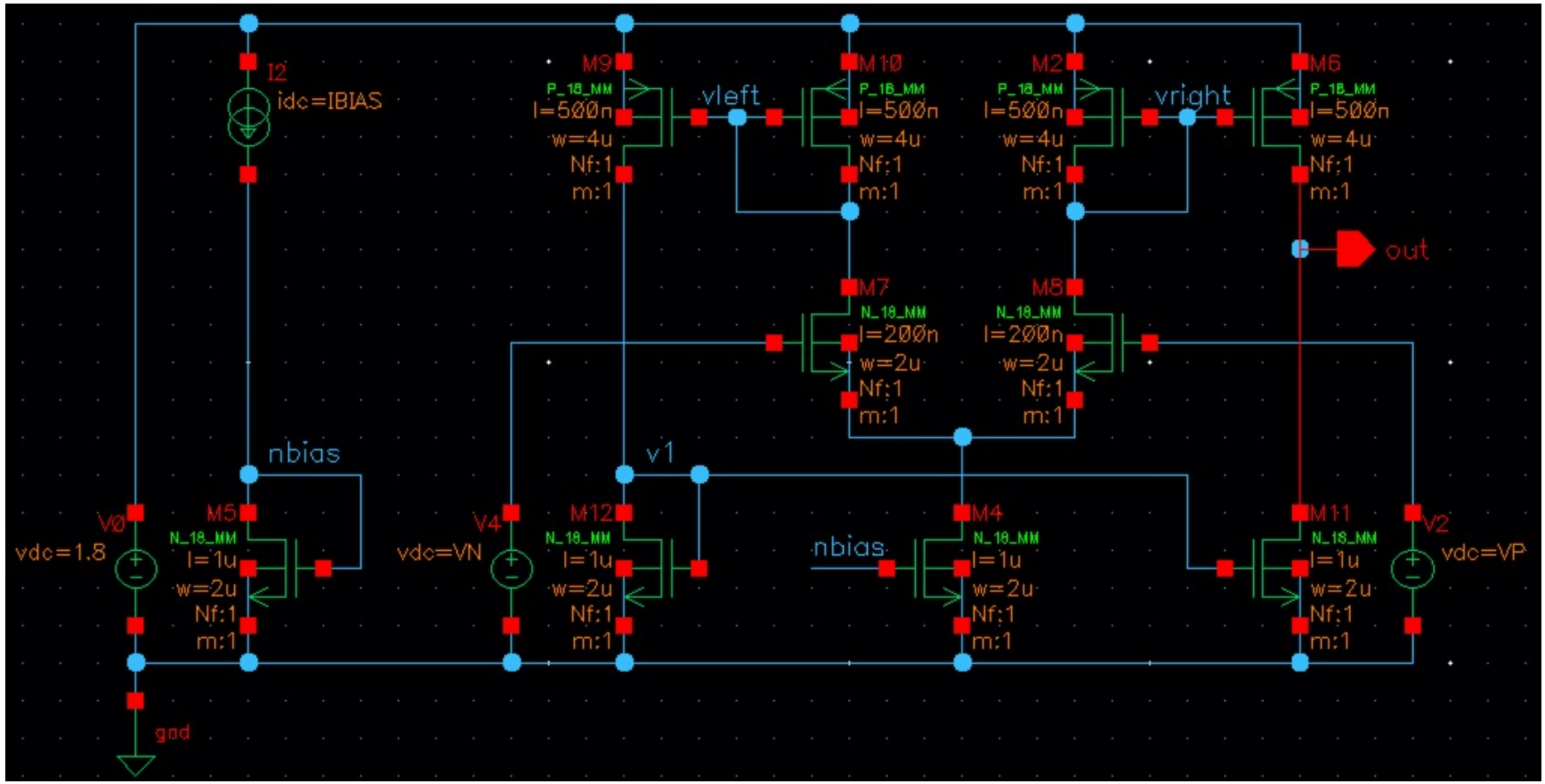
7. Mirrored Amplifier

- Implement the mirrored amplifier from page 23 of the lecture slides.

- Sweep V_+ for various constant V-. Observe the output. What is the difference to the normal differential amplifier?
- When used as transconductor (driving in a constant output voltage), what output voltages are possible?

Solution 7: Schematic

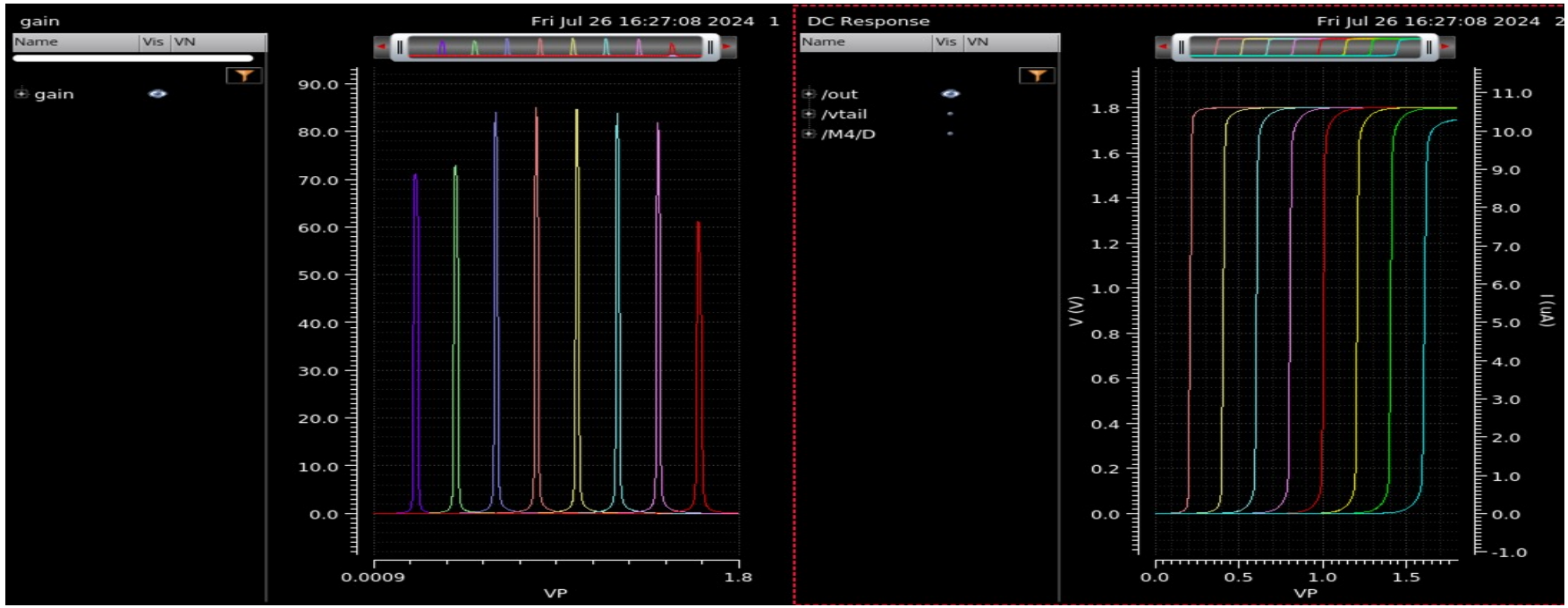
- Here with NMOS differential pair



- Note that positive input is now at the output side

Solution 7: DC Sweep

- Sweep VP for VN = 0.2V … 1.6V: Too good to be true…



- No output voltage effects over large input range! Nice!
- The output can go from $VD_{Sat,NMOS}$ to VDD-$VD_{Sat,PMOS}$!

- BUT: How can this work at VN = 0.2V? Vtail is much too low. -> Next page

Solution 7: Watch out!

- When VN is too low, vtail is low. The NMOS are very far in weak inversion and current is nearly zero. The DC sweep only works because the simulation is not afraid of nA currents…
- Check this by looking at the current in the tail source M4: Current starts to drop ‘illegally’ at VN = 0.6V, as expected.