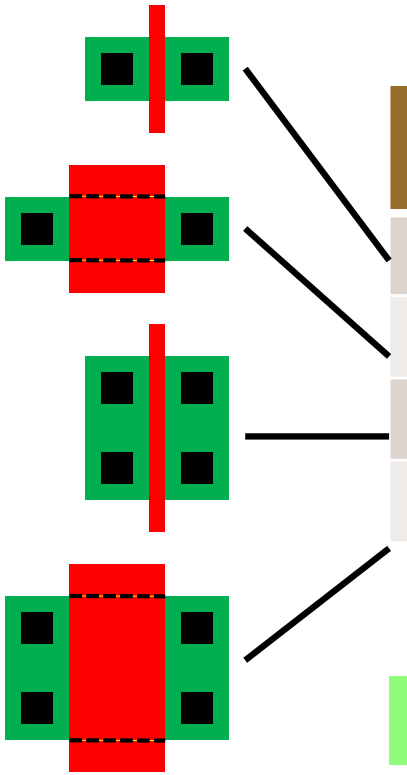
Current Mirrors

Our first ‘useful’ circuit

(you will understand later THAT this is REALLY useful)

Reminder: Effect of Transistor Sizes

- *Very* crude classification (at constant V_{GS}):

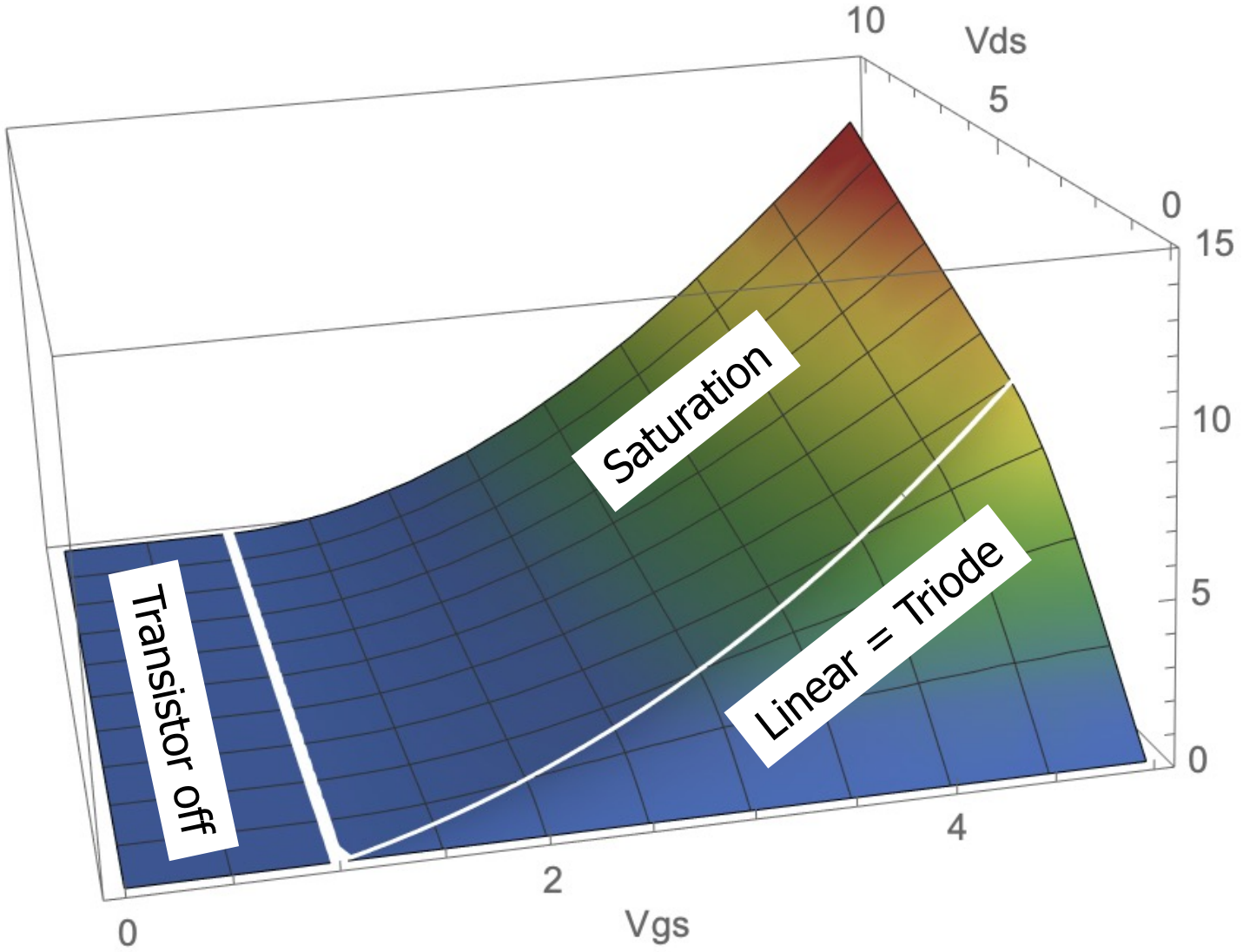


W	L	Current	Output Resistance	Gate Capacitance
small	small	0	low	small
small	large	-	high	high
large	small	+	low	high
large	large	0	high	very high

good | normal | bad

- There is no 'perfect' size – all depends on what we need!

Reminder: Transistor Characteristics

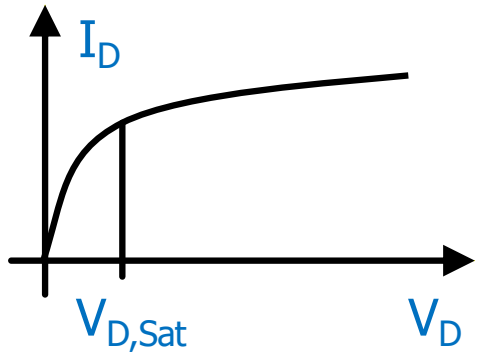


Reminder: Threshold and Saturation Voltage

$$I_D = \frac{K}{2}\frac{W}{L}\left(V_{GS} - V_T\right)^2 = \beta\left(V_{GS} - V_T\right)^2$$

$$V_{D,Sat} = V_{GS} - V_T = \sqrt{\frac{I_D}{\beta}}$$

$$V_{GS} = V_T + V_{D,Sat}$$



$$K \approx 100\,\mu A/V^2,\ W \approx 1\,\mu m,\ W \approx 0.2\,\mu m \quad \rightarrow \quad \beta \approx 250\,\mu A/V^2$$

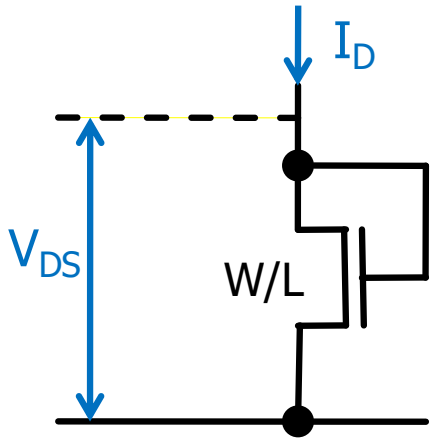
$$\text{For} \quad I_D = 10\,\mu A \quad \rightarrow \quad V_{D,Sat} \approx 0.2\,V$$

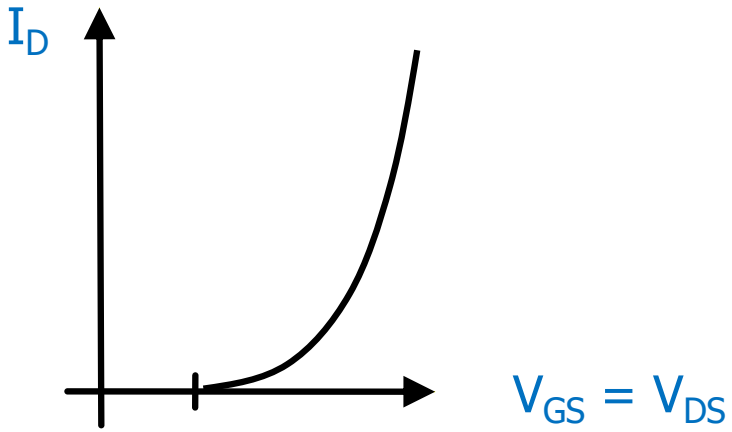
- This is all *only* valid for strong inversion (at 'large' currents)
- $V_{D,Sat}$ increases with larger current (with the $\sqrt{}$)

The Diode-Connect MOS

- Consider a MOS with Drain and Gate connected
- $\mathbf{V_{DS} = V_{GS}} \rightarrow \mathbf{V_{DS}} = V_{GS} > V_{GS} - V_T = \mathbf{V_{DSat}}$

→ A diode connected MOS is always in saturation!





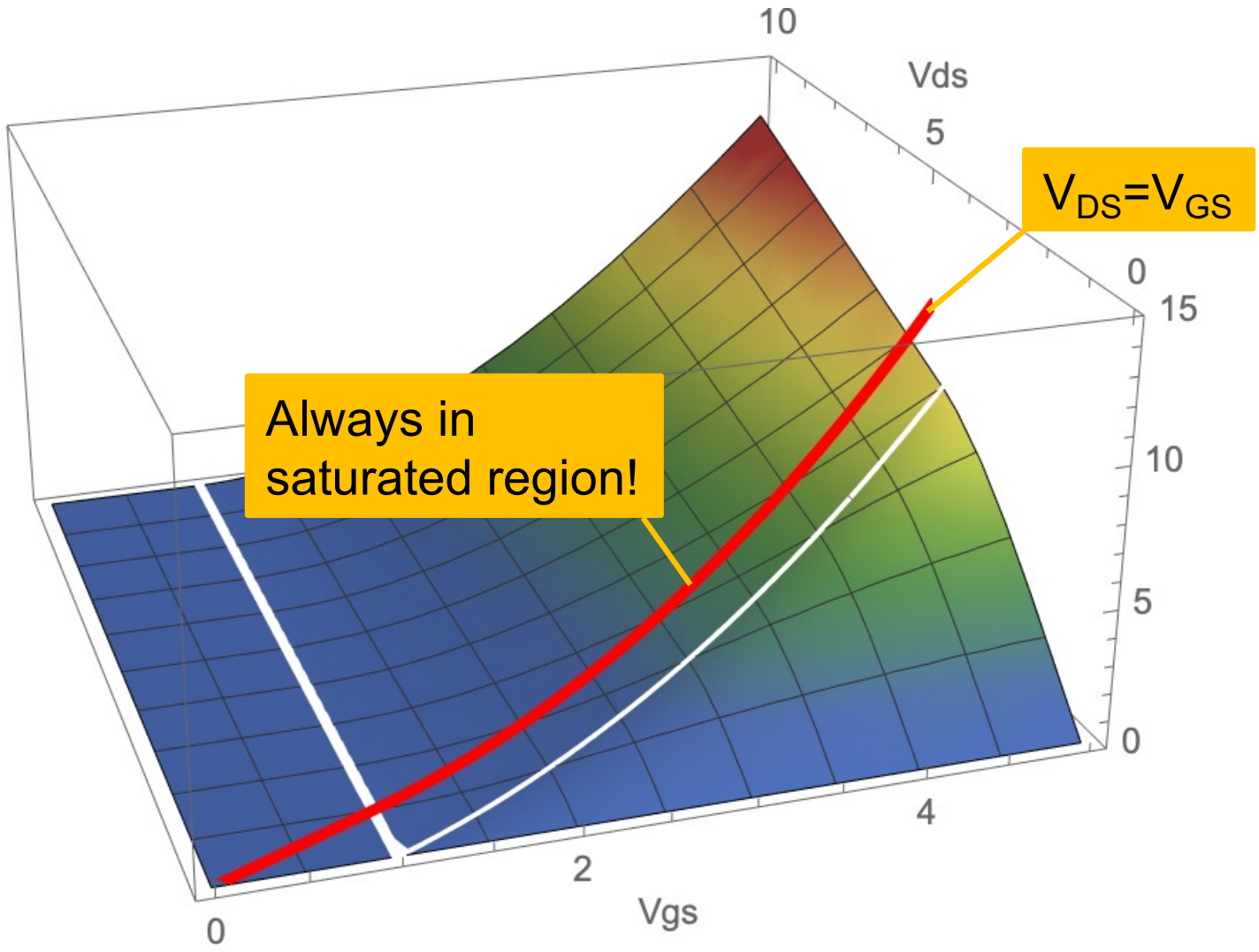
$$I_D = K/2\ W/L\ (V_{DS}-V_T)^2\ (1+\lambda\ V_{DS})$$

(in 'strong inversion')

- Important:

For *any* current I_D, V_{GS} adjust so that this current can flow!

Illustration: $V_{DS}=V_{GS}$



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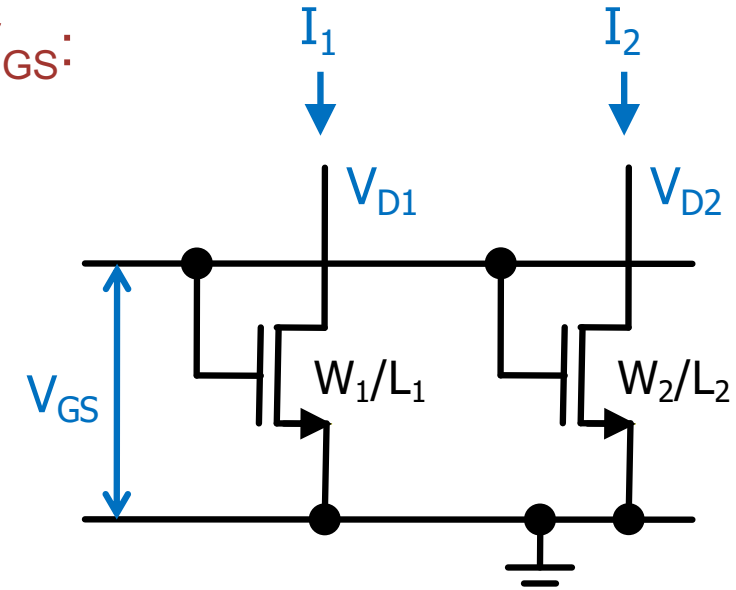
THE CURRENT MIRROR

Transistors with same V_{GS}

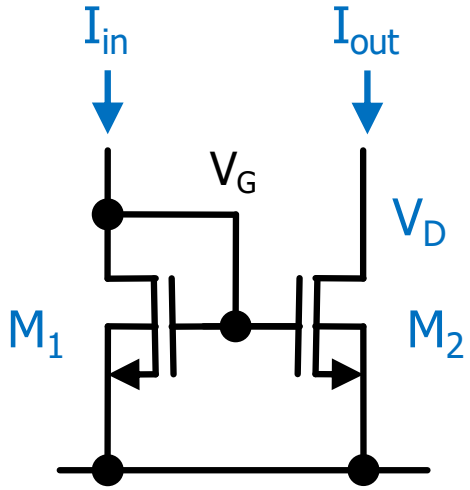
- Consider 2 NMOS with same V_{GS}:



- Assuming saturation:
  - $I_1 = \frac{K}{2}\frac{W_1}{L_1}(V_G - V_T)^2(1+\lambda_1 V_{D1})$
  - $I_2 = \frac{K}{2}\frac{W_2}{L_2}(V_G - V_T)^2(1+\lambda_2 V_{D2})$
- $\rightarrow \frac{I_2}{I_1} = \frac{W_2/L_2}{W_1/L_1}\frac{1+\lambda_2 V_{D2}}{1+\lambda_1 V_{D1}}$
- For $L_1 = L_2$:
  - The ratio of input/output current is roughly given by the ratio of the Ws
  - The Early effect leads to a ‚small' deviation
  - The Early effects cancel if $V_{D1} = V_{D2}$ (for same λ)

The Current 'Mirror'

- First, we assume that M_1 and M_2 are identical
  - $W_1 = W_2$, $L_1 = L_2$
- Now connect M_1 as a diode
  - V_G adjusts such that I_{in} flows into M_1
- M_2 and M_1 have the same gate voltage → $I_{out} = I_{in}$
  - The current is 'mirrored' from the input to the output

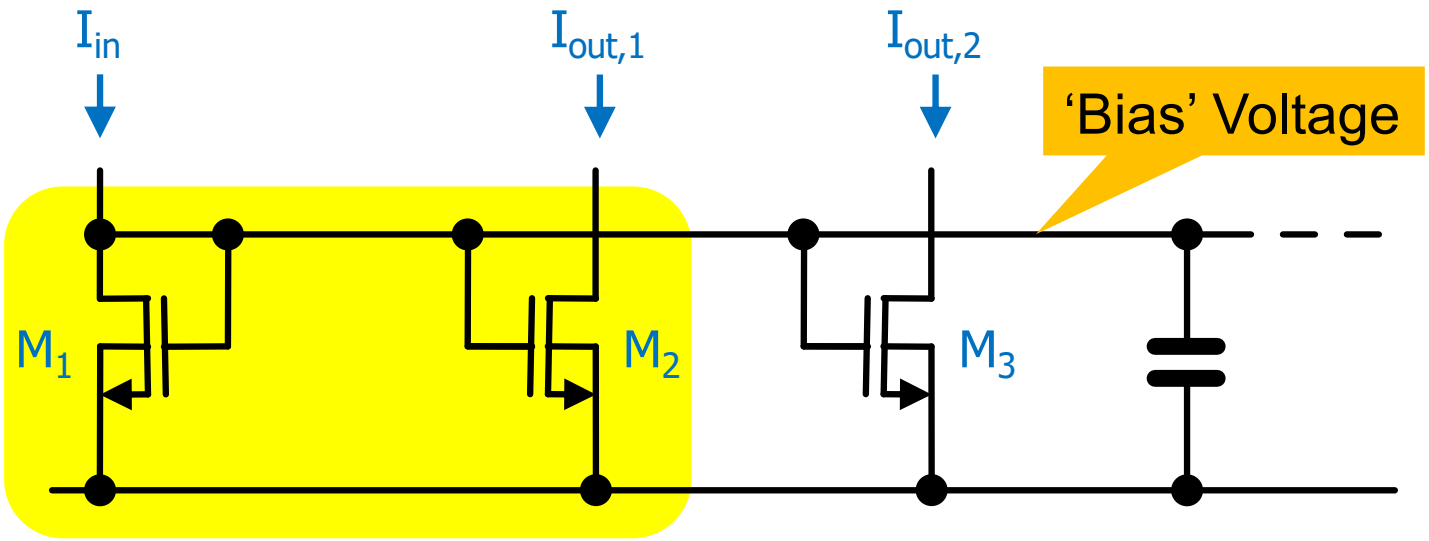


- In more detail, Early Effect must be taken into account
  - $I_{out} = I_{in}$ *exactly* only for $V_D = V_G$ (do you understand why?)

Varying the Output Current

- If $W_2 \neq W_1$ (assuming still $L_1=L_2$), then $I_{out} = W_2/W_1\ I_{in}$
- $L_1 \neq L_2$ should be avoided because Early Effects (i.e. λs) are different

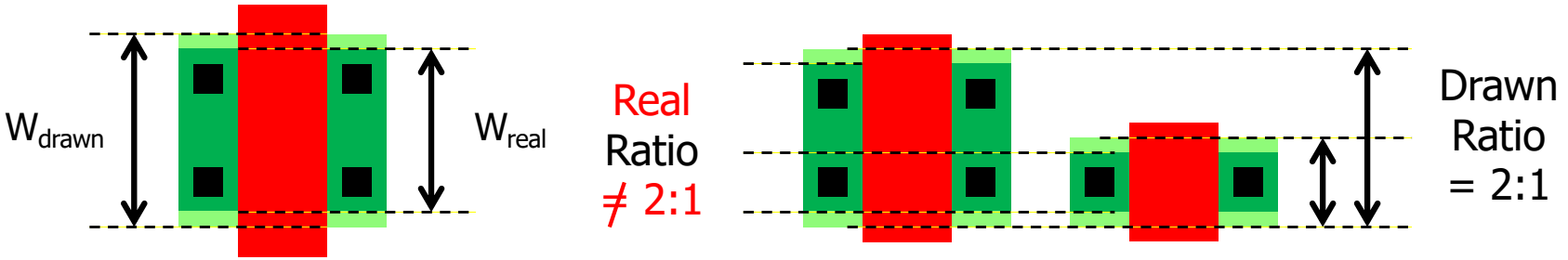
- Additional MOS can be connected to give further outputs



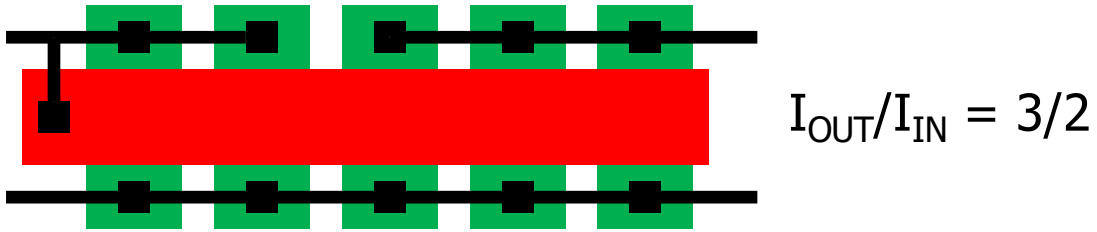
- The gate voltage of the sources is called a *'Bias'* Voltage
  - It should be 'decoupled' with capacitors to *the source potential* to be 'stable' and noise free.

Large W vs. Multiple MOS

- The *ratio* W_2/W_1 is used for current multiplication
- If this is implemented by MOSs with different layouts, *edge effects* can lead to unknown ratios.
  - To be more precise, the real W of a device is often $W_{real} = W_{drawn} - W_{offset}$ (W_{offset} can have both signs)

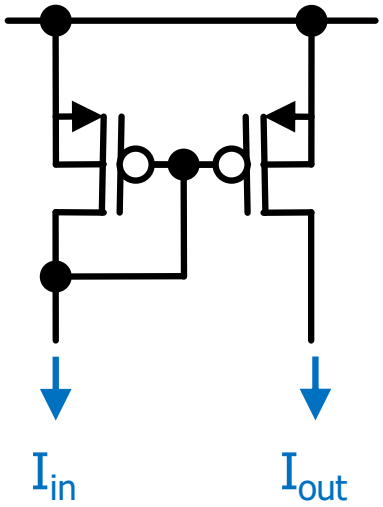


- Real Ratio != Drawn Ratio! ⟶ use *multiple identical* devices!
- For a non-integer ratio A/B, use B MOS on diode side and A MOS on output side. (In practice, add 'dummy' devices for matching)



The PMOS Mirror

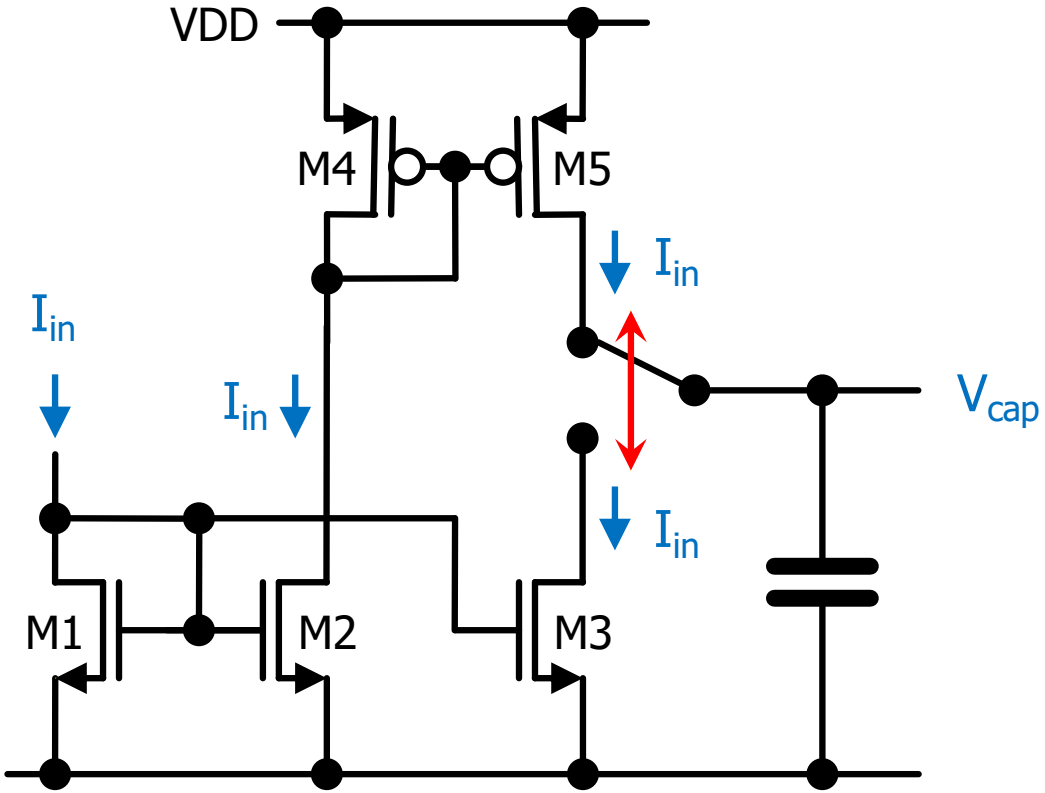
- Here is how a PMOS mirror looks like:



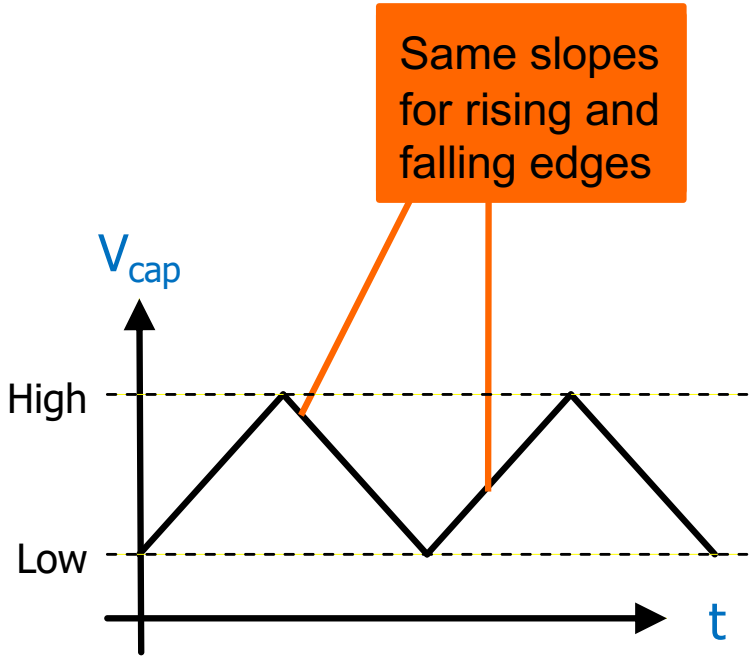
- Same principle and topology.
- Inverted polarities.

A Possible Application: Triangular Waveform

- A capacitor is charged / discharged with same current



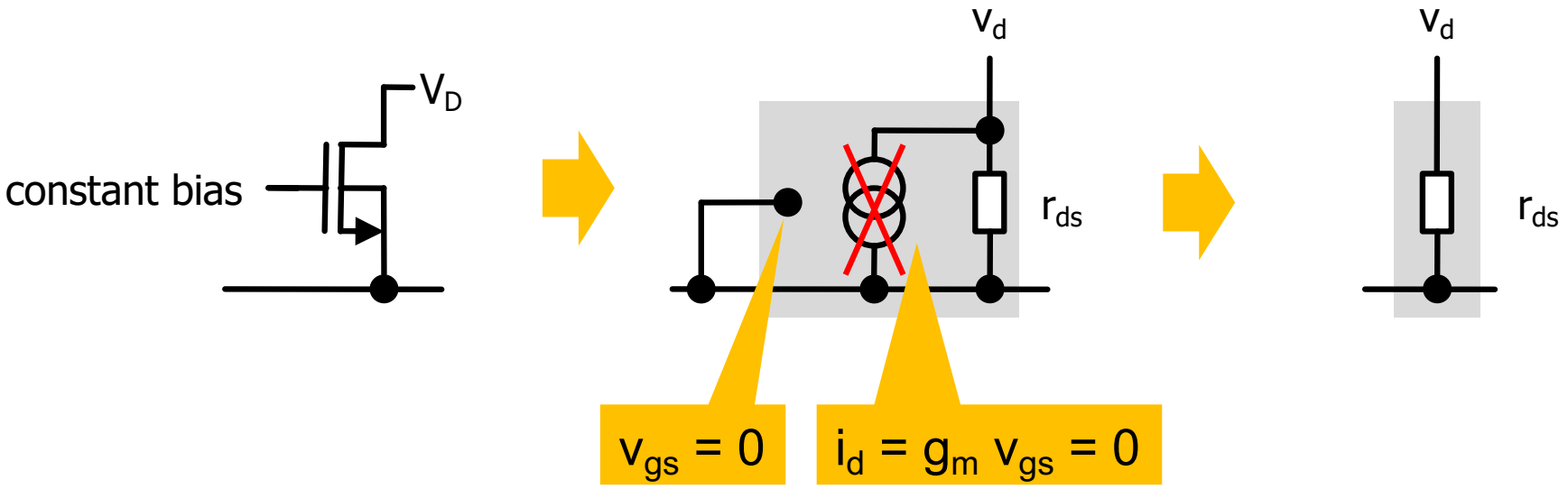
(M1-M3 and M4-M5 are identical, all bulk=source)



- Switches: MOS with large W/L controlled by 0/VDD
- Switching could be done by comparing V_{cap} to a high- and low- level…

Output Resistance

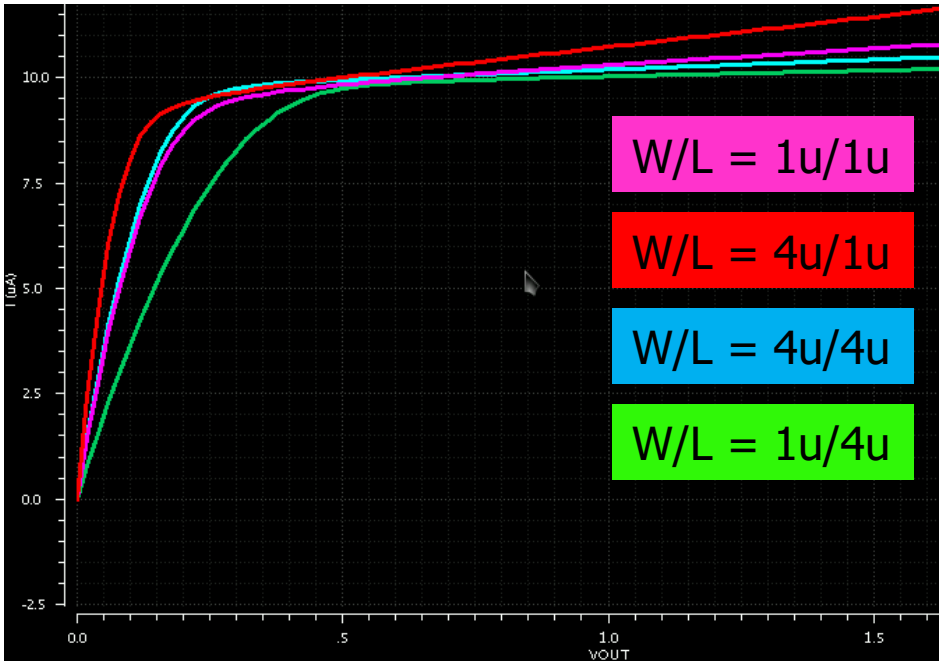
- The Output Resistance r_{out} of the Mirror is just that of the (output) MOS
- This is obvious from the small signal model
  - The Gate voltage is *constant*, so there is *no small signal*: $v_{gs} = 0$

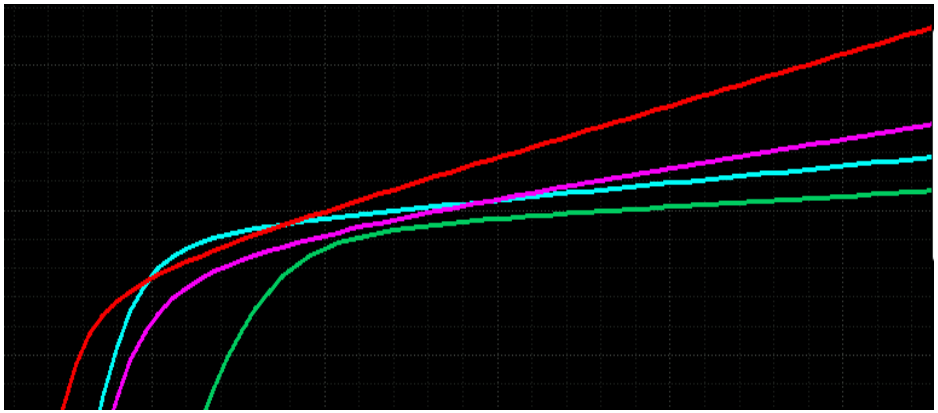


- r_{ds} depends on the current and on the geometry (W,L)

Good and Bad Mirrors

- Normally, the output MOS of the mirror is used as a *current source*. We therefore want
  - high output resistance r_{ds} → we need small I_D, large L
  - low saturation voltage → we need small I_D, small L, large W





- Therefore: Good mirrors must have large L and W
  - large L to increase output resistance
  - large W to lower saturation voltage

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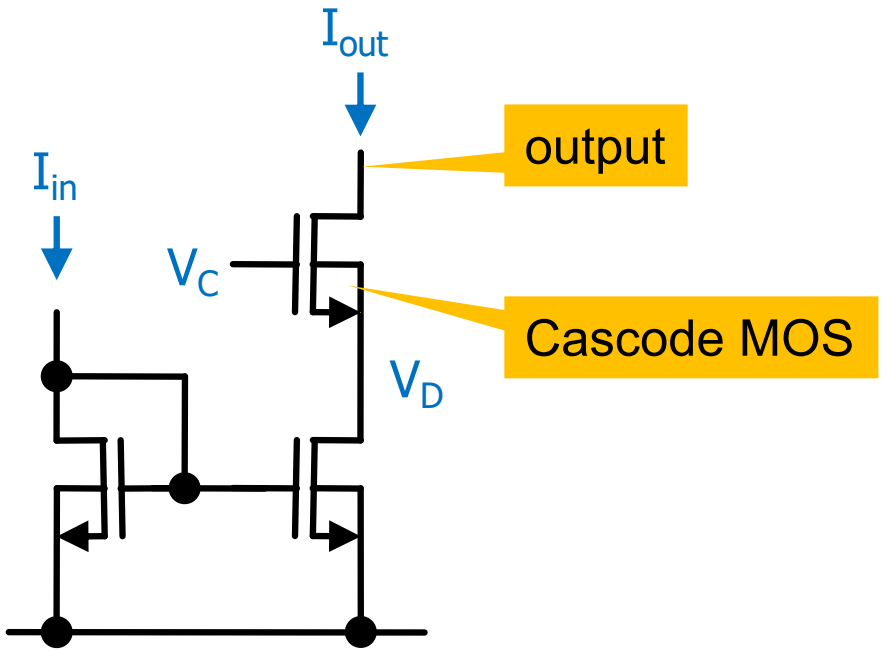
THE CASCODE

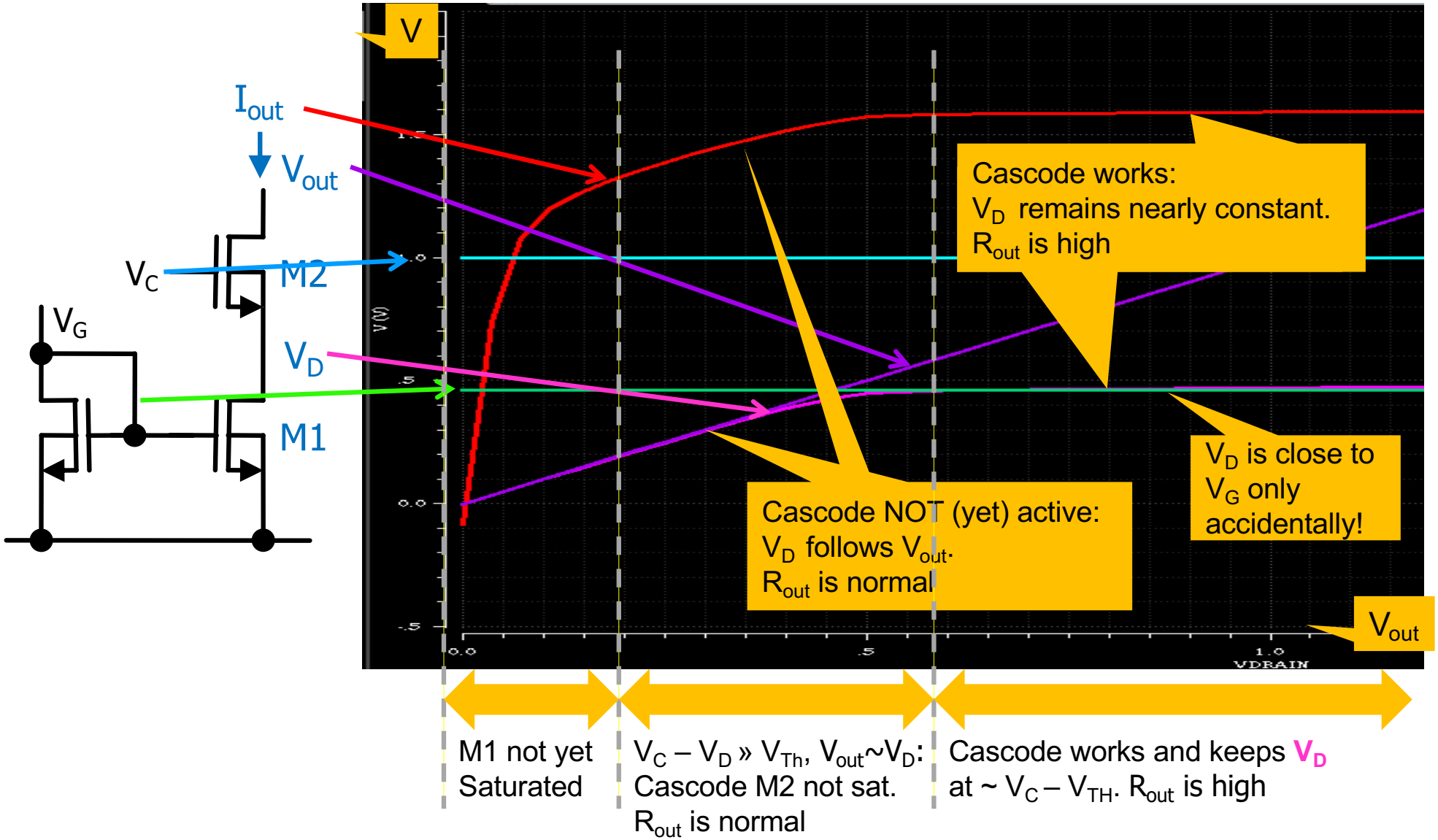
Improving the Mirror: The Cascode

- The output current in a normal mirror changes, because output voltage = drain voltage
- By inserting another MOS *between* output and drain, the drain voltage is kept (more) constant
  - the output current changes (less)
  - the output resistance is higher 😀
- The upper MOS is called a **CASCODE** (transistor)

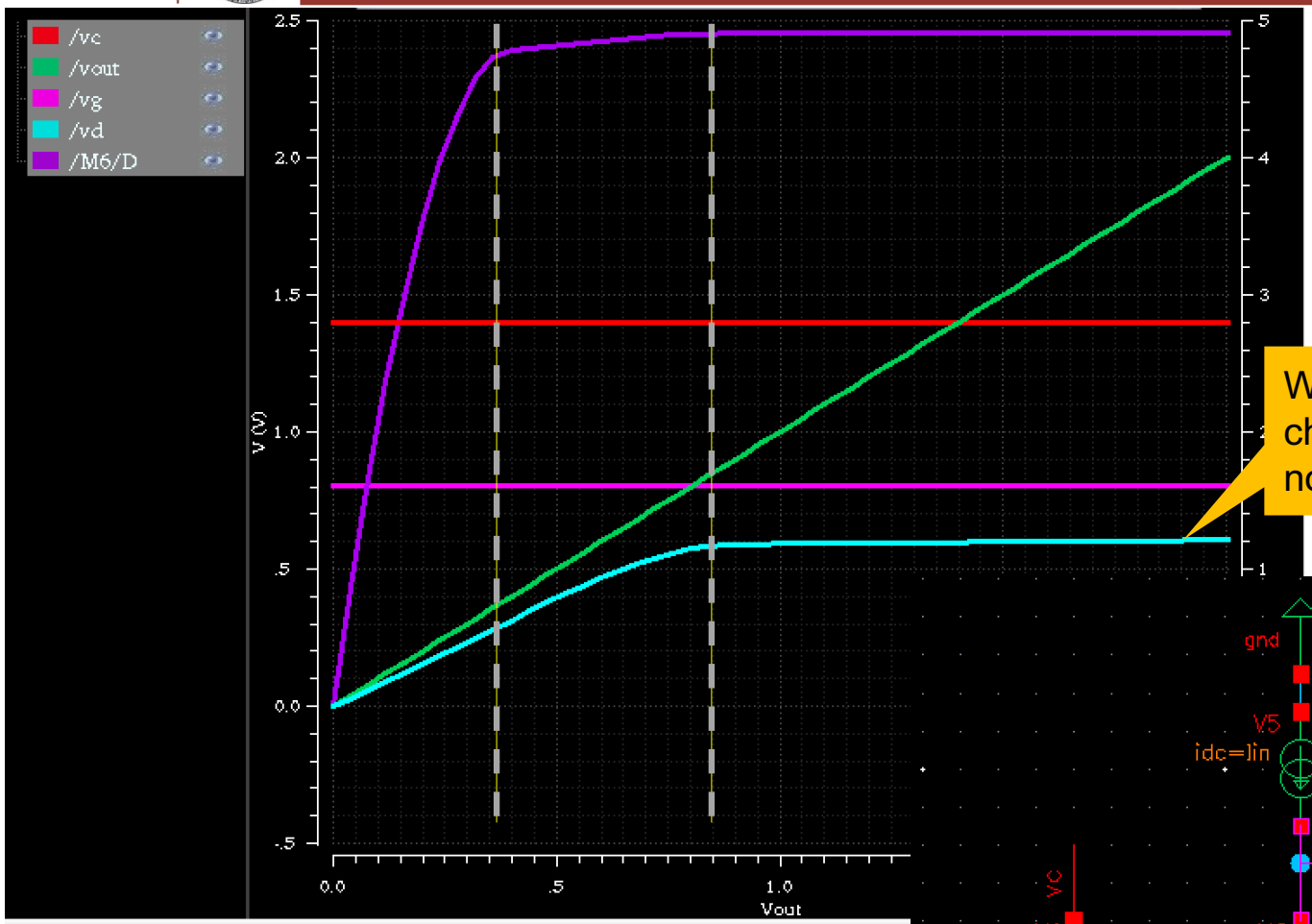


The Cascoded Current Source in Action

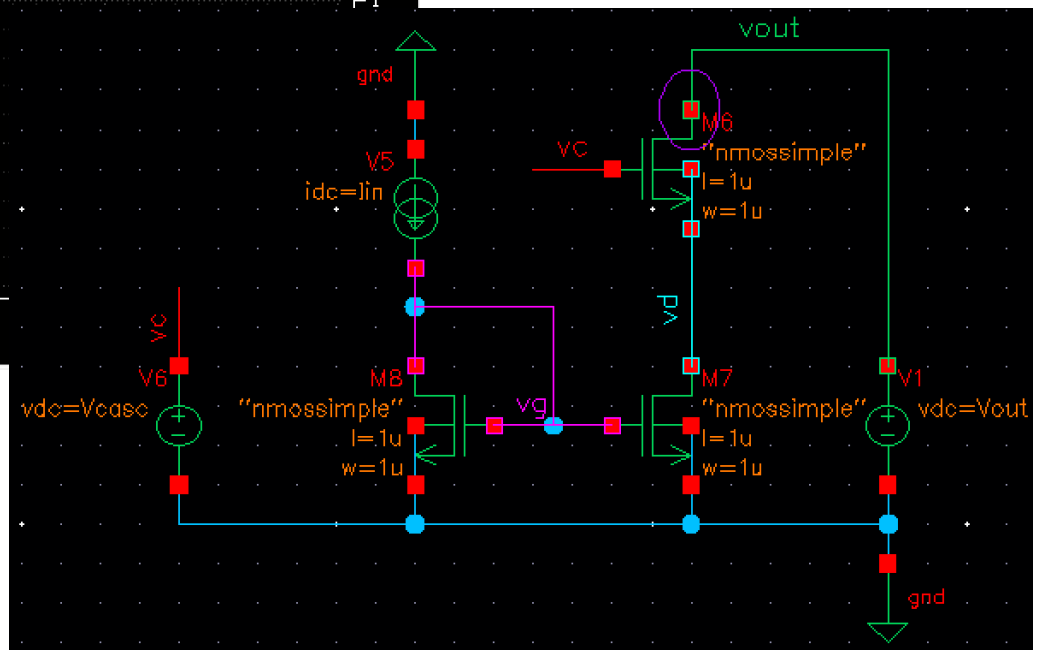
- Simulation for V_C = 1V (not optimal, see later...)



Using model ‘nmossimple’ :



With the settings chosen here, V_D is not approaching V_G

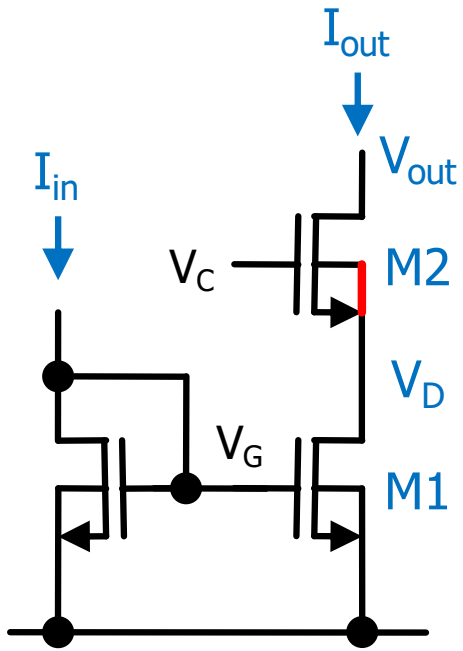


Crucial: Correctly Biasing the Cascode

- The *gate* voltage of the cascode MOS M2, V_C, defines the *drain* voltage V_D of the 'current setting' MOS M1
  - V_D is *roughly one threshold* voltage below V_C
  - More precisely, $V_D = V_C - V_T - \mathrm{Sqrt}(I_D\ 2/K\ L/W)$
  - (This holds when Bulk and Source are connected (-), otherwise, the Substrate Effect lowers V_D even more)

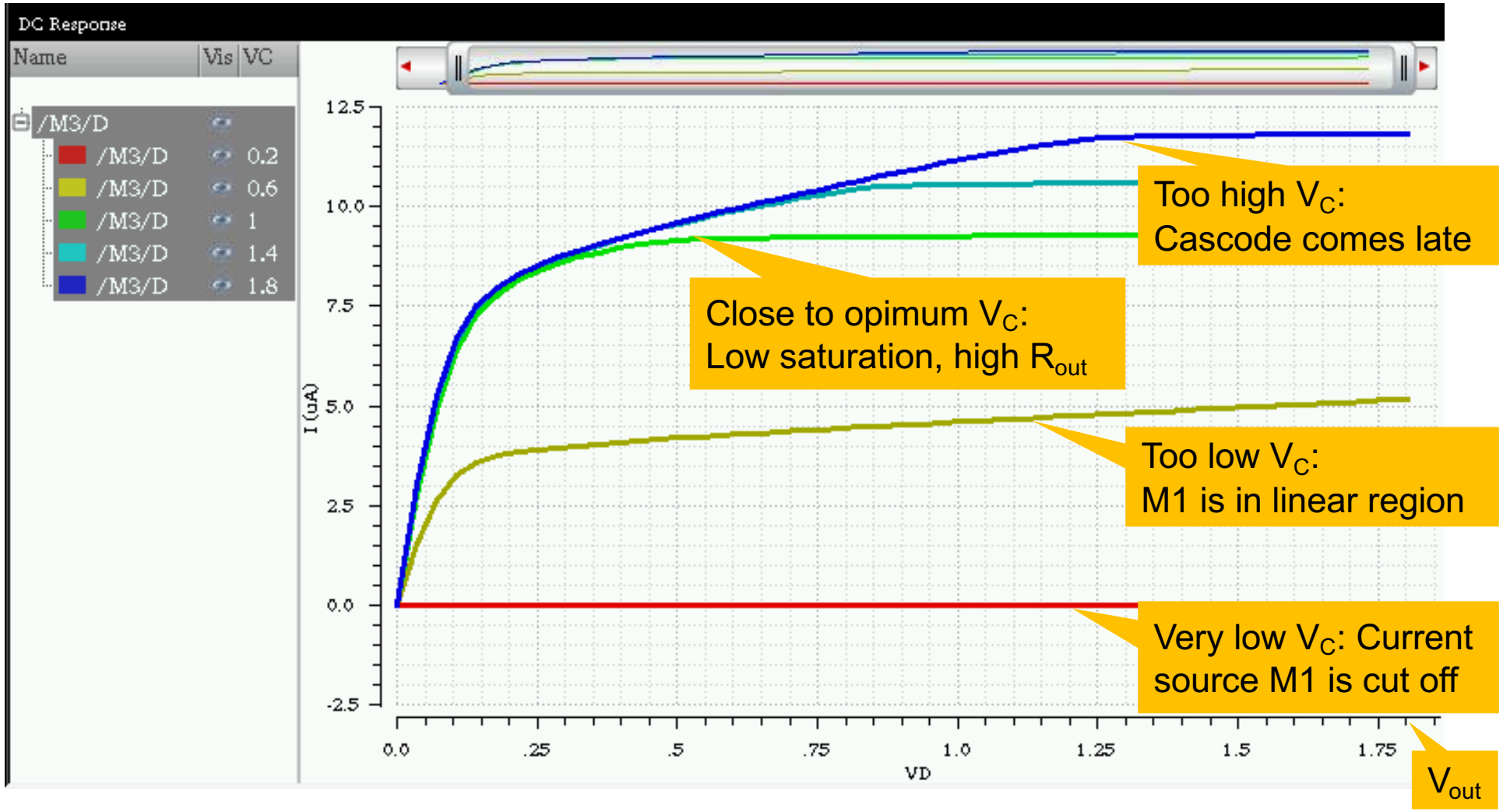
- V_D (and thus V_C) should be chosen
  - *High enough* to keep M1 'just' saturated
  - *As low* as possible so that V_{out} can be low

- The ‚total' saturation voltage at the output for optimal choice is ~ *twice* that of M1 (if M1 and M2 have same sizes)



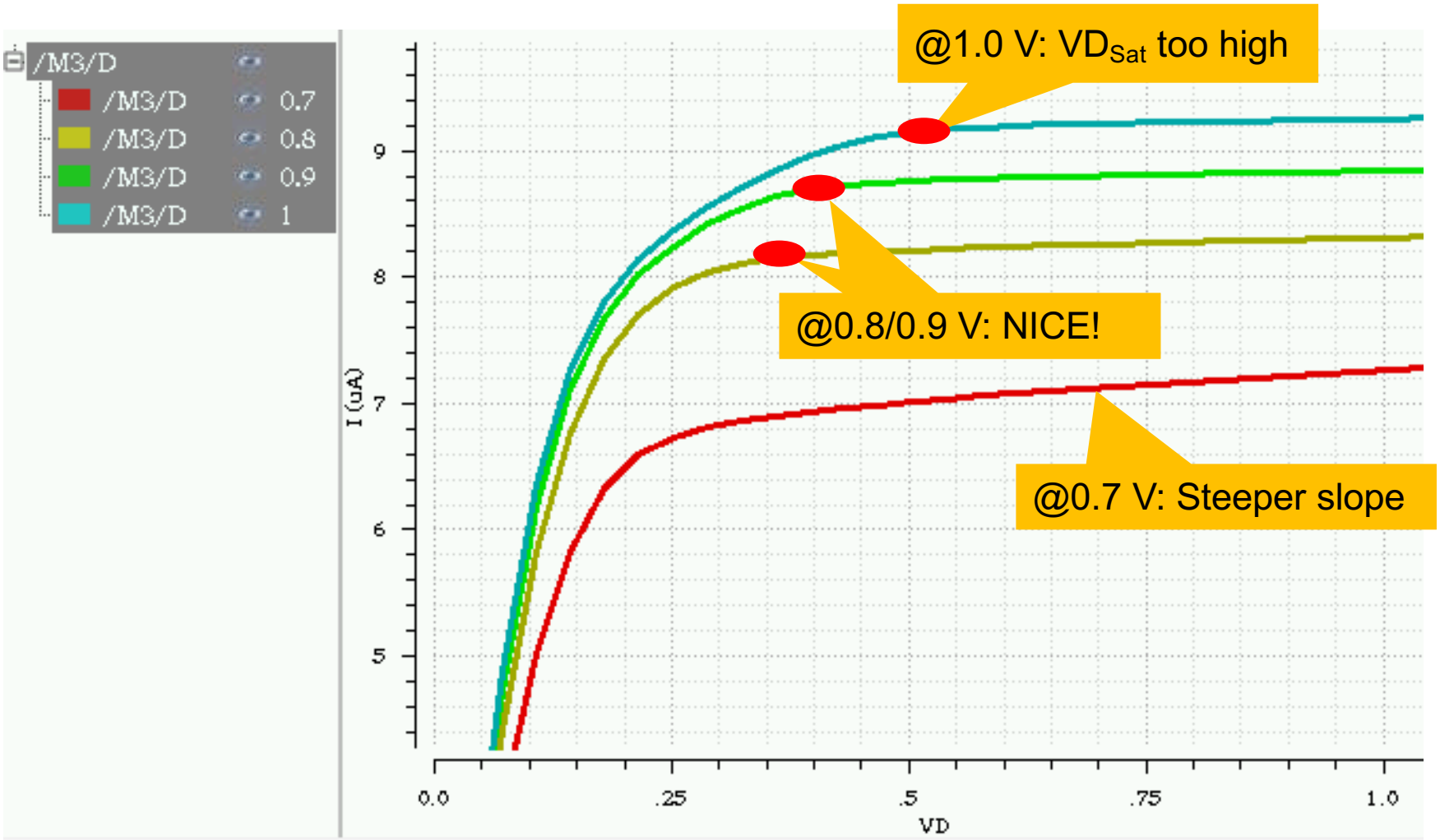
Simulation: Varying V_C

- Sweep V_C from 0.2...1.8 V:



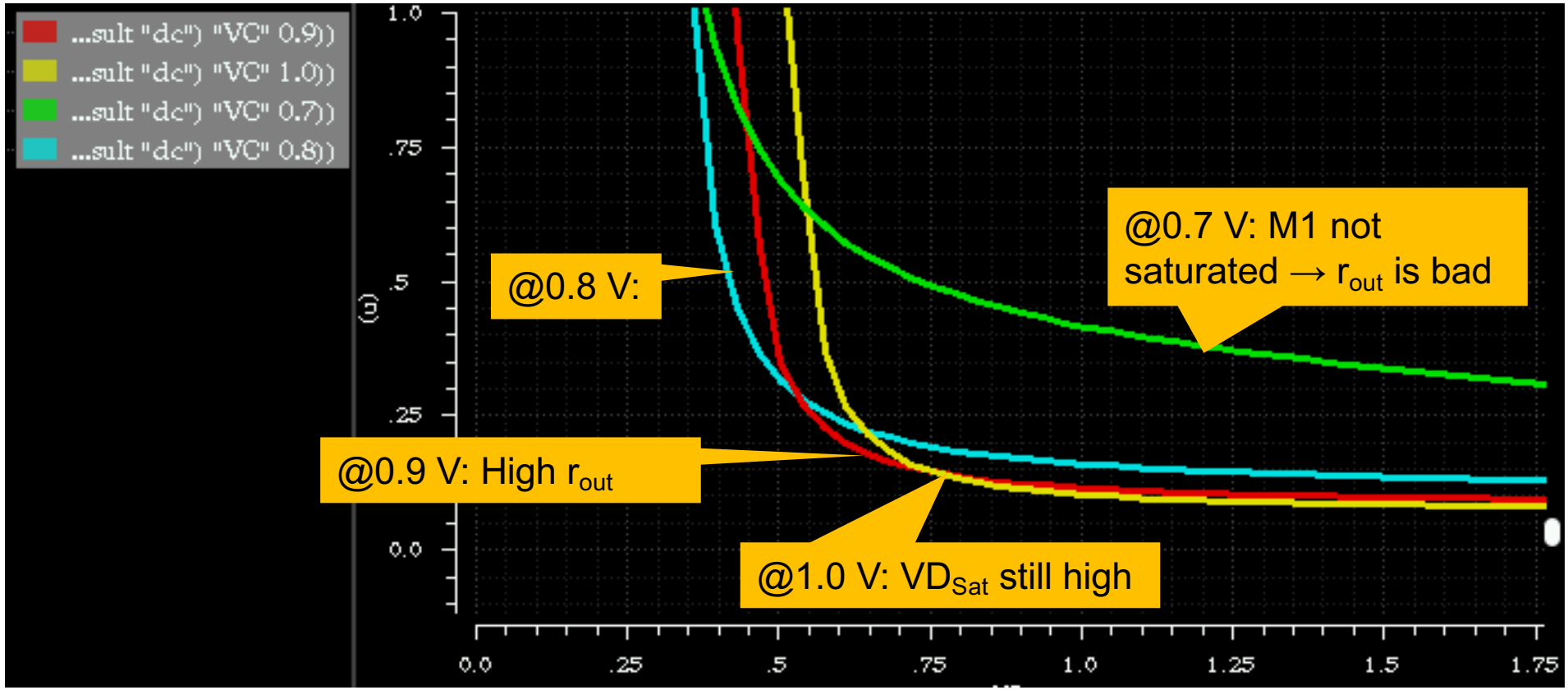
Zoom of 'Optimum' V_C:

- Sweep 0.7...1.0 V



R_{out} and *dynamic range* in more detail

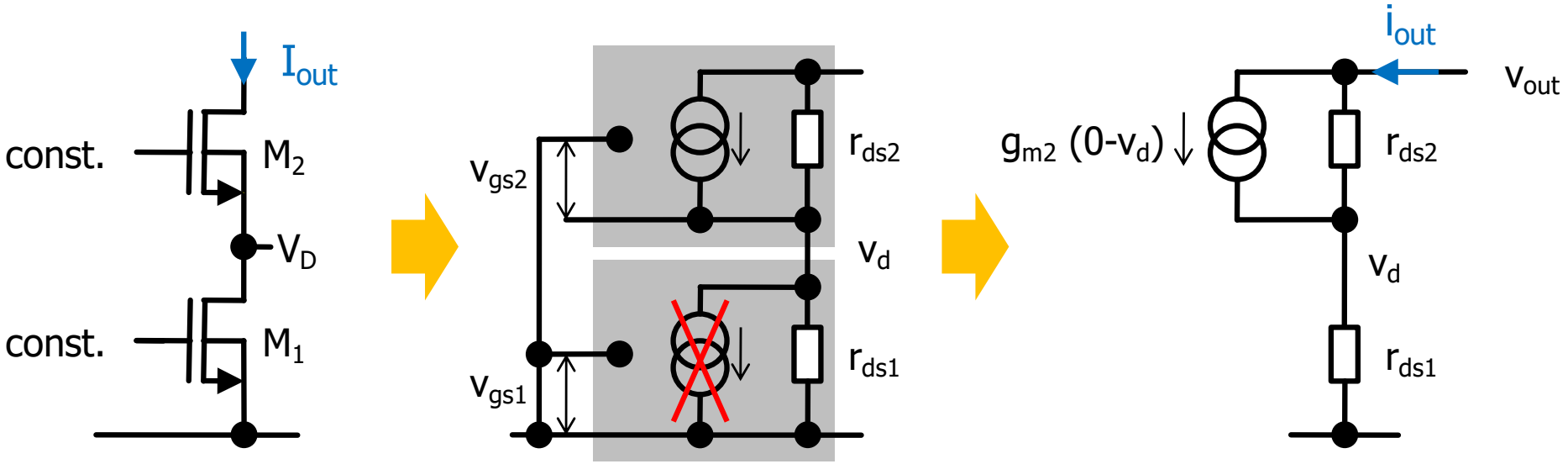
- Look at derivative of output characteristic ($\partial I_{out}/\partial V_{out} = 1/r_{out}$)
  - Small is good
- Again, blue (0.8 V) or red (0.9 V) are best...



- Note: Do not believe simulations to better than 50-100 mV!
  - 0.8 V is too close to 'bad' curve for 0.7 V. → Chose 0.9 V

Output Resistance of Cascoded MOS

- Small signal analysis
  - We only need to consider the output part
  - Fixed voltages are equivalent to ground (in small signal!)
  - The current source in M1 delivers no current (V_{GS} = fix)



- Current sums:
  - $i_{out} = (v_{out} - v_d)/r_{ds2} - g_{m2}\, v_d = v_d / r_{ds1} \rightarrow v_d = \ldots \rightarrow r_{out} = v_{out}/i_{out}$

$\rightarrow$ $r_{out} = r_{ds1} + r_{ds2} + g_{m2}\, r_{ds1}\, r_{ds2}$ $\rightarrow$ $r_{out} \cong r_{ds1} \times (g_{m2}\, r_{ds2})$

(The Calculation)

$$\frac{v_{out} - v_d}{r_{ds2}} - g_{m2} v_d = \frac{v_d}{r_{ds1}}$$

= i_{out}

$$\frac{v_{out}}{r_{ds2}} = \frac{v_d}{r_{ds1}} + \frac{v_d}{r_{ds2}} + g_{m2} v_d$$

$$\frac{1}{v_d} = \frac{r_{ds2}}{v_{out}} \left(\frac{1}{r_{ds1}} + \frac{1}{r_{ds2}} + g_{m2} \right)$$

$$r_{out} = \frac{v_{out}}{i_{out}} = \frac{v_{out} r_{ds1}}{v_d}$$

$i_{out} = v_d / r_{ds1}$

$$= v_{out} r_{ds1} \frac{r_{ds2}}{v_{out}} \left(\frac{1}{r_{ds1}} + \frac{1}{r_{ds2}} + g_{m2} \right)$$

$$= r_{ds2} + r_{ds1} + g_{m2} r_{ds1} r_{ds2}$$

Effect of the Cascode

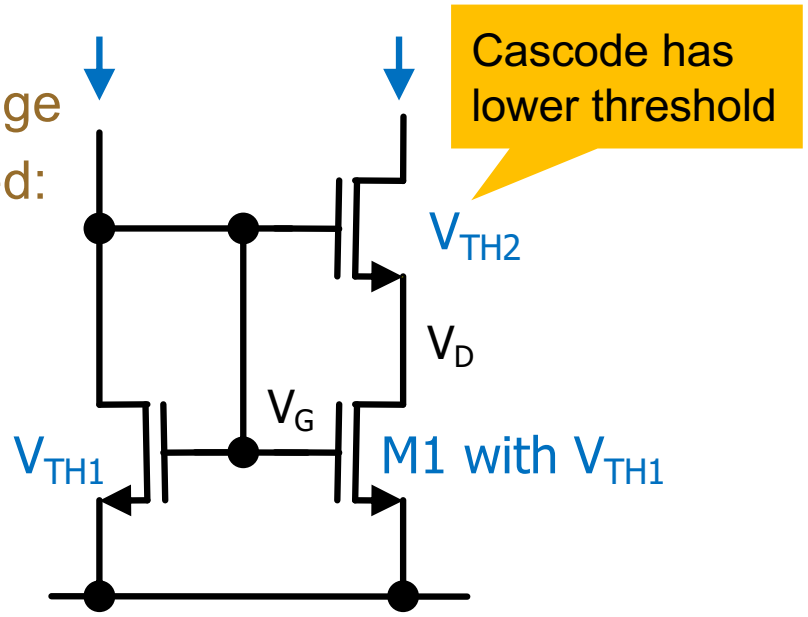
- The output resistance of a cascoded MOS is a factor of $g_m r_{ds}$ higher than without cascode 😀
- $g_m r_{ds}$ is the 'gain' of the Cascode MOS (as we will see…)
- It is typically 30

- The cascode gives a large improvement (in output resistance) for a very 'cheap' cost:
  - One more MOS
  - Loss of *one* saturation voltage (ideally)
  - NO additional power consumption!
- Achieving the same (high) output resistance with a long MOS is very difficult (more space than a second MOS, higher saturation voltage)

- → Cascodes are found in *many* places!

A useful cascode trick

- Generating the 'good' cascode voltage is not so easy…
  - See exercises
- In some technologies, transistors with ***different thresholds*** are available.
- This allows the following circuit:
  - We use the gate voltage V_G of the mirror *also* as cascode voltage
  - For M1 being saturated, we need: $V_D > V_G - V_{TH1}$
  - But $V_D = V_G - V_{TH2} - x$ where x depends on current
  - The saturation requirement becomes $V_G - V_{TH2} - x > V_G - V_{TH1}$ or $V_{TH2} < V_{TH1} - x$



- With a 'sufficiently low' V_{TH2}, this works!

Summary: The Cascoded Current Source

- A cascode MOS stabilizes the drain voltage of the current source
- The output resistance increases by a *factor* $g_{m2}\, r_{ds2}$
  - This is the 'intrinsic gain' of M2
  - It is typically >20 (depending on geometry and current)
- The cascode bias voltage should be chosen such that the current source is *just above* the *edge* of saturation
- The overall saturation voltage of the cascoded source is ~ 2 times the 'unit' saturation voltage
- For advanced circuits, see the exercises!

Design Goals for Current Sources

- High output resistance
  - Achieved by large L, cascode, regulation (see exercise)
- Low saturation voltage
  - Achieved by large W, optimal biassing
- Matching
  - Same Drain voltages (and of course same geometries)
- Speed (sometimes)
  - small devices (for small capacitances)
  - high current -> large W/L

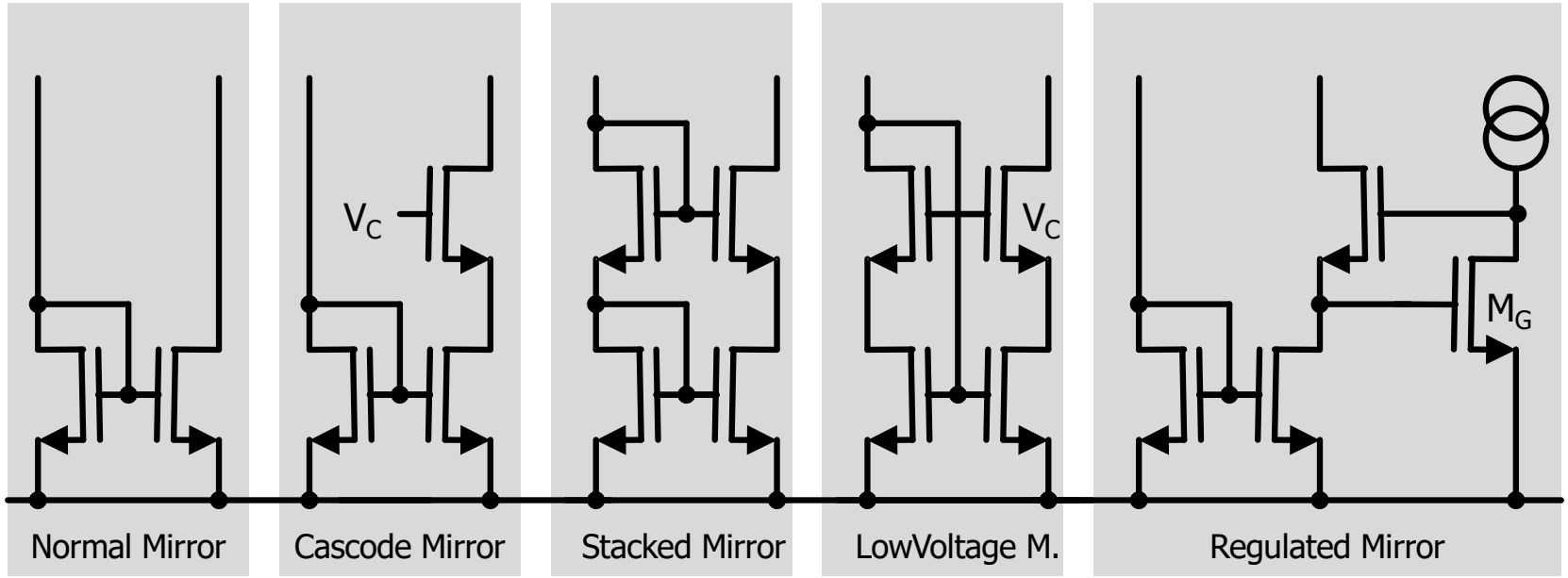
Ibias ?

- But how do we get the input current?
- There are tricky circuits (Bandgap Reference) which can produce voltages / currents which are rather independent of supply voltage, temperature and component parameters!
- See Lecture ‘Advanced Analogue Building Blocks’

Advanced Current Source Circuits

- See Exercises

Common Current Mirror Topologies



	Normal Mirror	Cascode Mirror	Stacked Mirror	LowVoltage M.	Regulated Mirror
r_{out}	r_{ds}	$R_{ds} \times g$	$R_{ds} \times g$	$R_{ds} \times g$	$R_{ds} \times g^2$
Best V_{min}	$V_{D,Sat}$	$2 \times V_{D,Sat}$	$V_T + 2 \times V_{D,Sat}$	$2 \times V_{D,Sat}$	$V_T + 2 \times V_{D,Sat}$
Matching	No	No	Yes	Yes	Yes if $I_{bias} = I_{in}$
Require V_C	No	Yes	No	Yes	No
Comment				Fails if V_C too high	May use Low V_T MOS for M_G for lower V_{out}