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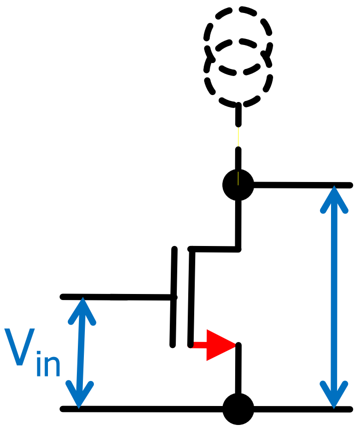
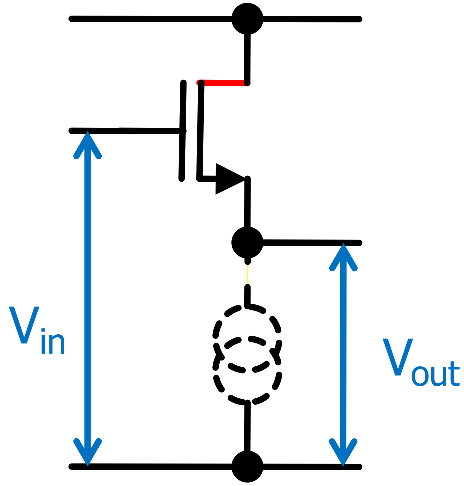
The Gain Stage (Common Source Amplifier)

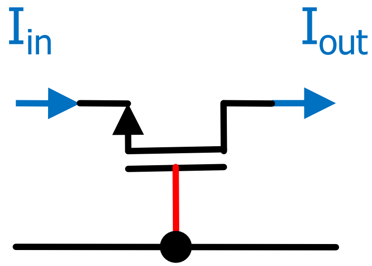
Finally: a voltage amplifier

The Three Basic Configurations:

- ‘Common xxx configuration’ means:
  Terminal xxx of the MOS is common to input and output







- common *source* config.
- ‘gain stage’
- inverting voltage gain
- *high* input impedance
- *high* output impedance

- common *drain* config.
- ‘source follower’
- voltage gain <~ 1
- *high* input impedance
- *low* output impedance

- common *gate* config.
- ‘cascode’
- current gain = 1
- *low* input impedance
- *high* output impedance

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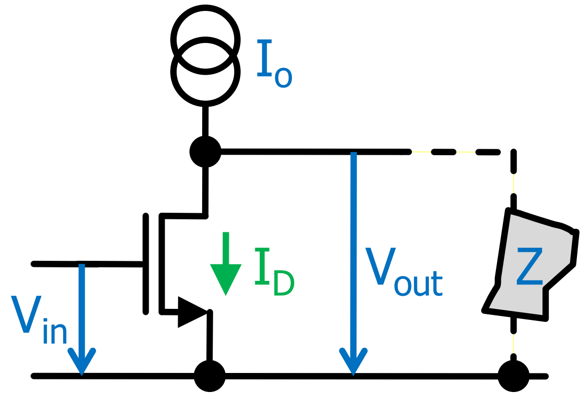
DC BEHAVIOR OF THE GAIN STAGE

The Principle

- The current in the MOS is set mainly by the (large signal) $V_{GS} = V_{in}$, but also by $V_D = V_{OUT}$
- We sent a constant current I_0 to the drain from a (for now) *ideal* current source
- In the operation point, V_{GS} and I_0 must 'correspond'!



- When V_{in} raises (above the op. point)
  - I_D increases. It becomes > I_0
  - Current is pulled out of the load
  - V_{out} drops
- When V_{in} drops
  - I_D decreases. It becomes < I_0
  - Current is pushed into the load
  - V_{out} increases

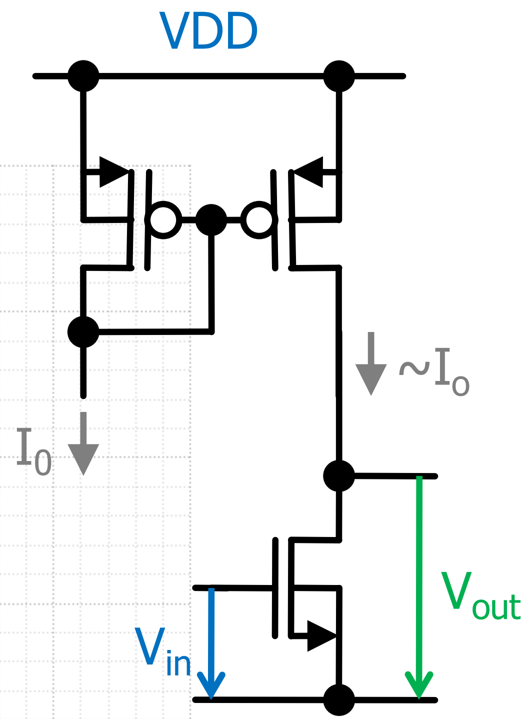
Inverting amplifier

Large Signal Behavior

- Use real current source now (PMOS mirror)
- Observe the 4 main operation regimes:

V_{in} is below NMOS threshold. No current in NMOS. PMOS can pull the output all the way to the positive supply 'VDD'

The NMOS starts to draw current. The PMOS is in the linear region, its output resistance is low, gain is low.



Both MOS are in saturation.

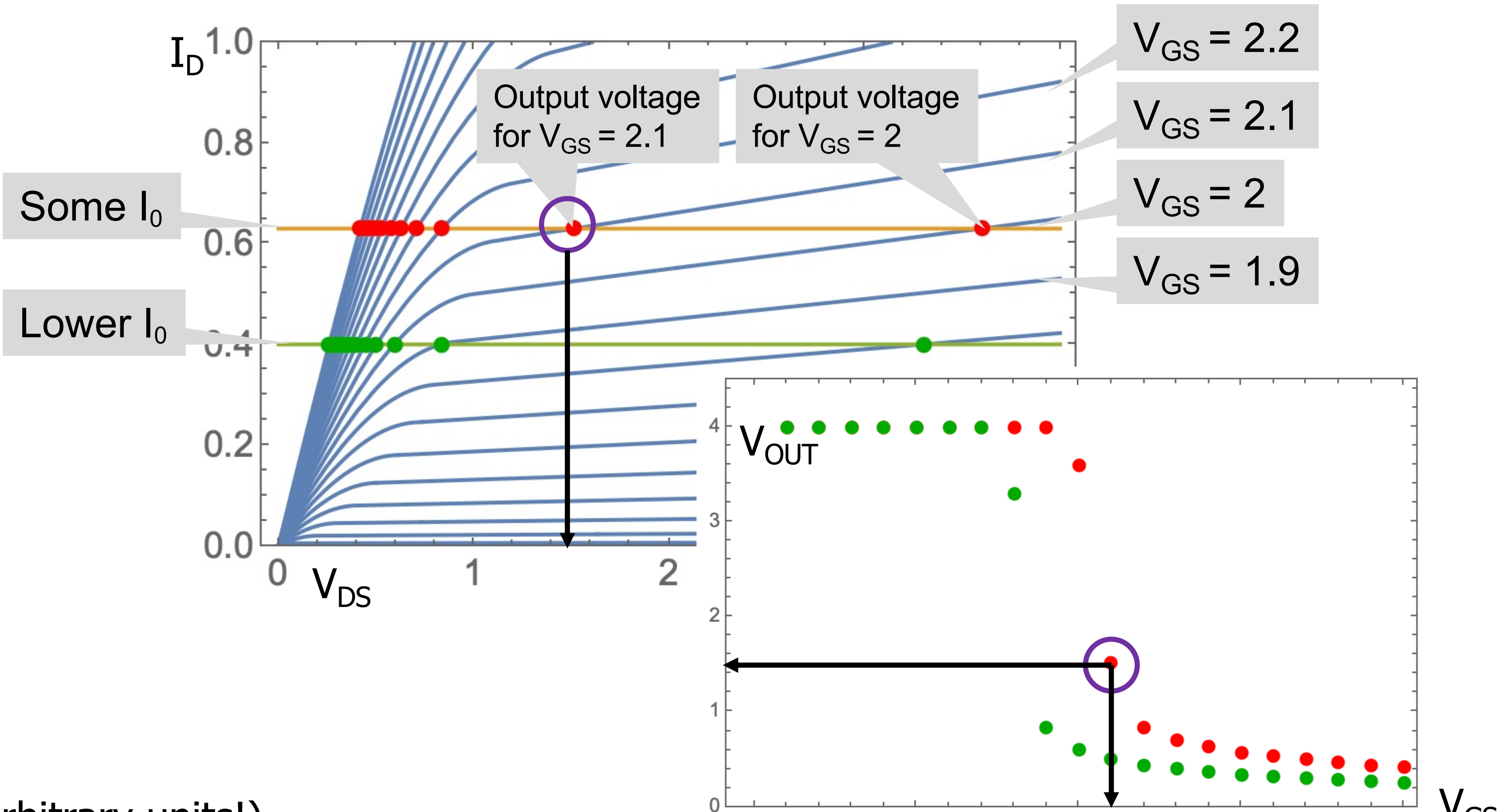
Gain is high.

We want to operate somewhere on this steep slope!

The drain voltage of the NMOS becomes too small. It goes into the linear region. Gain drops. Note that V_{out} = 0 is *never* reached

Understanding the Curve

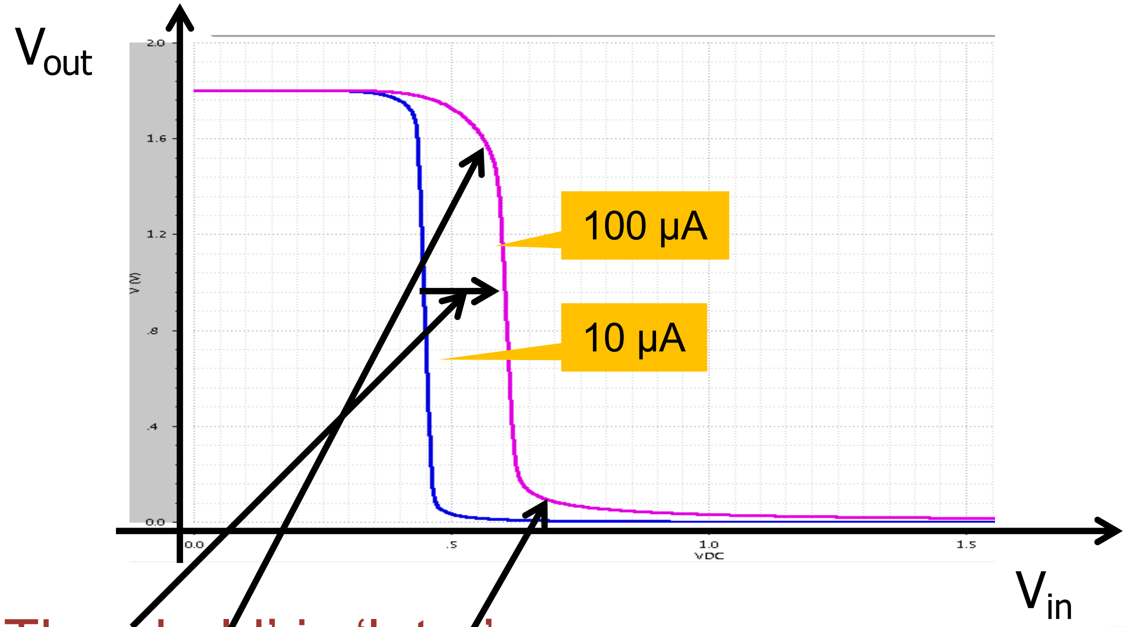
- The (blue) output characteristic 'increases' with V_{GS}
- The output voltage settles where $I_D = I_0$



(arbitrary units!)

Changing the Bias Current

- For more bias current ('stronger current source'):

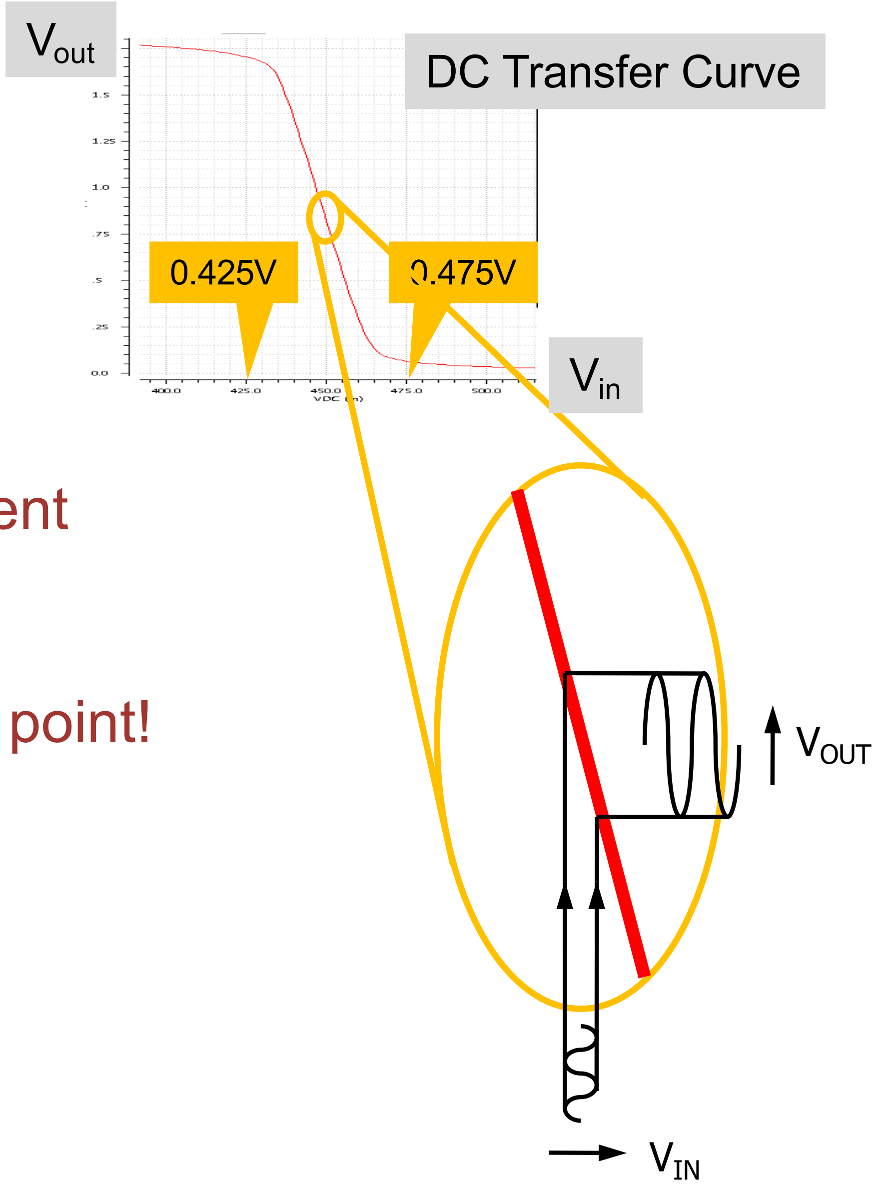


- 'Threshold' is 'later'
  - V_{IN} must be higher until I_D reaches 100µA
- 'Round region' is wider
  - The **P**MOS is longer in linear region because its V_{GS} is higher
- Output does not go so low (towards GND)
  - NMOS cannot deliver enough (relative to 100µA) current, it comes into the linear region

Therefore, the DC operation point of V_{in} must be adjusted!

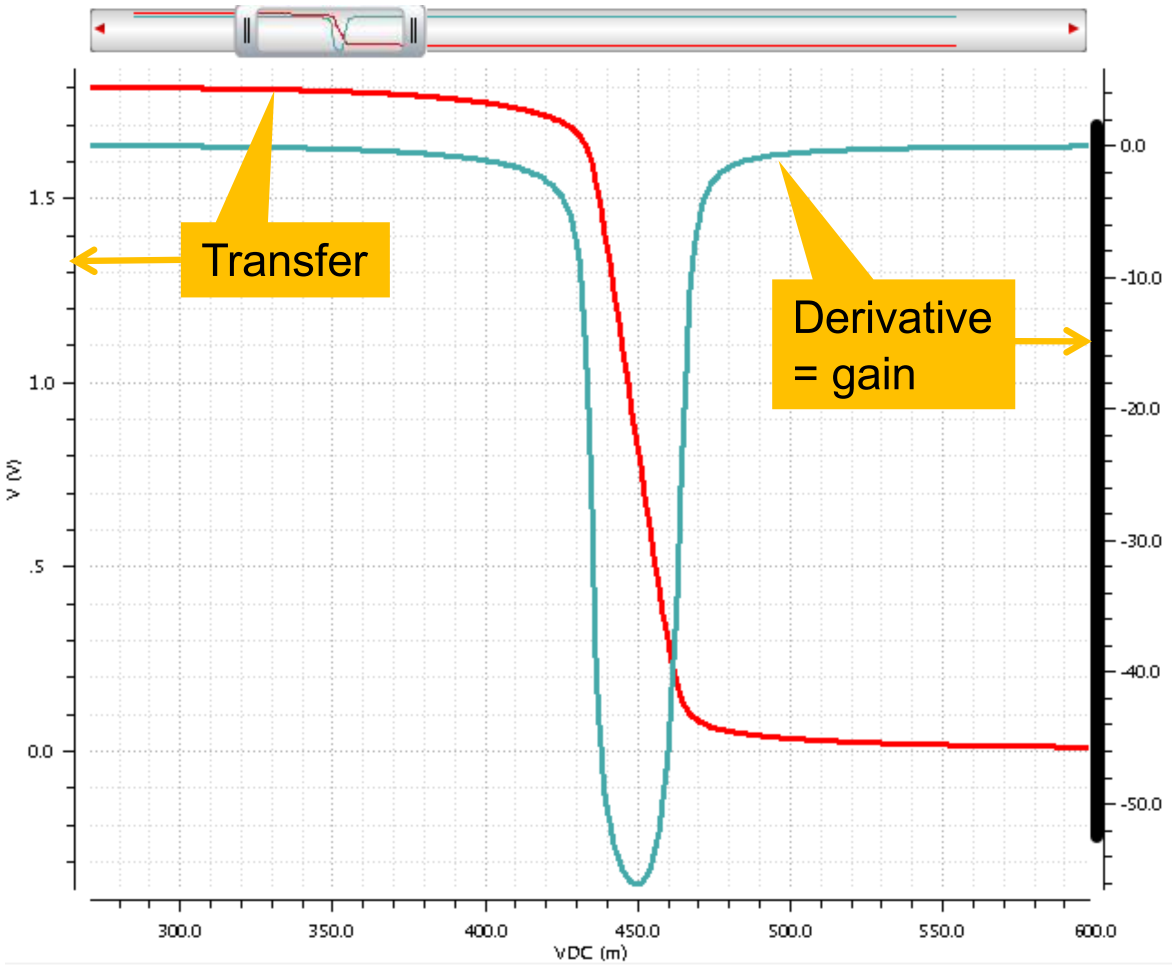
The gain

- A small change in V_{in} leads to a large change in V_{out} if the transfer curve is steep.
- The gain is the derivative of $V_{out}(V_{in})$
- NOTE that the gain is different along the curve, i.e. for different V_{in}!! It depends on the operation point!



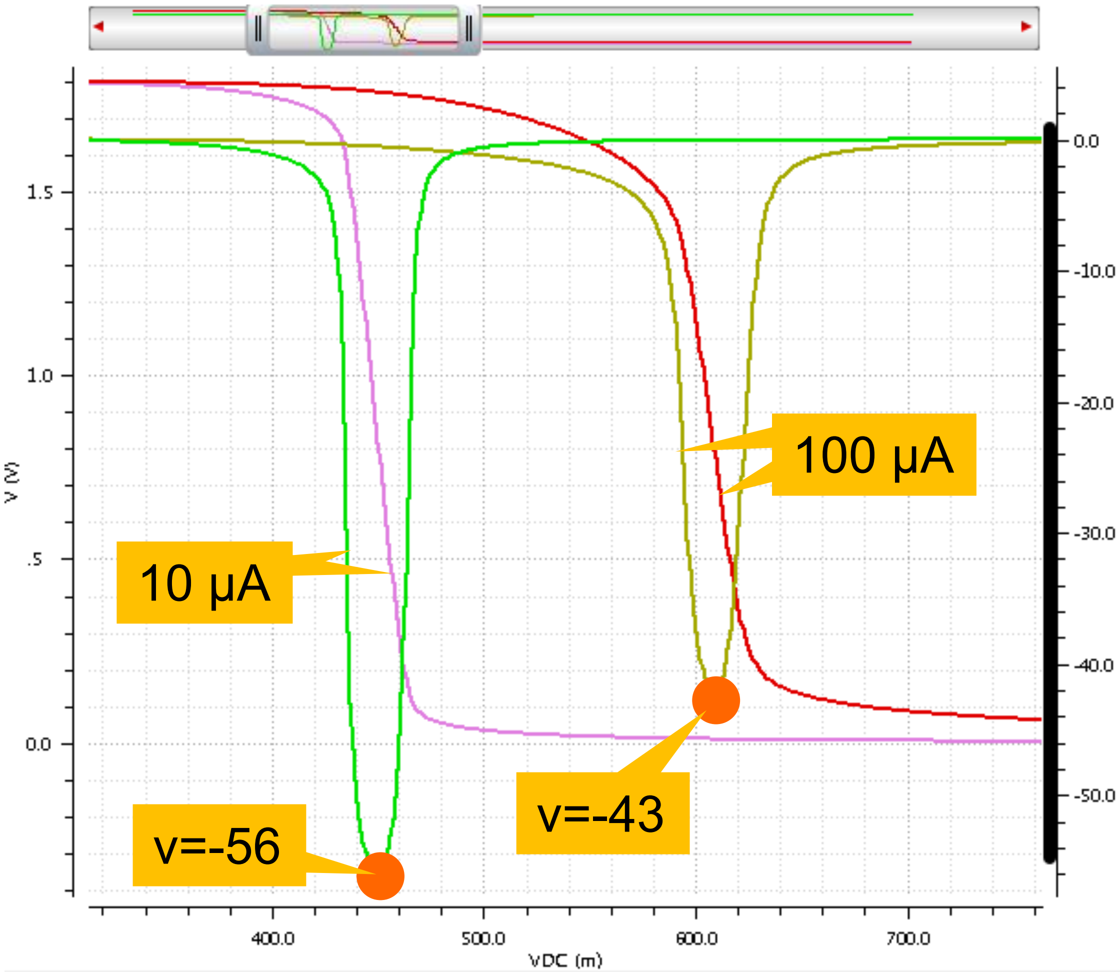
Gain vs. V_{IN}

- Can be obtained by taking derivative of transfer curve



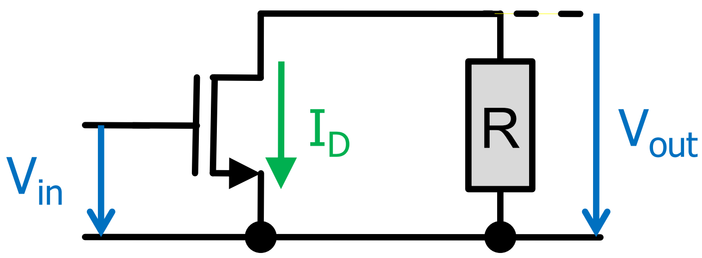
Gain at Different bias Currents

- Position of ‘maximal gain’ *depends on bias current*
- Max. gain is lower for high current (we will understand why!)



Gain of the Gain Stage: Intuitive Way

- When V_{in} changes by a small amount $\Delta V_{in} = v_{in}$, how much does V_{out} change, i.e. what is v_{out}?
  - Note difference in Capital and Small letters: $V_{in} \neq v_{in}$
  - Capitals: Large signal, small: small signal



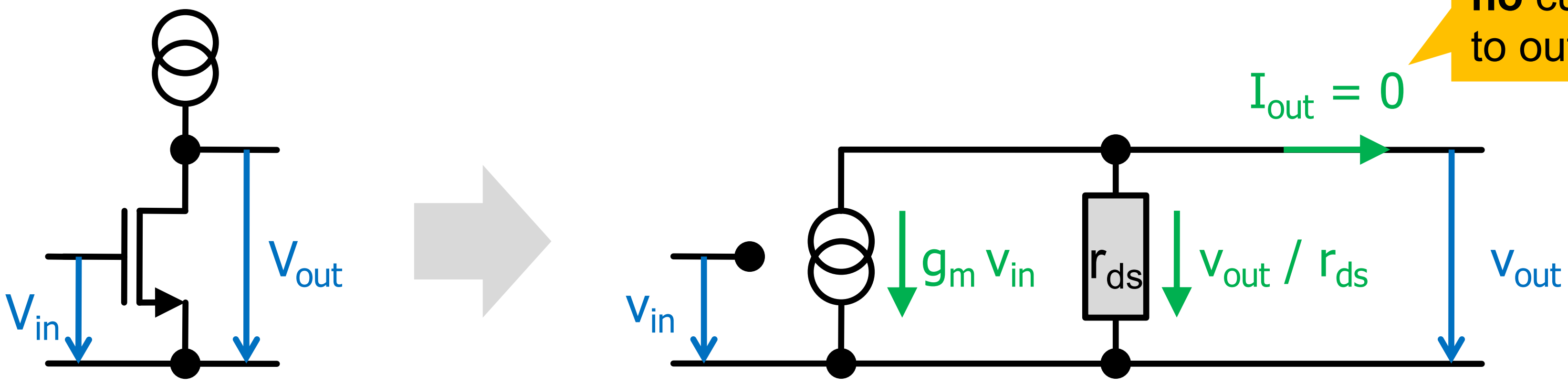
- What happens?
  - v_{in} leads to a change i_D of I_D of $\mathbf{i_D = g_m\, v_{in}}$ (Definition of g_m!)
  - With a resistive load R, this gives a voltage change $\mathbf{v_{out} = R \times i_D}$
  - This change is opposite in direction to v_{in}
  - Therefore: $v_{out} = - R \times g_m \times v_{in}$

gain $v = v_{out}/v_{in} = - R \times g_m$

Gain of the Gain Stage: Small Signal Calculation

- Consider only the MOS (i.e. use ideal current source for bias)
- Replace MOS by its small signal equivalent:

We assume that **no** current flows to output!



- Calculation
  - current at output node = 0 (Kirchhoff)
  - therefore: $0 = g_m \times v_{in} + v_{out} / r_{ds}$
  - so that $v = v_{out}/v_{in} = - g_m \times r_{ds}$ as before!

Numbers

- Typical gains are 10 ... 40
  - they depend on technology, current, transistor size,...
- Therefore: $|v| = g_m \, r_{ds} = g_m / g_{ds} > 10 >> 1$

  or $g_m > 10 / r_{ds} = 10 \, g_{ds}$

The transconductance g_m of a MOS is usually much larger than the output conductance g_{ds}.

- This can often be used to simplify small signal expressions!

Comparing to ‘abstracted circuits’

- The difference to the ‘abstract circuits’ exercise is that the ‘current source’ in the NMOS
  1. does not provide ‘negative’ current when V_{IN} is negative
     -> output cannot rise above VDD
  2. does not provide current any more when V_{OUT} is small (MOS gets out of saturation)
     -> output cannot fall below GND

- The analogy is in the steep, central part

- There is an offset created by the threshold voltage

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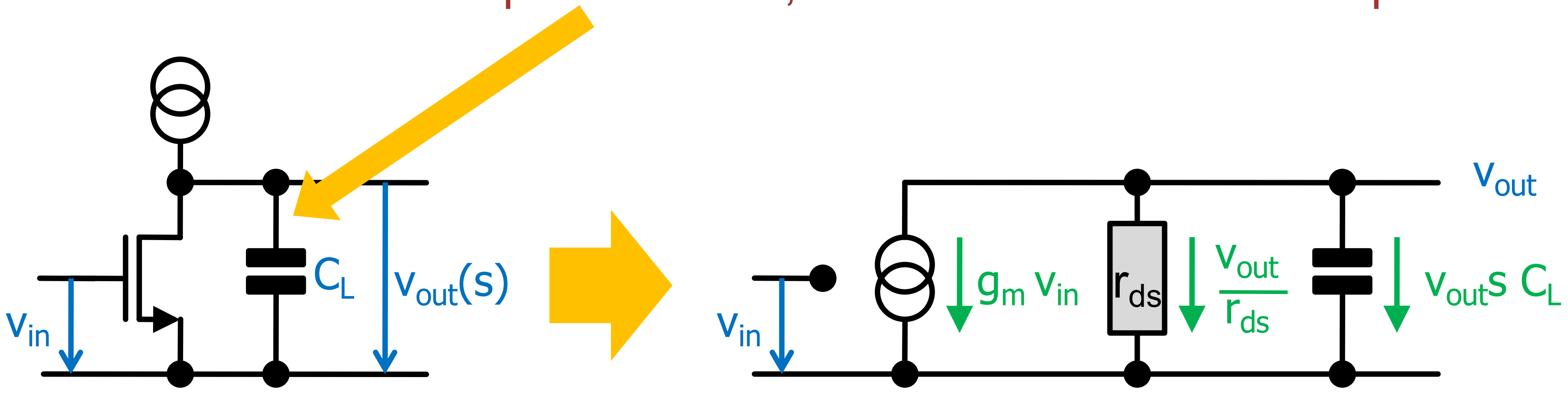
AC Behavior of the Gain Stage

Adding a Capacitive Load – ‘The Speed’

- With a capacitive load, we have another current path:



- Current sum at output node = 0:
  $0 = g_m\, v_{in} + v_{out} / r_{ds}$ $\mathbf{+ s\, C_L\, v_{out}}$

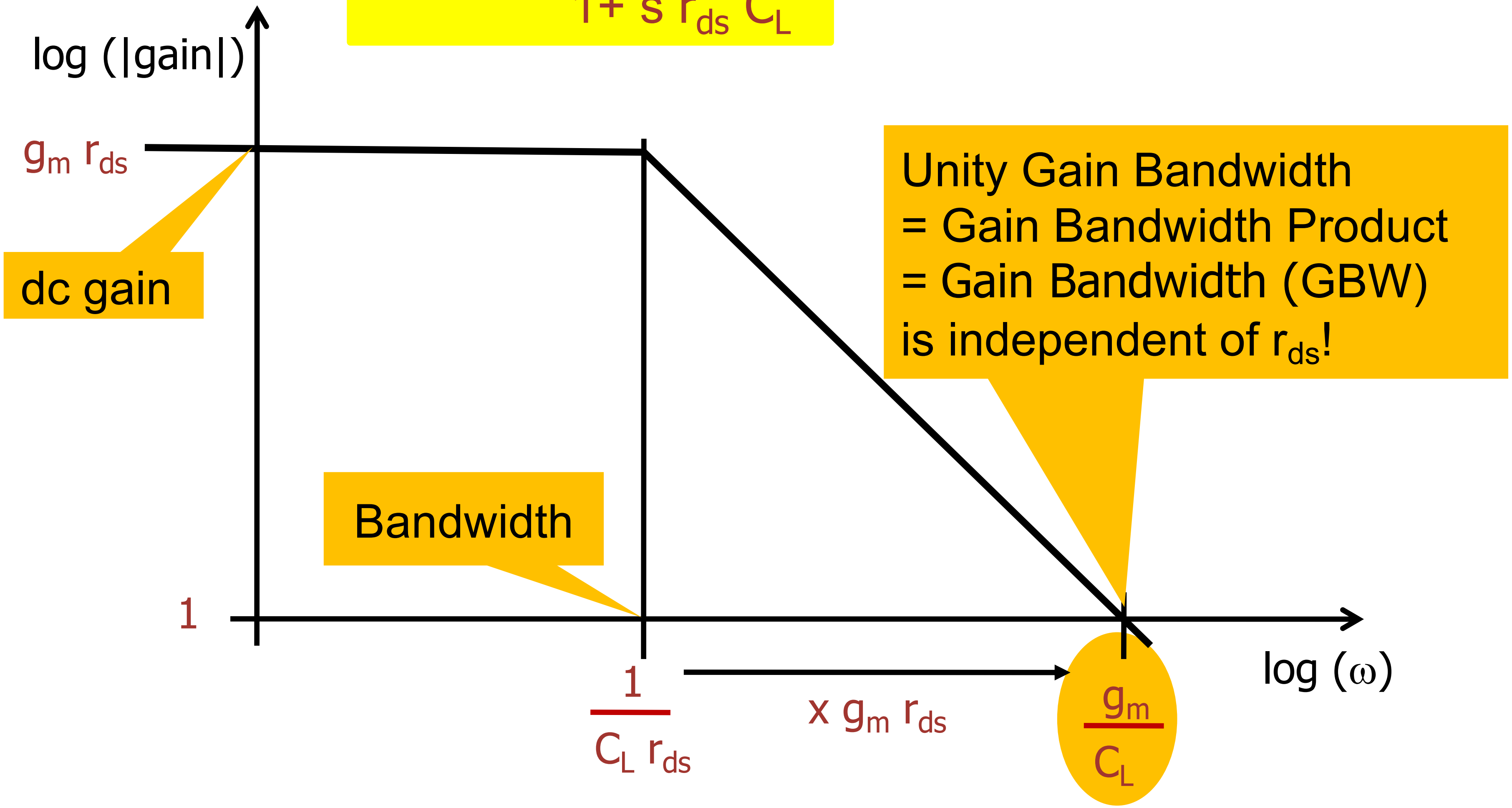
$$v(s) = -\frac{g_m\, r_{ds}}{1 + s\, r_{ds}\, C_L}$$

DC gain (as before)

Low pass behavior
Corner at $1/(r_{ds}\, C_L)$

Bode Plot of the Gain Stage

$$v(s) = -\frac{g_m\, r_{ds}}{1 + s\, r_{ds}\, C_L}$$



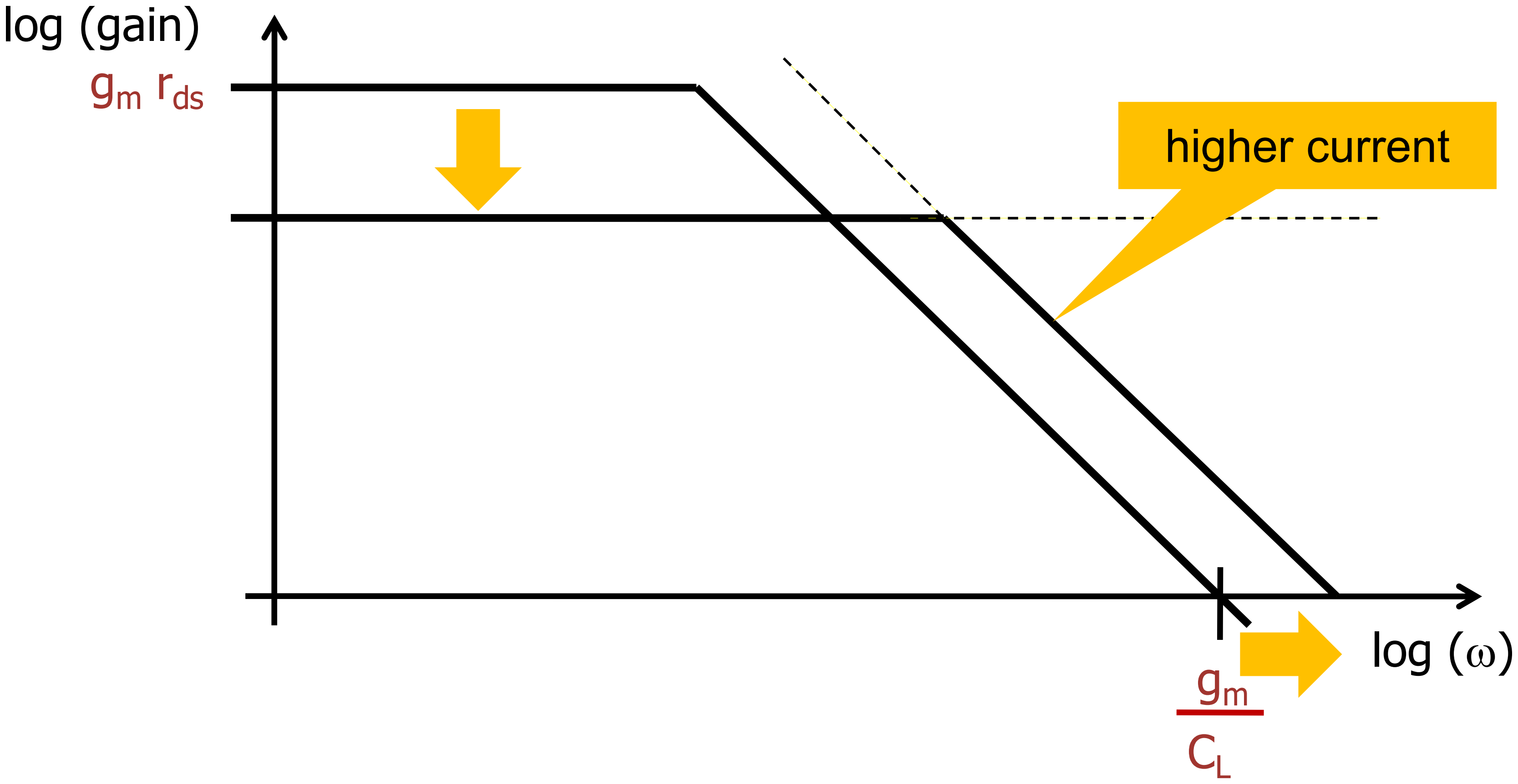
Remember: Gain-Bandwidth-Product

$$GBW = \frac{g_m}{C_L}$$

$$v = -\frac{g_m\, r_{ds}}{1 + s\, r_{ds}\, C_L}$$

Bode Plot for two current

- Increasing I_D
  - increases g_m and thus GBW
  - decreases r_{ds} and thus dc gain



Increasing the gain

- The gain of a single MOS is $v = g_m r_{ds}$.

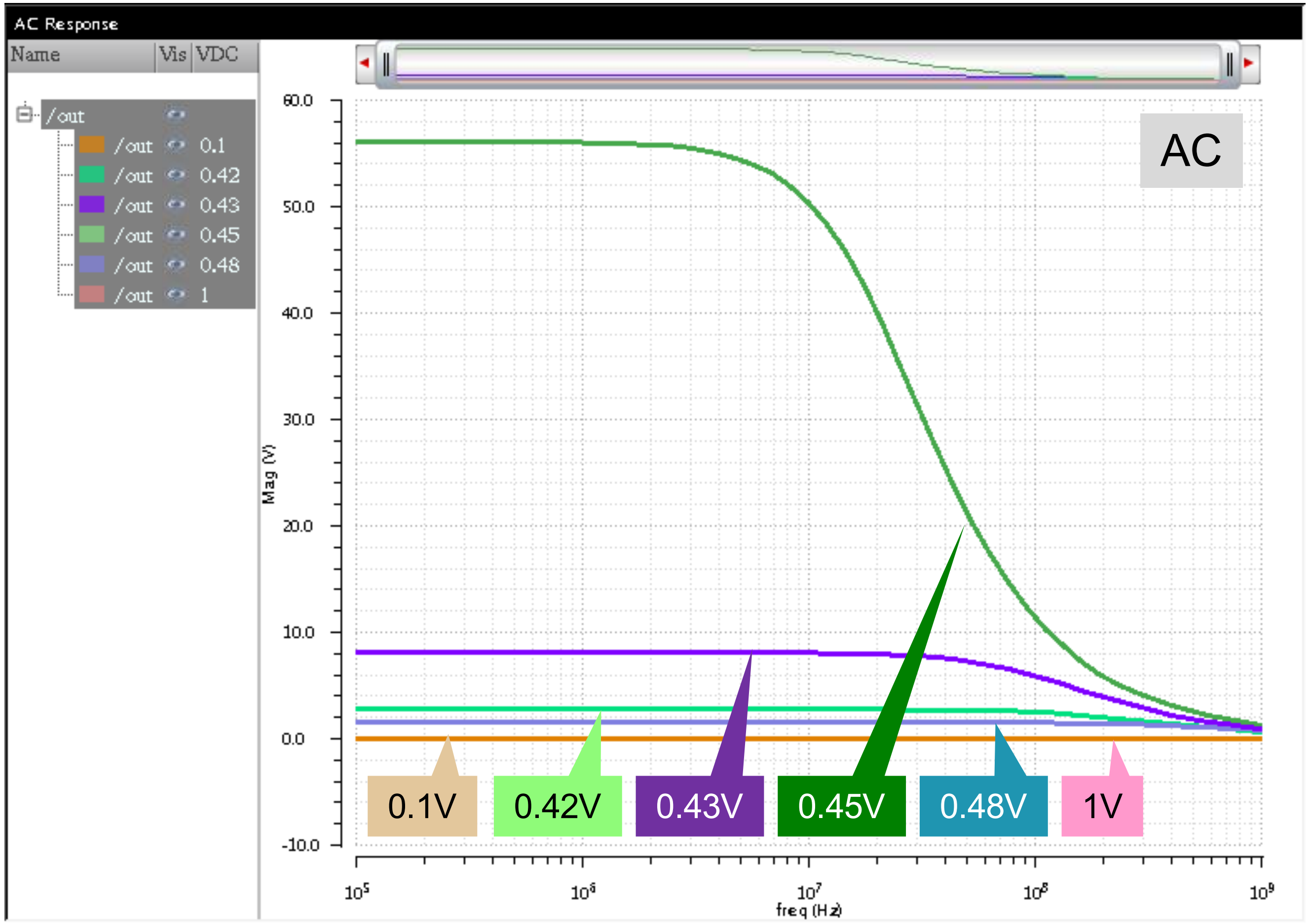
- $g_m \sim \text{sqrt}[2 K I_D W/L]$ (strong inversion)
- $r_{ds} \sim L / I_D$

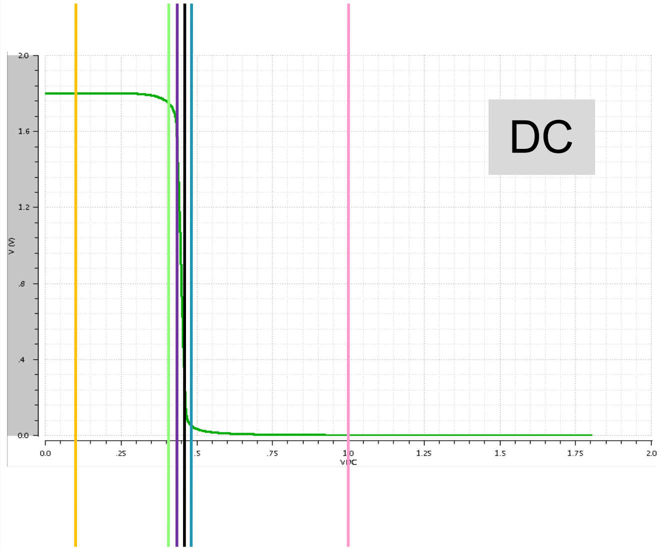
	$I_D \rightarrow 2 I_D$ (strong inv.)	$I_D \rightarrow 2 I_D$ (weak inv.)	$I_D \rightarrow 2 I_D$ (vel. sat.)	$W \rightarrow 2 W$ (s.i.)	$L \rightarrow 2 L$ (s.i.)
g_m	$\rightarrow \sqrt{2}\, g_m$	$\rightarrow 2\, g_m$	$\rightarrow g_m$	$\rightarrow \sqrt{2}\, g_m$	$\rightarrow g_m / \sqrt{2}$
r_{ds}	$\rightarrow r_{ds} / 2$	$\rightarrow r_{ds} / 2$	$\rightarrow r_{ds} / 2$	$\rightarrow r_{ds}$	$\rightarrow 2\, r_{ds}$
v	$\rightarrow v / \sqrt{2}$	$\rightarrow v$	$\rightarrow v / 2$	$\rightarrow \sqrt{2}\, v$	$\rightarrow \sqrt{2}\, v$

- We see:
  - gain is *increased* by *larger* W or L and by *smaller* I_D
  - *gain*-bandwidth only depends on g_m, i.e. mainly on I_D

AC sweeps at different Operation Point

- It the DC potential of V_{IN} is changed, we move to different points of the transfer curve:

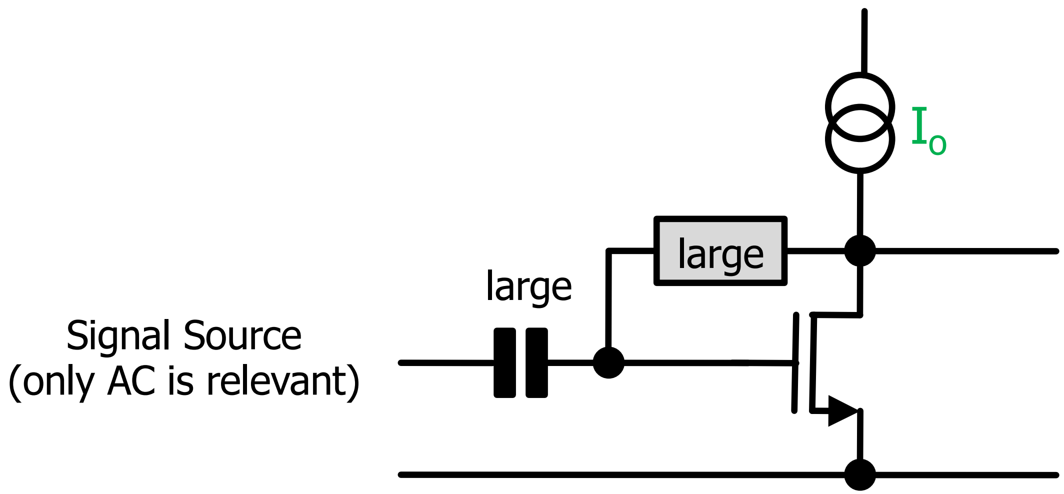




Transfer Curve with the chosen Operation points

Biasing the Gain Stage

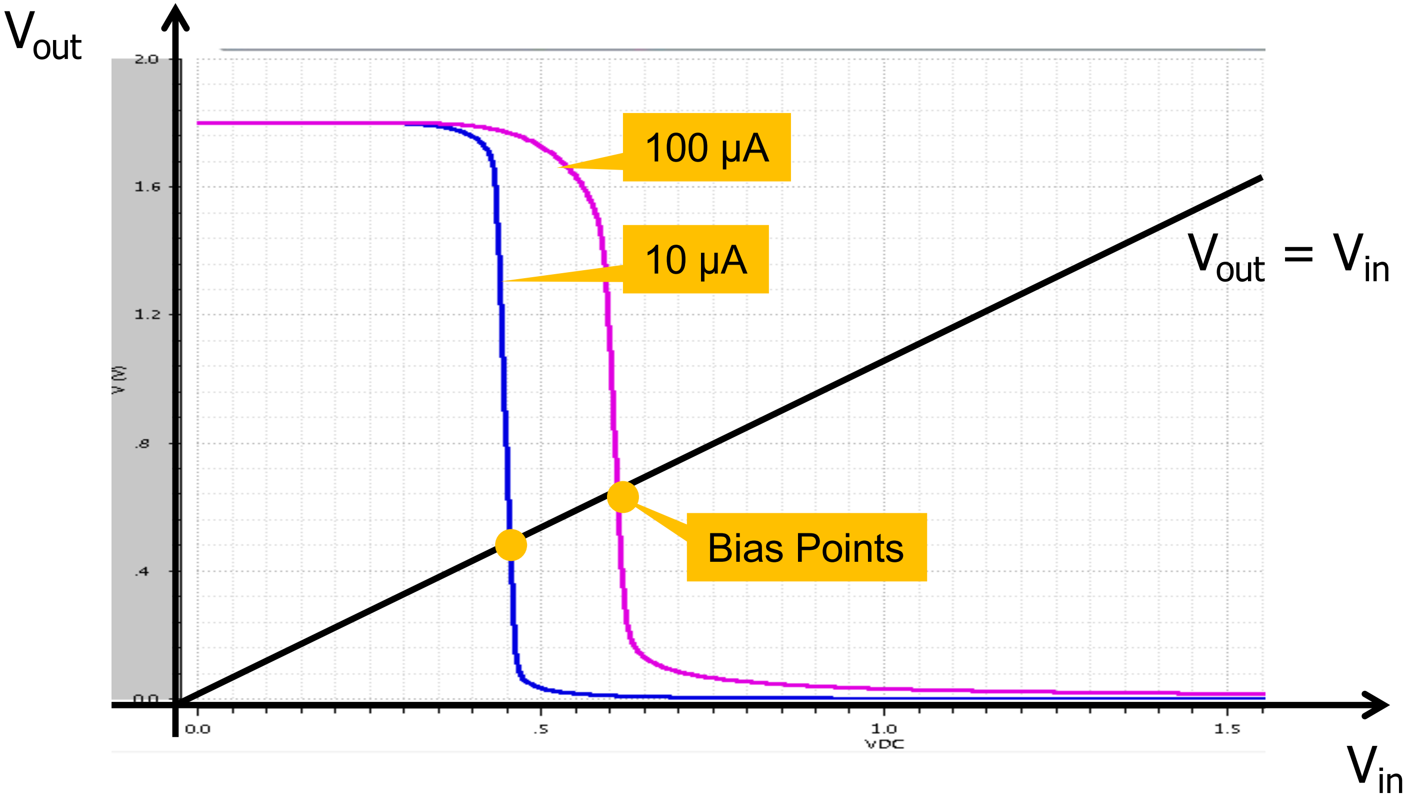
- In practice (& in simulation), V_{GS} and I_0 must 'correspond'
- This can be achieved (for instance) by a 'diode' connection of the MOS
- In simulation: To *let signals pass through*, the connection is done with a very large resistor and the input signal is ac coupled with an ‚infinite' capacitor.



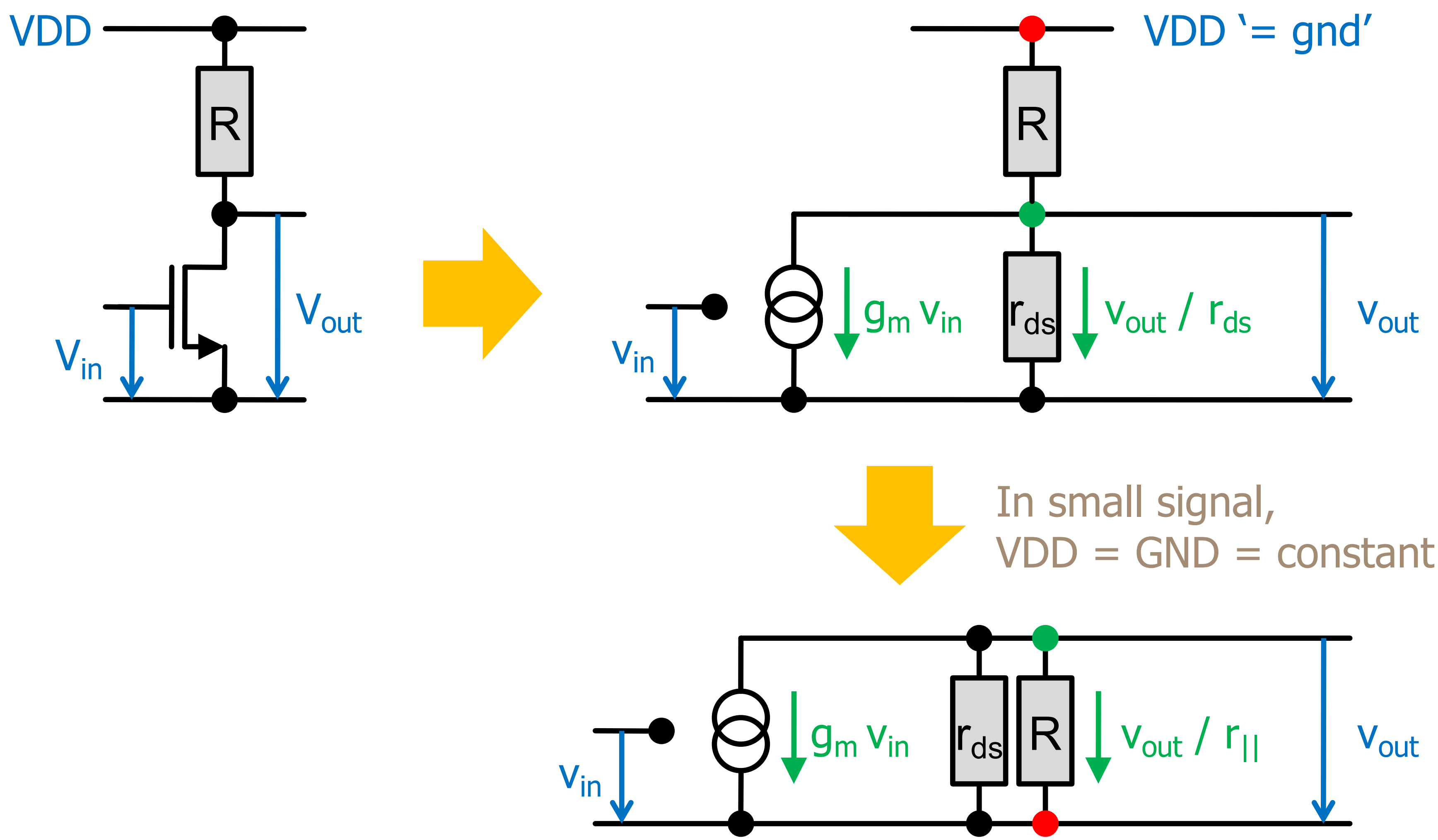
- In practice, other methods can be used…

Another View on the Bias Problem

- The resistor on the previous page forces $V_{out}=V_{in}$
- The operation point is the crossing between the *diagonal* ($V_{out}=V_{in}$) and the *transfer characteristic*
- This is usually a good point (maybe a bit low...)
- This works 'automatically' for changing bias & geometry



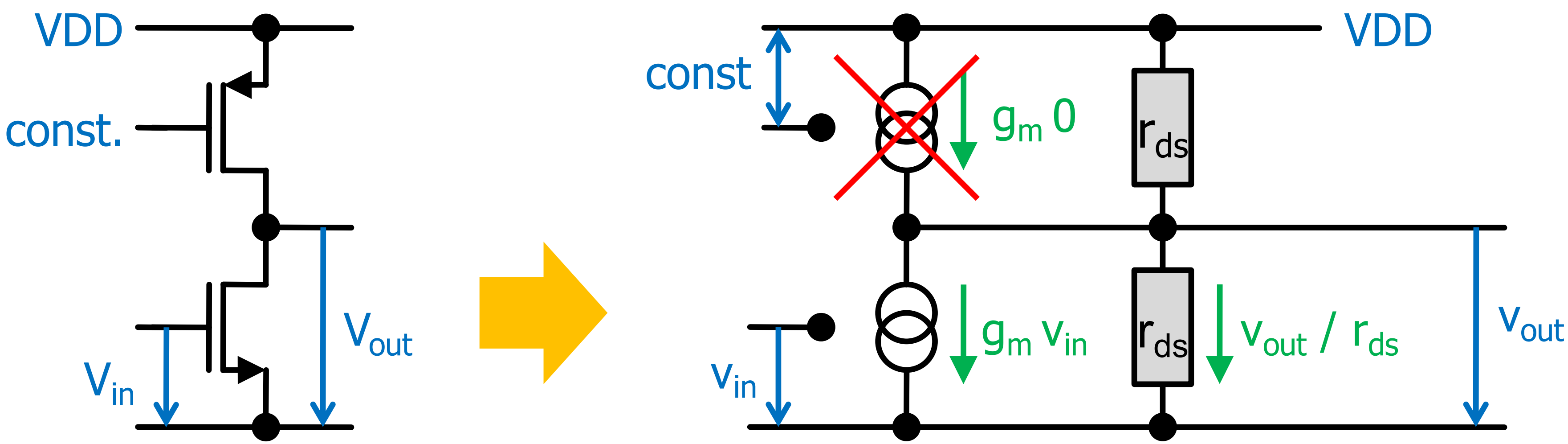
How about a Resistive Load?



→ R and r_{ds} act **in parallel: v = - g_m × (r_{ds} || R)**

Non-Ideal (PMOS) current source

- When a PMOS is used as current source, it ALSO has an output resistance.



- The transconductance part of the PMOS is off (v_{gs} = 0)
- The PMOS behaves just like a pure resistor (but r_{ds} is usually higher when in saturation)

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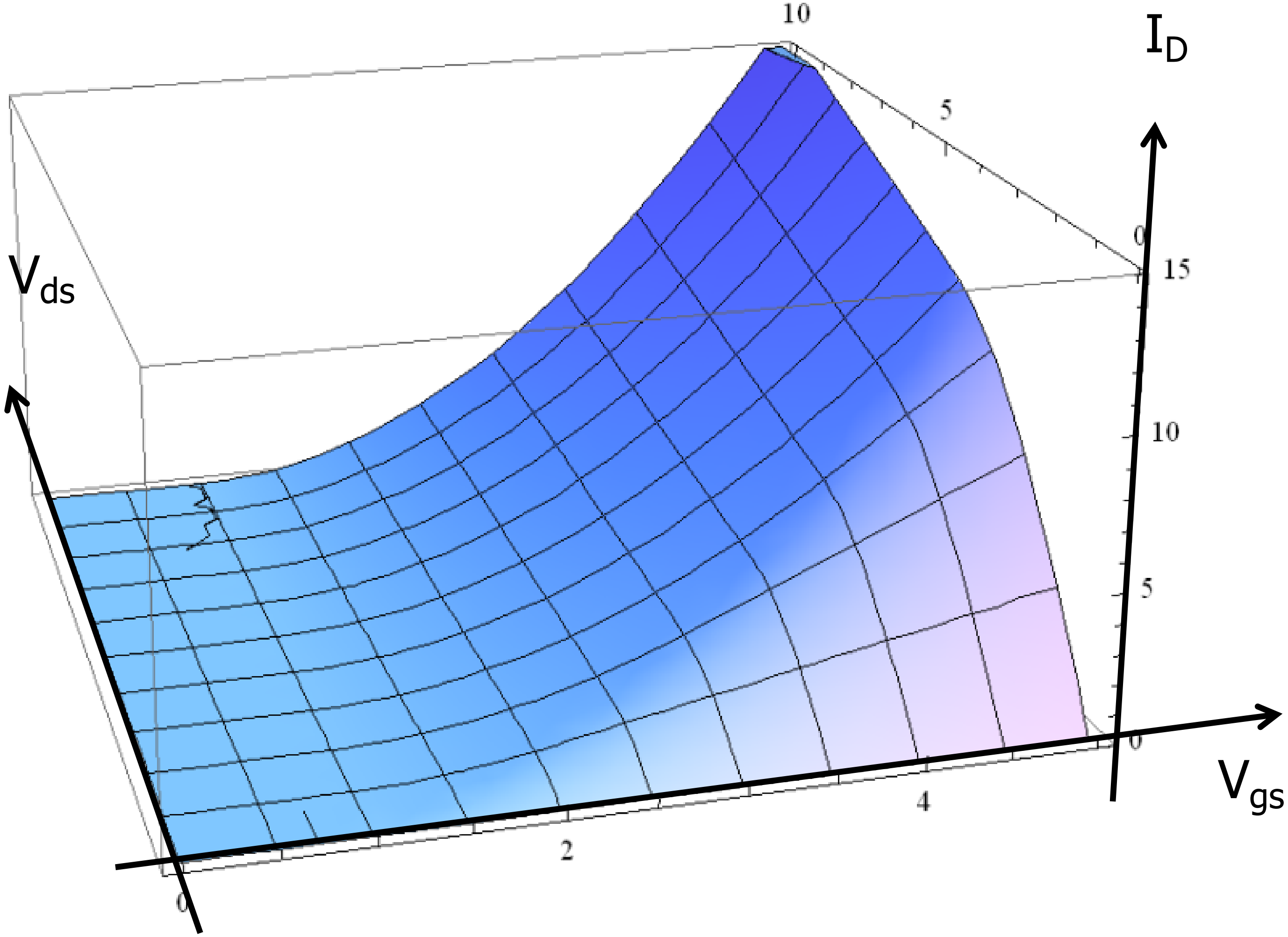
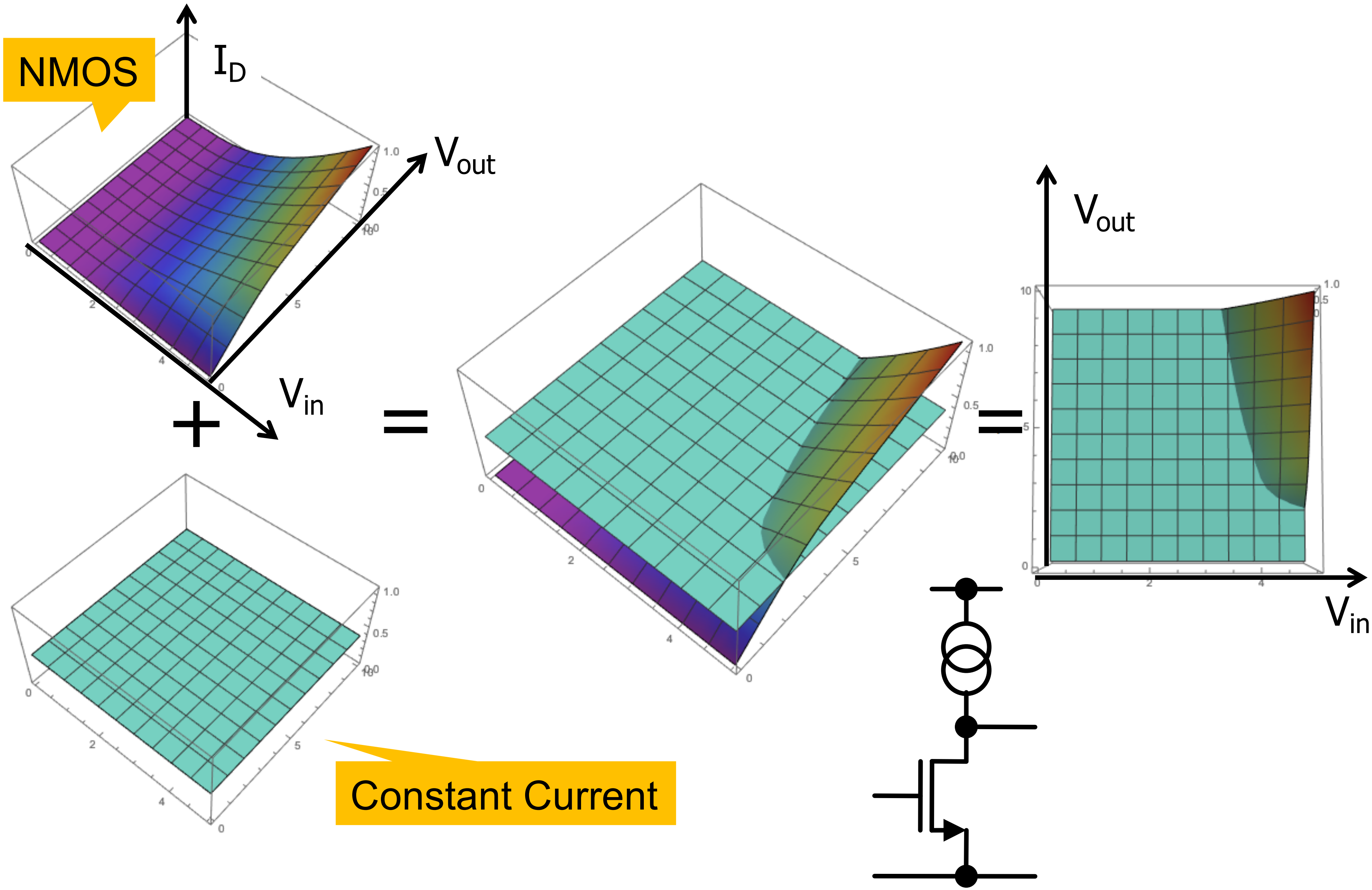
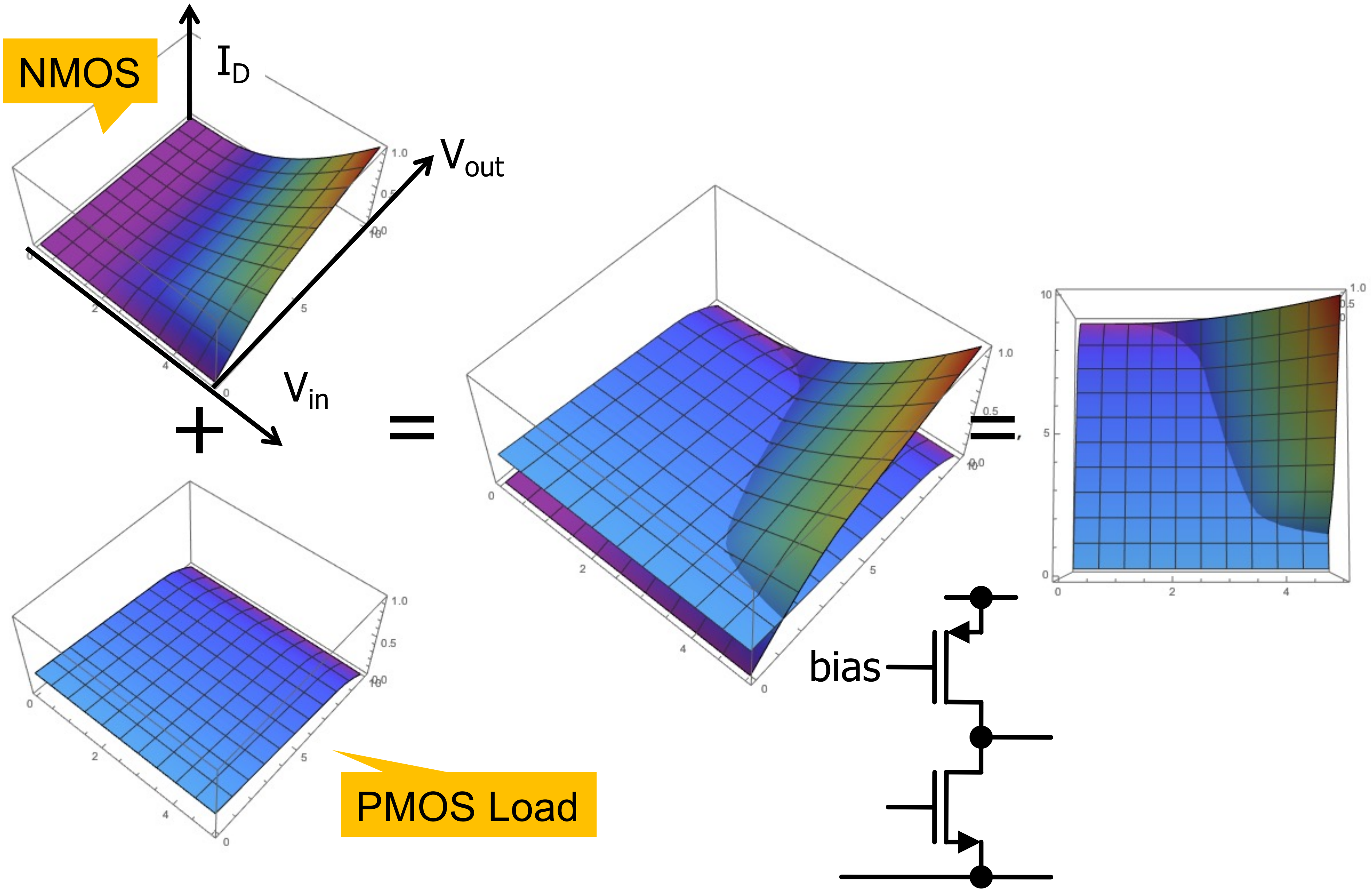
Reminder: Transistor Characteristics



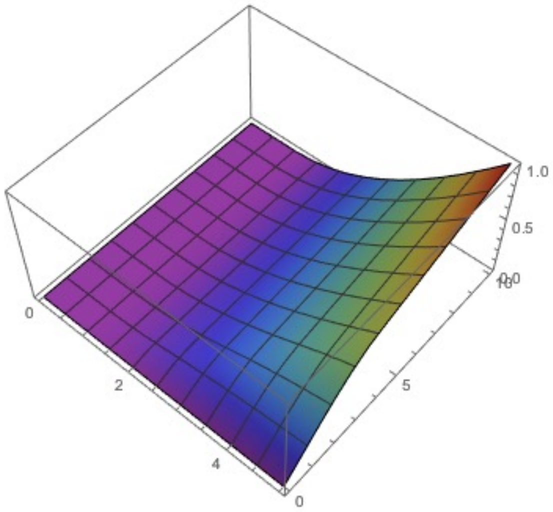
Visualization of Transfer Function: I-Load

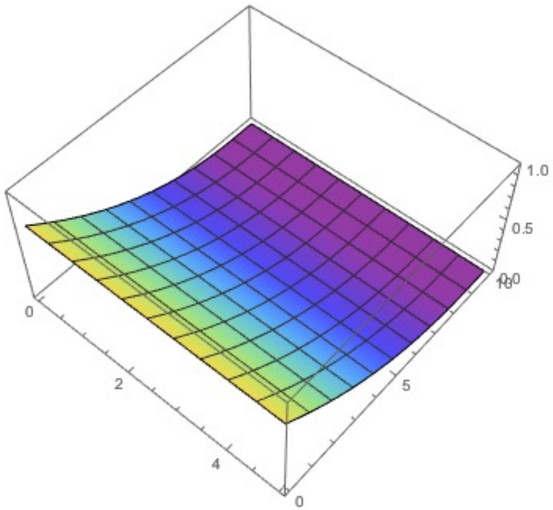


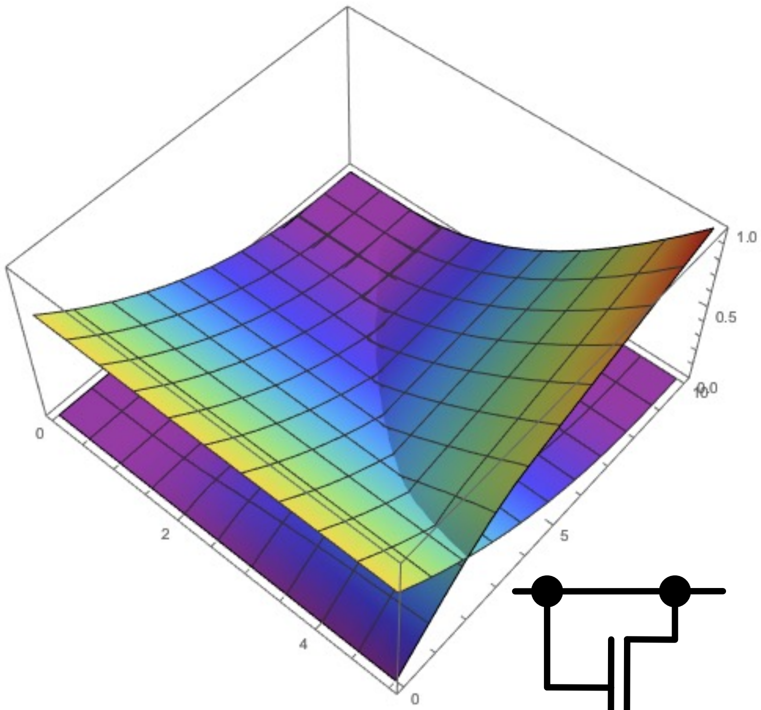
Visualization of Transfer Function: PMOS Load

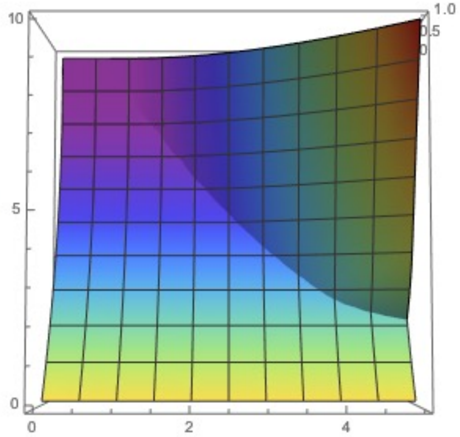


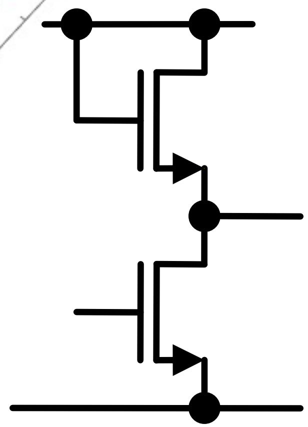
Load = Diode Connected (N)MOS



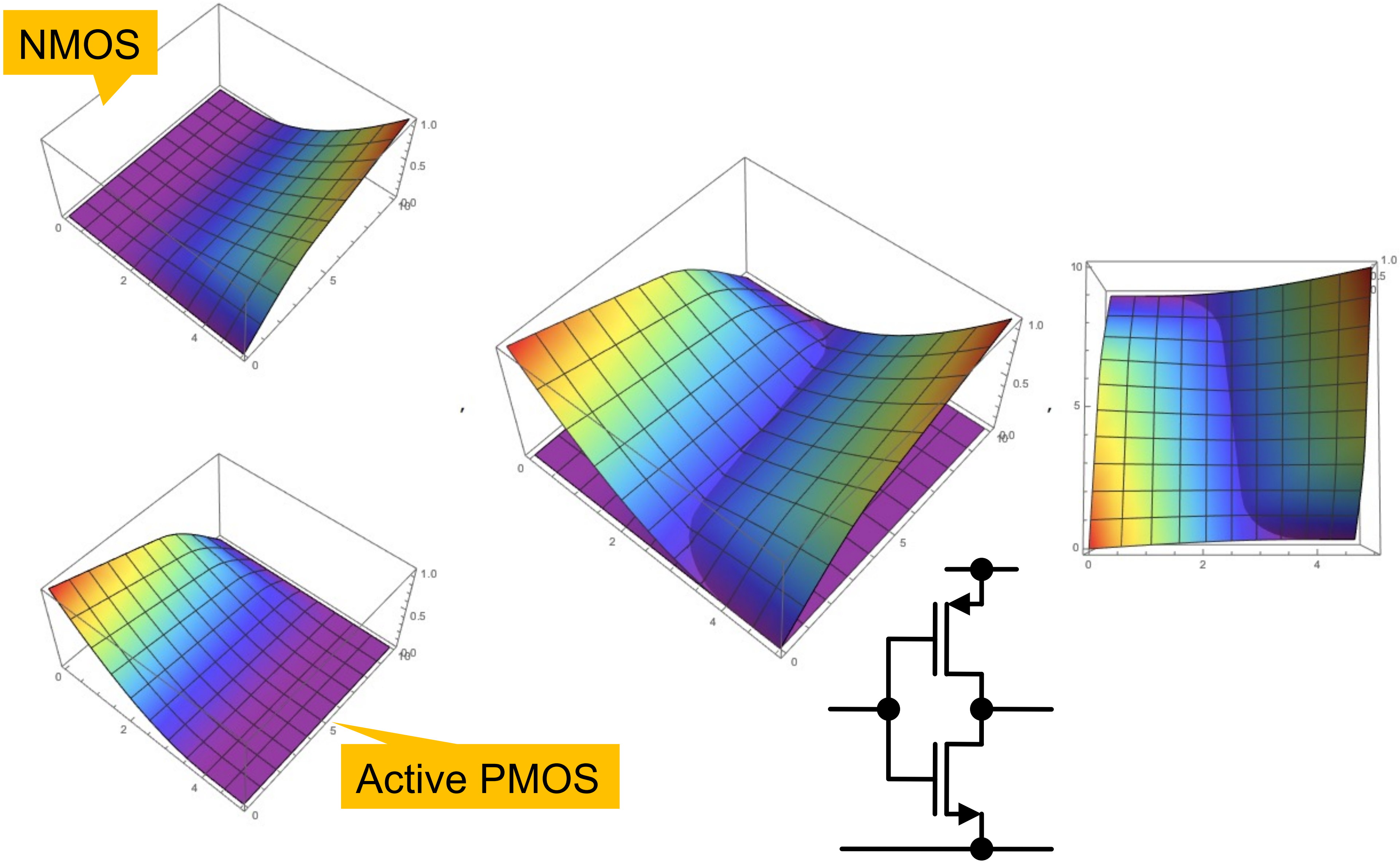






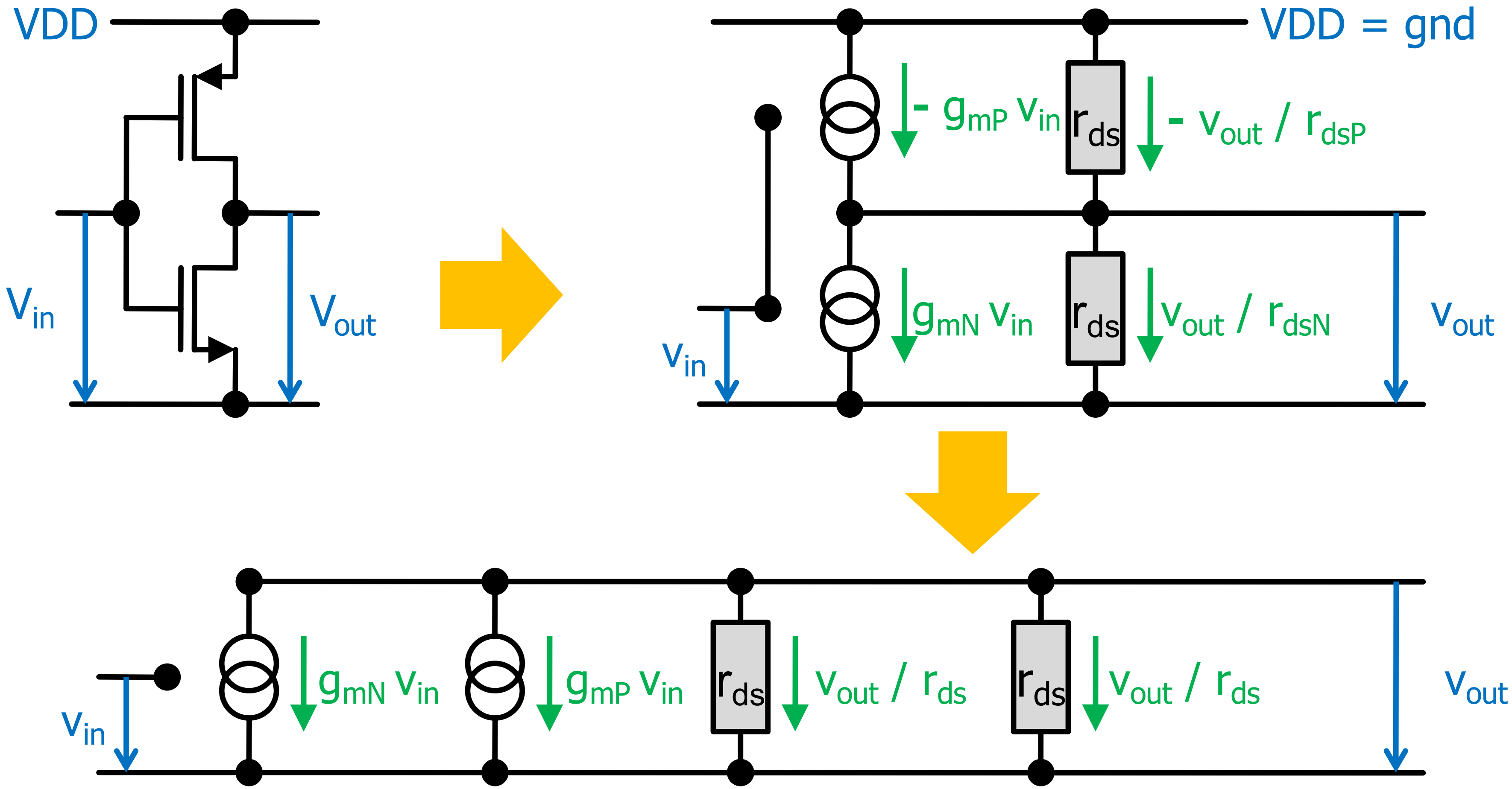


Visualization of Transfer Function: Inverter



CMOS Inverter

- Now consider a CMOS inverter:

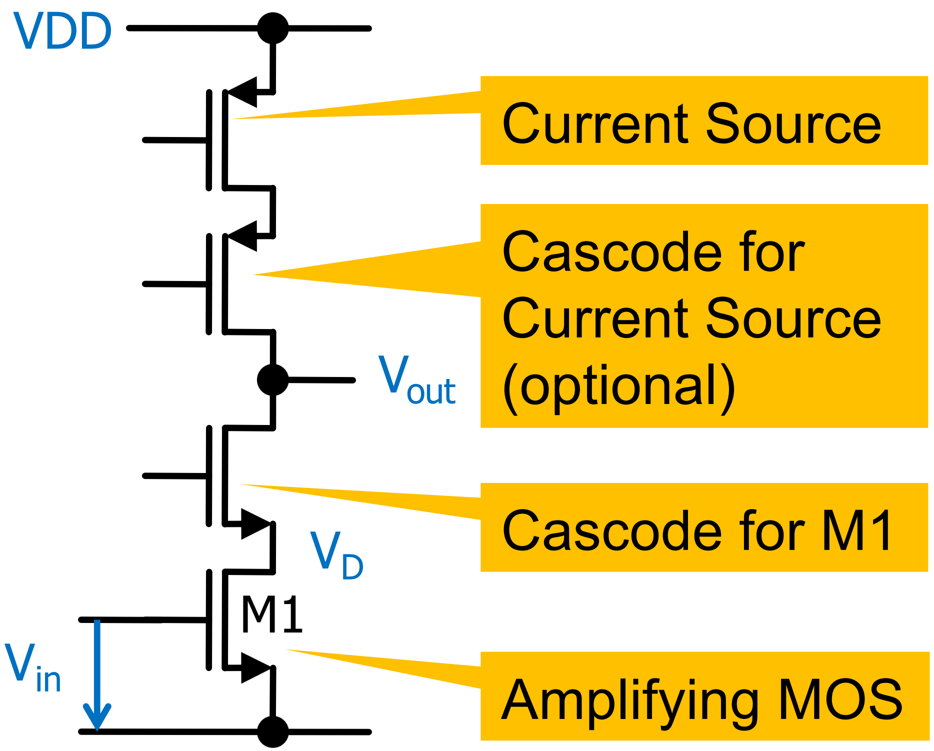


- g_m and r_{ds} of both MOS are in **parallel**
  $v = -(g_{mN} + g_{mP}) \times (r_{dsN} \,||\, r_{dsP})$

INCREASING THE GAIN

How to get very high gain ?

- g_m is very much limited by the current (can increase W…)
- r_{ds} can be increased by a cascode
- This leads to the 'straight' cascode gain stage:



Current Source: Defines Current

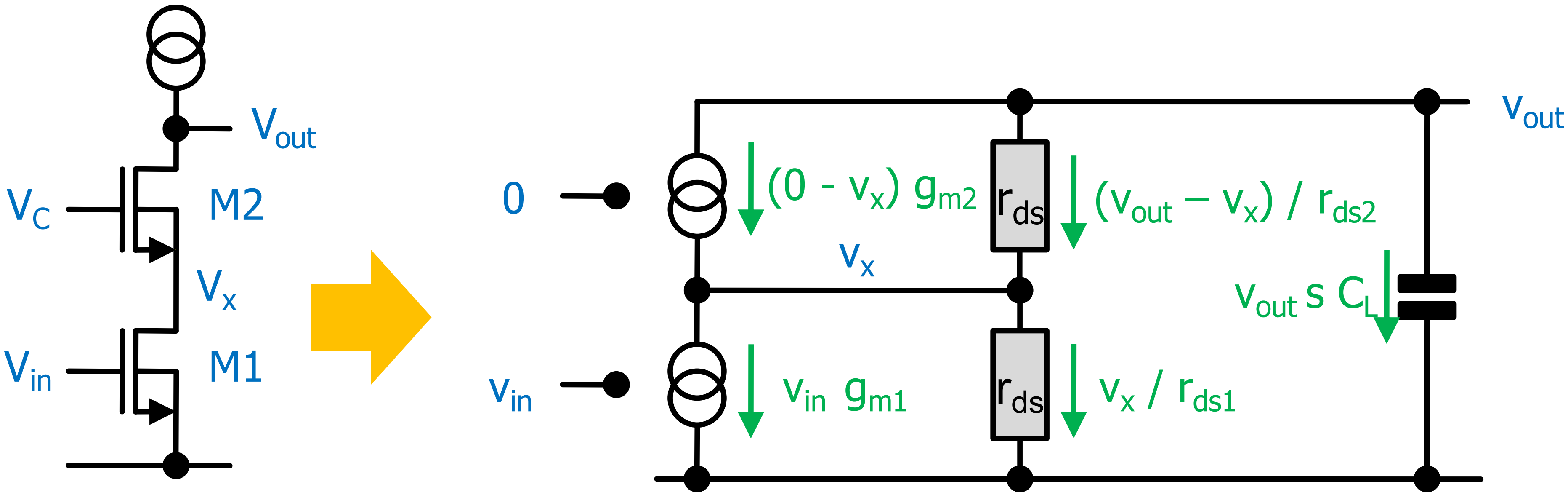
Cascode for Current Source (optional): Increase output Resistance of PMOS

Cascode for M1: Fix V_D so that changes In V_{out} do not lead to current change in M1

Amplifying MOS: Convert input voltage change to current change

Small Signal Analysis

- Assume bulks are connected to sources (no substrate effect)
  - Not always true in reality when NMOS are used...



- EQ1 (current sum at node v_{out}):

  $-v_x\, g_{m2} + (v_{out} - v_x)/r_{ds2} + v_{out}\, s\, C_L = 0$

- EQ2 (current sum at node v_x):

  $-v_x\, g_{m2} + (v_{out} - v_x)/r_{ds2} = v_{in}\, g_{m1} + v_x/r_{ds1}$

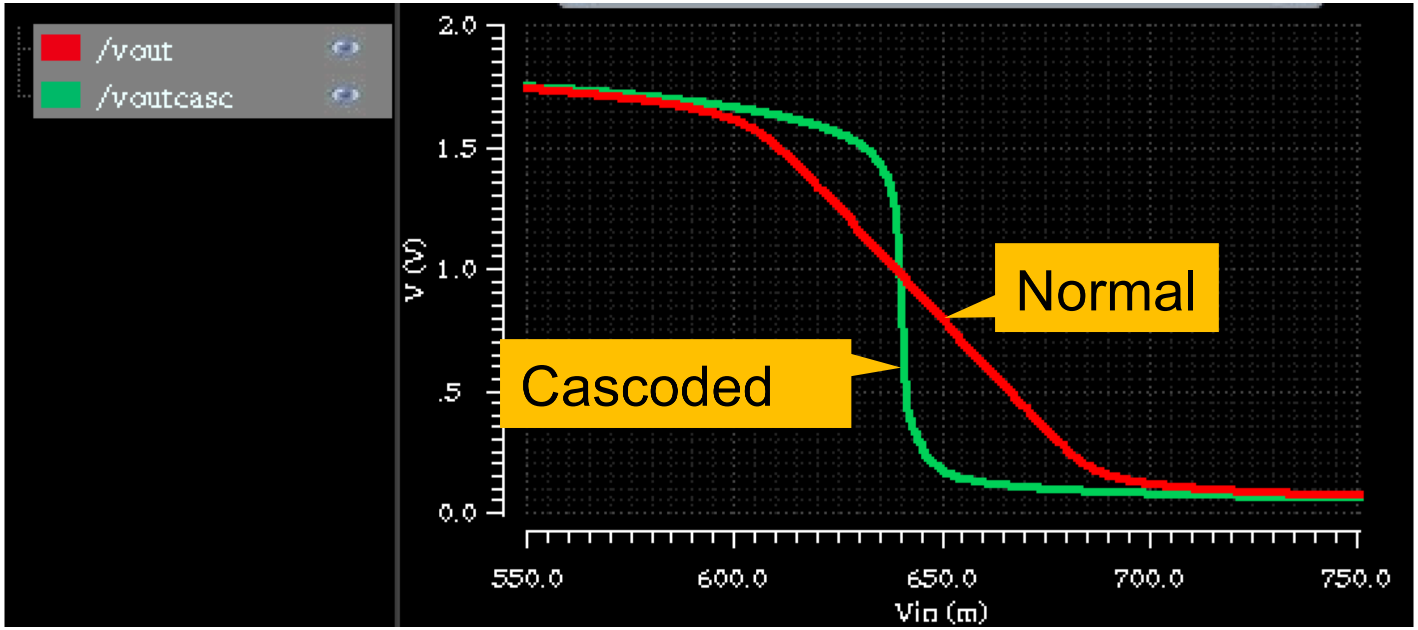
Solution

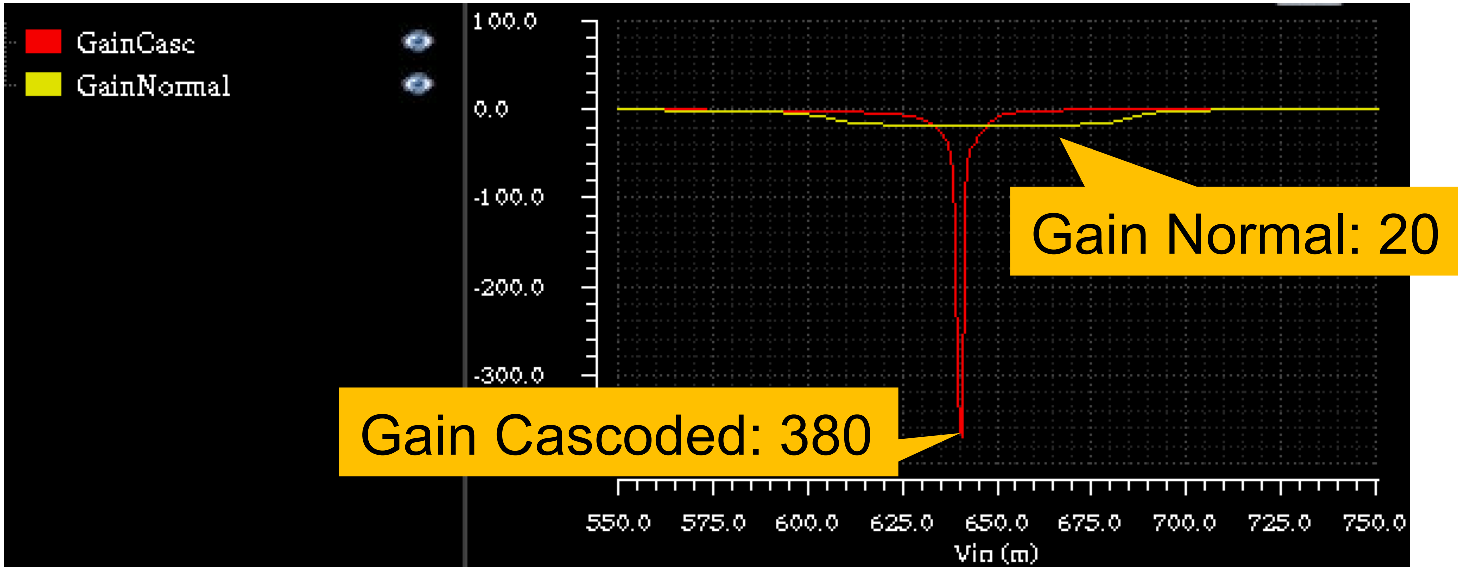
- $H(s) = -\dfrac{gm1\ rds1\ (1 + gm2\ rds2)}{1 + CL\ (rds1 + rds2 + gm2\ rds1\ rds2)\ s}$
- As usually $g_m\ r_{ds} \gg 1$, the parenthesis can be simplified:
- $H(s) \sim -\dfrac{gm1\ rds1\ gm2\ rds2}{1 + CL\ gm2\ rds1\ rds2\ s}$ (= single pole low pass)
- The *DC gain* is $|H(0)| = g_{m1}\ r_{ds1} \times g_{m2}\ r_{ds2}$

  (i.e. *squared* wrt. a simple gain stage!)
- The bandwidth is $BW = (C_L\ r_{ds1} \times g_{m2}\ r_{ds2})^{-1}$

  (*decreased* by same factor)
- The unity gain bandwidth is the **same** as simple stage! $GBW = BW \times |H(0)| = g_{m1}/C_L$

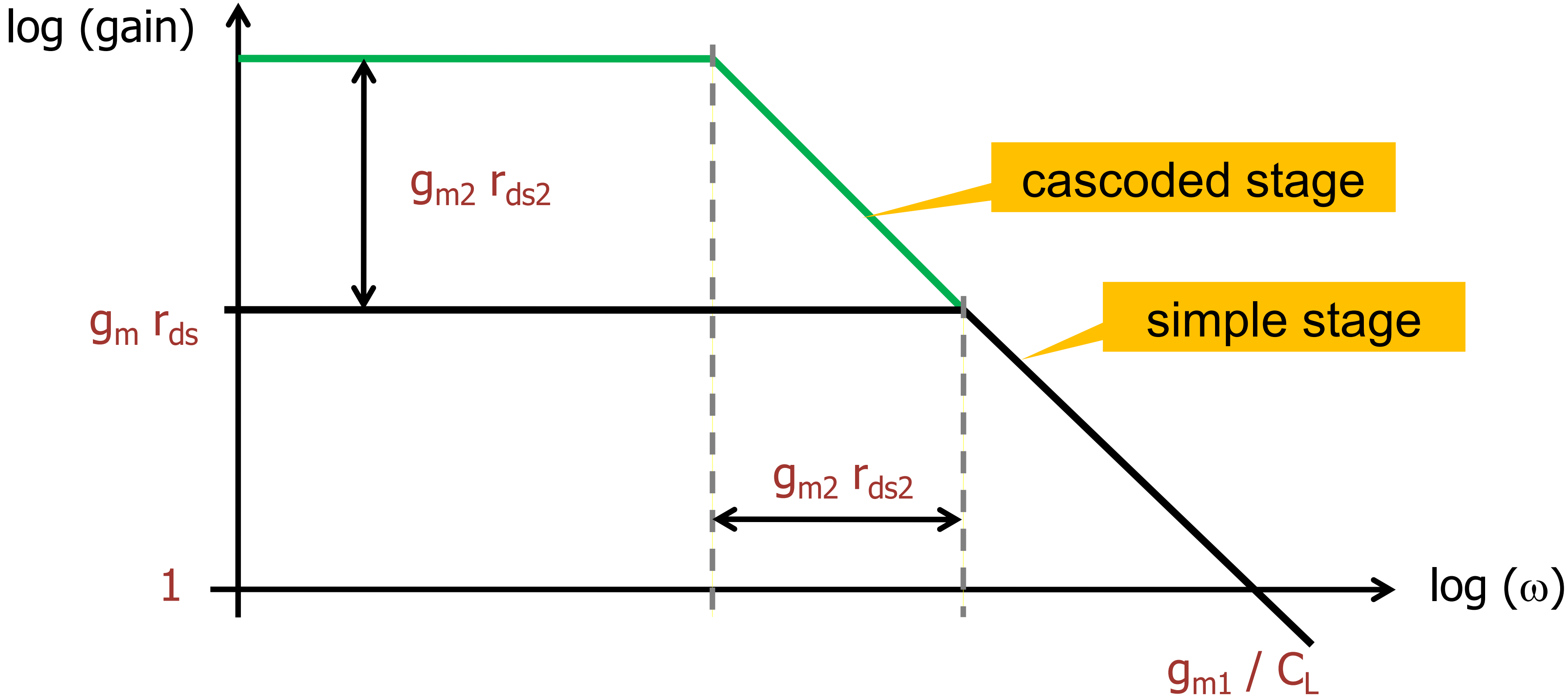
DC Sweep


/vout
/voutcasc
2.0
1.5
1.0
.5
0.0
V (V)
Normal
Cascoded
550.0
600.0
650.0
700.0
750.0
Vin (m)


GainCasc
GainNormal
100.0
0.0
-100.0
-200.0
-300.0
Gain Normal: 20
Gain Cascoded: 380
550.0
575.0
600.0
625.0
650.0
675.0
700.0
725.0
750.0
Vin (m)

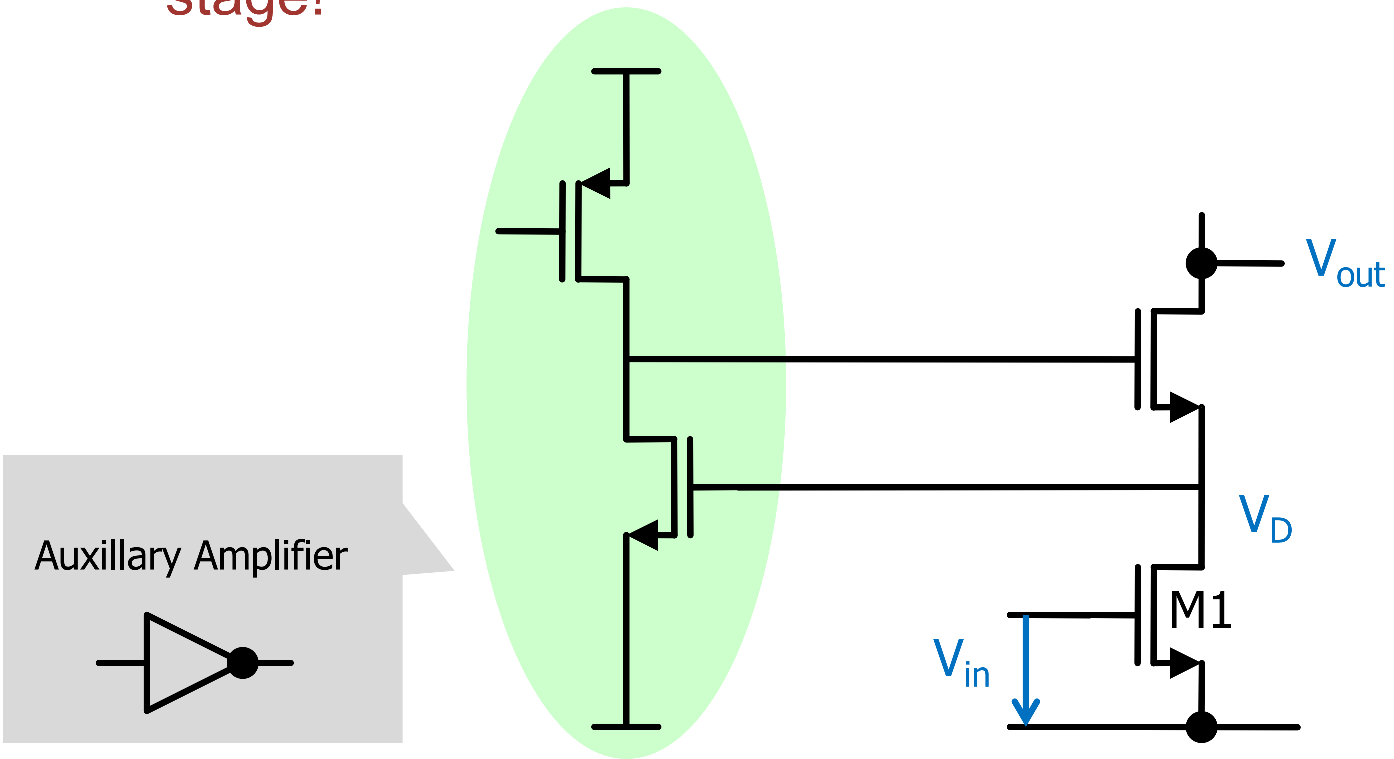
Comparing Simple / Cascoded Gain Stage

- DC gain is increased by the 'gain' $g_m \times r_{ds}$ of the cascode
  - the cascode 'boosts' the output resistance
- The GBW remains *unchanged* ☹
  - the current generated in M1 must charge C_L. The cascode does *not* help for speed ... We need more g_m → more power



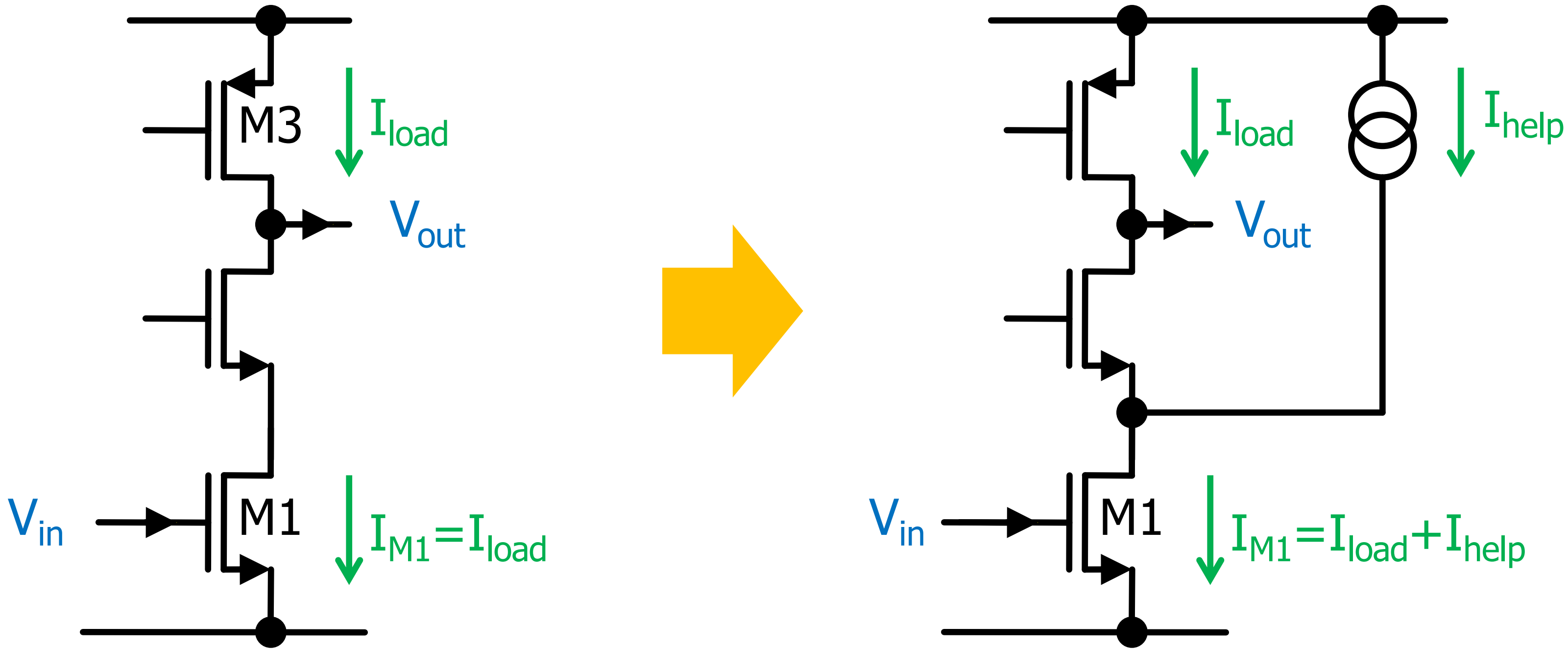
How to get EVEN higher gain ?

- Just like we have done in the 'regulated' mirror, we can use an amplifier to keep the drain of the amplifying MOS at constant potential.
- For the amplifier, we use (again) a simple gain stage…
- With this method, a gain of 10.000 can be reached in one stage!



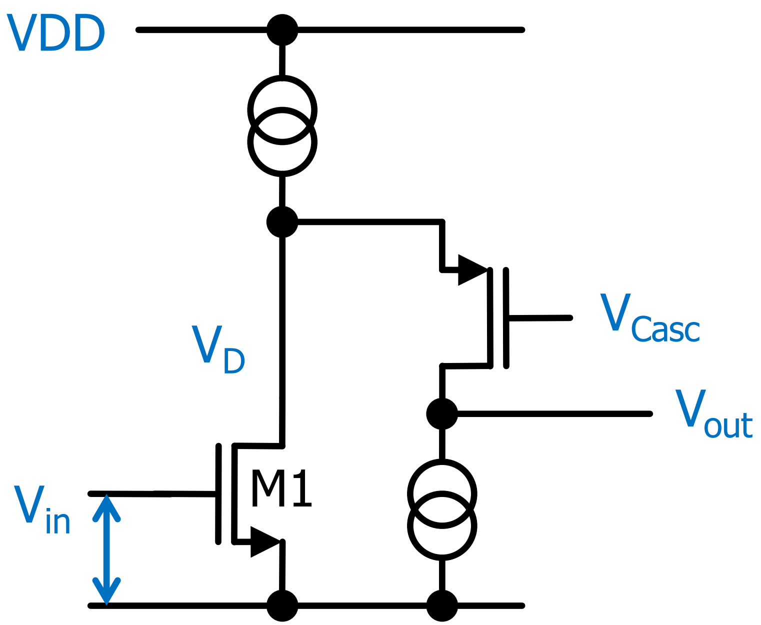
Increasing gain further

- The gain (left) is limited by the output cond. of the load M3
  - That is proportional to the current in the load
- Can we *reduce* the current in the *load*, keeping the current in the amplifying MOS M1 unchanged (for g_m)?
- Yes: Add an extra current to M1 at the cascode node:



For Experts: The ‘folded’ cascode

- The ‘straight’ cascode has some drawbacks
  - many MOS are stacked → dynamic range suffers
  - DC feedback ($v_{out} = v_{in}$) is marginal as v_{out} cannot go very low
- Alternative: use a PMOS to cascode the input NMOS M1:
  - Quite surprising that this works….



  - Current in output branch is smaller than in M1 → r_{out} is higher
- Note: It may *look* like this topology has non-inverting gain…

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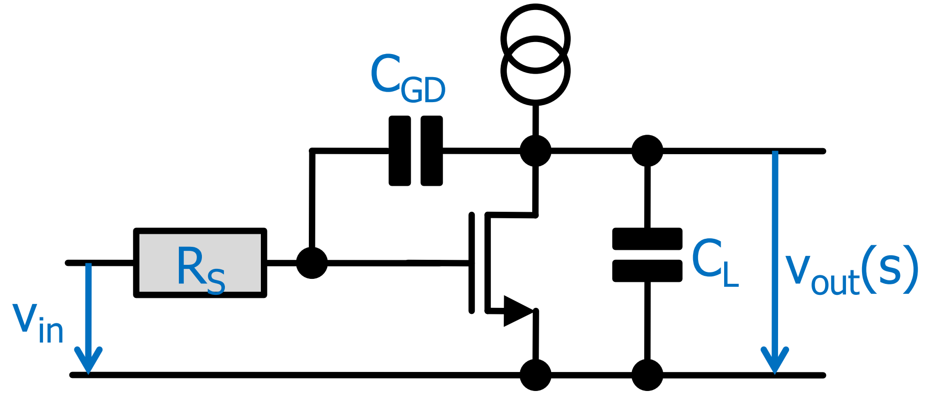
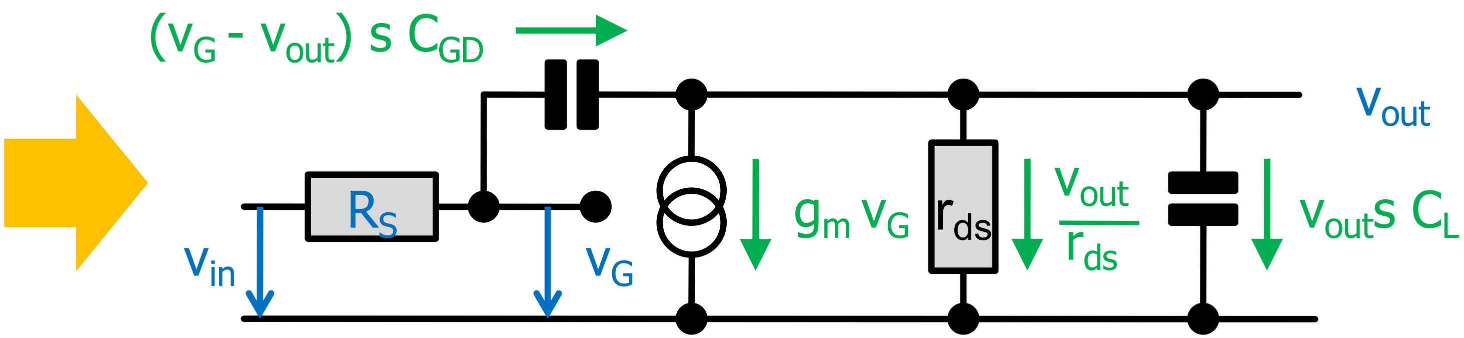
ADVANCED TOPICS

C_{GD}: Introducing a 'Zero' (Advanced Topic)

- Consider the effect of the gate-drain capacitance C_{GD}
  - Assume a finite driving impedance of the source R_S:

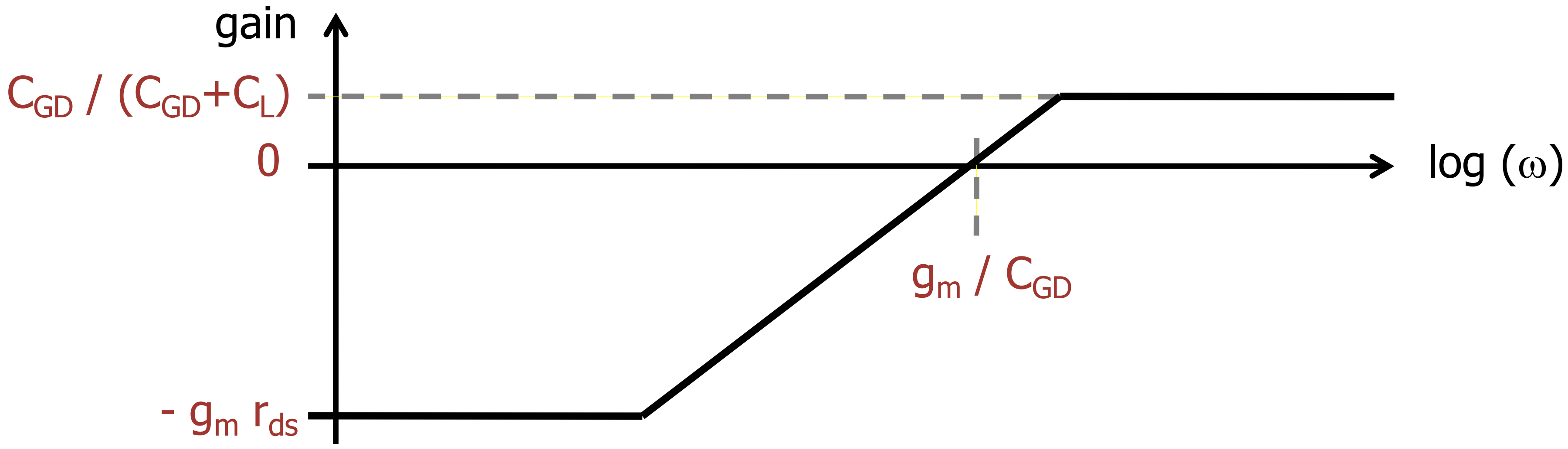




- $H(s) = \dfrac{-gm\ rds + CGD\ rds\ s}{1 + CL\ rds\ s + CGD\ s\ (rds + RS + gm\ rds\ RS + CL\ rds\ RS\ s)}$

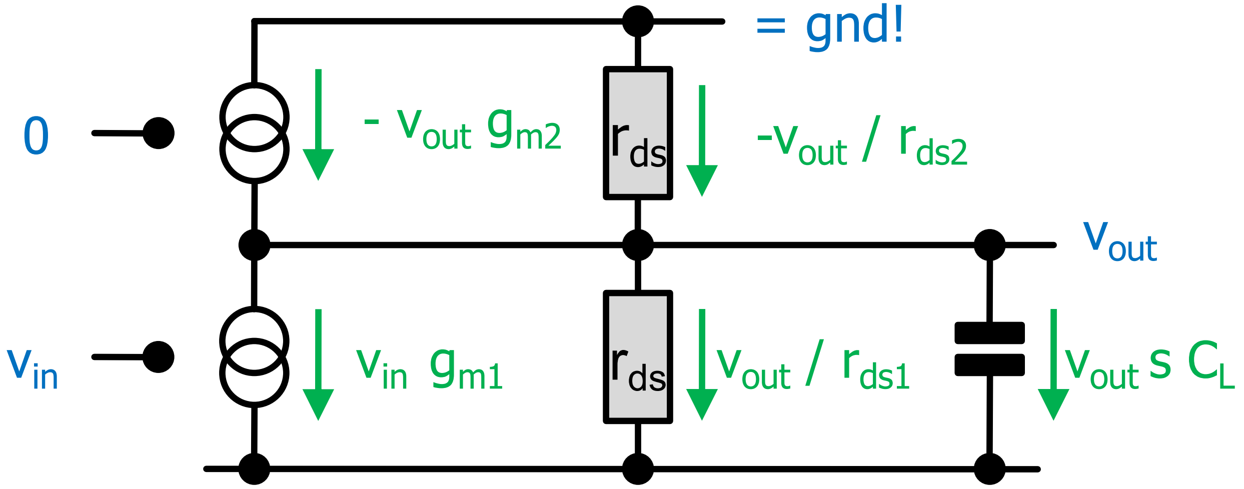
New: We get a Zero - What Happens?

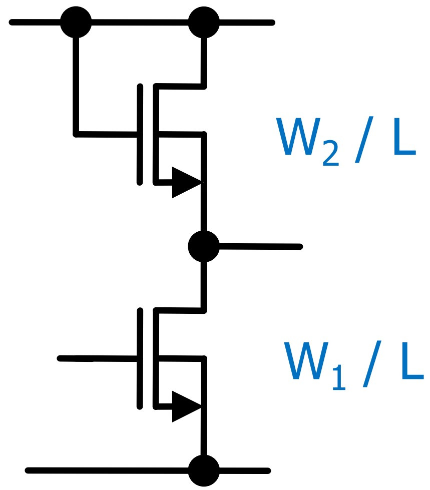
- We have $H(0) = - g_m r_{ds}$ as before.
- For $R_S=0$
  - The input signal propagates directly to the output via C_{GD}.
  - This same phase signal competes with the inverted signal through the MOS.
  - For very large frequencies, C_{GD} ‘wins’.
  - We therefore have zero gain at some point
  - At high frequencies, we have a capacitive divider with gain < 1



Check your Understanding:

- What is H(s) of a gain stage with a (NMOS) diode load:





- $H(0) = -\frac{g_{m1}\, r_{ds1}\, r_{ds2}}{r_{ds1} + r_{ds2} + g_{m2}\, r_{ds1}\, r_{ds2}} \sim -\frac{g_{m1}}{g_{m2}}$

- In strong inversion, this is the square root of the W-ratio
  - For instance: for $W_2 / W_1 = 4$, the gain is ~ 2.

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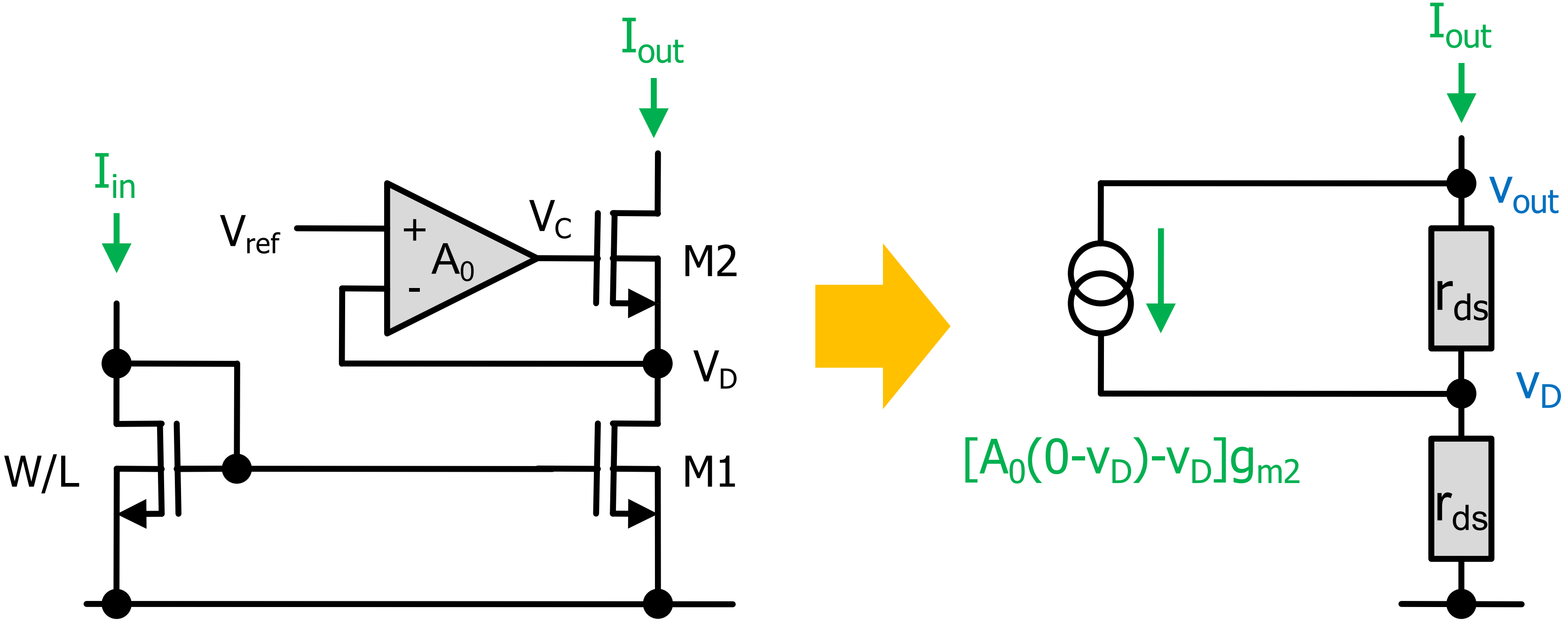
The Current Mirror - Again

Active Regulation of the Drain Voltage

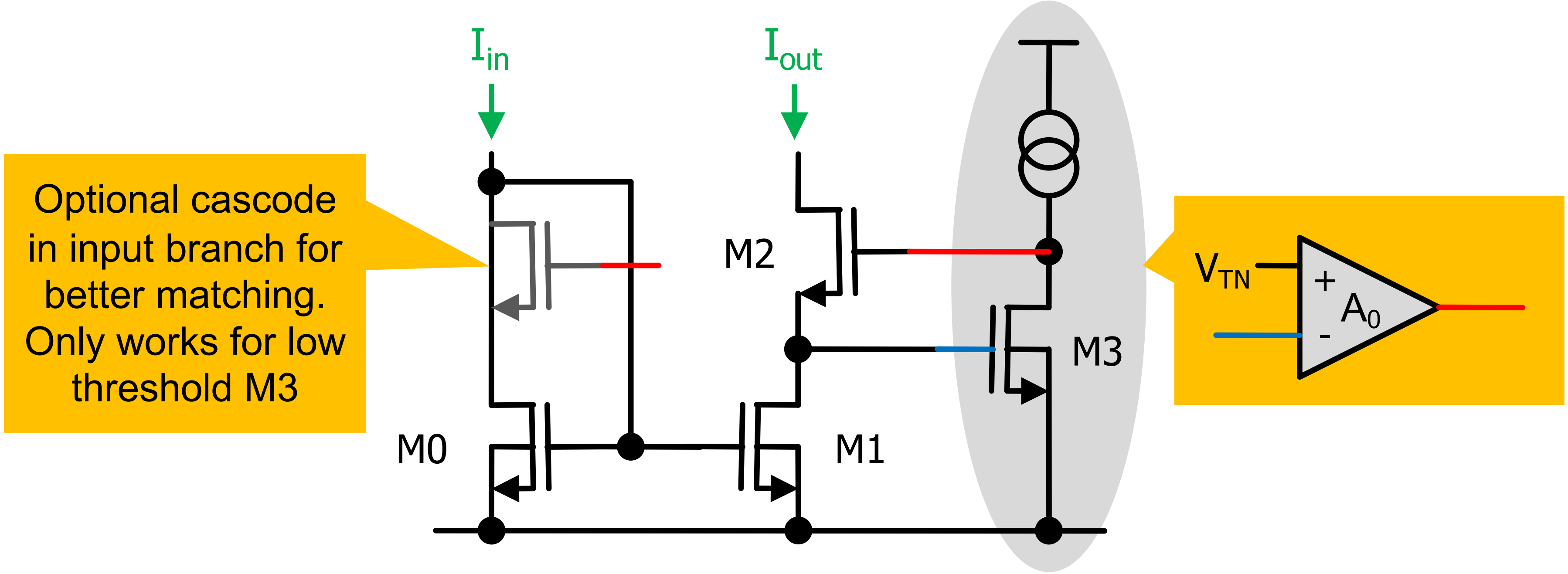
- The following circuit uses an amplifier with gain A_0 to keep V_D constant:
  - V_D is compared to a (fixed) reference V_{ref}.
  - $V_C = A_0 (V_{ref} – V_D)$
- For better *matching*, the input must be cascoded as well..



- r_{out} = rds2 + rds1 (1 + (1 + A0) gm2 rds2)

Practical Realization

- The amplifier can just be a gain stage...
- This gives the ‚regulated current mirror':



- Here, $A_0 \sim g_{m3}\, r_{ds3}$, Therefore $r_{out} \sim r_{ds1} \times g_{m2}\, r_{ds2} \times g_{m3}\, r_{ds3}$
- Note:
  - V_{DS} of M1 is ~ V_{TN}, which is higher than needed (wasting dyn.). (Using M3 with lower threshold helps)
  - Matching is *not* good, because $V_{DS0} \neq V_{DS1}$ -> add left cascode