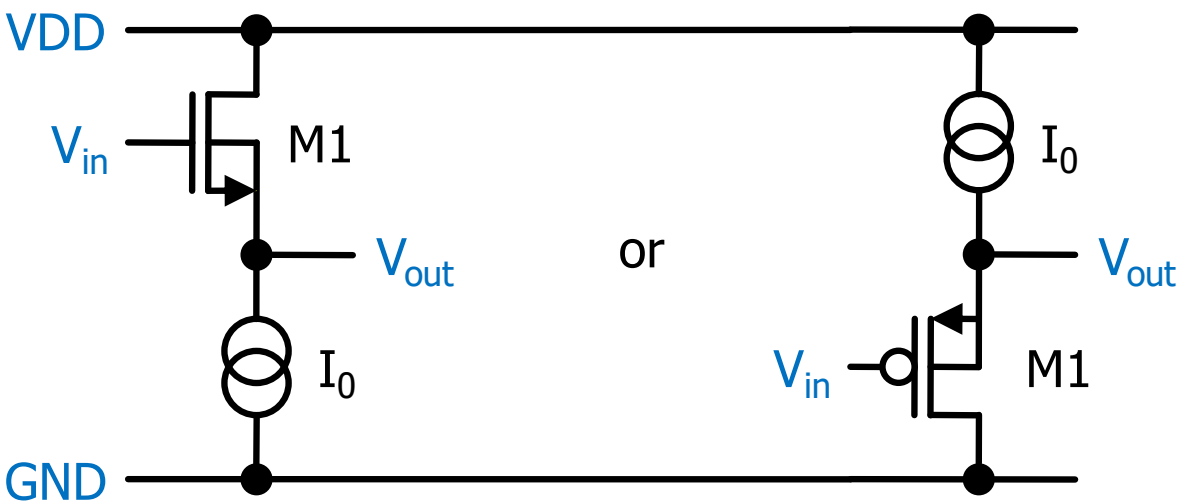
The Source Follower

The Source Follower (Common Drain Stage, SF)

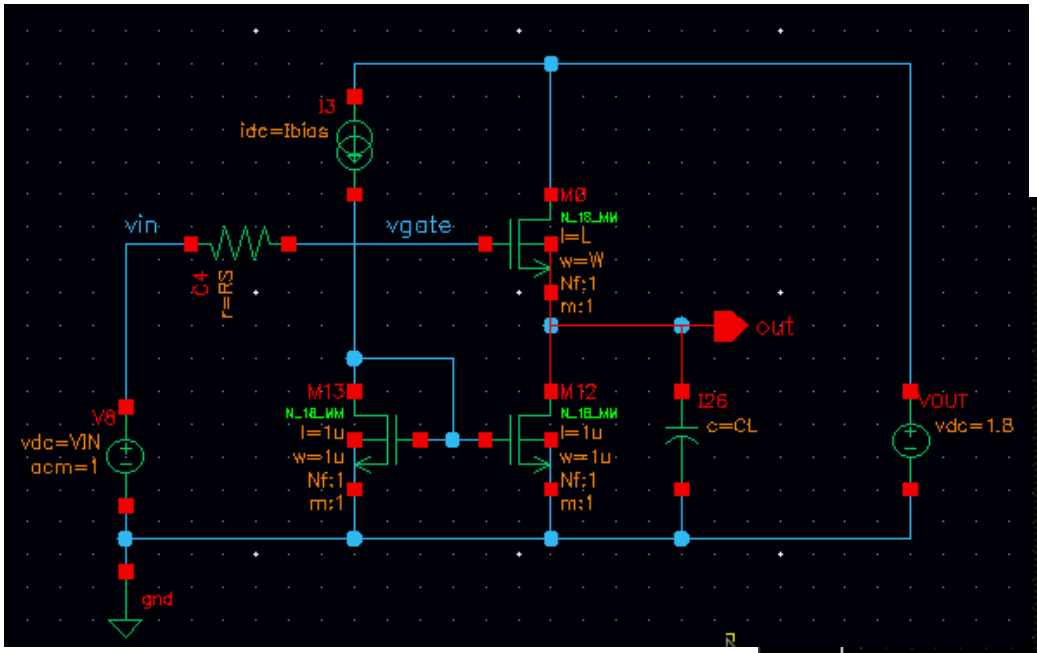
- Current source I_0 pulls a *constant* current through the MOS
- This fixes V_{GS} of M1 (to V_T + Sqrt(...))
- Therefore, $V_{in} - V_{out} = V_{GS}$ is *nearly* constant (see later)
- The small signal gain is close to 1

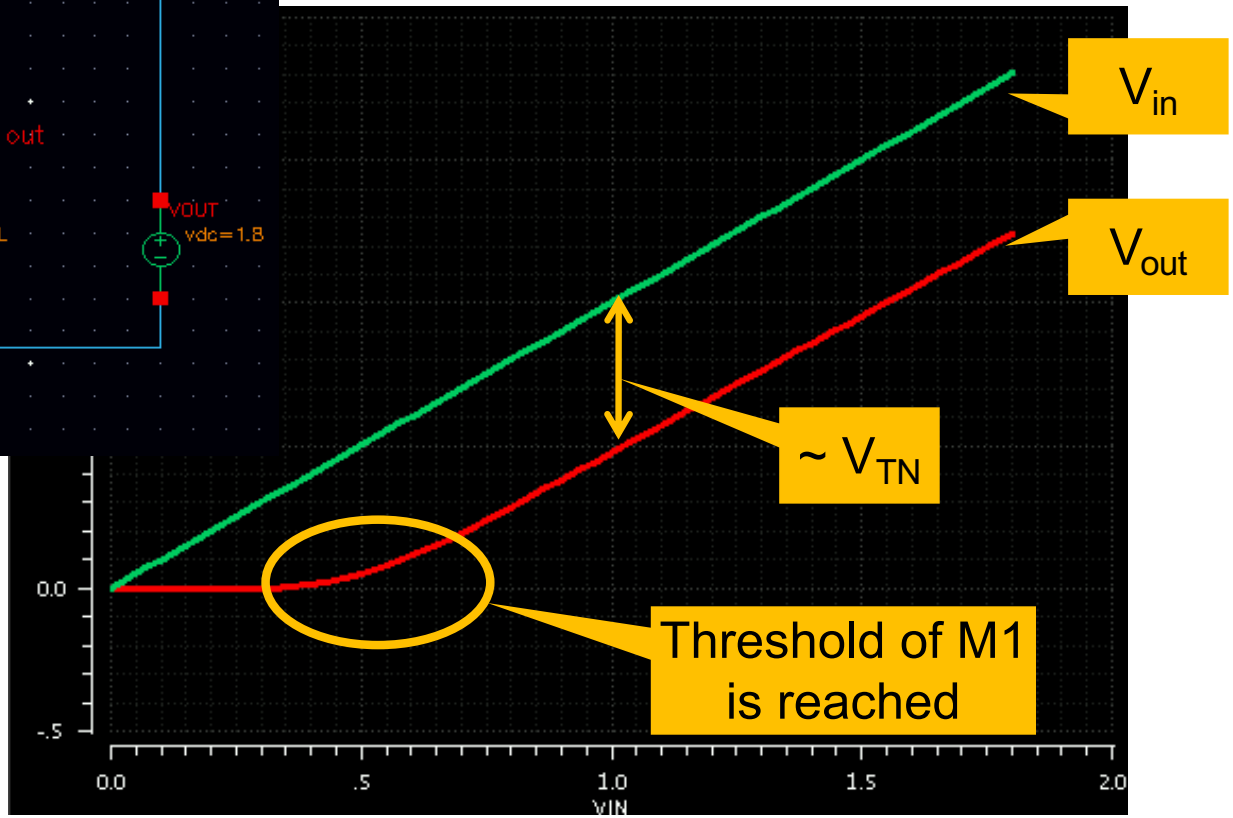
$$V_{out} \sim V_{in} - \text{constant} \rightarrow v_{out} \sim v_{in} \rightarrow g = v_{out}/v_{in} \sim 1$$



Simulation

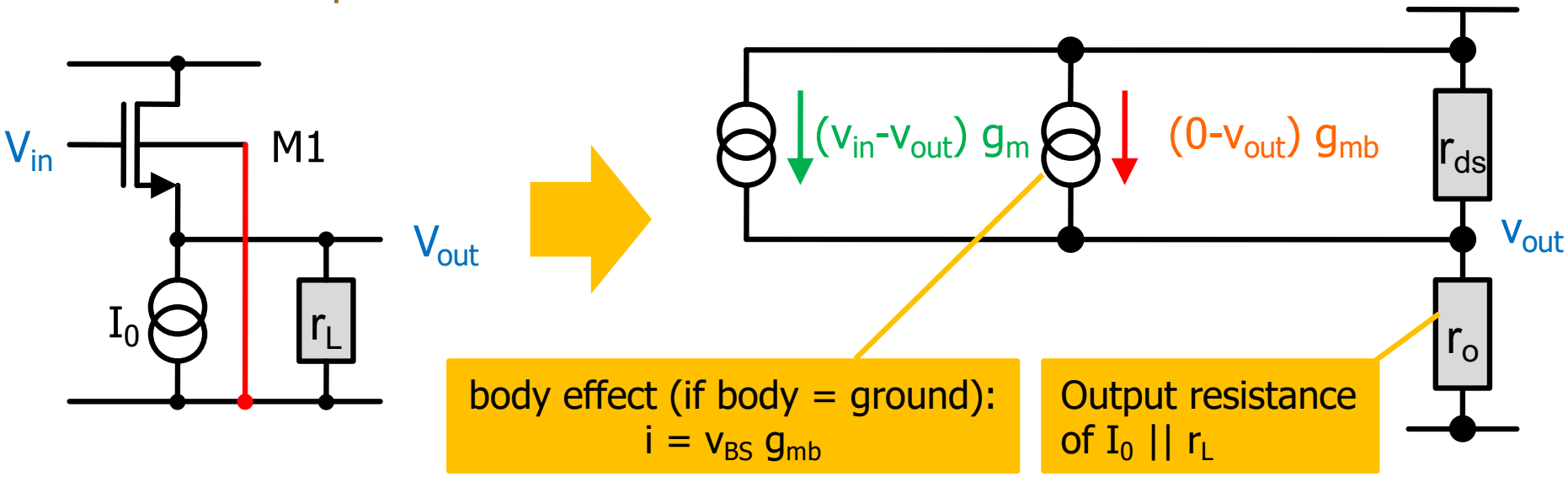
- NMOS Source Follower with NMOS current source:
  - Starts to works when Vin > $V_{T,NMOS} + V_{DSat,Source}$





Real Source Follower (Here *with* substrate effect)

- In reality, we must consider
  - r_{ds} of M1
  - the body effect of M1 (if $V_B \neq V_S$)
  - the finite output resistance of I_0
  - a possible load resistor



$$(vin - vout)\ gm + (0 - vout)\ gmb + \frac{(0 - vout)}{rds} == \frac{vout}{ro}$$

Real Source Follower (Here *with* substrate effect)

- DC Gain:

$$\text{gain} = \frac{gm}{gds + gm + gmb + go}$$

  - With $g_{ds} = 1 / r_{ds}$, $g_o = 1/r_0 + 1/R_L$

- Gain is *always* ≤ 1.
  - With body effect (remember: $g_{mb} = (n-1)\, g_m$), gain ~ 1/n ~ 0.7.
    Try to avoid body effect → PMOS in well or triple well NMOS
  - A load resistance R_L (→ g_o) lowers the gain.
    The SF cannot drive resistive loads well.
  - Output resistance of I_0 can be improved by long MOS or cascode.

- In transient situations, the NMOS SF can *source* a large current but can *sink* only I_0.

Source Follower with g=1 ?

- From $g = \frac{gm}{gds + gi + gm + gmb}$ we see that we approach g=1 with

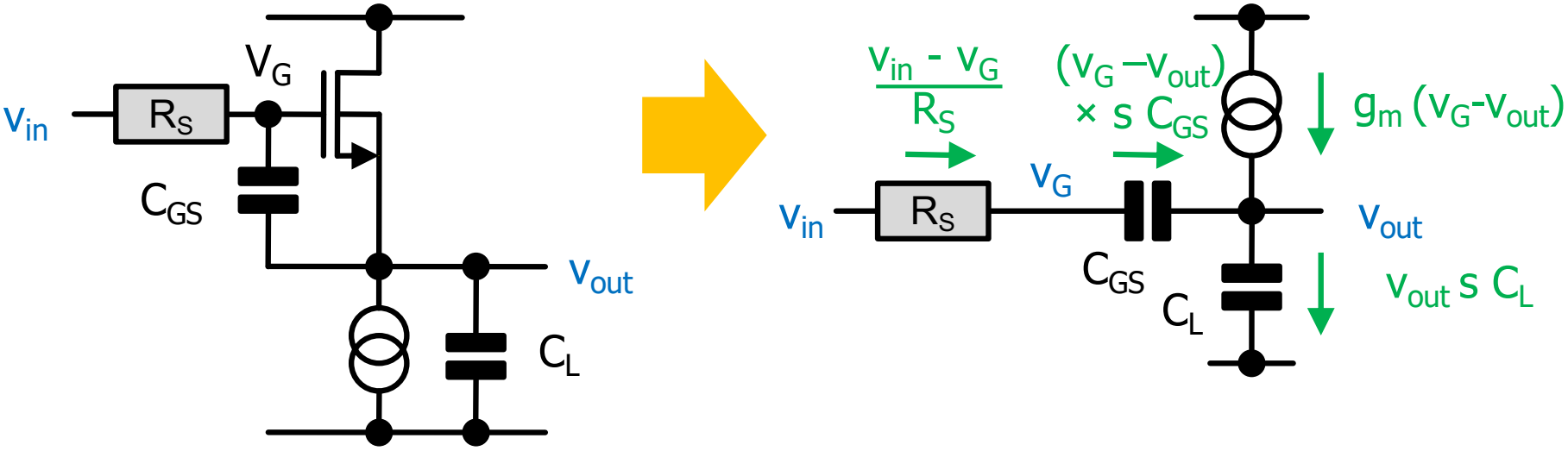
  - gmb = 0 → connect bulk an source of M1. This is often not possible for NMOS (bulk = substrate = ground)
  - gi = 0 → Make a good current source:
    - long MOS
    - Cascode, …

    This will lead to higher V_{DSat} so that SF works ‚later'
  - gds = 0 → Hard.
    - Longer MOS helps, but gm suffers (ratio does not increase quickly, speed suffers)
    - Cascode not possible because we change source!

Advanced: Source Follower with finite source imp.

For instance a gain stage

- Consider the case when the SF is driven by a ‚high impedance' source (with output resistance R_S):
  - Take into account the Gate-Source cap. C_{GS} and output cap. C_L
  - We neglect output impedances and g_{mb} for simplicity...



- Solving the current equations at the two nodes v_G and v_{out} yields the transfer function v_{out}/v_{in} :

$$\frac{gm + Cgs\, s}{gm + s\,(Cgs + CL + Cgs\, CL\, RS\, s)}$$

Analysis

- This Transfer function has two poles (denom. 2nd order in s)

$$\frac{gm + Cgs\ s}{gm + s\,(Cgs + CL + Cgs\ CL\ RS\ s)}$$

- The two poles are at $-\frac{Cgs + CL + \sqrt{(Cgs + CL)^2 - 4\ Cgs\ CL\ gm\ RS}}{2\ Cgs\ CL\ RS}$

- They become complex if the root is negative. This is at

$$RS \to \frac{(Cgs + CL)^2}{4\ Cgs\ CL\ gm}$$

- There can be an *Overshoot* if R_S is *larger* than this value
- Worst case (smallest RS) is for $C_{gs} = C_L$.
  Then the limit is at RS = $1/g_m$

Analysis

- This Transfer function has two poles (denom. 2nd order in s)

$$\frac{gm + Cgs\, s}{gm + s\,(Cgs + CL + Cgs\, CL\, RS\, s)}$$

- The two poles are at $-\dfrac{Cgs + CL + \sqrt{(Cgs + CL)^2 - 4\, Cgs\, CL\, gm\, RS}}{2\, Cgs\, CL\, RS}$

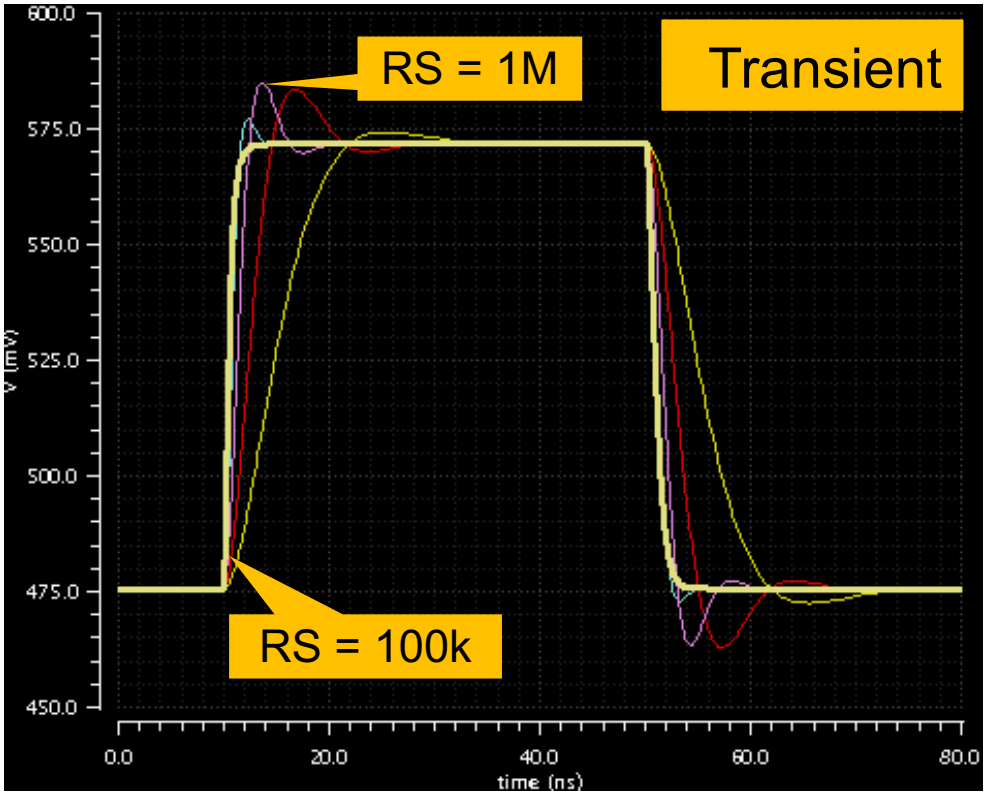
- They become complex if the root is negative. This is at

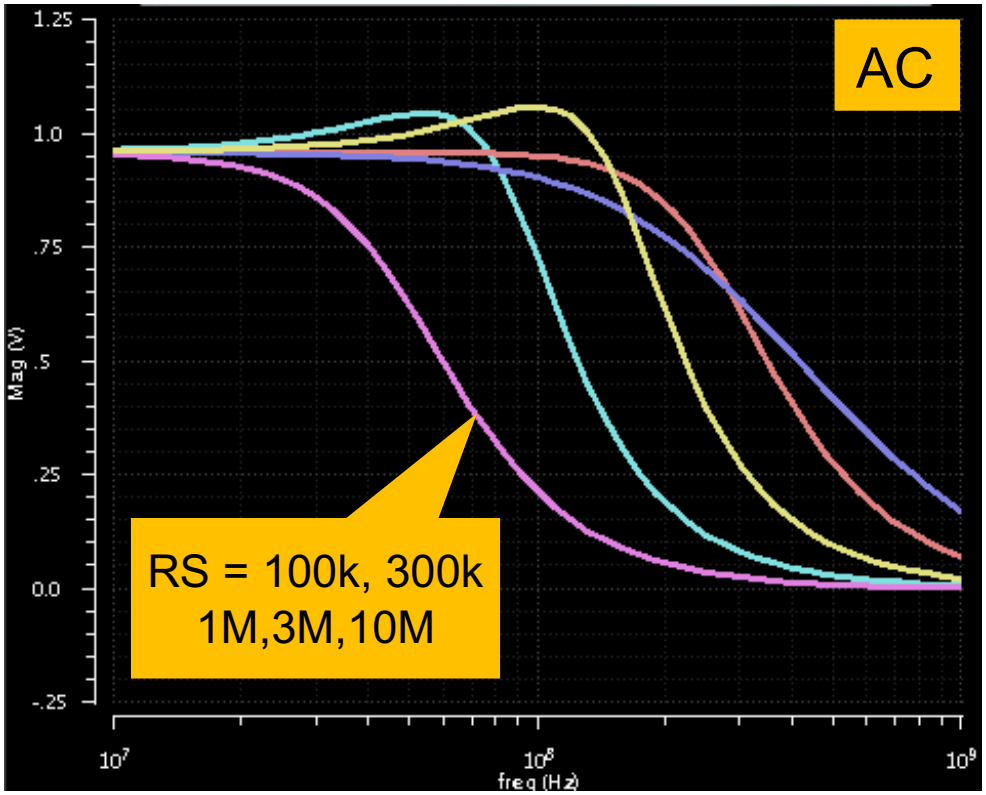
$$RS \rightarrow \frac{(Cgs + CL)^2}{4\, Cgs\, CL\, gm}$$

- There can be an *Overshoot* if R_S is *larger* than this value

Simulation

- 180nm Technology, W/L = 1µ/0.18µ, C_L = 100fF, I_{bias} = 10µA

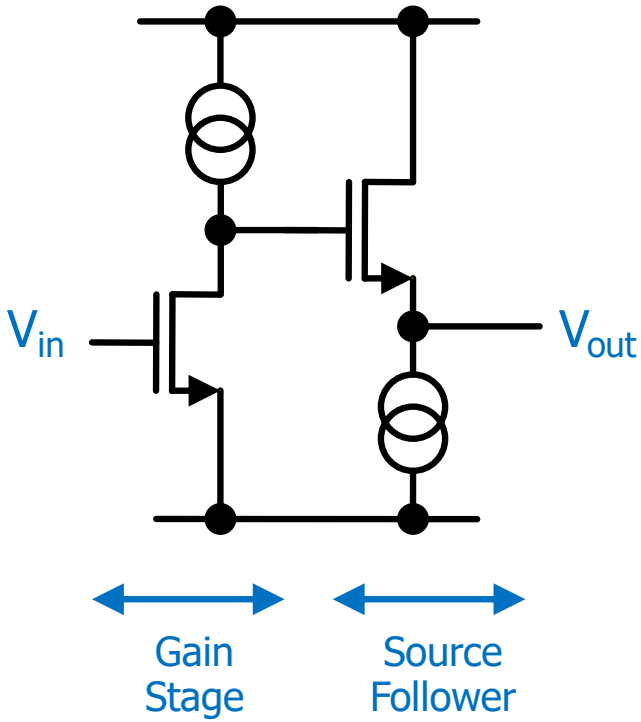




- Therefore remember:
  Source Followers driving capacitive loads are ***dangerous***!

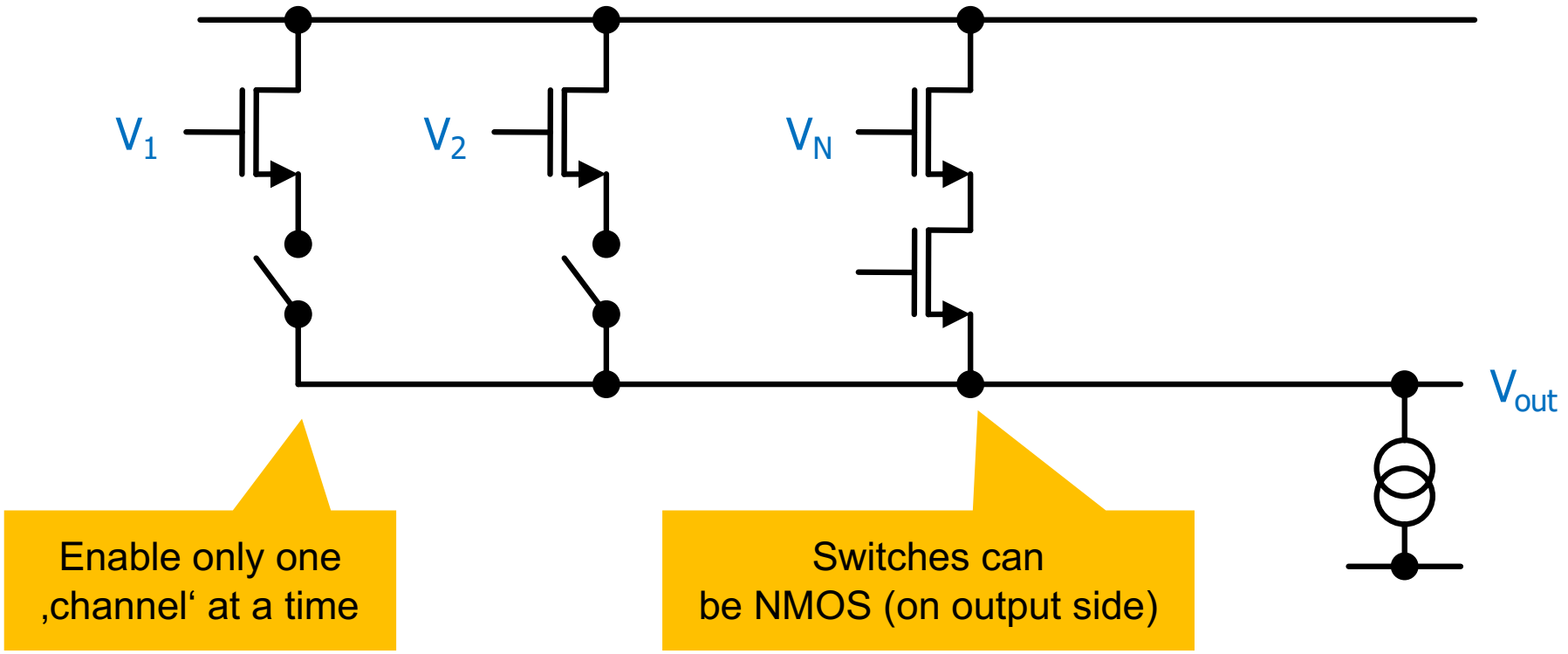
What for?

- The Source Follower has a low output impedance ($1/g_m$)
- It can ‘drive’ low-impedance (capacitive) loads
- Gain drops ‘only a bit’
  - gain of a gain stage drops ‘a lot’ with resistive loads
- Often used in combination with a gain stage:



Special Application

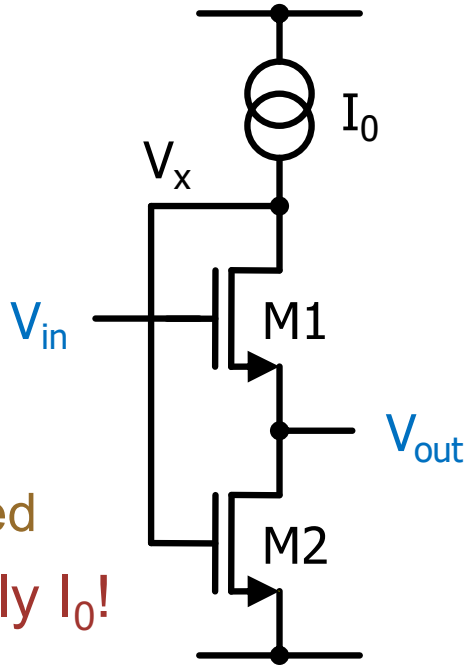
- SF be used to ‚send' a voltage
- Multiple Source Followers can be combined:



Advanced Followers

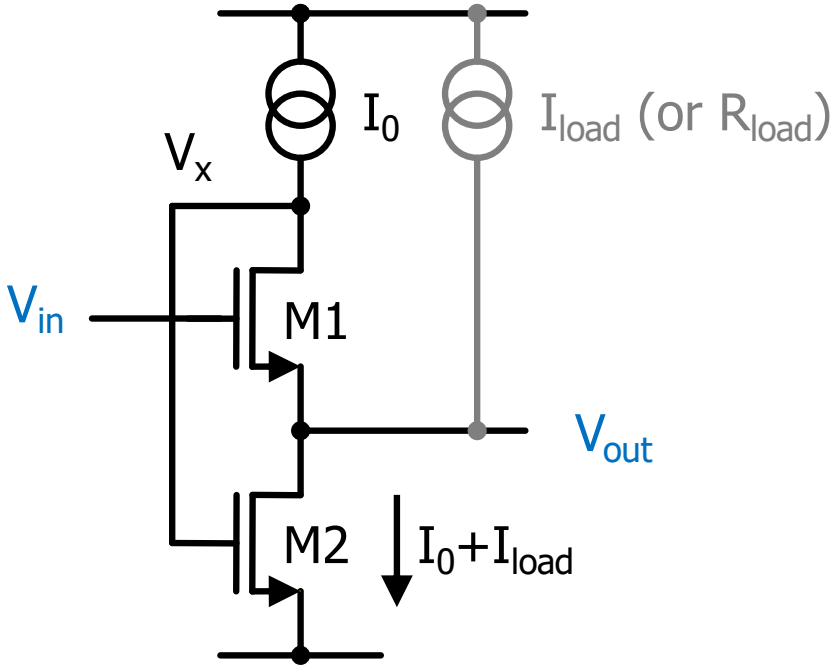
The 'Flipped Voltage Follower' (FVF)

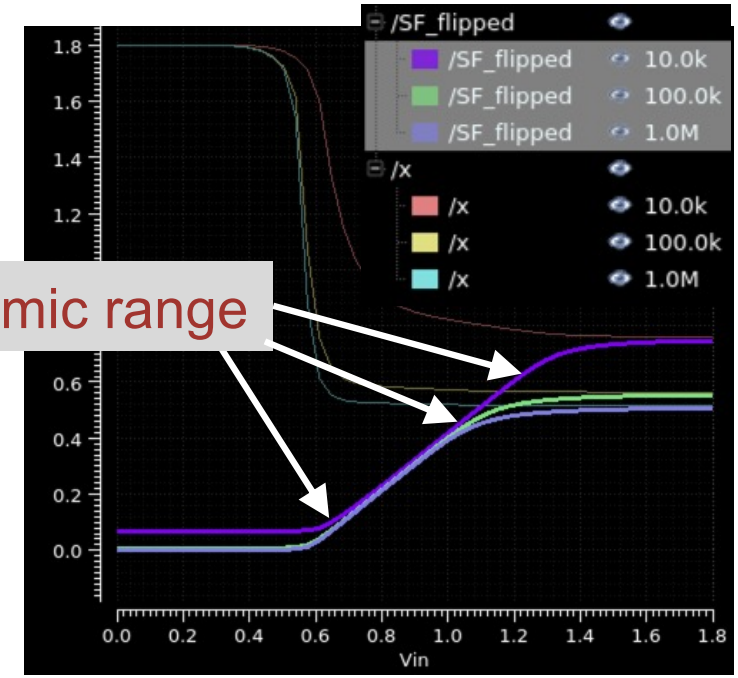
- A VERY clever and tricky circuit!
- V_{out} 'follows' V_{in} (as with normal SF), but
  - gain is much closer to 1, in particular for resistive load
  - Output impedance is much lower
- The current I_{M1} through M1 is always I_0, *independent* of load current → V_{GS1} of M1 is constant → g is closer to 1
- Regulation:
  - Assume V_{out} raises
  - V_{GS1} drops
  - I_{M1} drops
  - More current flows into node x than out of x
  - $V_x = V_{GS2}$ rises
  - I_{M2} rises, pulling V_{out} low until V_{in}-V_{out} is restored
- FVF can *sink* a lot of current and *source* only I_0!
- Very clever!



Biassing Issue of the FVF

- Assuming no load current:
  - $V_x = V_{GS2}$ is fixed by I_0. It is relatively 'low': $V_{TN}+\sqrt{\ldots}$
  - When V_{in} becomes too positive, the drain voltage of M1 becomes too low. The circuit stops working.
  - Input voltage range is *increased* with (positive!) load current Because more current flows in M2 and Vx rises!

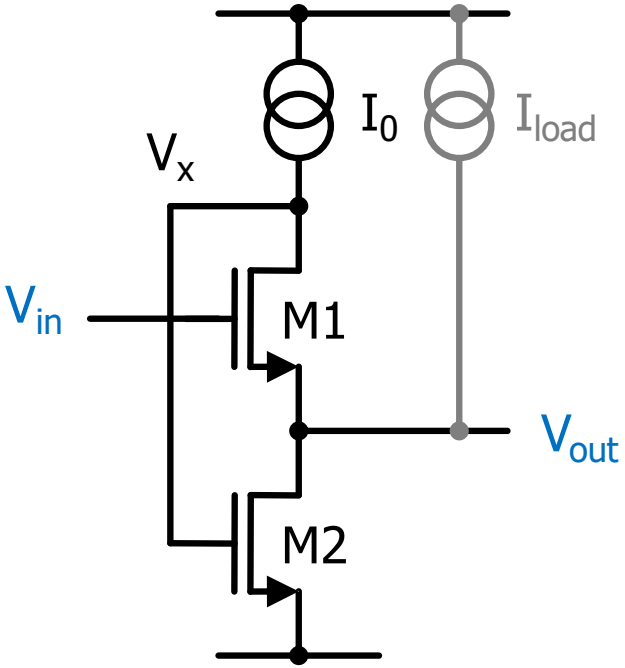


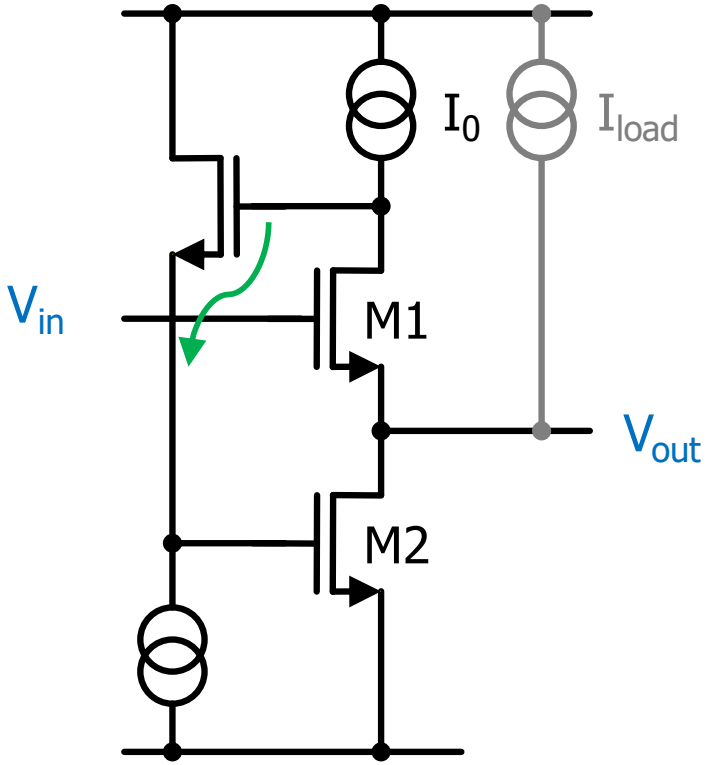


I_0 = 10uA, R_{load} = 10/100/1000 k

Improvement – With Level Shifter

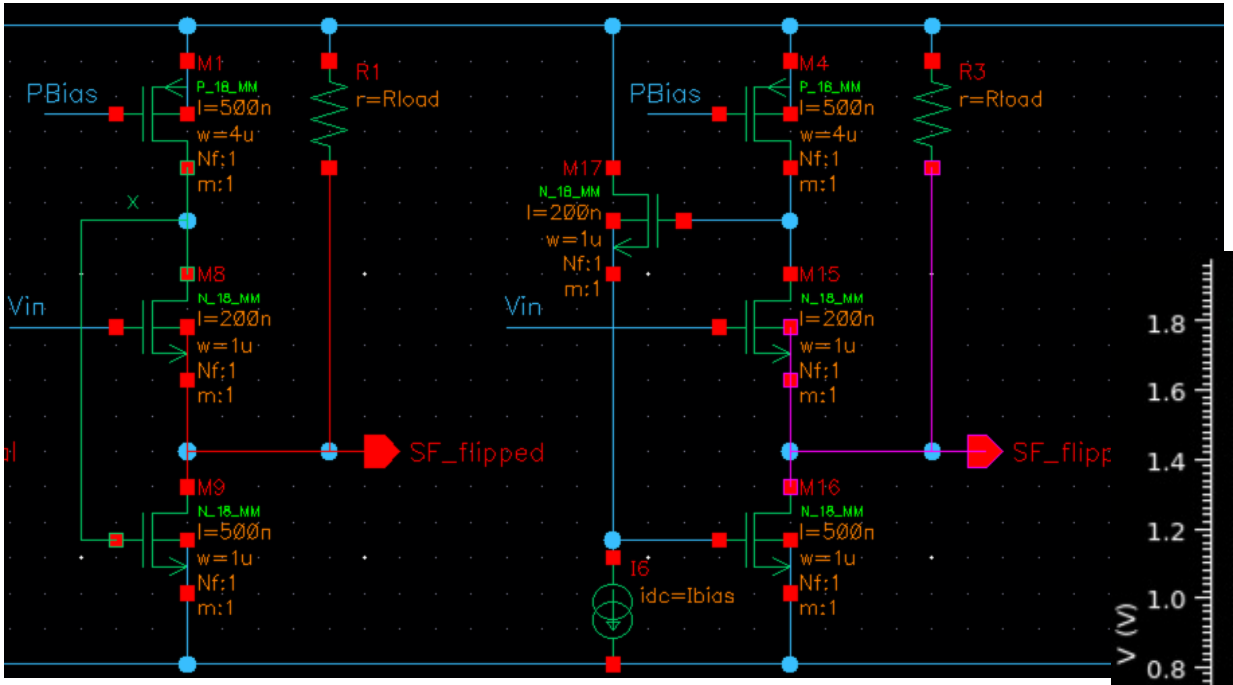
- The saturation issue can be reduced by shifting voltage x with a 'normal' source follower:

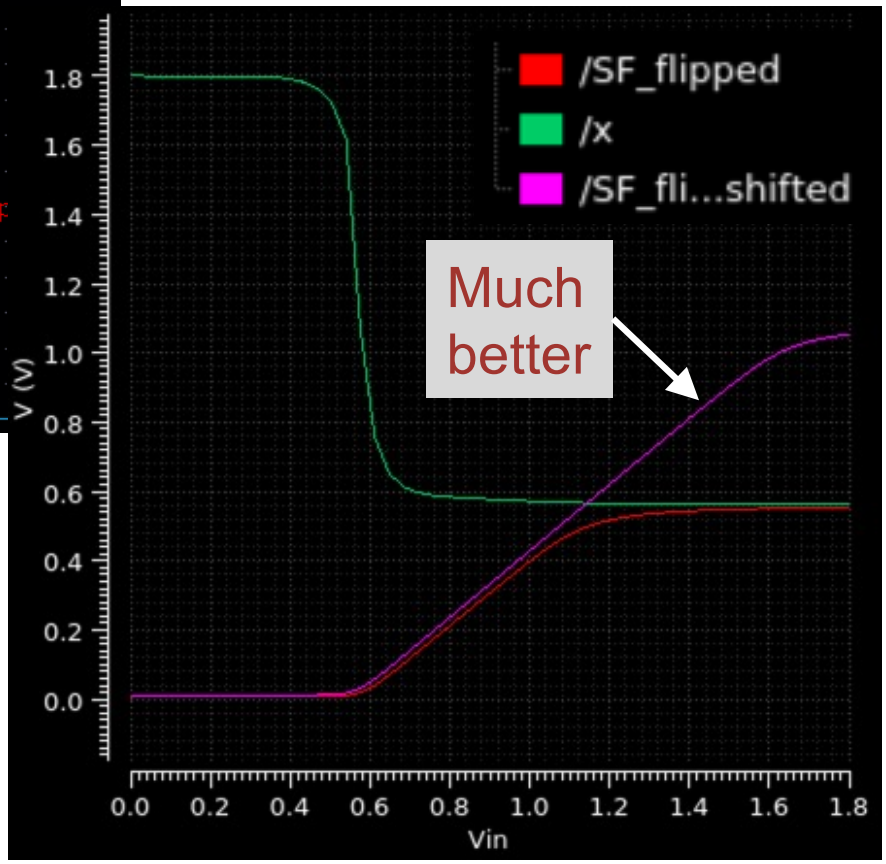




- If we have an MOS with high threshold, this helps for M2!

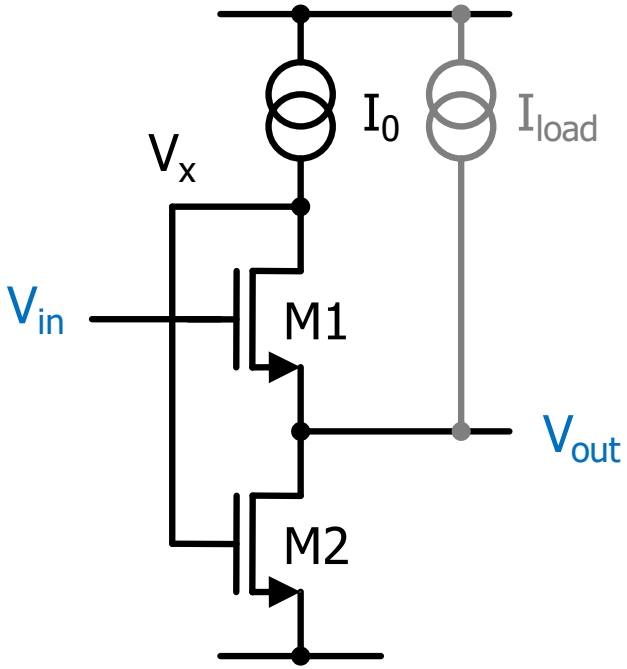
Simulation of improved version

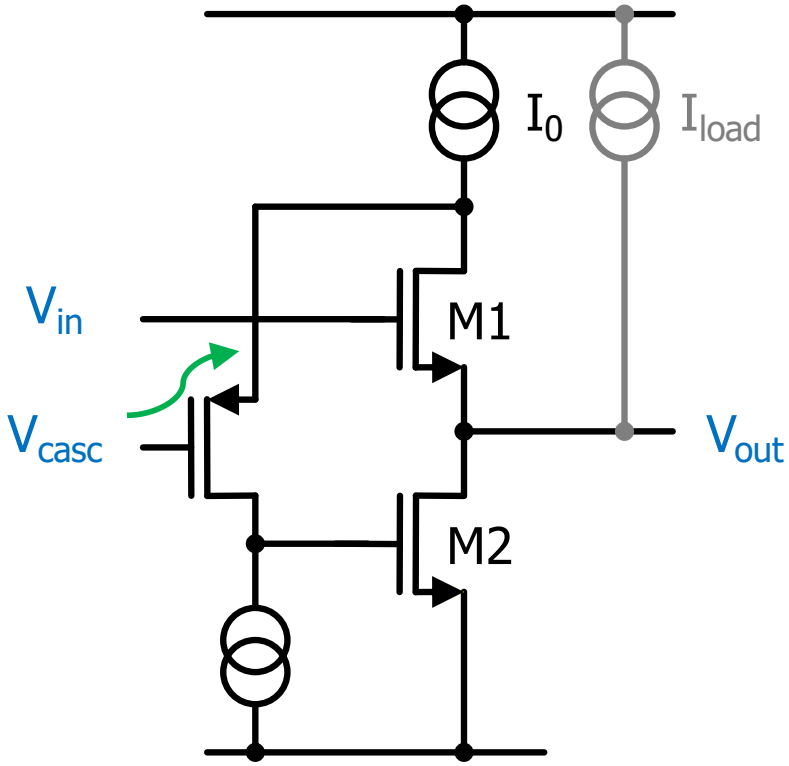




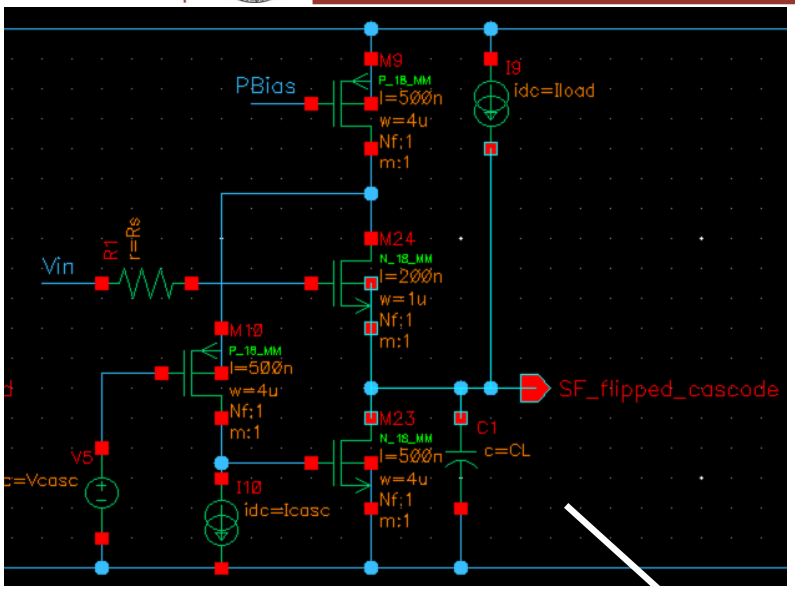
Improvement – With Cascode

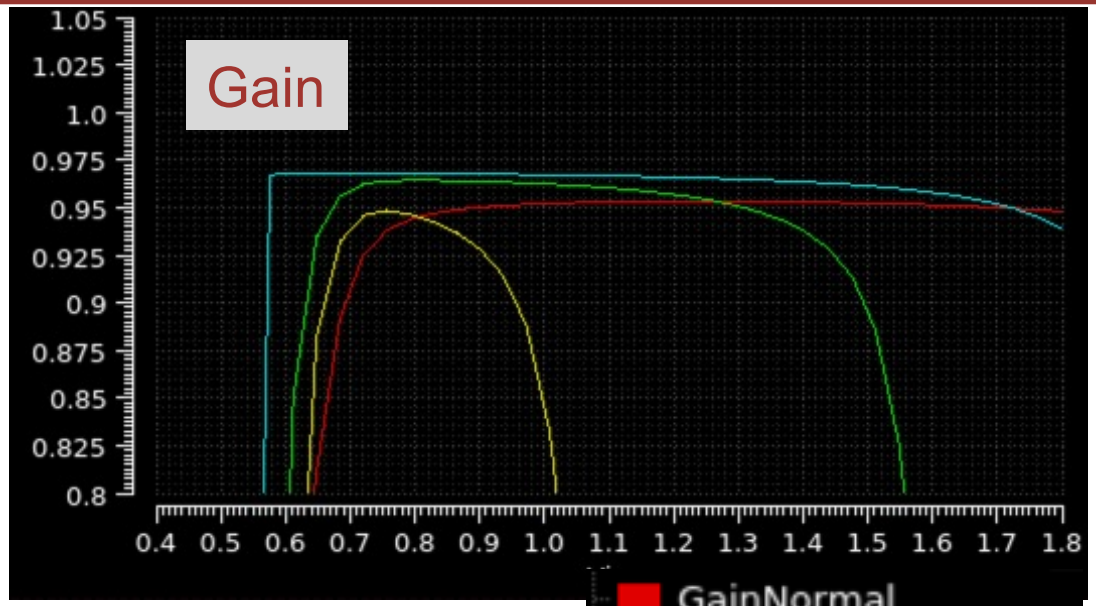
- We can also separate V_x from the gate of M2 and force V_x to a voltage with a PMOS cascode
  - Choose V_{casc} such that I_0 is just saturated for max. dyn. range

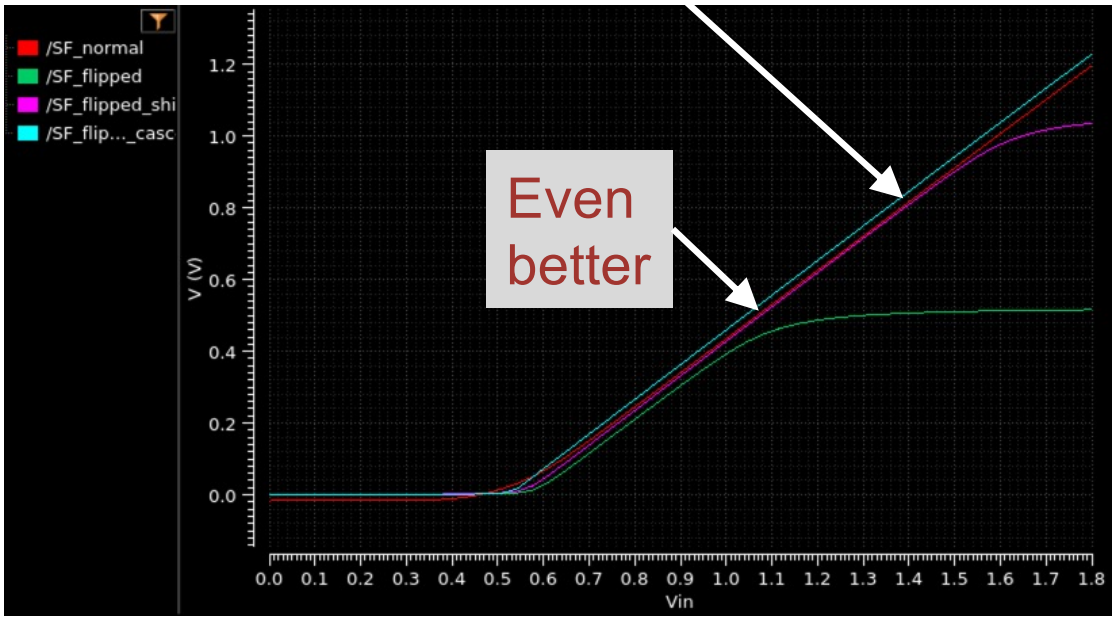




Simulation of Cascode Version



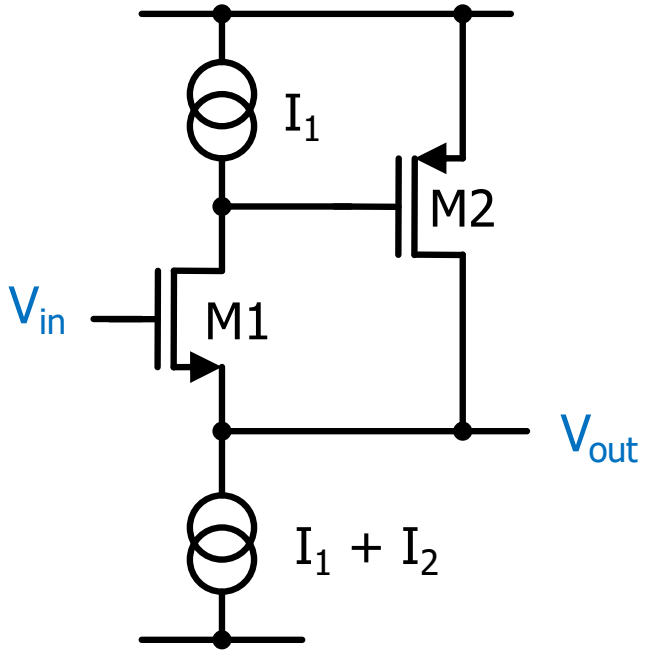




- Gain above is *without* load resistor and *without* substrate effect
- Limited by output resistances.

‘Super Source Follower’

- The ‘Super Source Follower’ is another circuit which keeps the current in M1 independent of the load current by providing a second current source (M2) for the load:



Back to the Normal SF

- For V_{BS}=0, no RL, and a 'good' current source, the gain of the 'normal' SF is limited by the Early effects in M1.

$$gain = \frac{gm}{gds + gm + \cancel{gmb} + \cancel{go}}$$

- The 'problem' is that V_{ds} of M1 changes with V_{out}
- Can we avoid that ? Yes!
  We 'cascode' the source to a voltage that follows V_{out}: