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Exercise 3:
Advances Nets & Multiple Instances

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Exercise 3A: Inverter Chain – Setting Up

- Create schematic and symbol of an Inverter
  - Use a minimum size NMOS and a PMOS with minimal length and parameterized width WP
  - Use global nets vddd! and gndd! for the circuit
  - Connect the substrate of the NMOS to global gnd!
  - Connect the well of the PMOS to vddd!
- Simulate the schematic in a new view
  - Connect gnd! to gndd! with a 0 Ω resistor or with a DC source with 0 V.
  - Provide vddd! of 1.8 V
  - Load the circuit with 100 fF or so
  - Provide a square wave input
  - Label your nets 'in' and 'out'
  - Chose WP such that rise and fall times are roughly equal. Use a parametric simulation!
  - Save the simulation state to the cell

Exercise 3A: Inverter Chain – The Chain

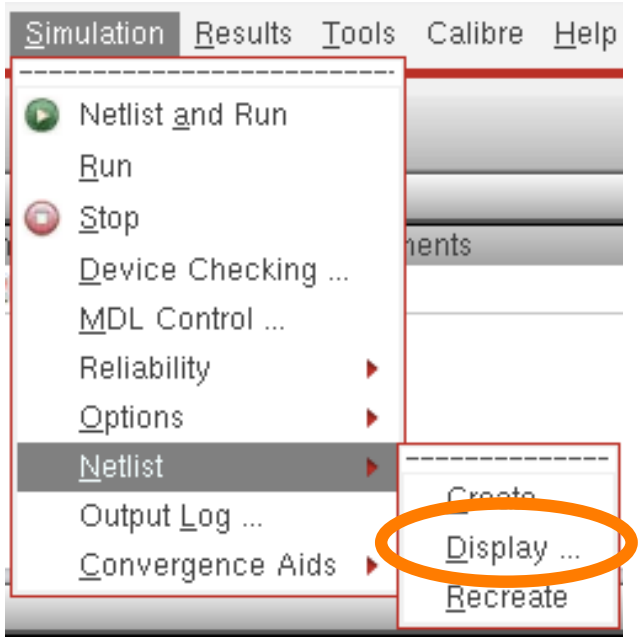
- Copy the simulation cell (incl. state) to a new schematic
- Change the schematic so that it contains a chain of 11 inverters. Use advanced nets and multiple instances
  - instantiate you inverters as Iinv<10:0>
  - Decide which inverter is the first in the chain.
  - Find out how to connect the inverter, and how to add the 'in' and 'out' nets
  - Note: You are not allowed to use the same name for signle nets ('out') and busses ('out<10:1>)
- Reduce the load capacitor to 1 fF
- Find out the delay between the input 'in' and the output of the last inverter 'out'.
  - Use the available state to start with
- For your understanding: Change the order of the chain, i.e. make the 'other' inverter the first in the chain. Change the signal naming correspondingly.

Exercise 3A: Inverter Chain – An Oscillator

- You can create a 'RING OSCILLATOR' by connecting the output of the chain to the input (remove the source!)

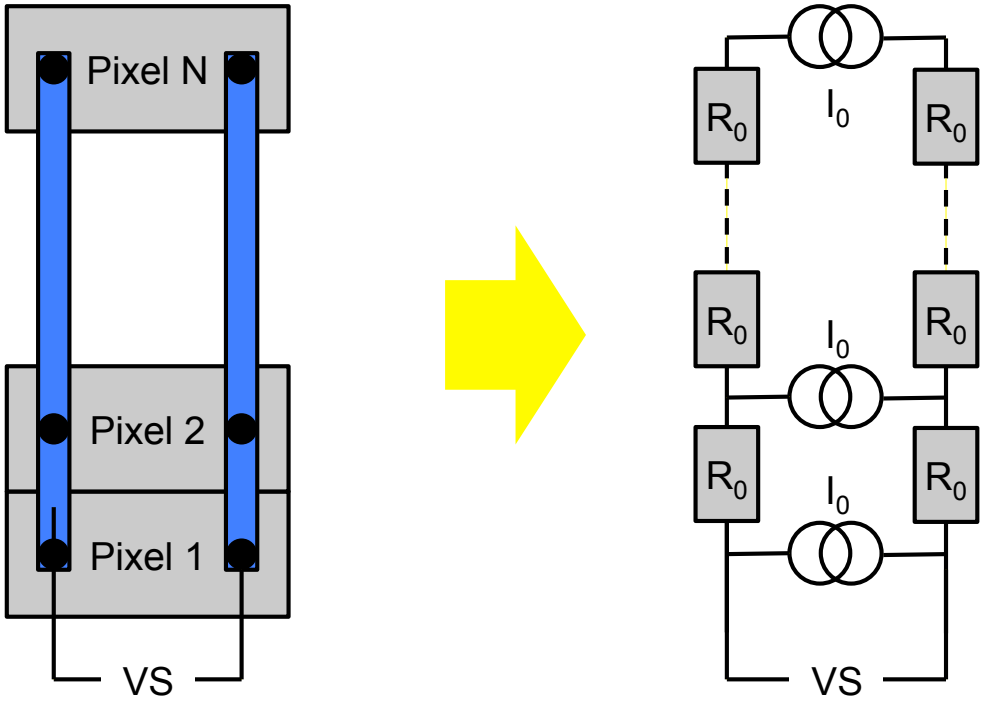
- Try to simulate this
  - you will probably see a constant level between 0V and 1.8V
  - Make sure the oscillation starts by setting an initial condition of 0V or 1.8V to the 1 fF capacitor at the output
- What is the oscillation frequency?
  Do you understand how this works?

- Have a look at the simulation netlist



Exercise 3B: Voltage Drop in a Large Chip

- A (Pixel) chip consist of N identical circuits in a column
- The pixels are powered by vertical metal traces
- Each pixel consumes a current I_0
- The trace resistance between two cells is R_0 (both supplies)
- ONLY the lowermost Pixel 1 is connected to a supply VS.



Exercise 3B: Voltage Drop

- Due to the voltage drop in the R_0s, the local supply voltages V_i become smaller and smaller from pixel 1 to pixel N

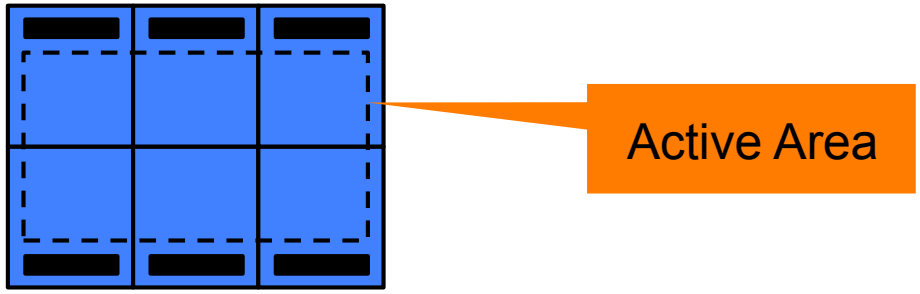
- Calculate the V_i analytically.
  - Hint: calculate the current in each resistor
  - Derive the voltage drop in each resistor
  - Sum up the drops from 1 to N.
- How much has the supply dropped at the topmost pixel?

- Now simulate the structure and confirm your analytical result for N=100, R_0=1Ω, I_0=100µA, VS=2V.
  - Obviously, you should usean 'advanced' schematic….

Exercise 3B: Are you clever ?

- What happens when the topmost pixel N is also connected to VS
  - Where is the largest voltage drop now?
  - How large is it (roughly)?
  - Surprised? Do you understand why?

- Note: Pixel chips usually have connections only on one side, so that many chips can be placed side-by-side to form a larger module.



- Voltage drop is a serious issue which cannot be avoid. Pixel circuitry must be able to 'live with it'