



Exercise 8: CAM – Part 3: RAM Sense Amplifier

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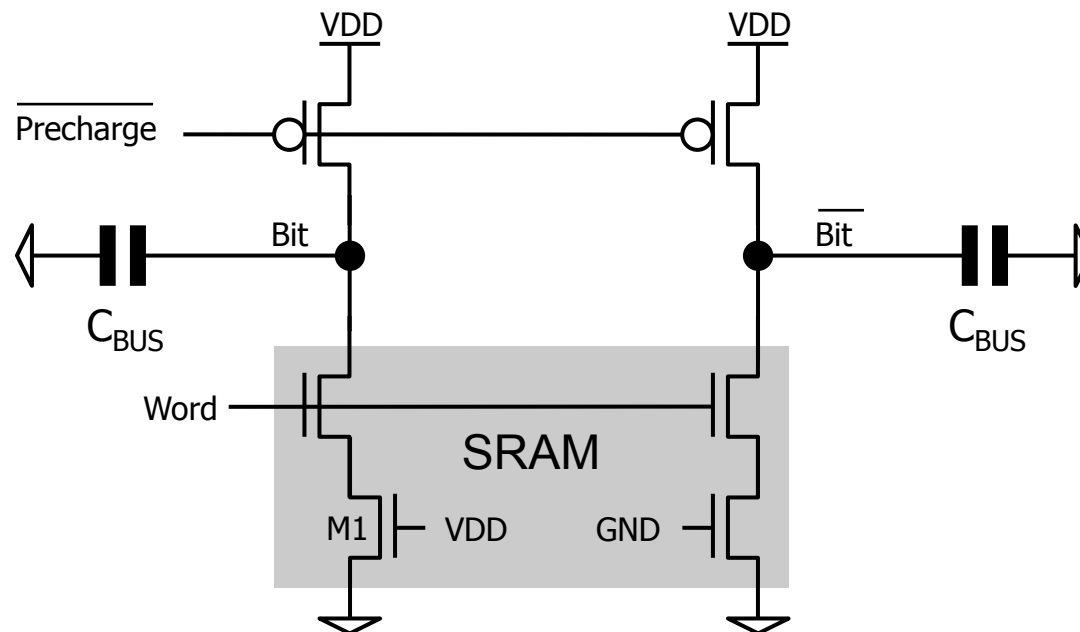
Decision Speed

- We deal here with 'normal' reading of the SRAM cells (not with CAM decision making)
- So far, the NMOSs in the SRAM cell must discharge the **Bit/BitB** busses down to the threshold of the following logic, i.e. by roughly $V_{DD}/2$.
- When many rows are connected, the **Bit/BitB** capacitance becomes large and the discharge is slow.



Simplified Simulation

- To simulate, we simplify to the minimum:
 - A 'SRAM cell' set to a fixed value
 - We add additional bus capacitance of, say, $C_{BUS} = 5\text{pF}$

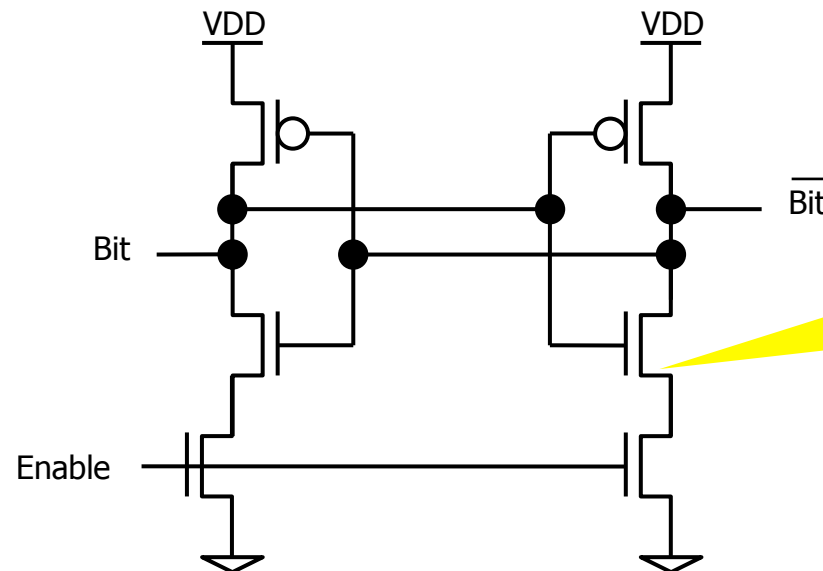


- Simulate how long it takes to discharge **Bit** to $VDD/2$.
- Is this consistent with the calculation (get the current in **M1**)?



A Sense Amplifier

- Add a 'sense amplifier' which consists of a cross coupled inverter pair which can be turned on/off:
 - When enable = 0, the circuit is inactive
 - When enable = 1, *one side* is pulled low (the other is *pulled up*)



Dimension the NMOS/PMOS so that they are stronger than in the SRAM cell, e.g. $W=2u$

- The 'side' which is pulled low is determined by *an initial mismatch*, introduced via **Bit** and **BitN**.
- Activate the circuit shortly after you enabled the wordline
 - How much faster is the discharge on **Bit**?



Getting Rid of the Bus Capacitance

- The sense amplifier (SA) still has to discharge the full bus capacitances.

- Add a switch between the **Bit/BitB** busses and the SA and open it just when the SA is enabled.
 - Do you need a NMOS or a PMOS?
 - How does the discharge speed at the SA side change?

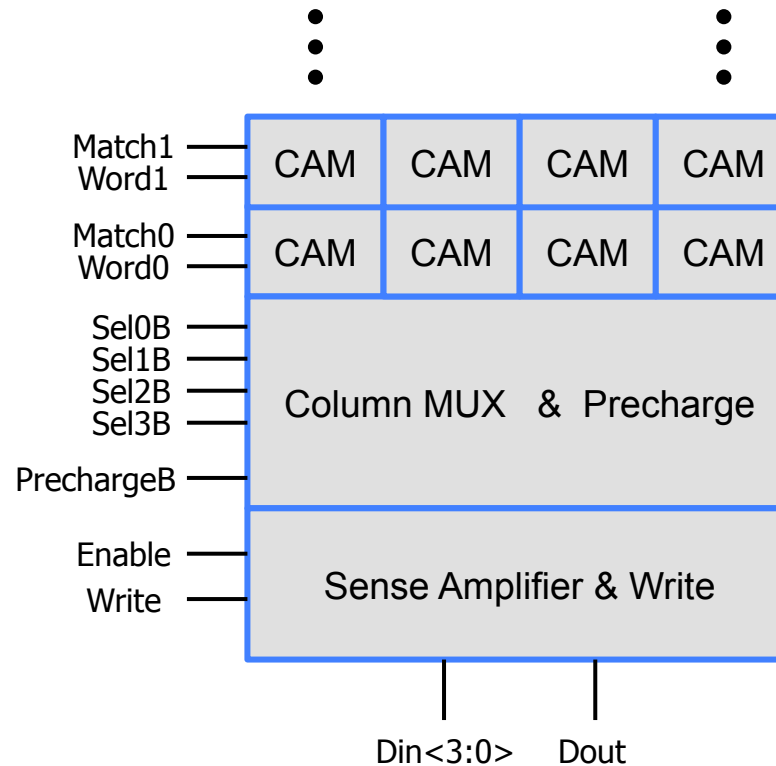
- Do NOT open (disable) the switch.
 - What happens? How do you explain that?

- Comment:
 - It is more important to have **Bit** and **BitB** be equal before evaluation than to have them at VDD. Therefore a switch shorting **Bit** and **BitB** is often used.



Column Multiplexors

- The SA is normally too large (it uses larger MOS) to fit in one SRAM column
- Therefore, several columns are *multiplexed* onto one SA
- A typical arrangement looks like this:





Putting Everything Together

- Make a schematic which has the above structure
 - Merge precharge and column-MUX
 - Think about how to merge the sense amplifier and the Write mechanism. There are many possibilities.
You could keep the write part parallel for all 4 bits

- Simulate everything

- Make a matching layout of the 3 parts