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Exercise 2:
Designing with (Schematic) Hierarchy

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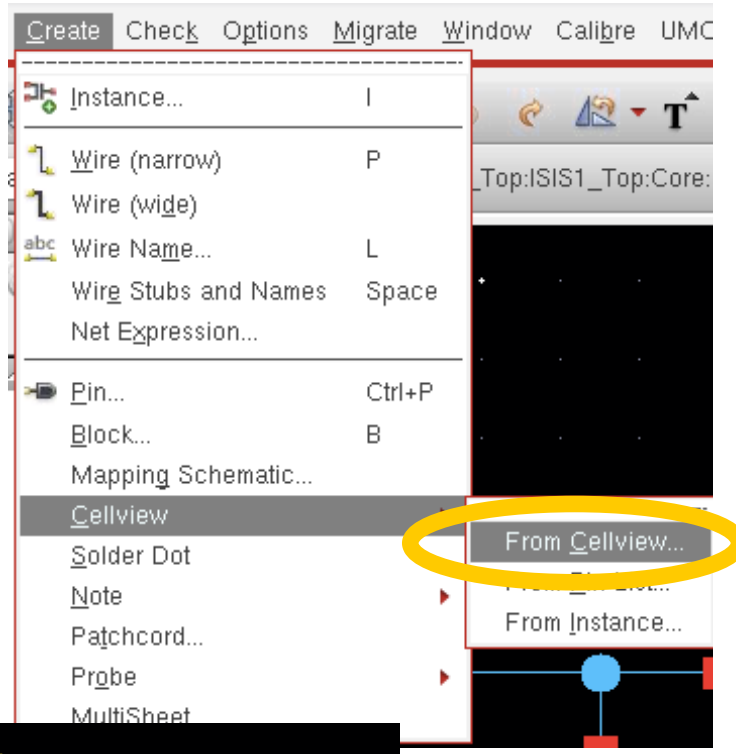
Implementation

1. You can create a *schematic* and a *symbol* view in the same *cell* independently.
   - When you save either cell, the number/names/types of the pins are checked against the other cell.

2. You can also create the 'second' view *automatically*: Create → Cellview → From CellView

- Two further forms are displayed..

- This works in both directions
  - Symbol → Schematic
  - Schematic → Symbol



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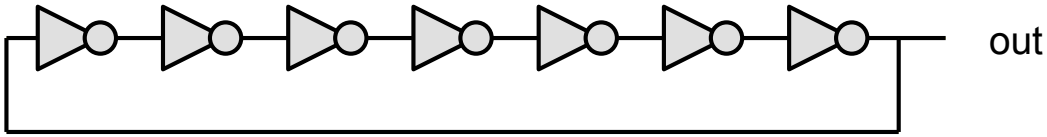
EXERCISE A: RING OSCILLATOR

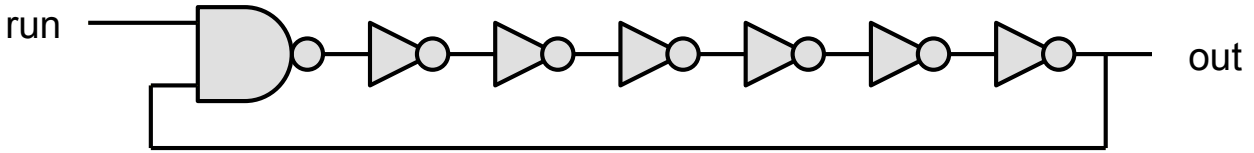
The Circuit

- A Ring Oscillator consists of a chain of N inverters connected to a ring:



- When N is odd (ungerade), the circuit oscillates
  - Understand why
  - What happens if N is even?

- To start in a well defined state, and to turn on/off the oscillator, we add a NAND2 gate:



Schematics / Symbols

- Implement such an oscillator
  - Use global power nets vddd! and gndd! and substrate gnd!

- Create 3 schematics + symbols:
  - Inverter
    - use pins **in, out**
    - use an NMOS with W/L = 0.5u/0.18u and a 3 times wider PMOS
  - Nand2
    - use pins **in1, in2, out**
    - use MOS such that the drive strength is roughly as for the inverter
  - Oscillator
    - use pins **run, out**
    - use (for instance) 10 inverters
    - use a compact notation, i.e. do NOT draw 10 inverters

Simulation

- Create another schematic SIM_RingOsc for simulation
- Instantiate
  - the oscillator
  - the power supply source (of 1.8 V)
  - a vpulse source to turn on the oscillator after 5 ns.
- Connect gnd! and gndd! with a 0V voltage source

- Does it oscillate ? What is the oscillation frequency ?
- So follow for the delay of one inverter (neglecting the NAND2)

- Change your circuit to N=50 or so and repeat.

- Such circuits are used in practice to easily measure the very small delay of an inverter or other cells