Parasitic Extraction

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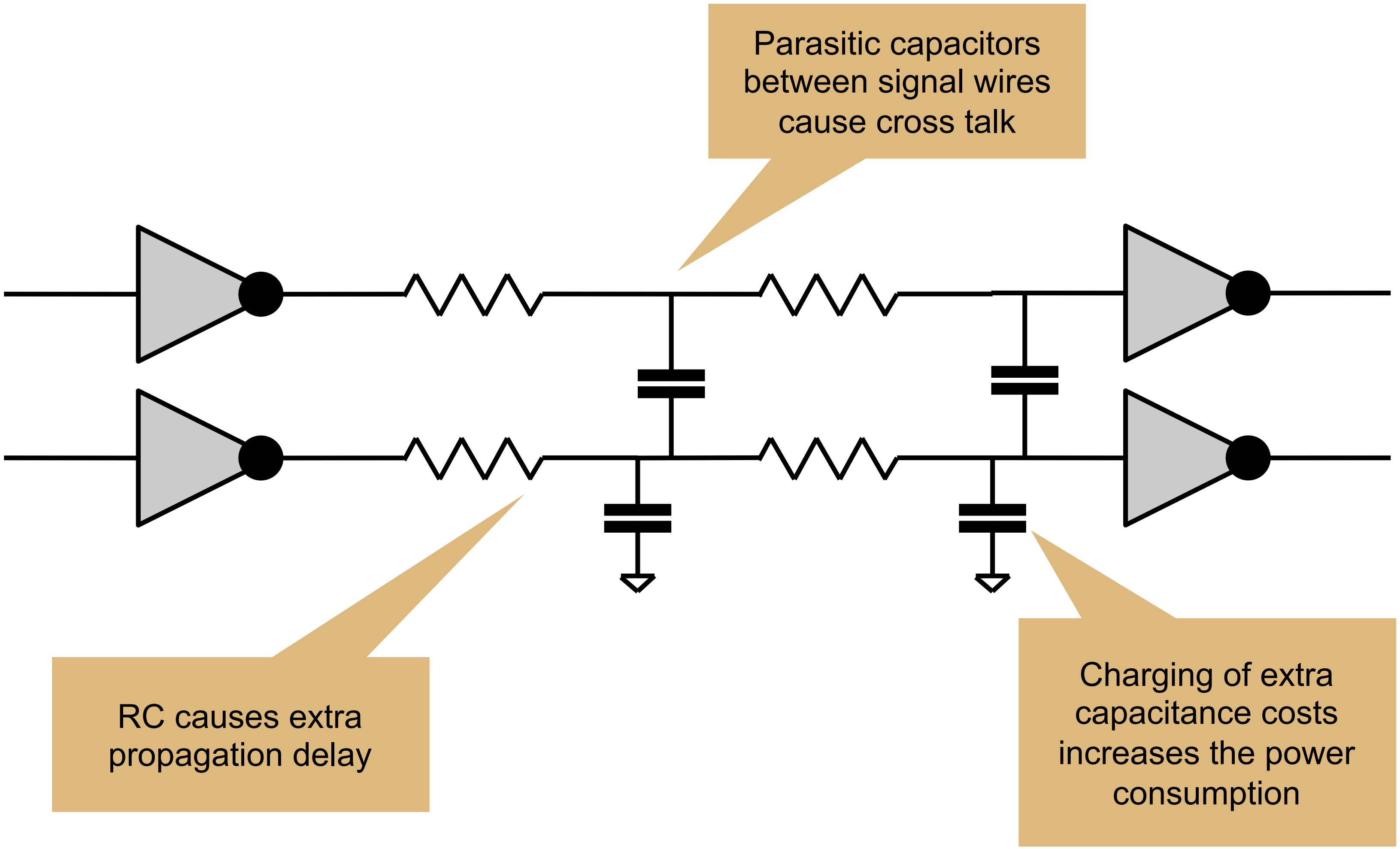
Parasitic Extraction

- **Parasitics** are ‘devices’ which are not intended but intrinsic to any physical representation of a circuit
- For instance: interconnect traces have
  - Resistance
  - Capacitance to their surrounding
  - Inductivity
- **Parasitics** → sound bothersome, and they are!
- The circuit schematic does (in first order) not include any physical layout information
  - ‘Full custom’ circuit design → usually bare schematics first
  - Digital place and route tools might use estimates already in the placement phase
- Only after the layout exact parasitics can be extracted
- Simulation with *annotated* parasitics models the circuit behavior most accurately

Effects of Parasitics in Digital Circuits

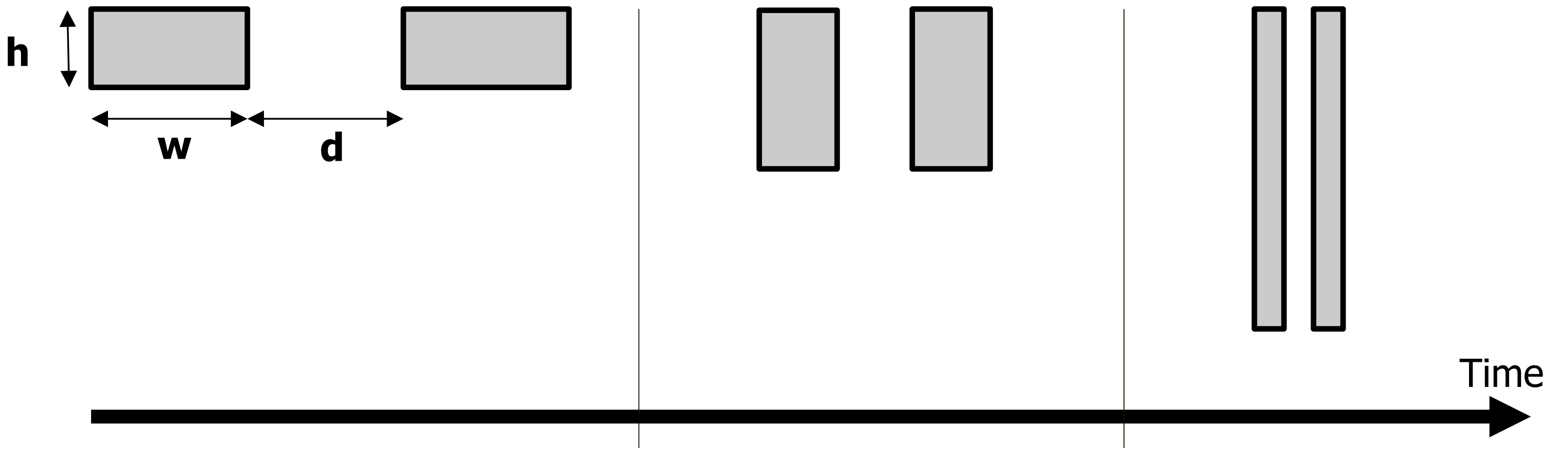


Parasitic capacitors between signal wires cause cross talk

RC causes extra propagation delay

Charging of extra capacitance costs increases the power consumption

Relevance of Parasitics



Technology Evolution:

- Decreasing interconnect feature size increases parasitics
  - d ↓ → C_{side} ↑ (C ~ 1/d)
  - w ↓ → $C_{up,down}$ ↓
  - Aspect ratios (h/w) ↑ → trying to keep R const,
  - h ↑ → C_{side} ↑ ↑
- Decreasing transistor feature size → weaker drivers
- → **Parasitics become more relevant** (can even become dominant) as **feature sizes shrink**

Parasitic Extraction Tutorial

Overview / Requirements

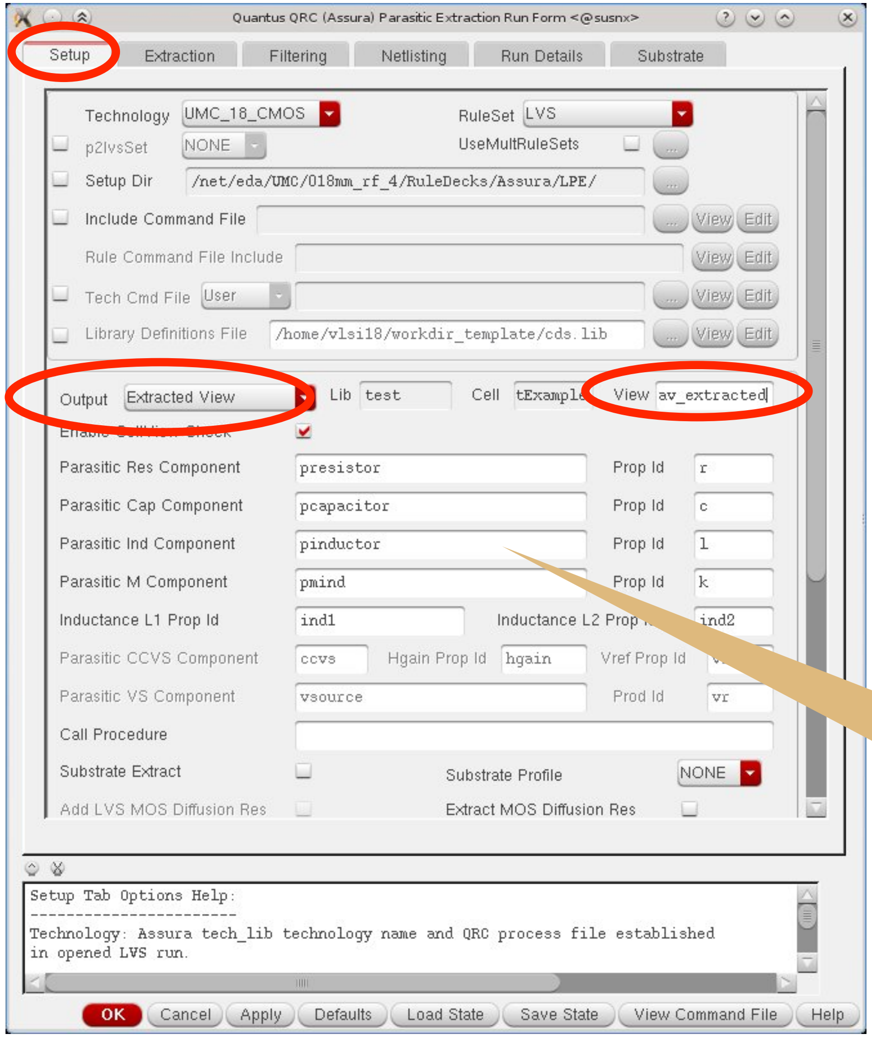
- This tutorial shows how to:
  - Run different extraction types
  - Analyze the results
  - Simulate with extracted parasitics

- We will use the tool ASSURA QRC
- Required inputs are:
  - A schematic view
  - A layout view (a ‘standalone’ layout view cannot be extracted)
  - A **clean** LVS

- Open the layout to extract and run an LVS or open an existing LVS result (Assura → Open Run)

Extraction Setup

- Now select: QRC → Run Assura – Quantus QRC…



Quantus QRC (Assura) Parasitic Extraction Run Form <@susnx>

Technology: UMC_18_CMOS RuleSet: LVS

□ p2lvsSet: NONE UseMultRuleSets □

□ Setup Dir: /net/eda/UMC/018mm_rf_4/RuleDecks/Assura/LPE/

□ Include Command File:

Rule Command File Include:

□ Tech Cmd File: User

□ Library Definitions File: /home/vlsi18/workdir_template/cds.lib

Output: Extracted View Lib: test Cell: tExample View: av_extracted

Enable Collision Check ☑

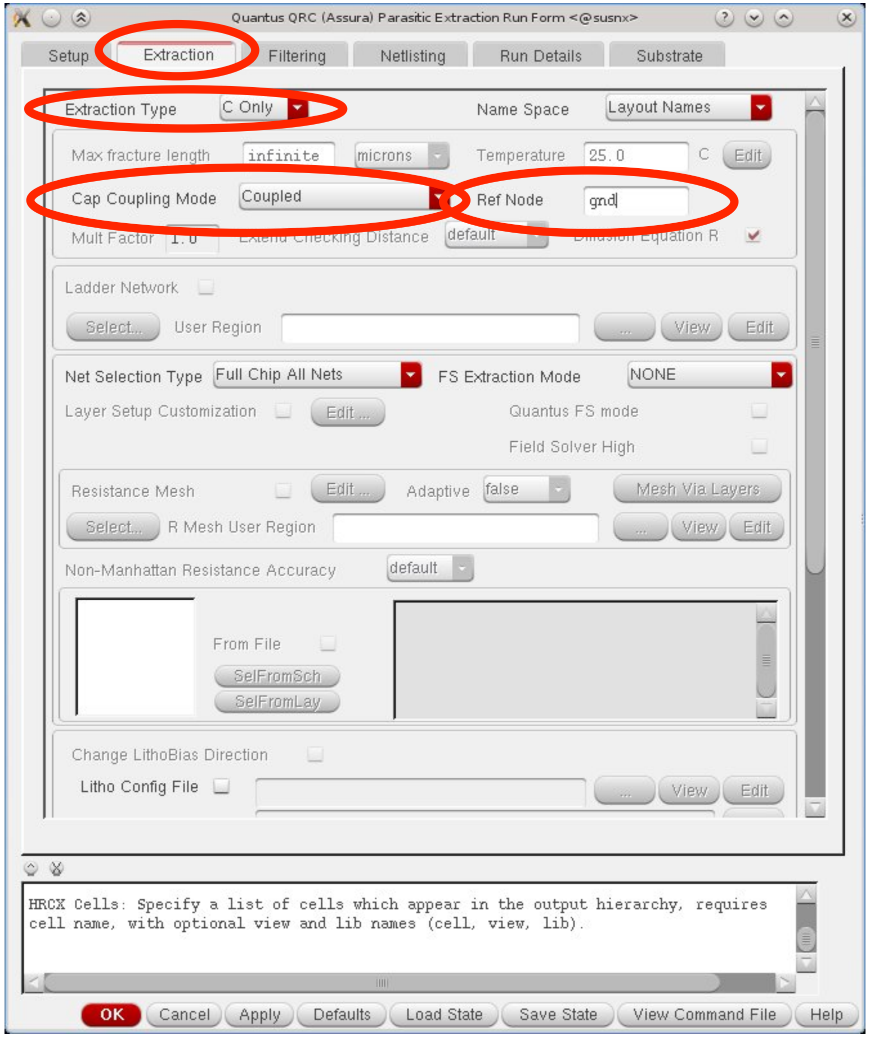
Parasitic Res Component	presistor	Prop Id	r
Parasitic Cap Component	pcapacitor	Prop Id	c
Parasitic Ind Component	pinductor	Prop Id	l
Parasitic M Component	pmind	Prop Id	k
Inductance L1 Prop Id	ind1	Inductance L2 Prop Id	ind2
Parasitic CCVS Component	ccvs Hgain Prop Id: hgain	Vref Prop Id	
Parasitic VS Component	vsource	Prod Id	vr
Call Procedure			
Substrate Extract	□	Substrate Profile	NONE
Add LVS MOS Diffusion Res	□	Extract MOS Diffusion Res	□

```
Setup Tab Options Help:
------------------------
Technology: Assura tech_lib technology name and QRC process file established
in opened LVS run.
```

- We will use the default output type 'Extracted View'
- The 'Extracted View' can be analyzed with the GUI and is most illustrative for the tutorial
- Other output view types are possible, e.g.:
  - Netlist in spice / spectre format
  - SPEF - Standard Parasitic Exchange Format (input for static timing analysis for digital designs)

The resulting parasitic components to use can be specified in this area. All defaults are fine.

Extraction Type

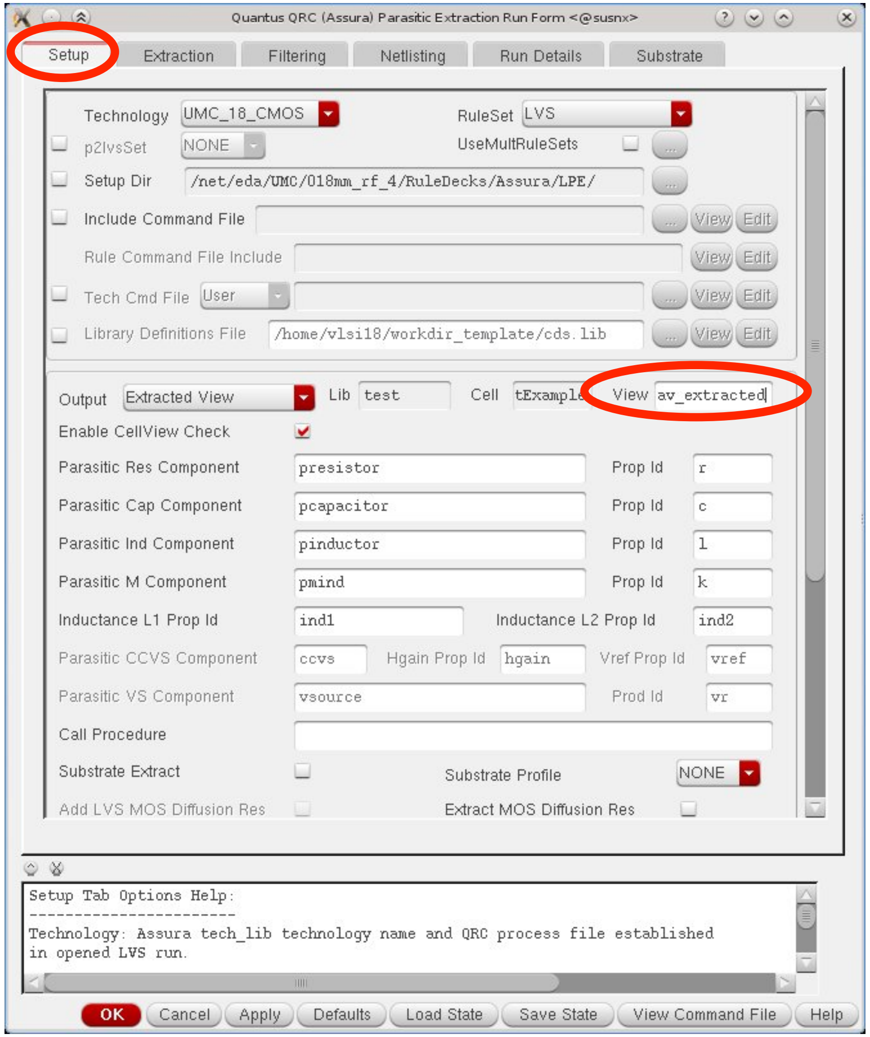


- Extraction Type: C Only
- Name Space: Layout Names
- Max fracture length: infinite microns
- Temperature: 25.0 C
- Cap Coupling Mode: Coupled
- Ref Node: gnd
- Mult Factor: 1.0
- Extend Checking Distance: default
- Diffusion Equation R: ✓
- Ladder Network: □
- User Region:
- Net Selection Type: Full Chip All Nets
- FS Extraction Mode: NONE
- Layer Setup Customization: □
- Quantus FS mode: □
- Field Solver High: □
- Resistance Mesh: □
- Adaptive: false
- R Mesh User Region:
- Non-Manhattan Resistance Accuracy: default
- From File: □
- Change LithoBias Direction: □
- Litho Config File: □

```
HRCX Cells: Specify a list of cells which appear in the output hierarchy, requires
cell name, with optional view and lib names (cell, view, lib).
```

- The ‘Extraction Type’ defines which components to extract and determines the complexity of the result
- We will use:
  - C only   or
  - RC
- The ‘Cap Coupling Mode’ specifies the ‘backside’ of the extracted capacitors
  - **Decoupled**: all capacitors couple against *ONE* specified ‘Ref Node’ which MUST be specified and be present in the cell.
    → Less accuracy but also less complexity, no cross coupling can be simulated
  - **Coupled**: all capacitors are extracted as they are → Higher complexity and cross coupling can be simulated

Extraction Type



Quantus QRC (Assura) Parasitic Extraction Run Form <@susnx>

Technology UMC_18_CMOS

RuleSet LVS

□ p2lvsSet NONE

UseMultRuleSets □

□ Setup Dir /net/eda/UMC/018mm_rf_4/RuleDecks/Assura/LPE/

□ Include Command File

Rule Command File Include

□ Tech Cmd File User

□ Library Definitions File /home/vlsi18/workdir_template/cds.lib

Output Extracted View Lib test Cell tExample View av_extracted

Enable CellView Check ☑

Parasitic Res Component presistor Prop Id r

Parasitic Cap Component pcapacitor Prop Id c

Parasitic Ind Component pinductor Prop Id l

Parasitic M Component pmind Prop Id k

Inductance L1 Prop Id ind1 Inductance L2 Prop Id ind2

Parasitic CCVS Component ccvs Hgain Prop Id hgain Vref Prop Id vref

Parasitic VS Component vsource Prod Id vr

Call Procedure

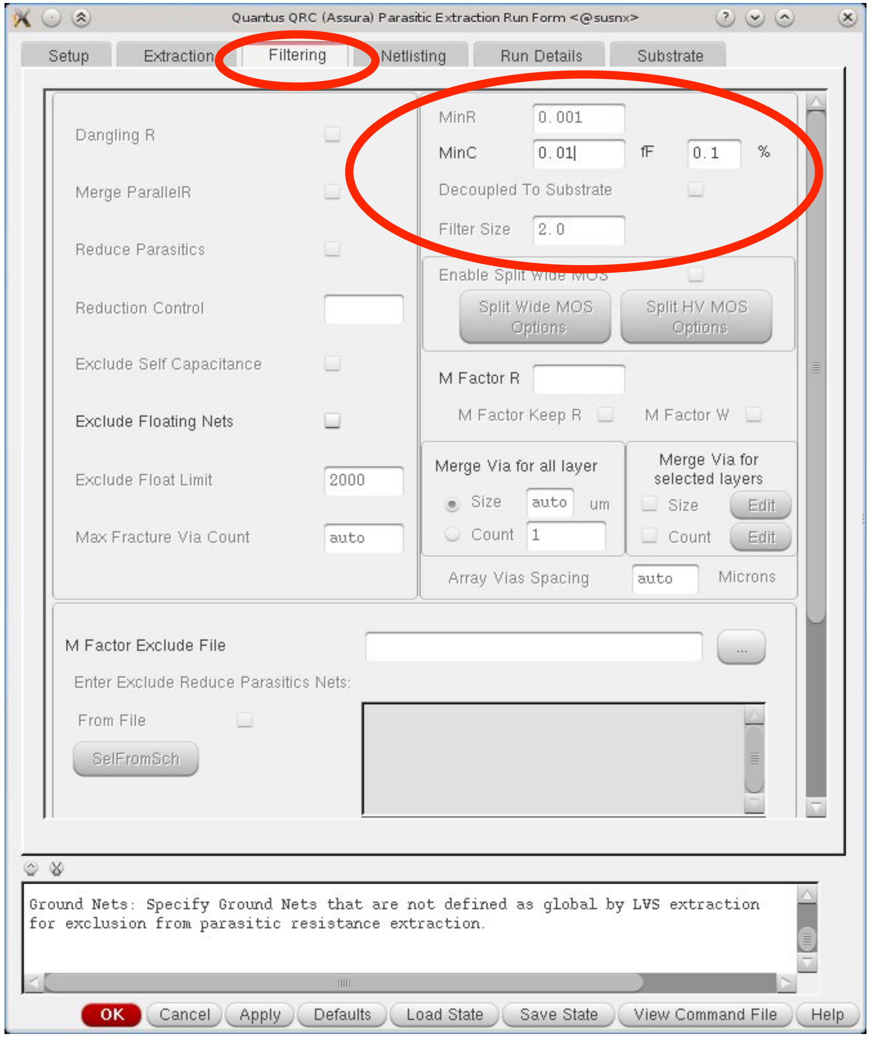
Substrate Extract □ Substrate Profile NONE

Add LVS MOS Diffusion Res □ Extract MOS Diffusion Res □

```
Setup Tab Options Help:
----------------------
Technology: Assura tech_lib technology name and QRC process file established
in opened LVS run.
```

- To remember the extraction type I like to add it to the view name: (in the ‘Setup’ tab), e.g.
  - av_extracted_C (for decoupled C only)
  - av_extracted_CC (for coupled C only)
  - av_extracted_RCC (for coupled RCC)

Filtering



Dangling R □

Merge ParallelR □

Reduce Parasitics □

Reduction Control

Exclude Self Capacitance □

Exclude Floating Nets □

Exclude Float Limit 2000

Max Fracture Via Count auto

MinR 0.001

MinC 0.01 fF 0.1 %

Decoupled To Substrate □

Filter Size 2.0

Enable Split Wide MOS □

M Factor R

M Factor Keep R □ M Factor W □

Merge Via for all layer

● Size auto um

○ Count 1

Merge Via for selected layers

□ Size

□ Count

Array Vias Spacing auto Microns

M Factor Exclude File

Enter Exclude Reduce Parasitics Nets:

From File □

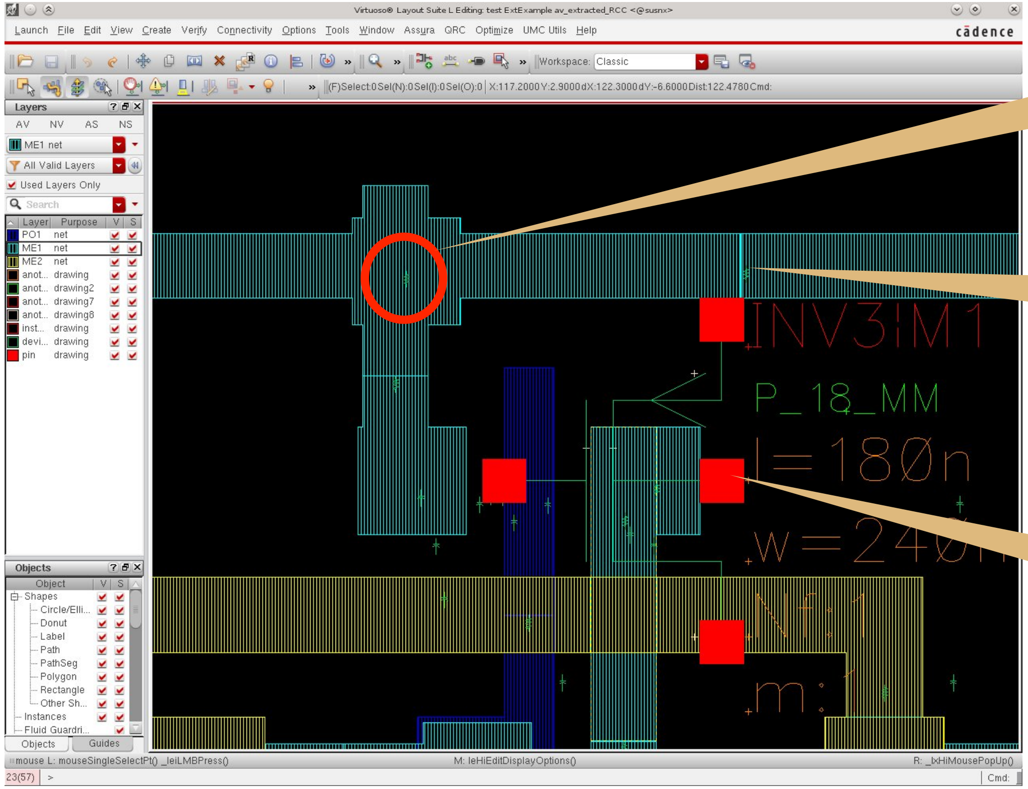
```
Ground Nets: Specify Ground Nets that are not defined as global by LVS extraction
for exclusion from parasitic resistance extraction.
```

- In the ‘Filtering’ tab the ‘chopping’ of the parasitic elements can be controlled
  - Minimum resistor values
  - Minimum capacitor values
  - …
- Can be used to reduce complexity or increase accuracy of the extraction
- The default values are fine for us

- Now we can start the extraction!

The Extracted View

- Open the extracted view (default: av_extracted) with the library manager
- It looks like a layout but contains devices and parasitic elements



Virtuoso® Layout Suite L Editing: test ExtExample av_extracted_RCC <@susnx>

(F)Select:0 Sel(N):0 Sel(I):0 Sel(O):0 | X:117.2000 Y:2.9000 dX:122.3000 dY:-6.6000 Dist:122.4780 Cmd:

☑ Used Layers Only

Layer	Purpose	V	S
PO1	net	☑	☑
ME1	net	☑	☑
ME2	net	☑	☑
anot...	drawing	☑	☑
anot...	drawing2	☑	☑
anot...	drawing7	☑	☑
anot...	drawing8	☑	☑
inst...	drawing	☑	☑
devi...	drawing	☑	☑
pin	drawing	☑	☑

Object	V	S
Shapes	☑	☑
Circle/Elli...	☑	☑
Donut	☑	☑
Label	☑	☑
Path	☑	☑
PathSeg	☑	☑
Polygon	☑	☑
Rectangle	☑	☑
Other Sh...	☑	☑
Instances	☑	☑
Fluid Guardri...		☑

mouse L: mouseSingleSelectPt() _leiLMBPress()   M: leHiEditDisplayOptions()   R: _lxHiMousePopUp()

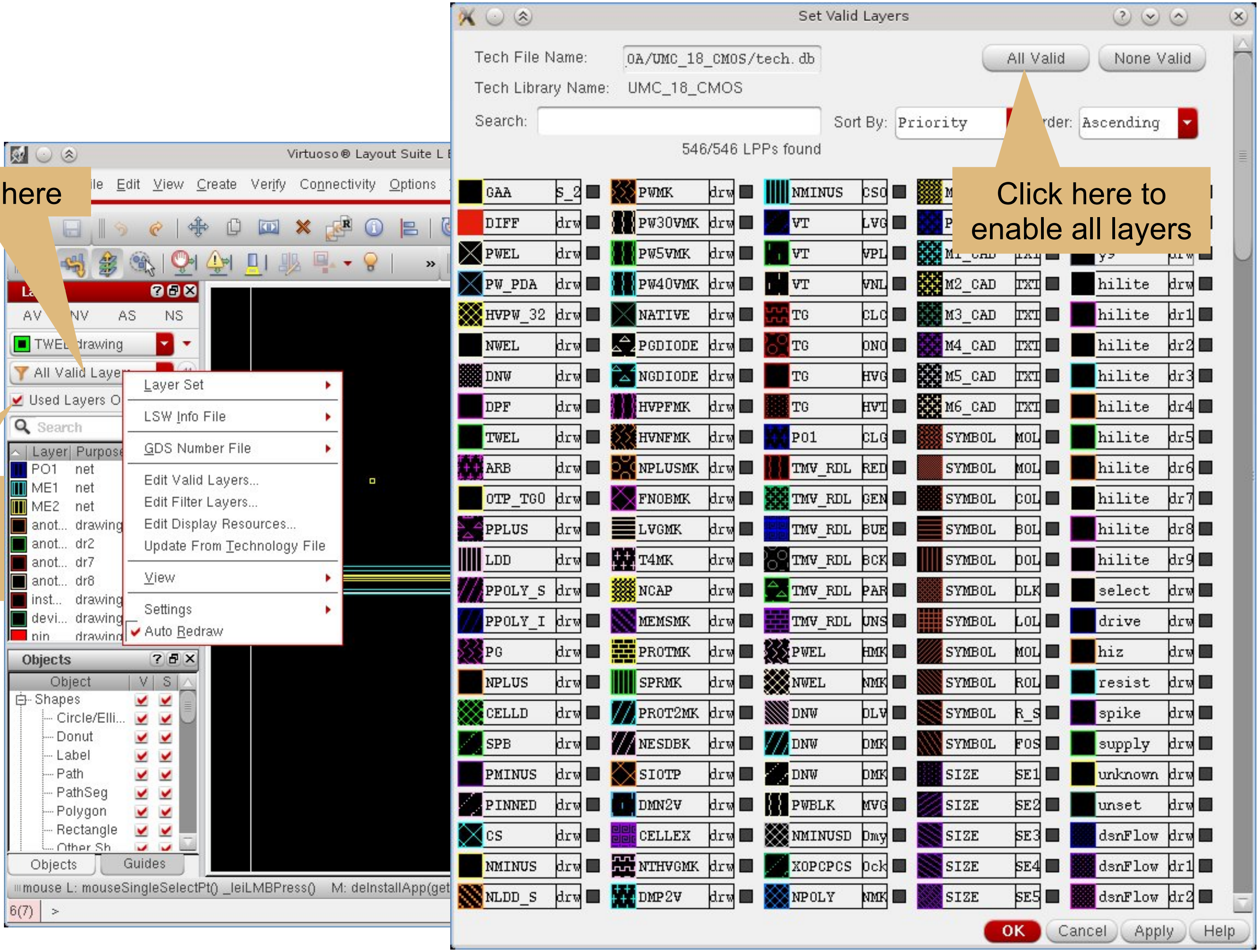
23(57) >   Cmd:

Parasitic resistor (cell ‘presistor’).

The type of the metal lines is ‘net’ (not drawing as in the layout)

NFET as in the schematic

Enable the ‘Net’ Layers (UMC specific)



Righ click here

Check here to show only used layers

Click here to enable all layers

Layer	Purpose
PO1	net
ME1	net
ME2	net
anot...	drawing
anot...	dr2
anot...	dr7
anot...	dr8
inst...	drawing
devi...	drawing
pin	drawing

mouse L: mouseSingleSelectPt() _leiLMBPress() M: deInstallApp(get

6(7) >

Tech File Name: OA/UMC_18_CMOS/tech.db

Tech Library Name: UMC_18_CMOS

Search:

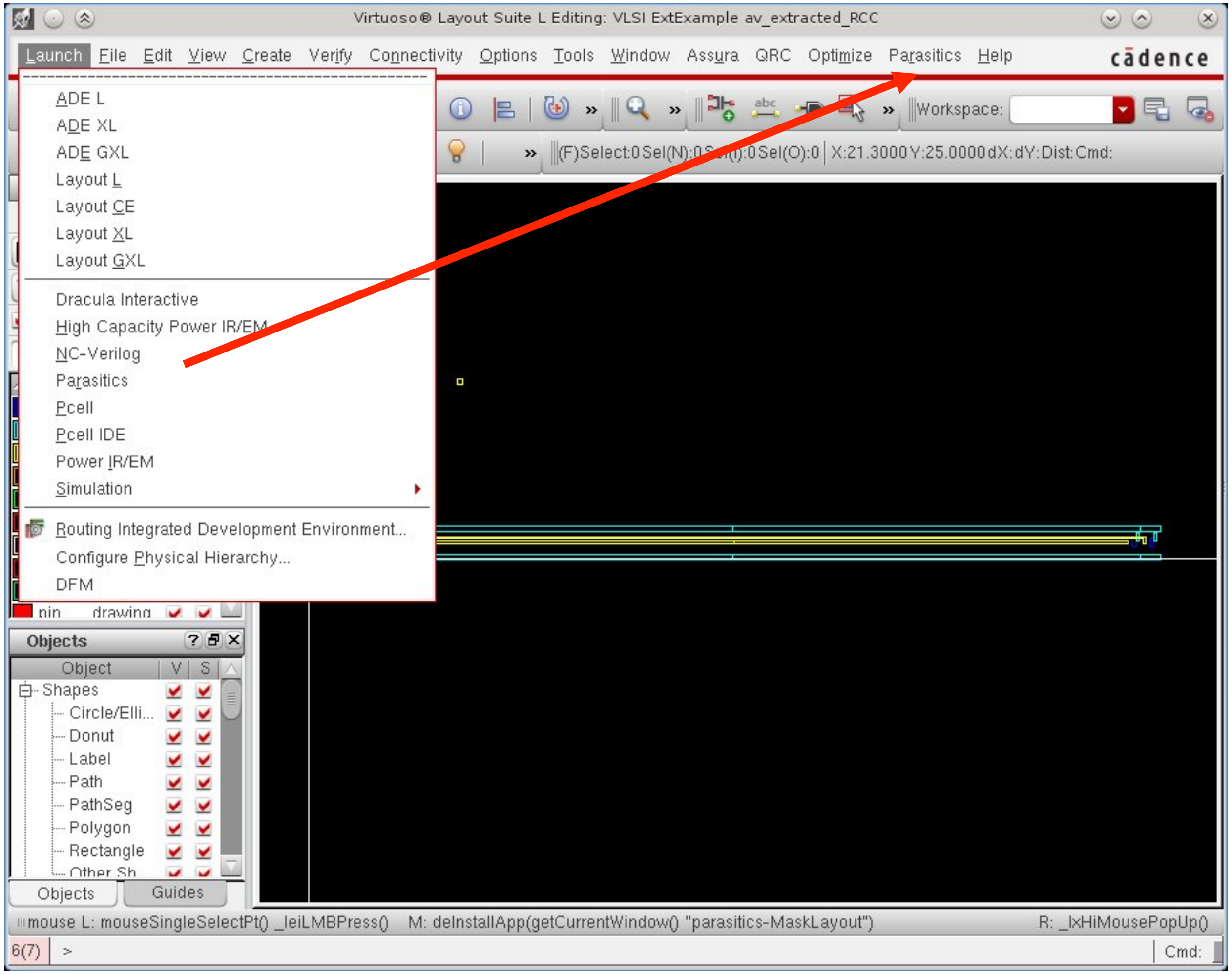
Sort By: Priority Order: Ascending

546/546 LPPs found

GAA	s_2	PWMK	drw	NMINUS	CSO	M			
DIFF	drw	PW30VMK	drw	VT	LVG	P			
PWEL	drw	PW5VMK	drw	VT	VPL	M1_CAD	TXT	y9	drw
PW_PDA	drw	PW40VMK	drw	VT	VNL	M2_CAD	TXT	hilite	drw
HVPW_32	drw	NATIVE	drw	TG	CLC	M3_CAD	TXT	hilite	dr1
NWEL	drw	PGDIODE	drw	TG	ONO	M4_CAD	TXT	hilite	dr2
DNW	drw	NGDIODE	drw	TG	HVG	M5_CAD	TXT	hilite	dr3
DPF	drw	HVPFMK	drw	TG	HVT	M6_CAD	TXT	hilite	dr4
TWEL	drw	HVNFMK	drw	P01	CLG	SYMBOL	MOL	hilite	dr5
ARB	drw	NPLUSMK	drw	TMV_RDL	RED	SYMBOL	MOL	hilite	dr6
OTP_TG0	drw	FNOBMK	drw	TMV_RDL	GEN	SYMBOL	COL	hilite	dr7
PPLUS	drw	LVGMK	drw	TMV_RDL	BUE	SYMBOL	BOL	hilite	dr8
LDD	drw	T4MK	drw	TMV_RDL	BCK	SYMBOL	DOL	hilite	dr9
PPOLY_S	drw	NCAP	drw	TMV_RDL	PAR	SYMBOL	DLK	select	drw
PPOLY_I	drw	MEMSMK	drw	TMV_RDL	UNS	SYMBOL	LOL	drive	drw
PG	drw	PROTMK	drw	PWEL	HMK	SYMBOL	MOL	hiz	drw
NPLUS	drw	SPRMK	drw	NWEL	NMK	SYMBOL	ROL	resist	drw
CELLD	drw	PROT2MK	drw	DNW	DLV	SYMBOL	R_S	spike	drw
SPB	drw	NESDBK	drw	DNW	DMK	SYMBOL	FOS	supply	drw
PMINUS	drw	SIOTP	drw	DNW	DMK	SIZE	SE1	unknown	drw
PINNED	drw	DMN2V	drw	PWBLK	MVG	SIZE	SE2	unset	drw
CS	drw	CELLEX	drw	NMINUSD	Dmy	SIZE	SE3	dsnFlow	drw
NMINUS	drw	NTHVGMK	drw	XOPCPCS	Ock	SIZE	SE4	dsnFlow	dr1
NLDD_S	drw	DMP2V	drw	NPOLY	NMK	SIZE	SE5	dsnFlow	dr2

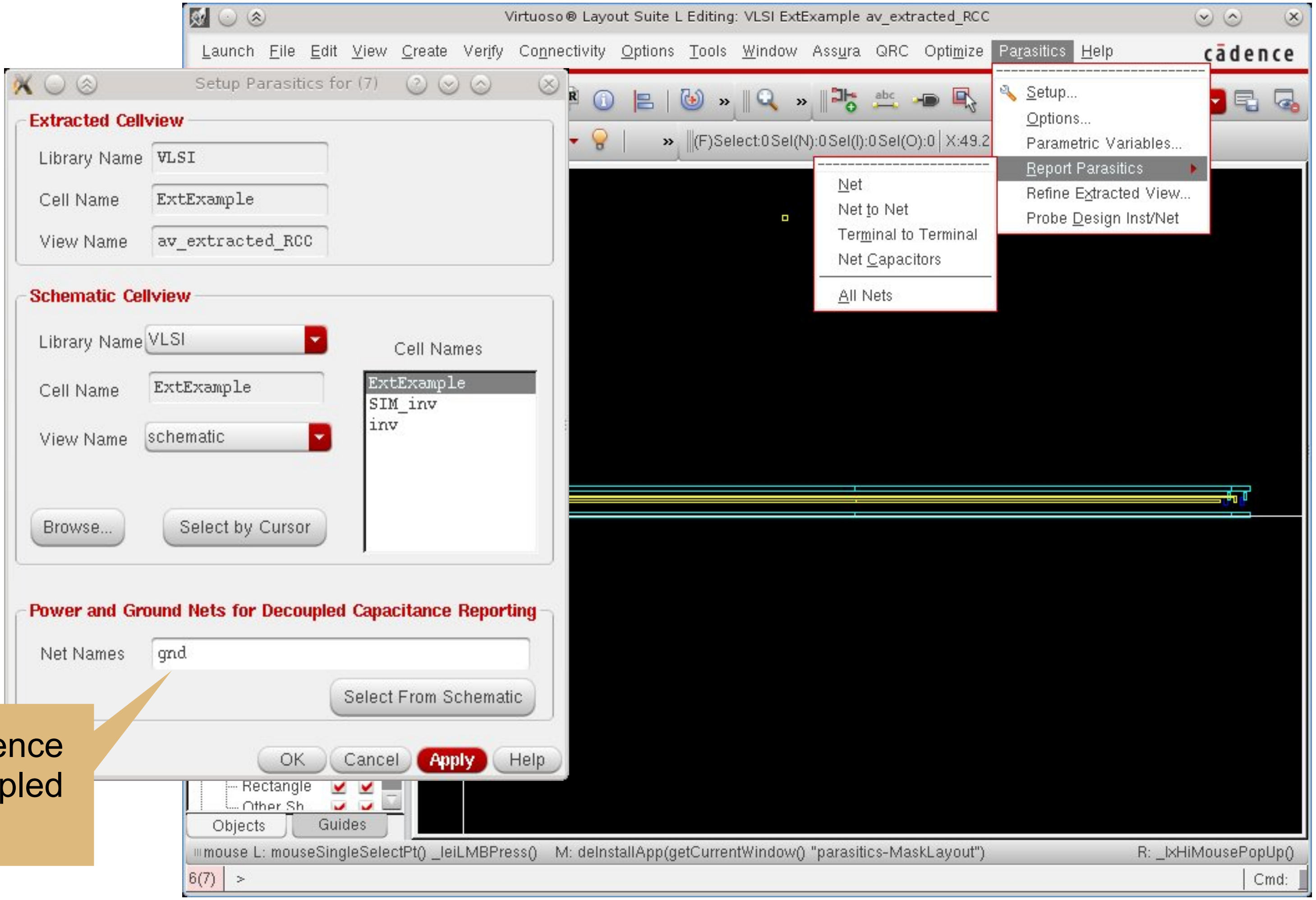
Examining the Parasitics

- To enable the ‘Parasitics’ option in the menu bar do: Menu bar → Launch → Parasitics


Virtuoso® Layout Suite L Editing: VLSI ExtExample av_extracted_RCC
Launch File Edit View Create Verify Connectivity Options Tools Window Assura QRC Optimize Parasitics Help
cādence
ADE L
ADE XL
ADE GXL
Layout L
Layout CE
Layout XL
Layout GXL
Dracula Interactive
High Capacity Power IR/EM
NC-Verilog
Parasitics
Pcell
Pcell IDE
Power IR/EM
Simulation
Routing Integrated Development Environment...
Configure Physical Hierarchy...
DFM
Workspace:
(F)Select:0 Sel(N):0 Sel(I):0 Sel(O):0 X:21.3000 Y:25.0000 dX: dY: Dist: Cmd:
pin drawing
Objects
Object V S
Shapes
Circle/Elli...
Donut
Label
Path
PathSeg
Polygon
Rectangle
Other Sh...
Objects Guides
mouse L: mouseSingleSelectPt() _leiLMBPress() M: deInstallApp(getCurrentWindow() "parasitics-MaskLayout") R: _lxHiMousePopUp()
6(7) >
Cmd:

Reporting Parasitics

- First select Parasitics → Setup
- This enables the 'Report Parasitics' options



Setup Parasitics for (7)

Extracted Cellview

Library Name: VLSI

Cell Name: ExtExample

View Name: av_extracted_RCC

Schematic Cellview

Library Name: VLSI

Cell Name: ExtExample

View Name: schematic

Cell Names: ExtExample, SIM_inv, inv

Power and Ground Nets for Decoupled Capacitance Reporting

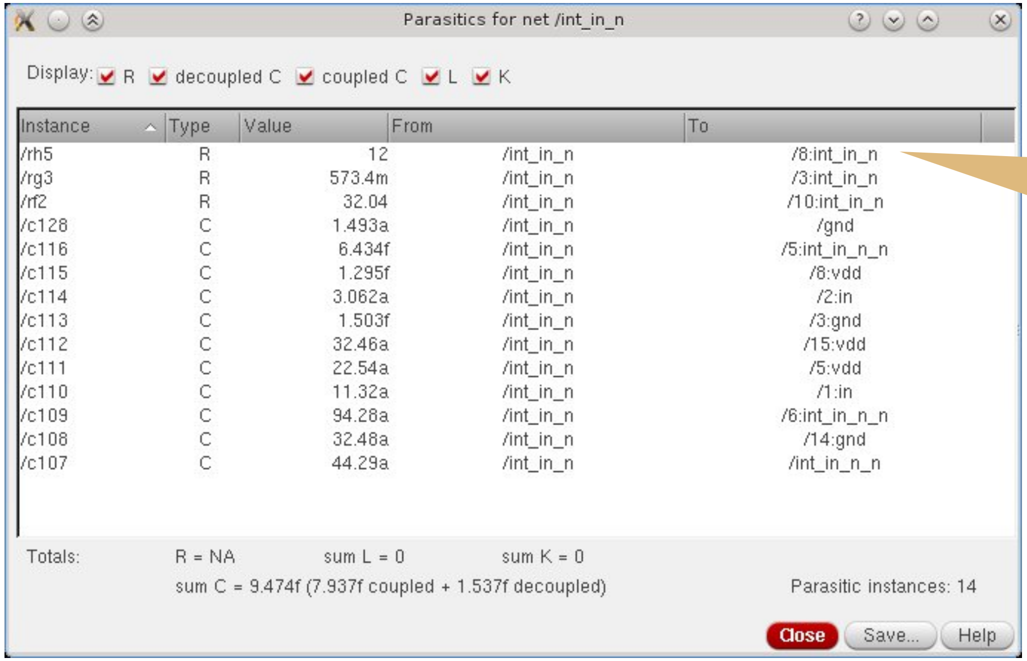
Net Names: gnd

mouse L: mouseSingleSelectPt() _leiLMBPress()   M: deInstallApp(getCurrentWindow() "parasitics-MaskLayout")   R: _lxHiMousePopUp()

Enter the reference node for decoupled reporting

Example Net Report

- Select: Parasitics → Report Parasitics → Net
- Select some net in the extracted view
- A detailed net report is shown



Parasitics for net /int_in_n

Display: ☑ R ☑ decoupled C ☑ coupled C ☑ L ☑ K

Instance	Type	Value	From	To
/rh5	R	12	/int_in_n	/8:int_in_n
/rg3	R	573.4m	/int_in_n	/3:int_in_n
/rf2	R	32.04	/int_in_n	/10:int_in_n
/c128	C	1.493a	/int_in_n	/gnd
/c116	C	6.434f	/int_in_n	/5:int_in_n_n
/c115	C	1.295f	/int_in_n	/8:vdd
/c114	C	3.062a	/int_in_n	/2:in
/c113	C	1.503f	/int_in_n	/3:gnd
/c112	C	32.46a	/int_in_n	/15:vdd
/c111	C	22.54a	/int_in_n	/5:vdd
/c110	C	11.32a	/int_in_n	/1:in
/c109	C	94.28a	/int_in_n	/6:int_in_n_n
/c108	C	32.48a	/int_in_n	/14:gnd
/c107	C	44.29a	/int_in_n	/int_in_n_n

Totals: R = NA sum L = 0 sum K = 0

sum C = 9.474f (7.937f coupled + 1.537f decoupled)

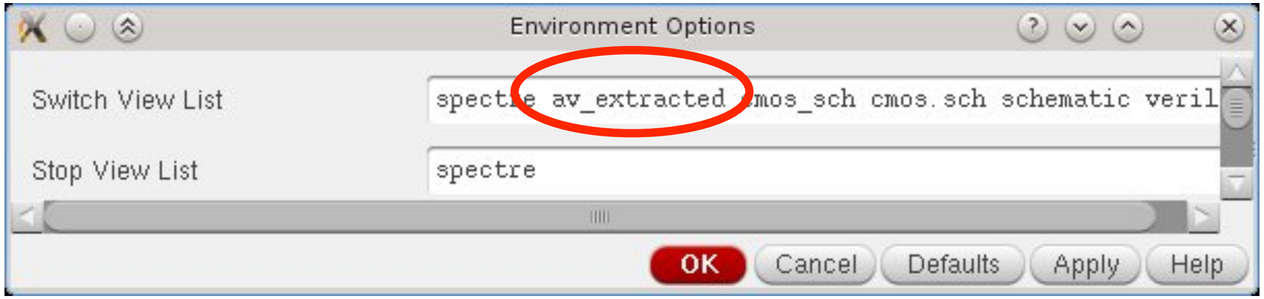
Parasitic instances: 14

If resistances were extracted the nets now have numbered segments

- Select some entry to highlight the parasitic element in the extracted view

Simulating an Extracted View

- Set up a simulation schematic
  - Instantiate the symbol of the cell which you have extracted
  - Add power sources, signal sources, etc.
- Launch → ADE
  - Go to Session → Environment
  - In the Switch View List add the view name of your extracted view (default: ‘av_extracted’) somewhere BEFORE ‘schematic’ → the netlister now prefers ‘av_extracted’ over ‘schematic’



Environment Options

Switch View List: spectre av_extracted cmos_sch cmos.sch schematic veril

Stop View List: spectre

- Setup a transient simulation as usual and simulate

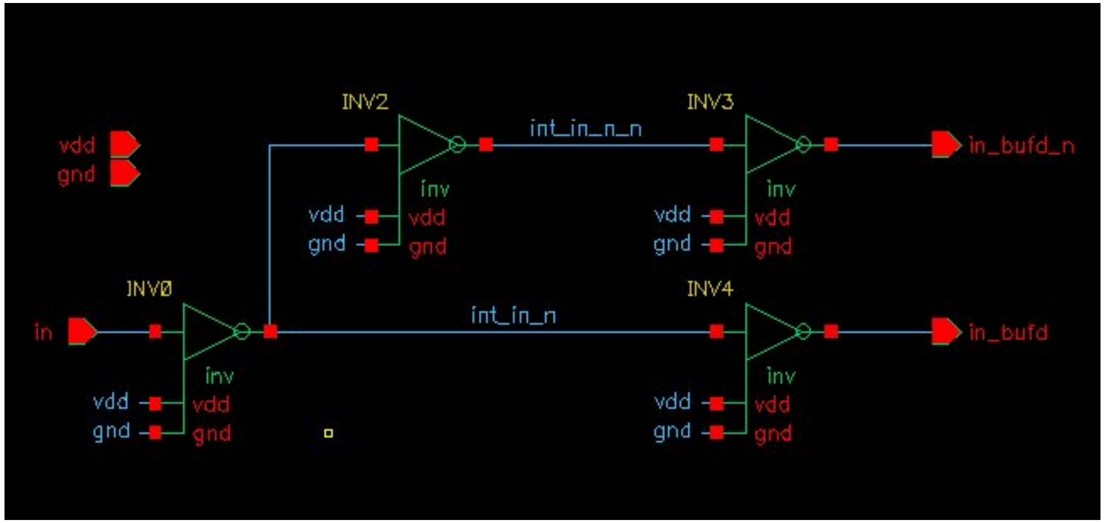
Viewing the Simulation Results

- Select results as usual
  - ADE Menu Bar → Outputs → Select From Schematic
  - You can descend into the av_extracted view and select nets
- Use the ‘Results Browser’
  - ADE Menu Bar → Tools → Results Browser
  - Browse through the ‘tran’ folder

Exercise: Parasitic Simulation

Exercise: Signal Delay & Integrity

- Step 1: Create the following (or similar) schematic



- Step 2: Draw the according layout
  - Draw the in_n and in_n_n nodes in parallel @ minimum pitch and width for at least 100µm
  - Make the layout LVS clean
  - DRC does not matter for now…

Exercise: Signal Delay & Integrity

- Step 3: Extract the layout
  - Run all three extraction types and save them to separate views
    - C only decoupled → av_extracted_C
    - C only coupled → av_extracted_CC
    - RC coupled → ac_extracted_RC
- Step 4: Analyze the extracted view
  - How big is the total coupling capacitance between your in_n and in_n_n node?
- Step 4: Simulate the schematic and all 3e extracted views
  - HINT: You can copy the results after the simulation
    - cd /tmp/ADE-sim-vlsiXX/
    - cp –r psf someNewName
    - You can then reopen them in the 'Results Browser'
  - Can you see any cross coupling in the waveforms?
  - What is the difference in the propagation delays between the plain schematic and your layout?

Advanced: Using a Config View

- In larger designs, you may only want to include parasitics to some cells. This can be controlled with a 'config' view

- Create a new cell view of type 'config view'.
  - File -> new -> cell view
  - View is 'schematic'
  - The tool associated is the 'Hierarchy editor'
  - Use Spectre as simulator

- In the Tree/Table view panel you can select which view is used for simulation for each cell

- To simulate, you must open ADC from the config view
- Alternatively, when doing a simulation on the schematic, switch to config in Design->…