SPADIC - A Self-Triggered Pulse Amplification and Digitization ASIC

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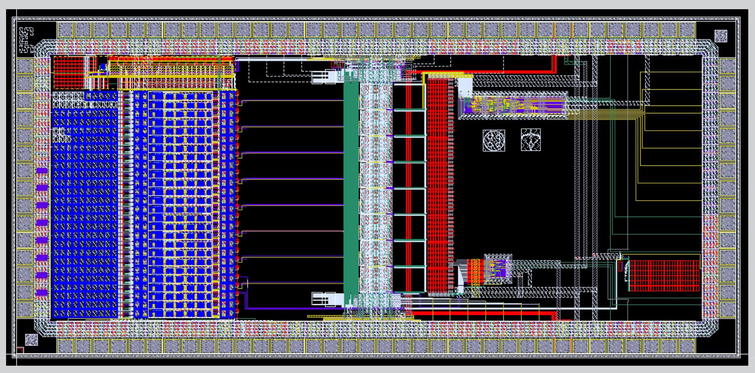
Introduction

For the readout of the TRD sub-detector of the planned fixed-target CBM experiment at FAIR/GSI (Darmstadt, Germany), a new self-triggered amplification and digitization chip is being developed.
The final mixed-signal chip will have 32-64 channels each composed of a low noise and power charge preamplifier, a 7-9 Bit pipeline ADC running at 25 MSamples/s and some digital data processing units carrying out detector specific tasks such as ion-tail cancellation and baseline correction. A token ring network will act as a balancing arbiter between channels and output serializer.
The latest 180 nm test-chip has 26 preamplifier/shaper channels and 8 ADCs. For control signal generation and output decoding two synthesized blocks have also been integrated. By connecting both preamplifier and ADC, digital snap-shots of injected test-pulses have been recorded successfully, showing the proper oscilloscope-like operation of the whole mixed-signal data chain from analog amplification to digital output encoding.

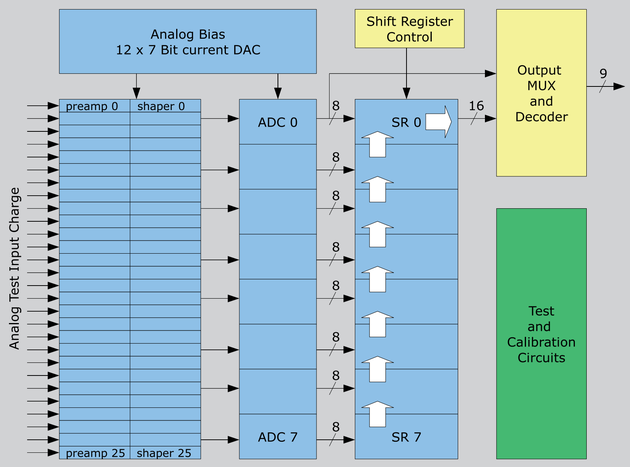
Parameters of Prototype

Technology	UMC 1P6M, 180 nm
Chip Area	1.5 x 3.2 mm²
Area of Channel / ADC	40 x 540 / 130 x 120 µm²
Number of Channels /ADCs	26 / 8
Number of Complete Channels	8 (Preamplifier, Shaper, ADC)
Power per Channel /ADC	3.8 / 4.5 mW
Shaper Noise (ENC)	800 e @ 30 pF
Shaping Time	82 ns
ADC Resolution	7.5 Bit effective
ADC Speed	25 MSamples/s

Layout of Prototype



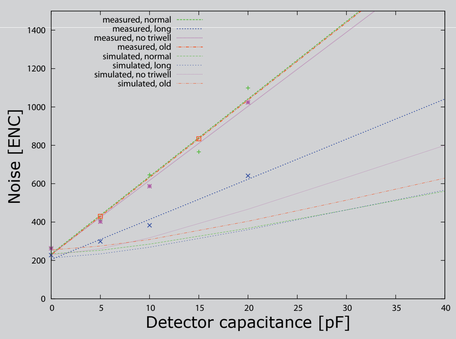
Latest Test Chip



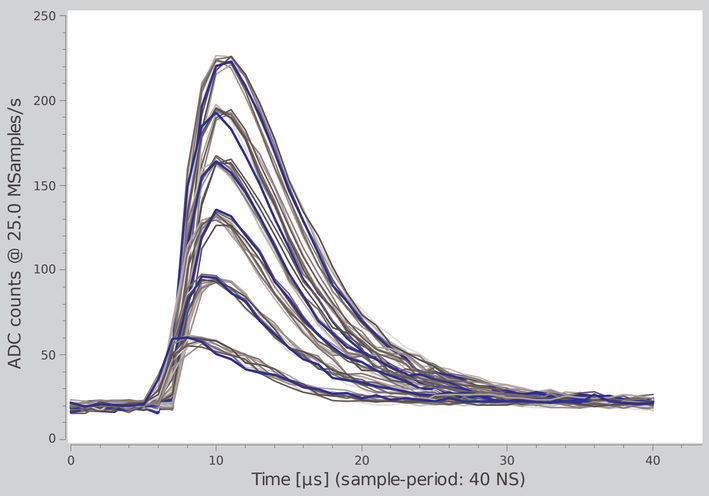
The latest 180 nm prototype has as size of 3.2 x 1.5 mm² and carries 26 CSA channels, 8 pipeline ADCs, a 5.3 kBit shift register matrix, two synthesized control/decoder blocks and different test and calibration circuits.

Each CSA channel basically consists of a single ended preamplifier with pole-zero cancellation feedback followed by a 2nd order T-feedback shaper with 82 ns shaping-time. For the self-triggered scheme an analog discriminator is connected to the shaper output. Different versions of the preamplifiers were realized to figure out what the lowest possible noise values are and how they can be achieved.
For both, preamplifier and shaper, several copies of a unified amplifier cell is connected in parallel. A special injection cell is used for test charge injection. The complete channel block is hand-layouted and covers about 40 x 540 µm² die area.
8 CSA channels are each connected to a current-mode pipeline 8 Bit ADC running at 25 MSamples/s. In doing so, complete shaper pulses could be digitized. The raw data stream of each ADC can reach up to 400 MBit/s and is fed into a large dynamic buffer matrix continuously holding the last 45 output values. When a trigger occurs the complete matrix content gets shifted through some raw data to signed binary converter out of the chips. Hit readout rates of about 10 kHits/s (3.5 MByte/s per channel) from chip via a FPGA board and USB into the PC have been reached so far.

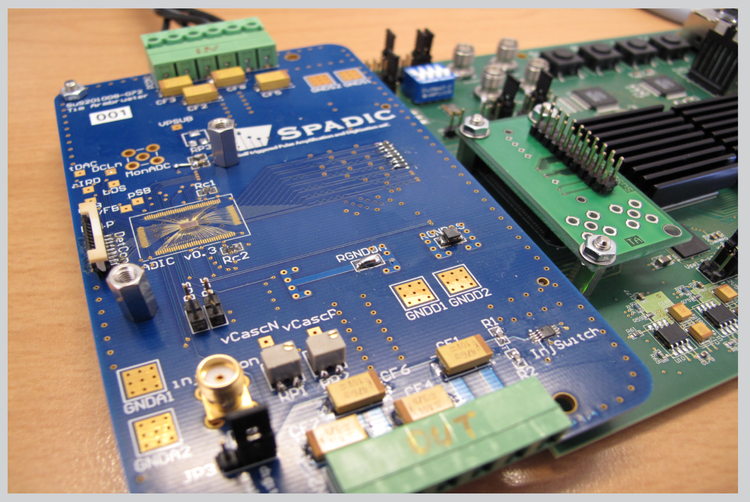
Latest Test Results



The overall pulse shapes and the general amplifier behavior matches nearly perfectly the simulation, whereas, as shown in the graphic above, the measured noise curves deviate. All noise values have been measured via s-curve scans by using previously well calibrated on-chip injection capacitors. Although the noise offset (at 0 pF detector capacitance) is for both simulations and measurements at about 200 e ENC, the measured slopes of the different channel versions differ significantly from both simulation and each other (see graph above).
The most important result here is that hardly any parameter variation (input N-MOS with and without triwell, many minor layout and schematic refinements) did have a real impact on the measured noise, whereas using a longer input N-MOS (320 nm instead of 180 nm) caused a dramatic decrease of the noise slope by about a factor of a 2. Interestingly this behavior is obviously not integrated in the transistor models.
Nevertheless the best channel has a measured noise of only 800 e ENC for a parasitic input capacitance of 30 pF while consuming only 3.6 mW and therewith already satisfies the project requirements.
The static ADC transfer characteristic has been measured at a conversion speed of 25 MSamples/s and shows a good DNL and INL, proving the ADC to have an effective resolution of 7.5 bit while consuming only 4.5 mW and covering only 130 x 120 µm² of chip area.
The most important dynamic system-wide measurement was to connect an amplifier to an ADC and that way to digitize analog pulses coming out of the shaper. Indeed the sophisticated readout setup is feasible to reliably read out all 8 channels in parallel at channel rates of up to 10 kHits/s. Some measured pulses with different amplitudes are shown below. Due to this success a testbeam at CERN with 8 readout setups (a total of 64 channels) in November is currently being prepared.



Readout Setup



The readout setup consists of the Spadic chip wire-bonded to an adaptor PCB (blue in the picture) that is plugged onto a Virtex 5 readout board. Data and control packages go via the FTDI chip (USB 2.0) to the PC where they get further processed by a test and readout software.

Final Architecture

The final mixed signal chip will have 32-64 channels each consisting of a low noise and power preamplifier together with a 2nd order shaper, a 7-9 bit pipeline ADC running at 25 MSamples/s and several data processing units carrying out detector specific tasks such as ion-tail cancellation and baseline correction.
The digital readout concept still foresees to record and send out complete snap-shots of the incoming pulses together with additional meta information such as internal time-stamp, channel ID, status flags, extracted trigger ID, et cetera. An integration of some feature extraction unit adapted to the special physical requirements (extraction of amplitude, higher resolution time-stamp, ...) probably will due to a significant loss of flexibility probably not been realized.
A token ring network will work as a fair arbiter between the output FIFOs of the channels and the fast (1 Gbps) output serializer that is embedded into a sophisticated deterministic latency network protocol currently being adjusted to the certain project needs.
It is planned to submit the first full-blown test-chip having a nearly final architeture in the middle of 2011. First test results hopefully will have been gathered until end of 2011.

SPADIC

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