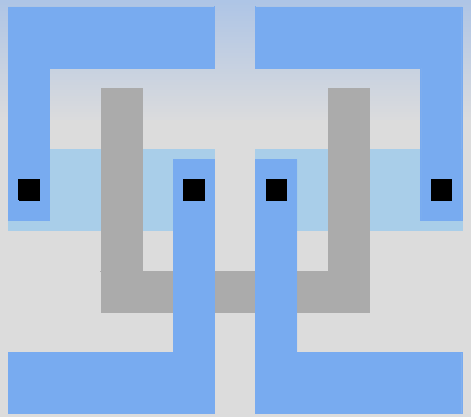
CSA Test-ASIC in UMC018

a brief design overview



Schaltungstechnik
und Simulation

Tim Armbruster

tim.armbruster@ti.uni-mannheim.de

CBM 9. Collaboration Meeting

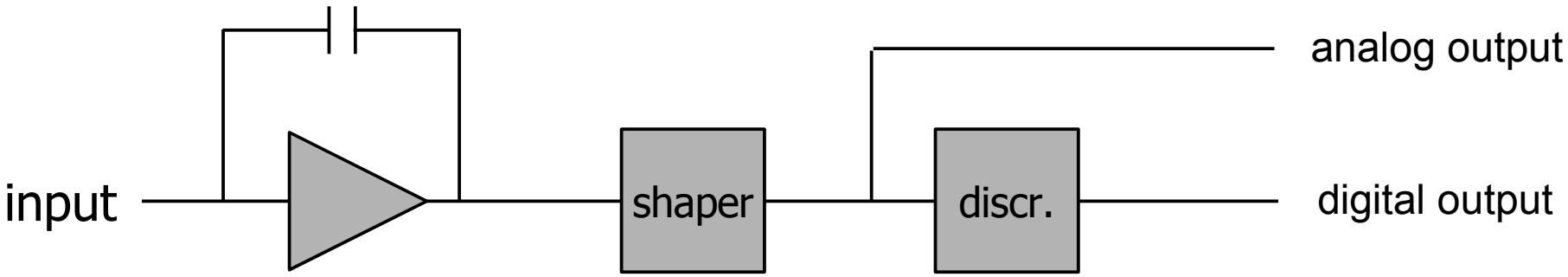
in Darmstadt

Introduction

- NXYTER self triggering strip detector readout chip is being studied for application in CBM
- Now migration to different technology may be beneficial (from AMS035 to ?)
- Goal of this work: Study performance gain when going to 0.18µm
- To reach this aim noise behaviour of UMC018 needs to be explored by comparing simulated and measured values
- Later: Results will be compared to 0.35µm and 0.13µm designs
- General problem: Various sensor parameters are not well defined yet, e.g.:
  - Detector capacitance (20 - 40pF assumed)
  - Particle hit rate
  - Detector size

=> An ASIC-Testchip was designed to become familiar with a common charge amplifier design in UMC018. This design will be described now.

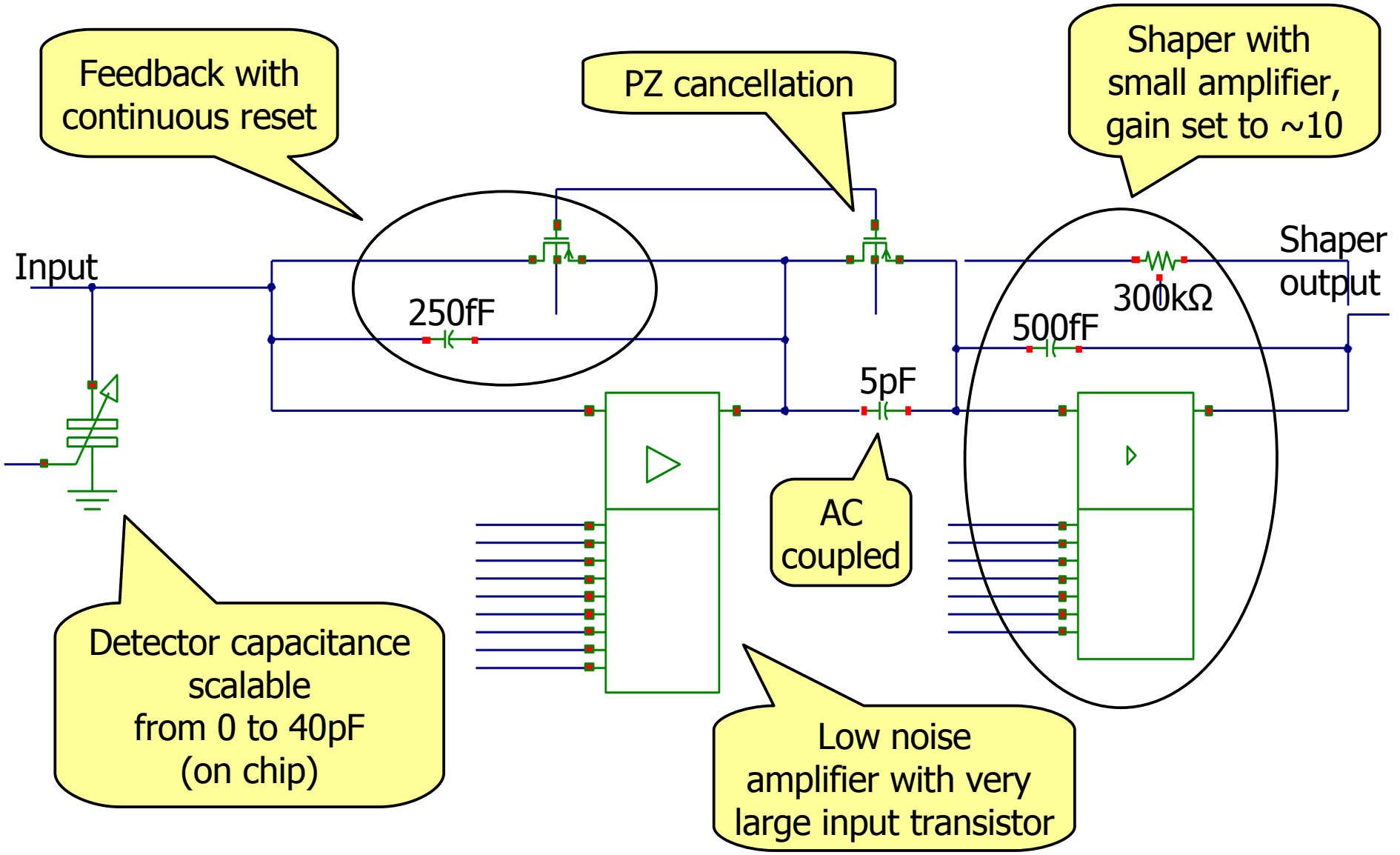
Single channel overview



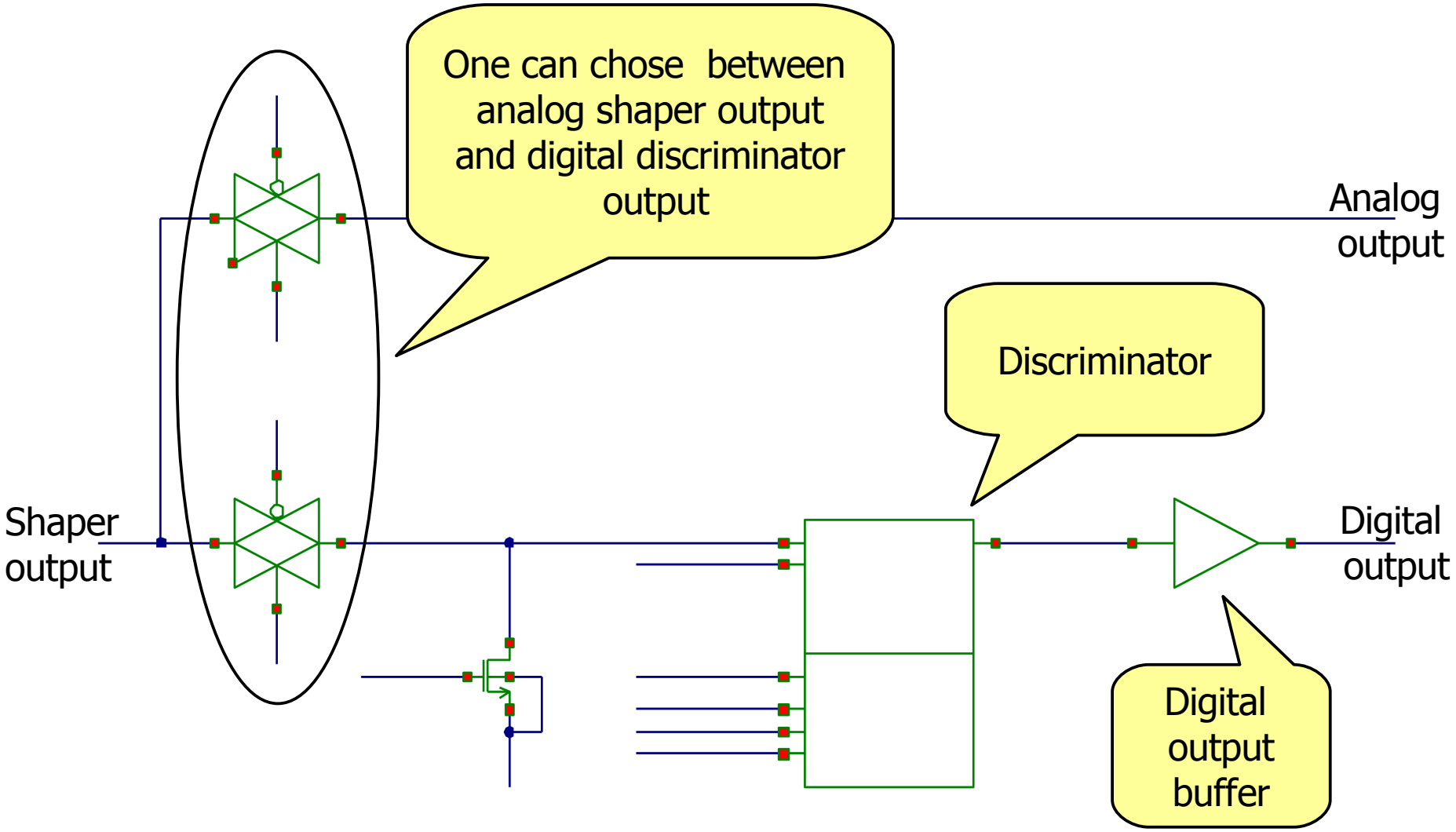
Main parameter:

- Size of Cf: 250fF
- Detector capacitance: variable
- DC-Feedback: O'Connor
- Shaper type: simple 1st order
- Digital and analog outputs
- Size of input MOS: variable

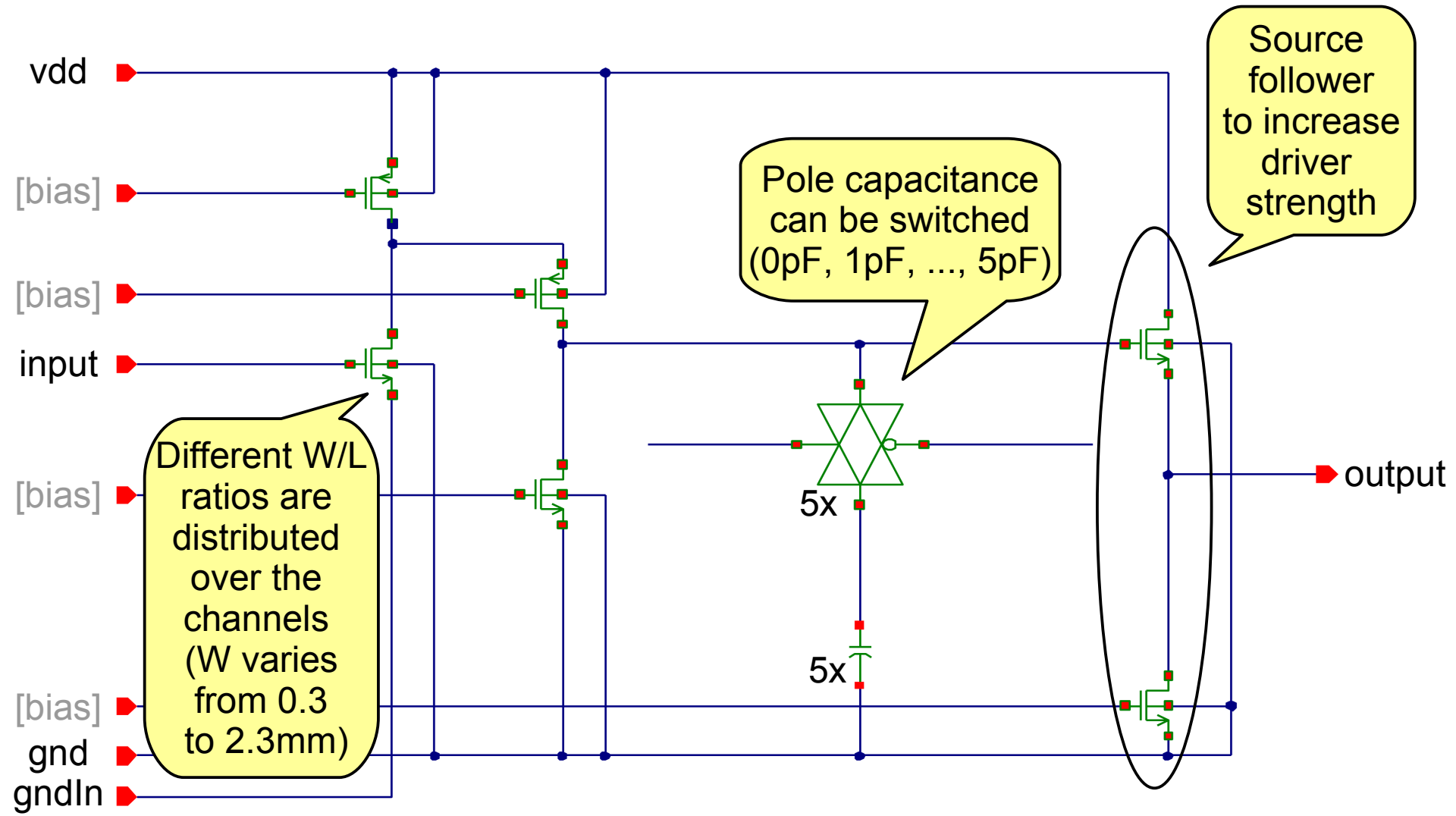
Single channel schematic (1/2)



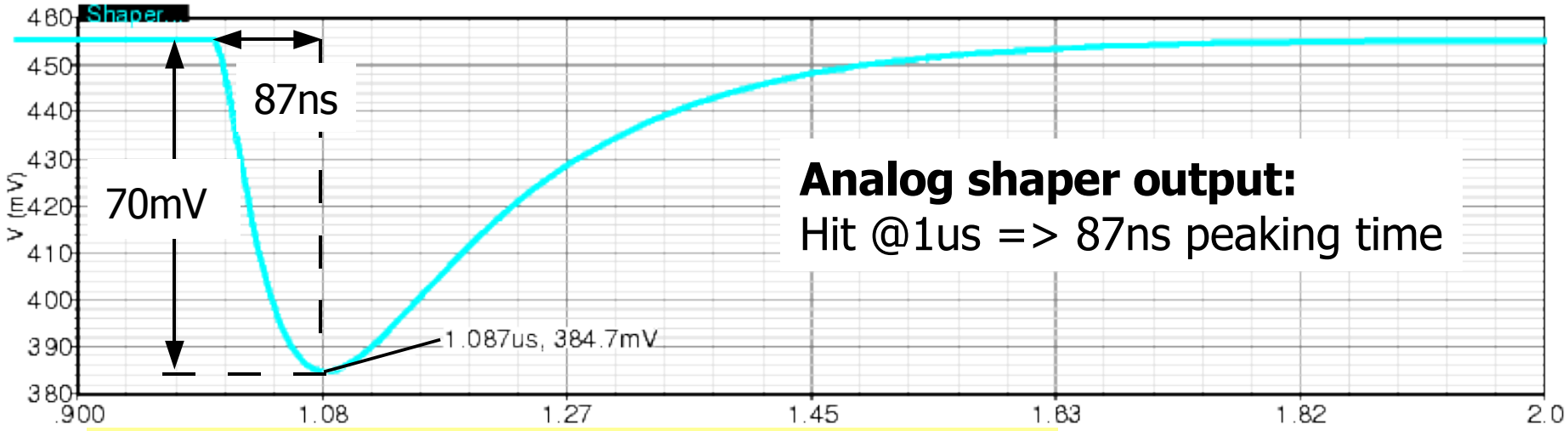
Single channel schematic (2/2)



Schematic of the low noise amplifier stage

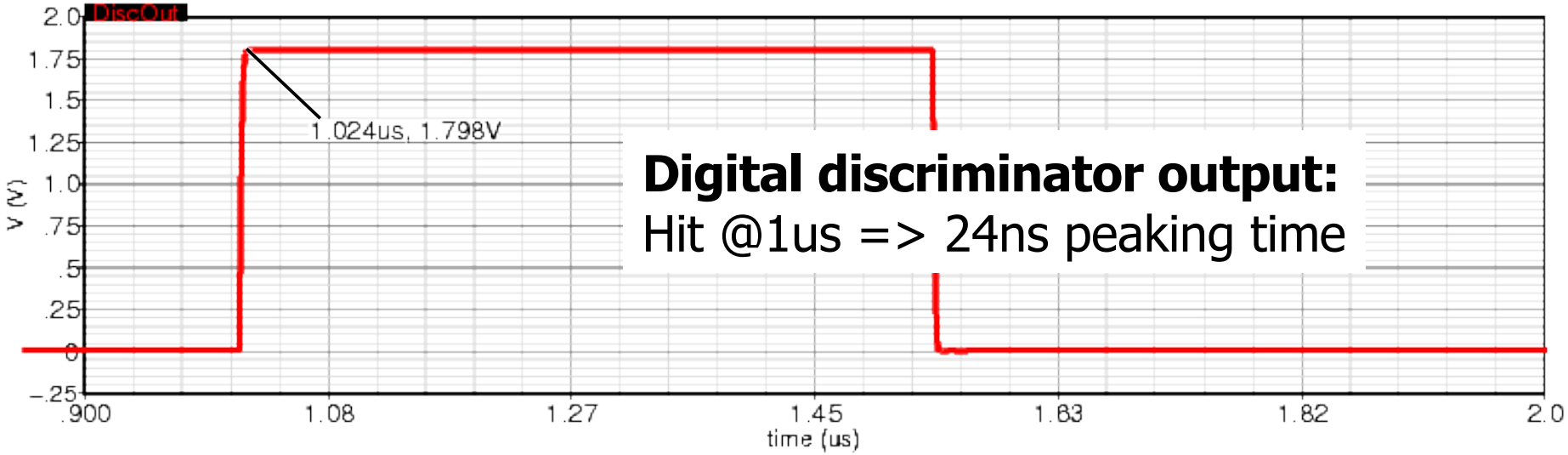


Transient simulation



Analog shaper output:
Hit @1us => 87ns peaking time

(Cdet = 30pF, Winput = 1.7mm, MIP charge ~3.7fC)

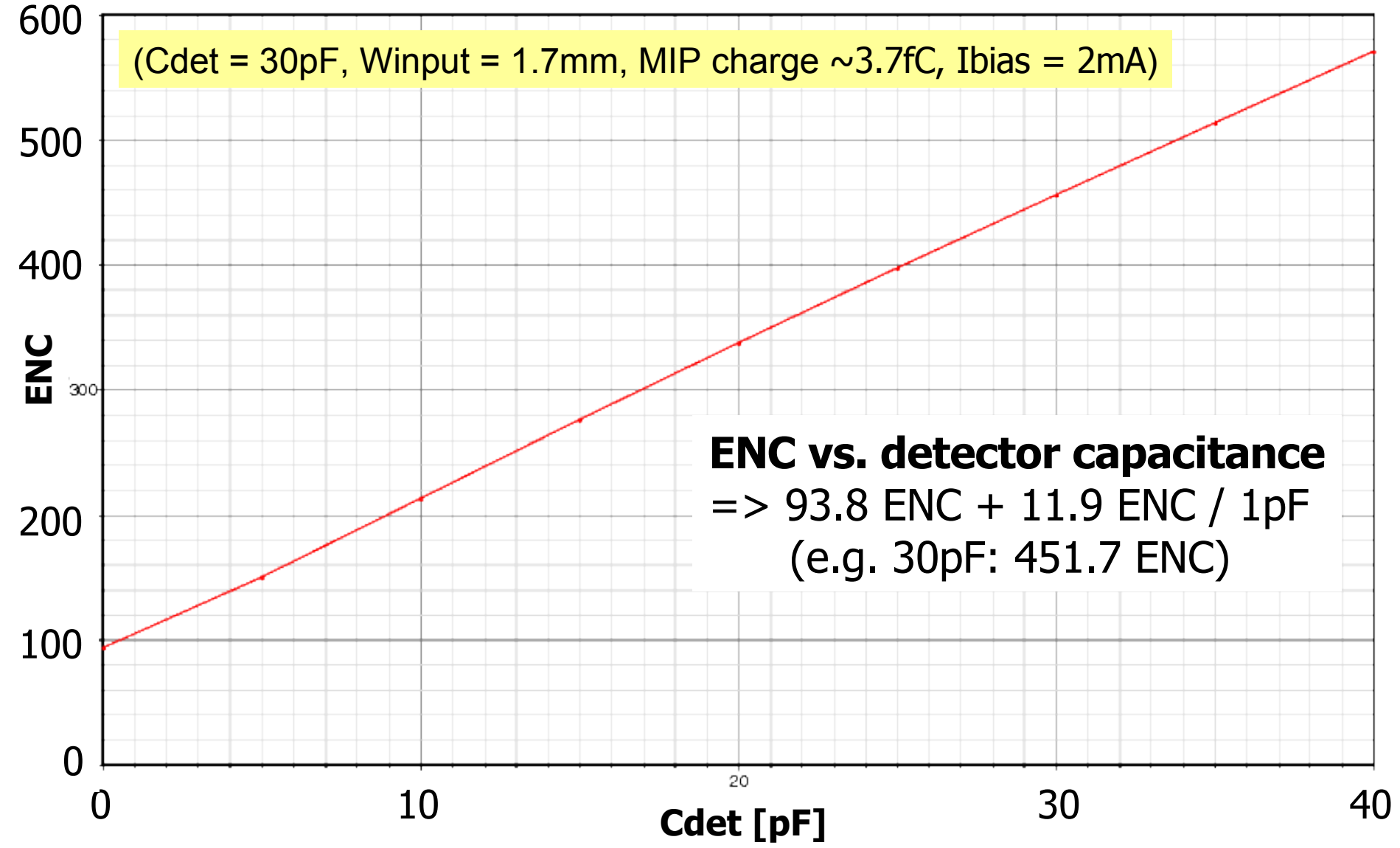


Digital discriminator output:
Hit @1us => 24ns peaking time

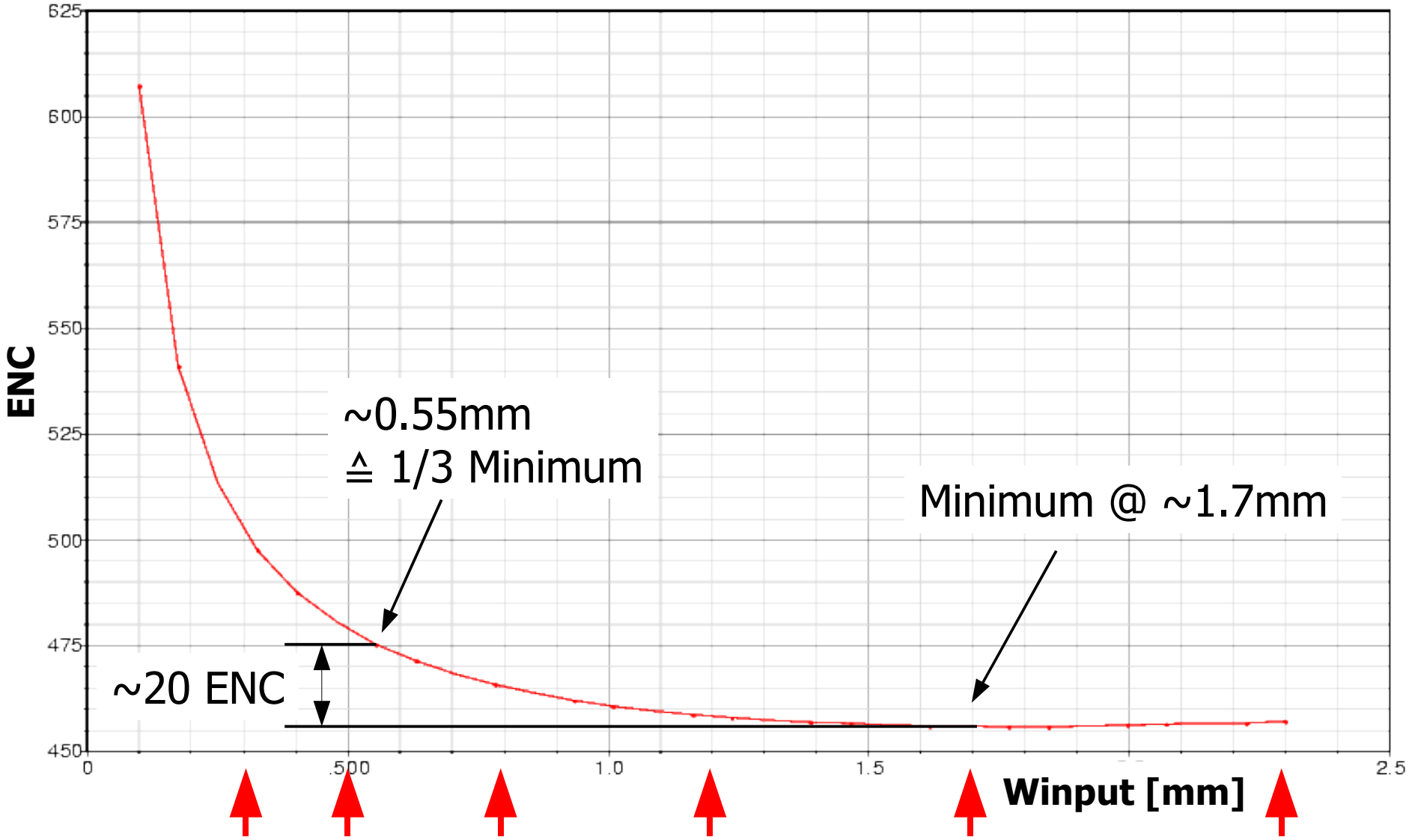
Noise simulation

- Noise sources:
  - White noise in all UMC MOS models (preamp, shaper, fb, pz)
  - No 1/f noise contribution
  - No Leakage current (low contribution at fast shaping times)
  - White noise of UMC resistor models (feedback)
- Gain was determined from transient simulation (possible shaping loss included)
- rms noise [Volt] was calculated via noise simulation
- ENC = rms/gain

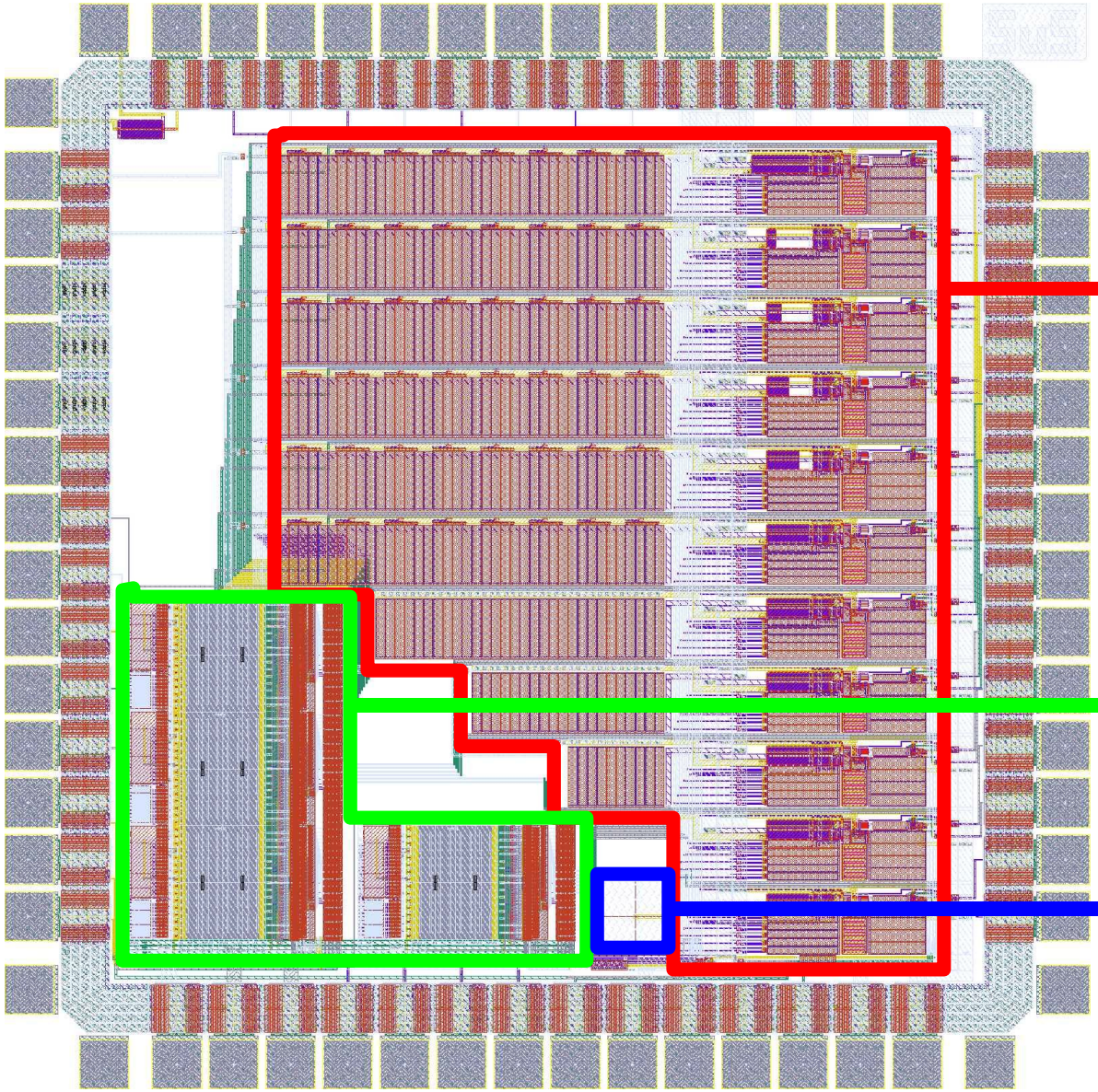
Equivalent noise charge (ENC) simulation



ENC vs. input transistor size (simulated)



Chip Layout

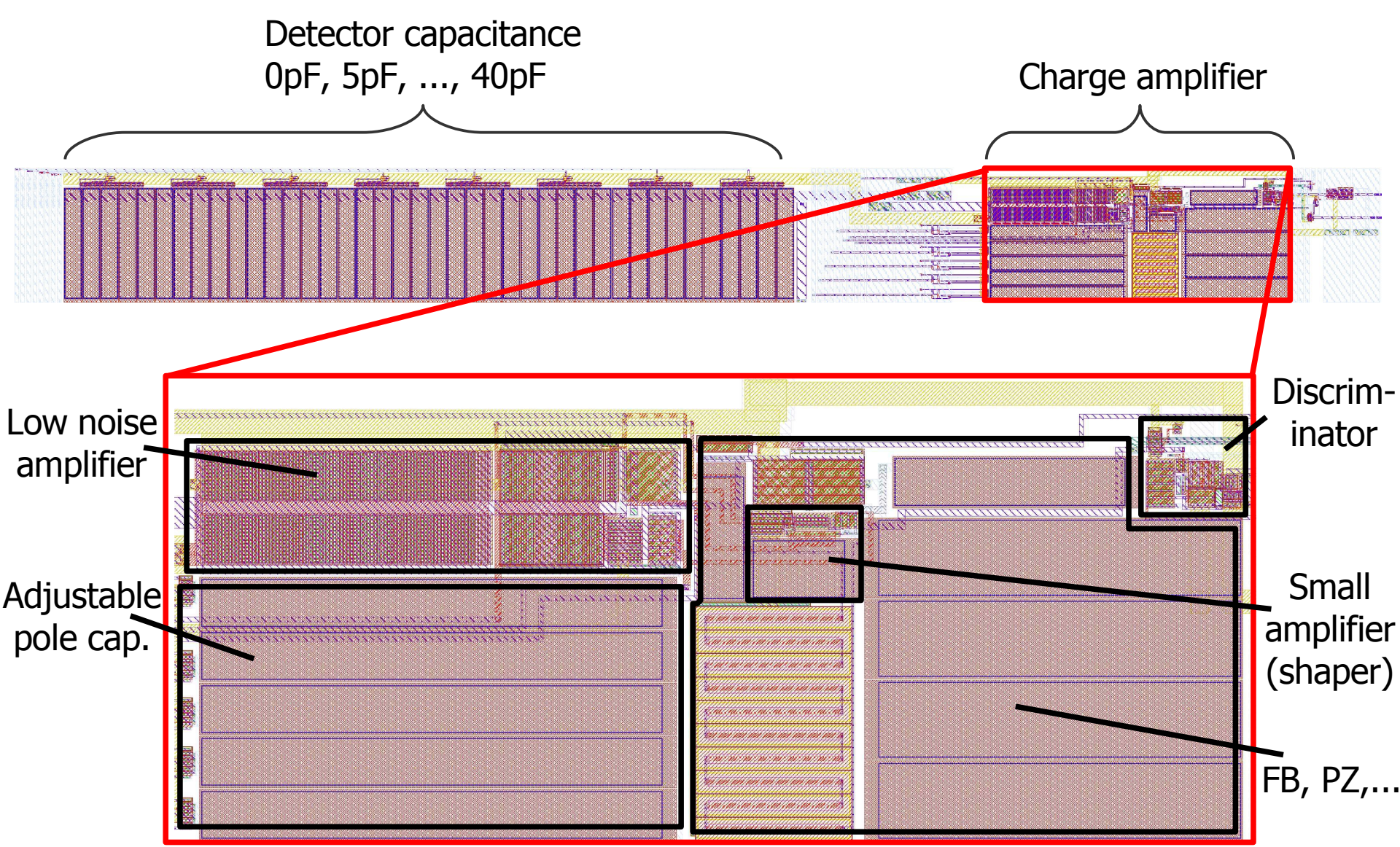


11 channels
- Various sized input transistors
- Fixed and scalable detector capacitances
- Digital and analog outputs

4 Bias DACs
- Internal bias voltage generation
- Configuration register

N-well detector diode
- To measure real particle hits

Channel Layout



Summary

- UMC018 mini@sic (1.5mm x 1.5mm)
- Power consumption per channel: ~4 mW
- ~452 ENC for MIP @ 30pF detector capacitance
- Rise-time (hit to max. output): ~87ns analog, ~24ns digital
- Size of CSA in layout (without Cdet): ~100µm x 260µm

CSA testchip was submitted on 19 February,
first measurements will be available in the middle of July!

Noise comparisons to 0.35µm and 0.13µm are in preparation