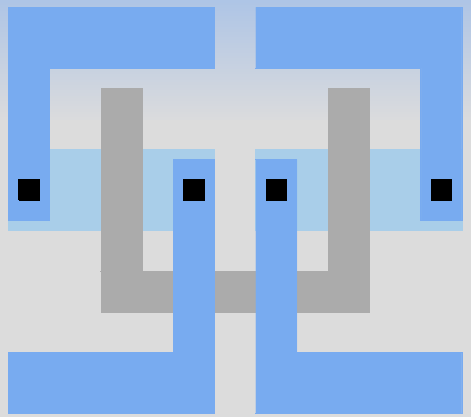
First results of CSA Testchip



Schaltungstechnik
und Simulation

Tim Armbruster

tim.armbruster@ziti.uni-heidelberg.de

11. CBM Collaboration Meeting

in Darmstadt

26.02.2008 - 29.02.2008

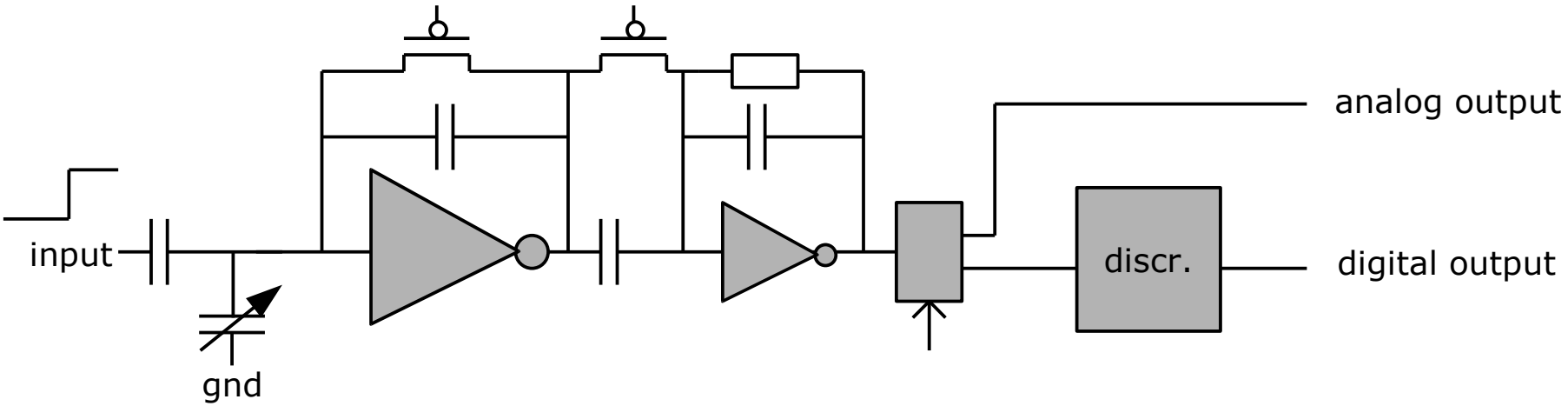
Chip Overview

Reminder: Goals and Features

- **Chip goals**
  - Gain more experience in UMC018 technology
  - In general: Compare simulations and measurements
  - Main focus on noise:
    - How good are the spectre models?
    - What about flicker noise?
    - Check theory: ENC dependency on detector cap., on input transistor size, ...

- **Main Characteristics**
  - Common designed charge sensitive amplifiers
  - 11 channels, each with different parameters:
    - Switchable detector capacitors (on chip)
    - Switchable dominating pole of preamp
    - Different sizes of input transistors
  - Each channel has disriminator
  - All bias currents are generated via internal DACs

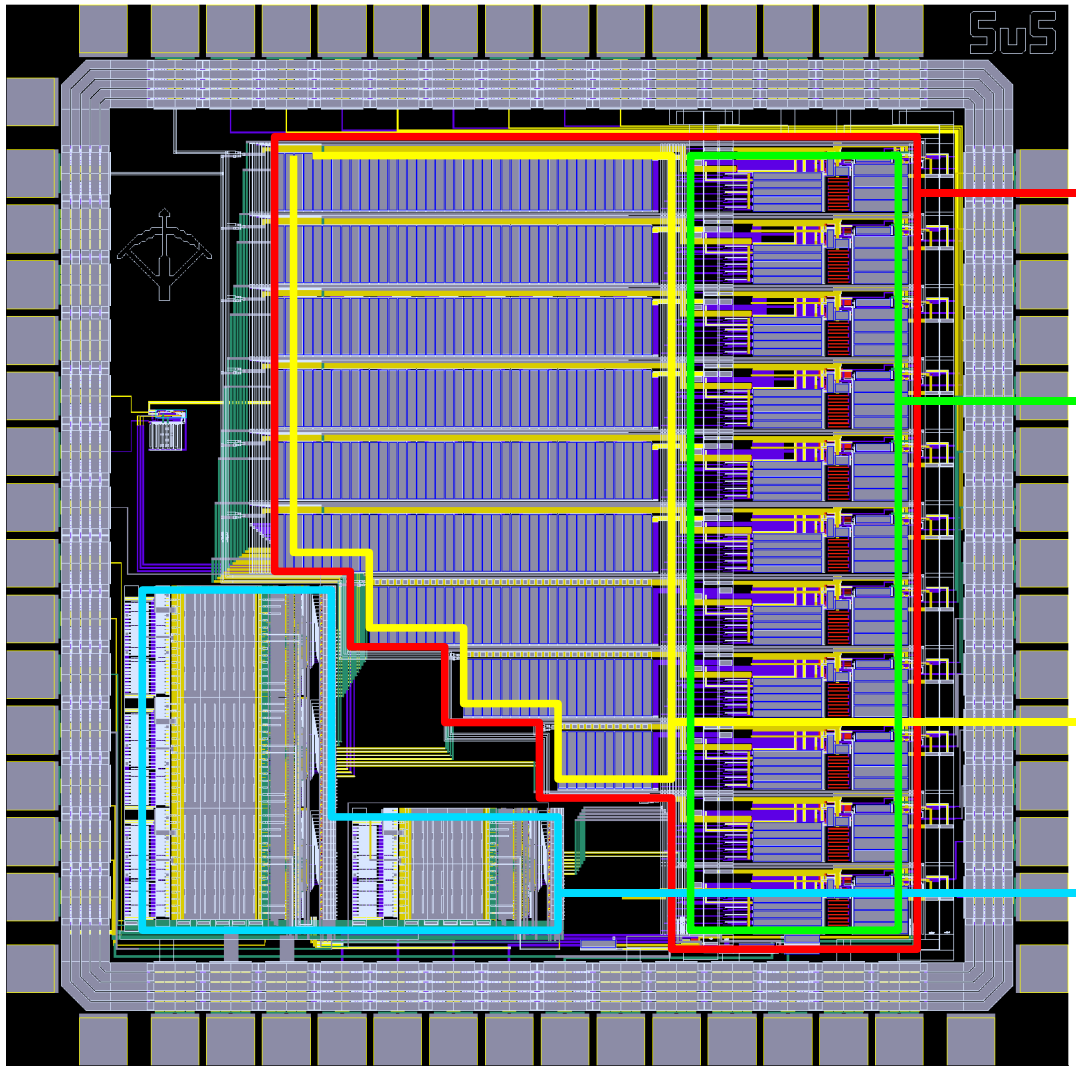
Block Diagram



Design parameter

- Input:
  - AC coupled, input cap. 3fF
  - => Voltage step for MIP (23ke) = 1.22V
- Detector capacitance: 0..40pF (5pF/step)
- Preamp:
  - Folded cascode
  - Cf: 250fF
  - Different sizes of input n-mos
  - O'Connor Feedback
  - Dominating pole is switchable
- Shaper:
  - Folded cascode (1st order)
  - AC coupled to preamp
  - Gain: 5pF/500fF = 10
  - RC time = 300kΩ * 500fF = 150ns
- Switchable outputs:
  - Analog shaper output
  - Digital discriminator output
- Power (sim.):
  - ~2mW per channel (11 channels)

Layout



11 Channels

Preamp, Shaper, Disc.,...
100µm x 280µm
(>50% of area cap. + res.)

Detector capacitors
(some are not switchable: no noise contribution of switches)

4 Current DACx
(bias + config. register)

Measurements

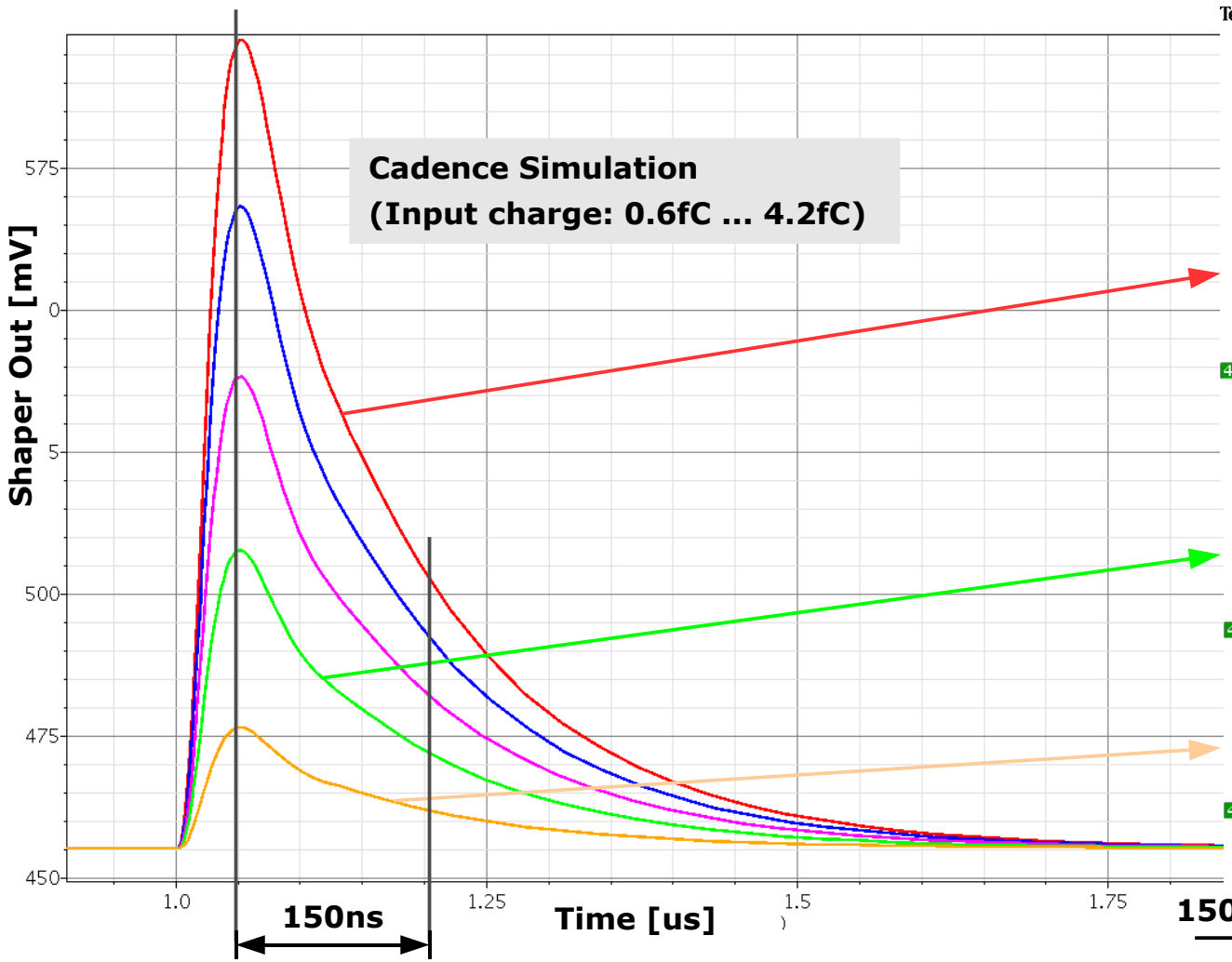
Test Setup and First Steps

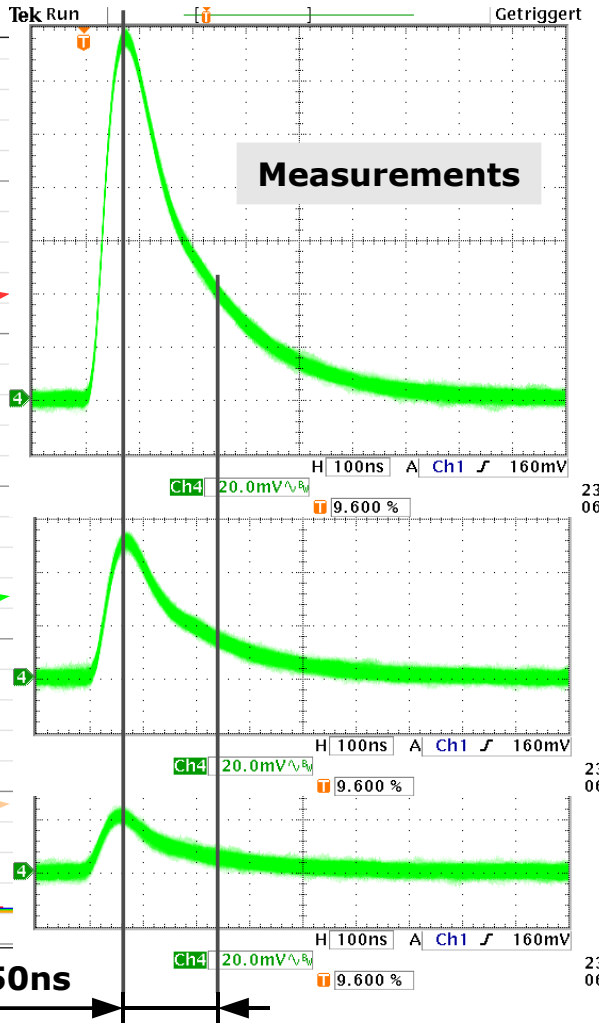
Chip has just arrived last Tuesday!

=> Only some very first results can be presented here.

- **Test Setup**
  - Chip attached to self-made PCB
  - PCB pluged on our "Uxibo" (simple FPGA Board with USB)
  - Analog measurements can directly be made via PCB connectors
  - Digital results (disc. outputs) are send to PC (via Uxibo)
- **First Steps**
  - Power consumption ~40mW, goes to 18mW if channels are switched off -> ok!
  - DACs works as expected, all bias voltages/currents are correct
  - Note: All following results are obtained from channel 3 (input transistor size W/L = 0.8mm/180nm)

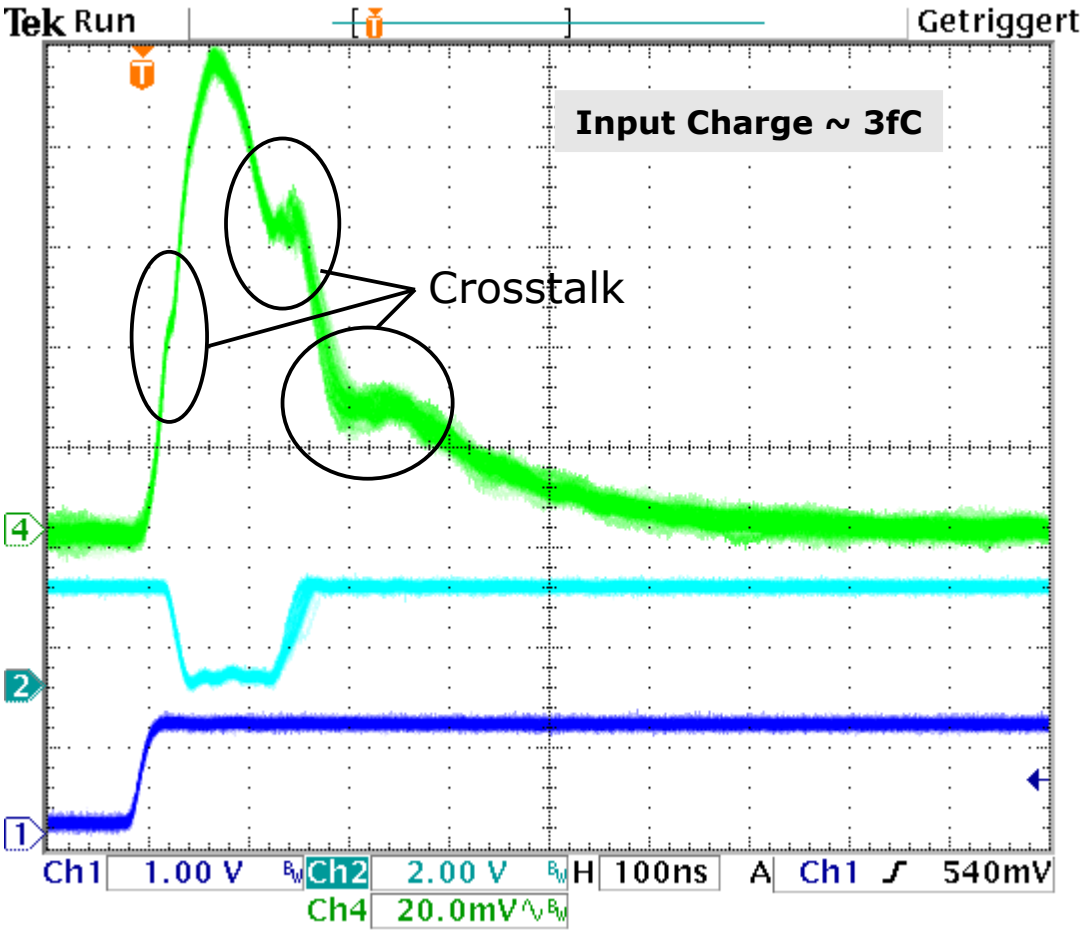
Pulse shapes





- RC-time: Simulation = Measurement = 150ns
- Amplitudes: No differents between sim. and meas. visible!

Discriminator



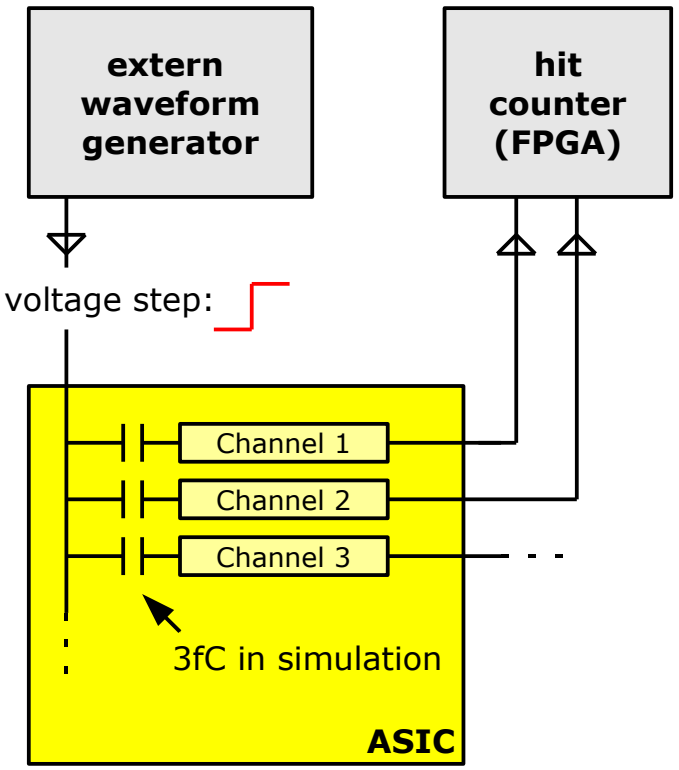
Shaper output

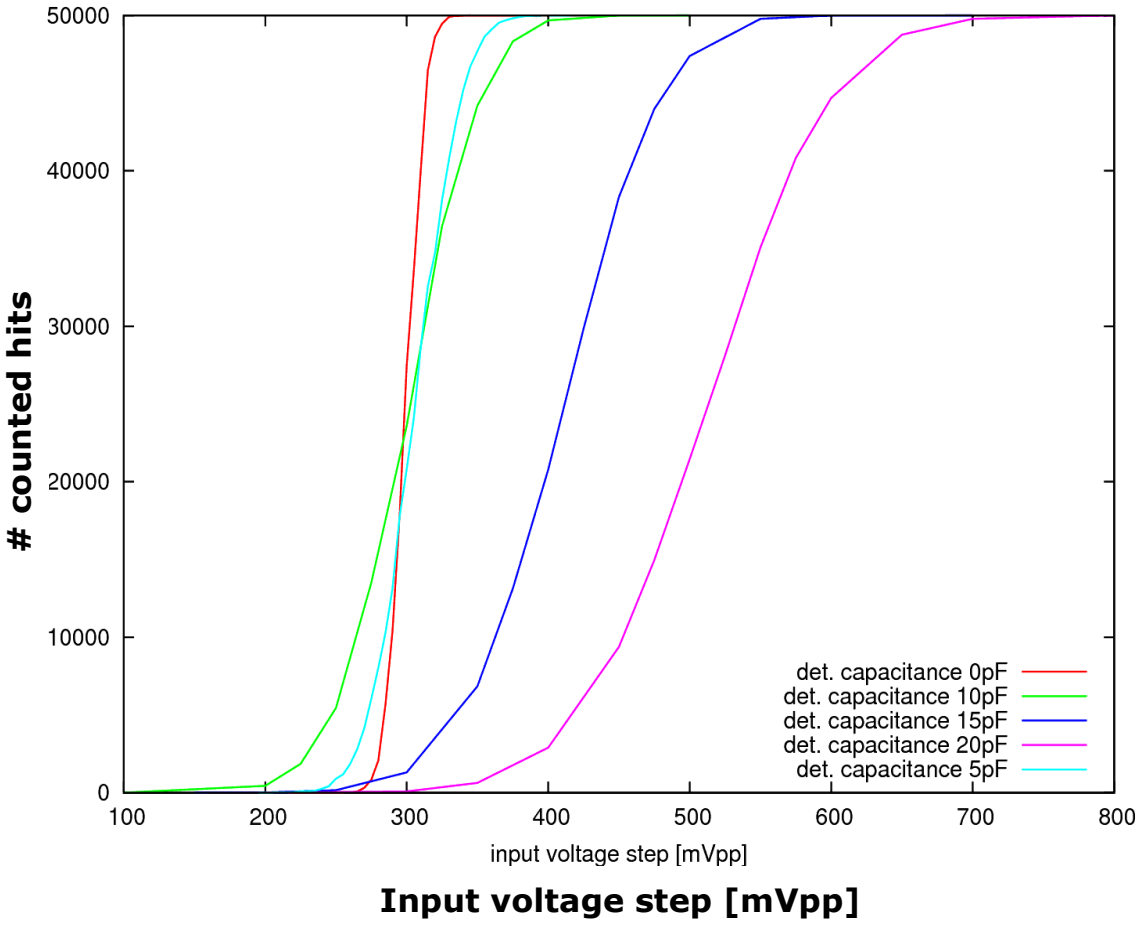
Discriminator output

Input voltage step

- Discriminator works fine
- High load of discriminator output (probe, FPGA input pin, PCB wires) causes crosstalk to shaper (uncritical)

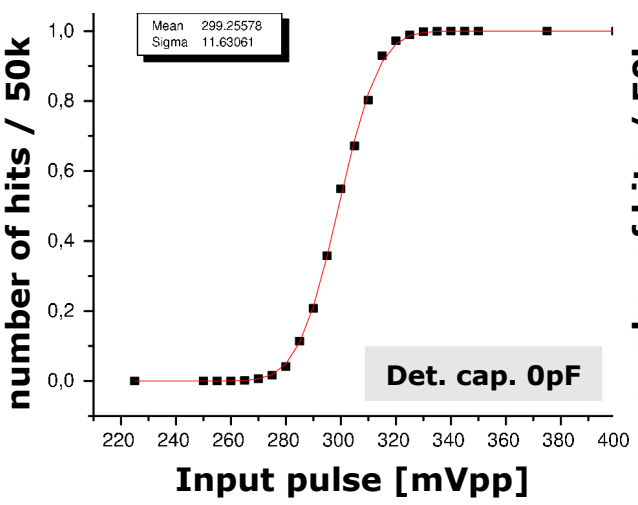
Threshold Scan (s-Curves)

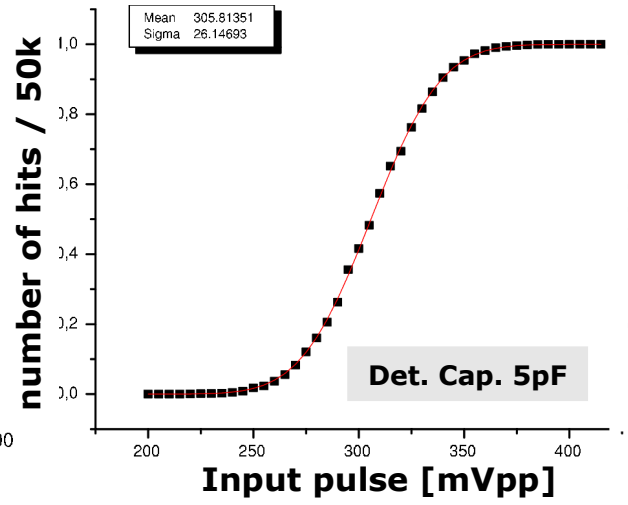


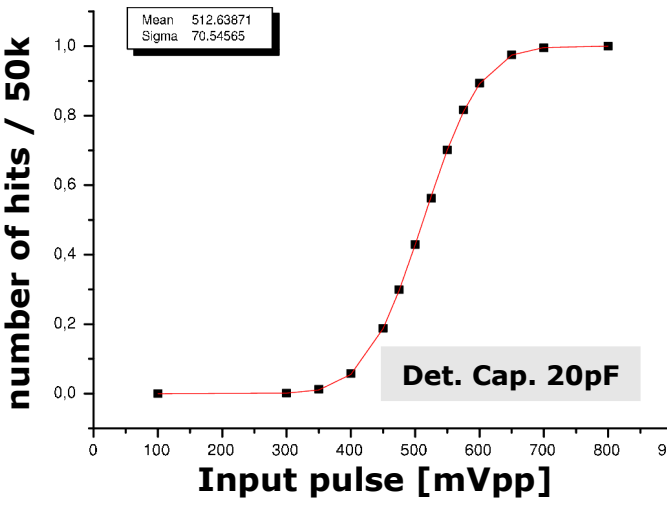


- 50000 hits/input voltage injected -> results counted via FPGA
- Different curves: Det. capacitor (channel 3) changed: 0pF, 5pF, 10pF, 15pF, 20pF
- Noise increases (as expected)

Gauss Fit (s-Curve)

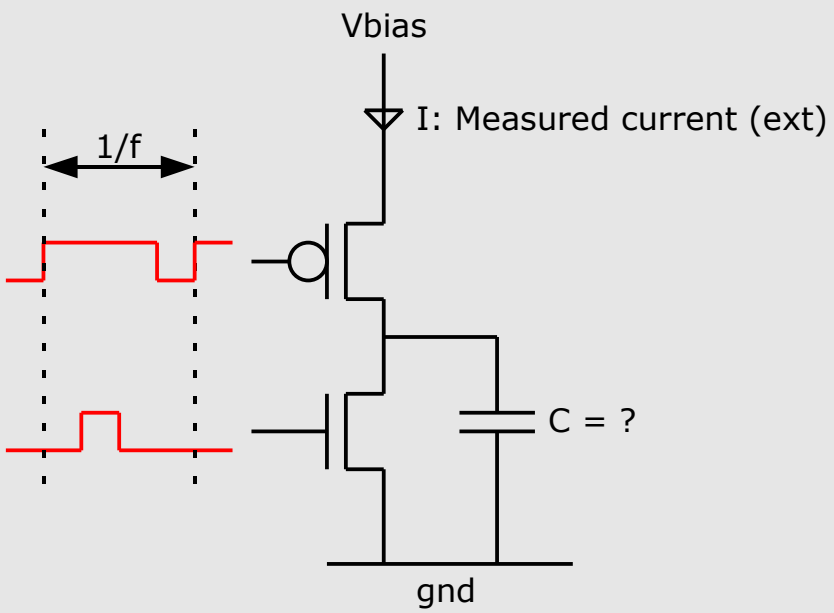




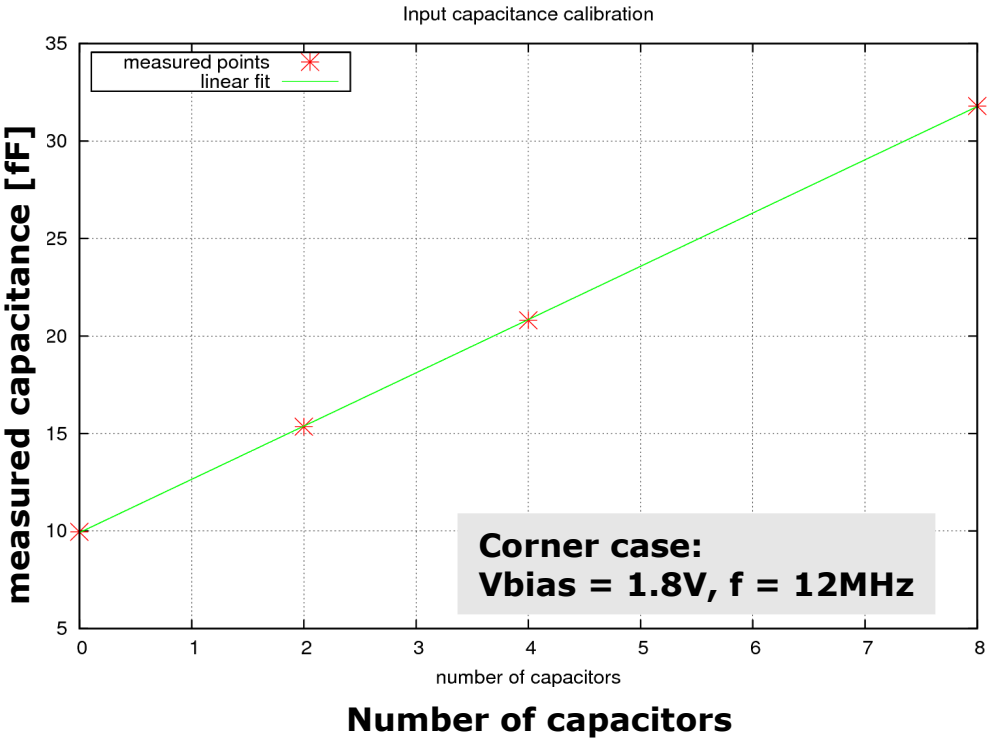


- Sigma (standard deriv.) evaluated from each s-Curve via Gauss fit (plots above)
- Calibration:
  - For ENC input amplitudes must be refered to input capacitor
  - Exact measurement of input capacitor needed...

Calibration of Input Capacitor



- Simple charge pump circuit on chip
  => C = avg(I) / (Vbias * f)
- Corner cases:
  - Variate f and Vbias
  - 4 circuits: 0, 2, 4, 8 * C

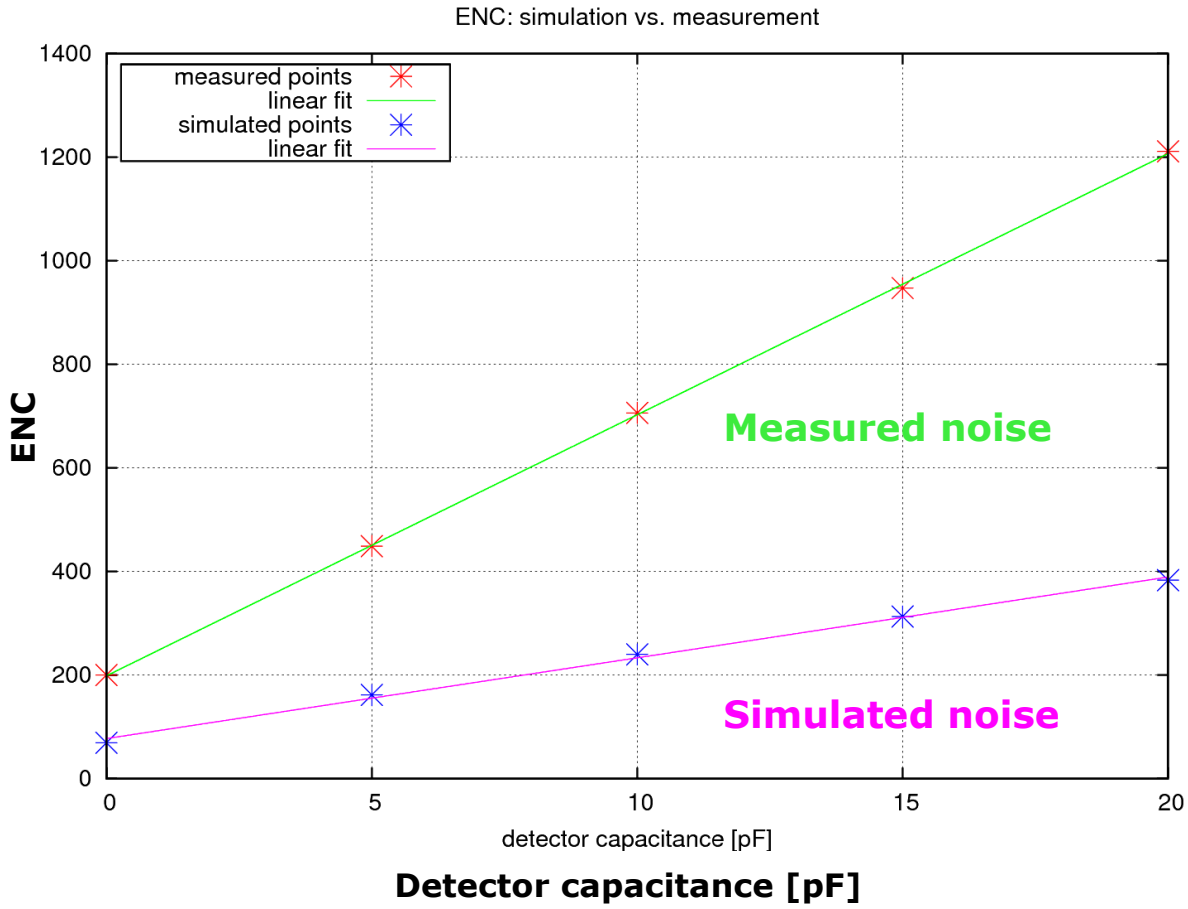


Number of capacitors

=> "Real" input capacitor ≈2.75fF (3.0fF sim.)
=> Variation of 8.3%!

Need to test more corner cases...
(For following ENC calculation, 2.75fF is assumed)

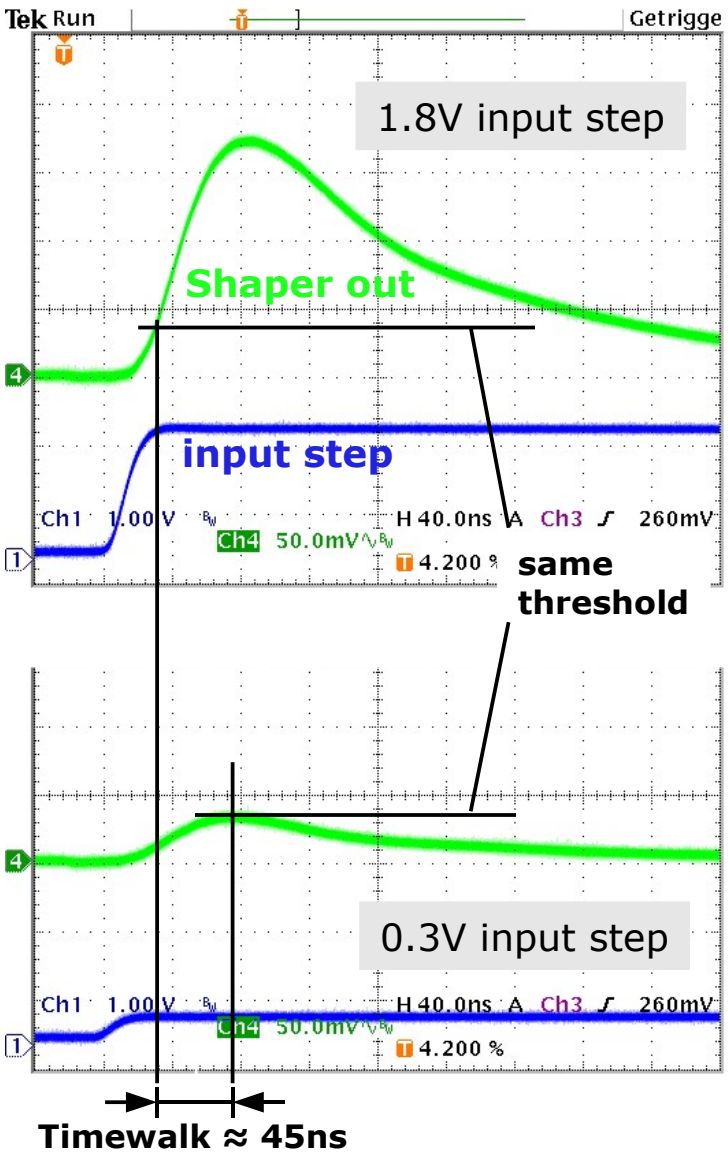
Noise: Simulation vs. Measurement

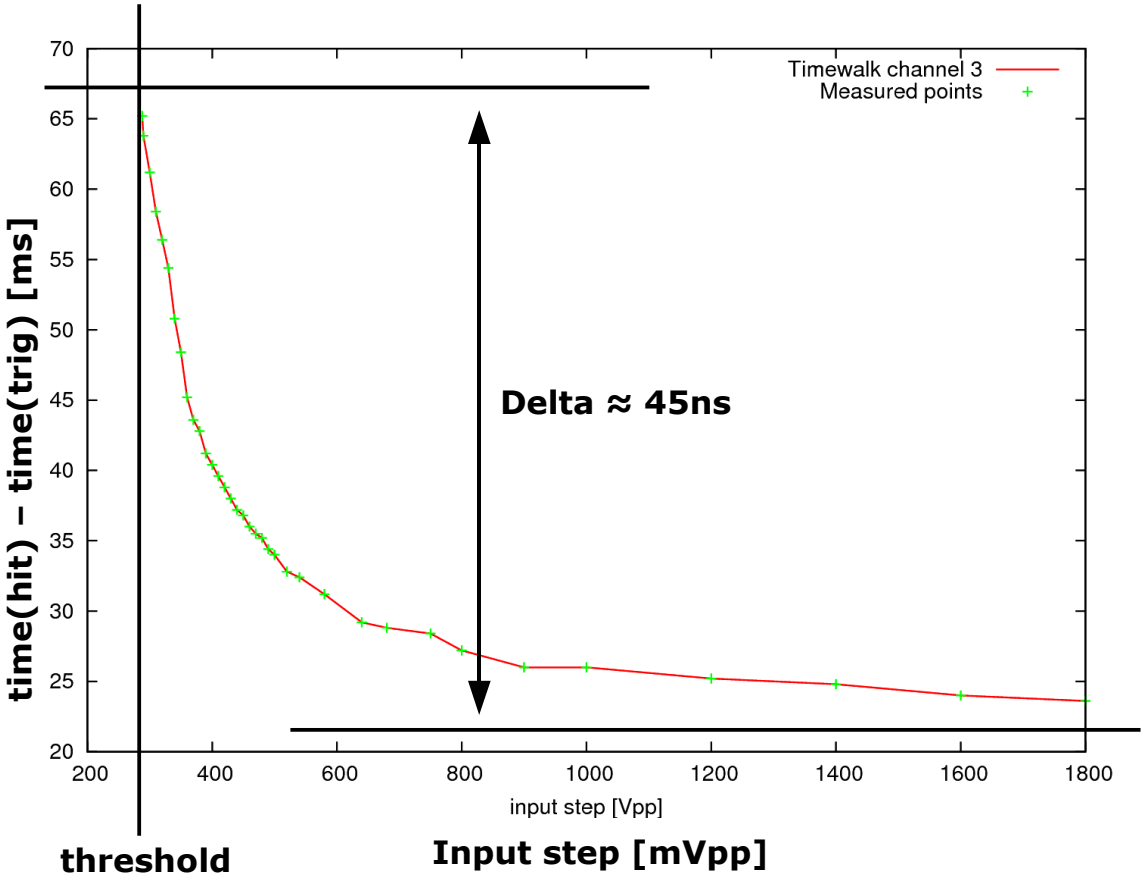


Simulated noise: 68e + 15.7e/pF vs. Measured noise: 199e + 50.5e/pF

=> Measured noise is about 3 times larger than in simulation

Timewalk





=> “Visual” timewalk equals measured timewalk

But: Rise-time of used input signal very large (25ns), real timewalk may be something smaller -> TODO

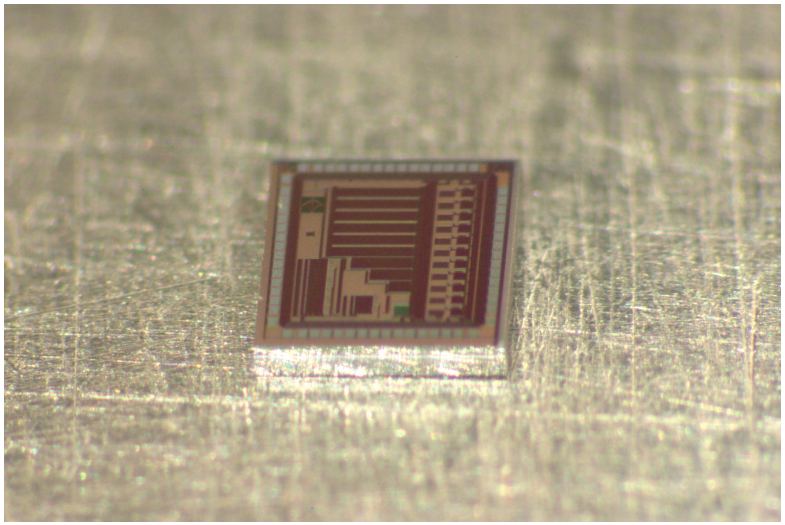
Future Plans

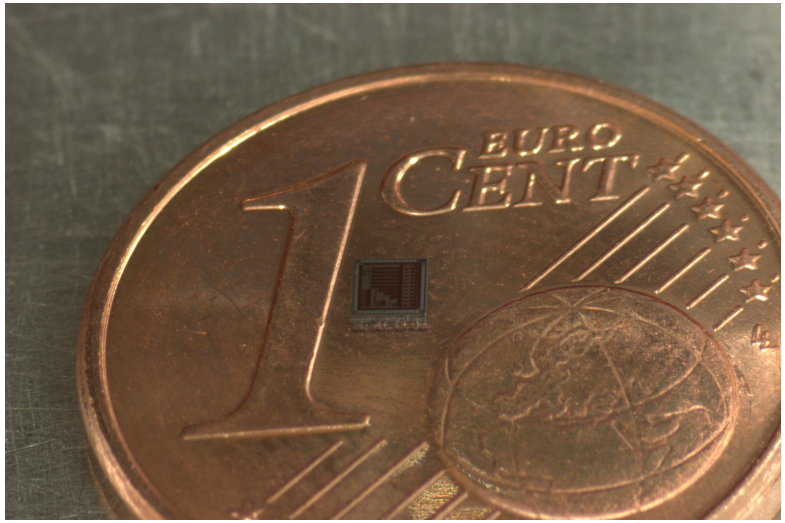
Unsolved Problems (only one chip tested...):

- Feedback voltage (O'Connor fb.) must be set ≈300mV smaller than in simulation
- Noise much larger than in simulation -> 1/f noise? -> Adjust bias voltages?
- First two chips attached to PCB didn't work

Open tasks:

- Optimization of setup for minimum noise
- Automated measurements
- Compare to simulation: noise/timewalk vs. Cin/Cdet/bias/...)
- Figure out double hit precition (two input capacitors per channel available)
- Test all 11 channels
- Test some more chips





Thank you!