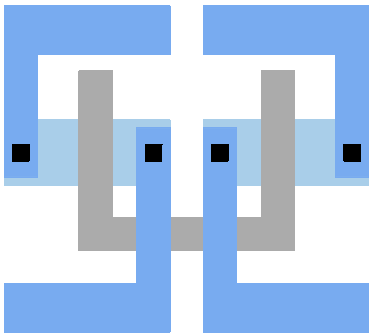
UNIVERSITÄT HEIDELBERG

2nd CSA Test ASIC

New Submitted Charge Sensitive Amplifier Test Chip for Application in STS or TRD



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12. CBM Collaboration Meeting in Dubna

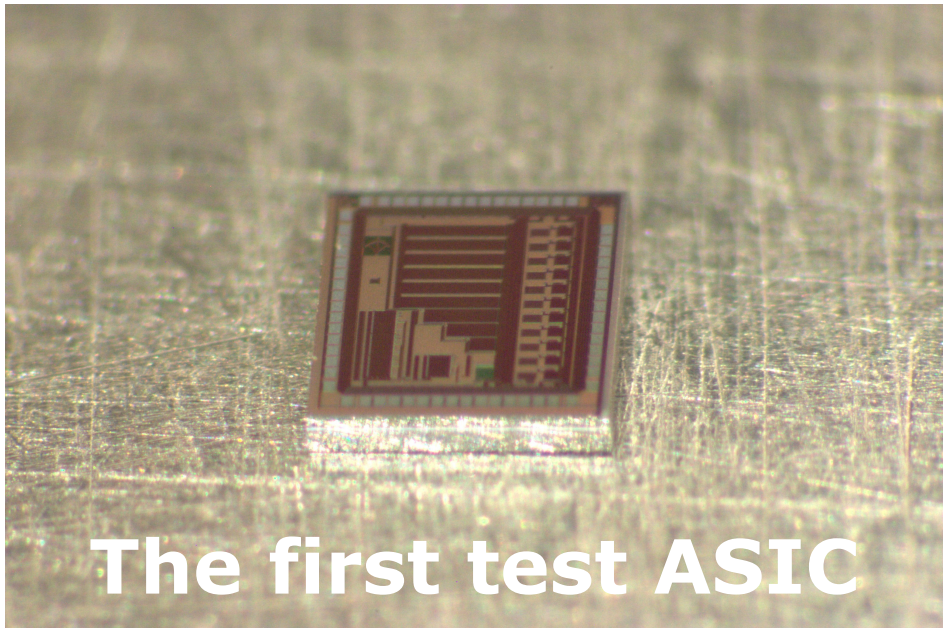
October 2008

Introduction

The **first UMC018 test ASIC** has been designed and tested some time ago (as it has been reported):

- 11 channels on a MPW Mini@sic
- Very simple preamp/1st order shaper topology
- Differential discriminator with C-MOS output
- Layout and design were more or less tentative

=> Chip worked well in lab, but some results were not as predicted by simulation (e.g. too high noise)



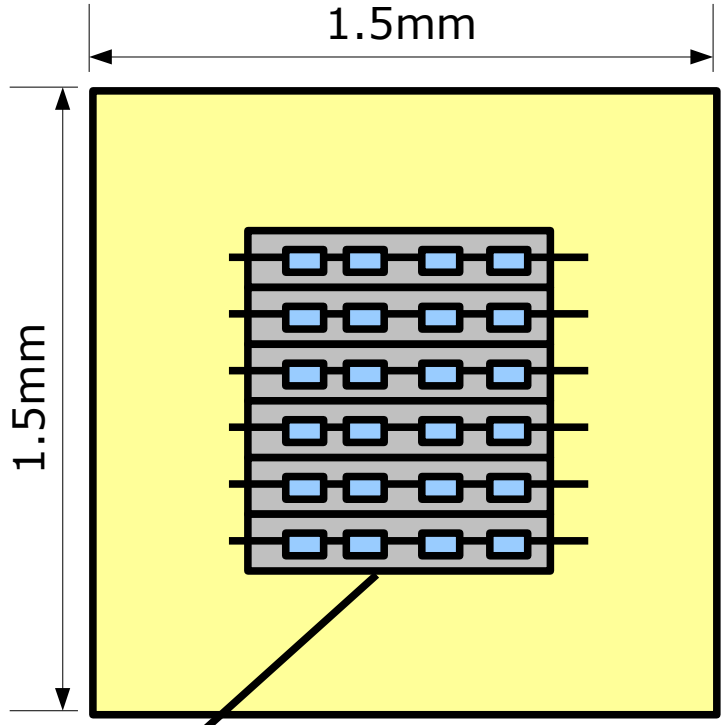
Now, we have just **submitted a second iteration** of the test chip nearly from scratch, also providing some new features...

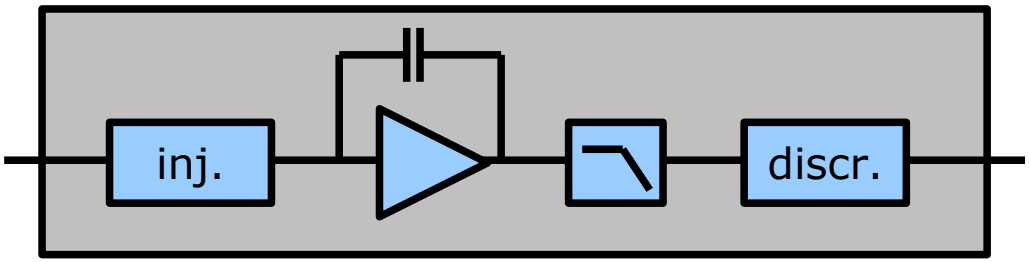
2nd Test Chip - Overview

The new test chip:

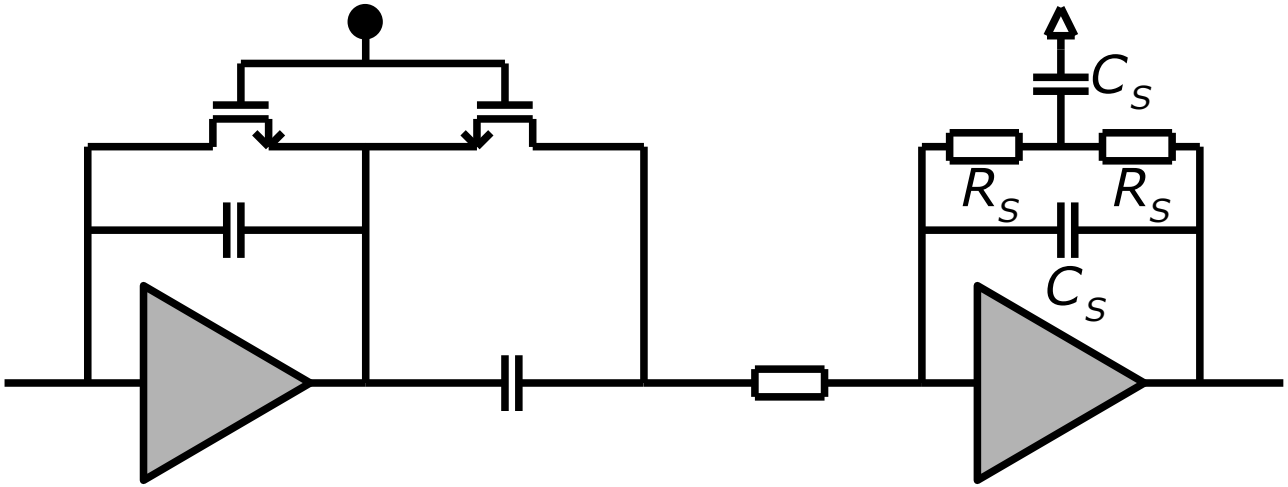
UMC018 MPW Mini@sic (1525µm x 1525µm)

- 26 channels
- Channel pitch is 40µm
- Each channel consists of
  - Injection circuit
  - Preamplifier
  - 2nd order shaper
  - Discriminator with CML-output
  - Local threshold trim DAC (8 bit)
  - 15 bit configuration register
- 7 global DACs (8 bit) for bias generation





Preamplifier/Shaper Circuit



$$with\ \ H(s) \approx \frac{A_{DC}}{(1+sR_sC_s)^2}$$

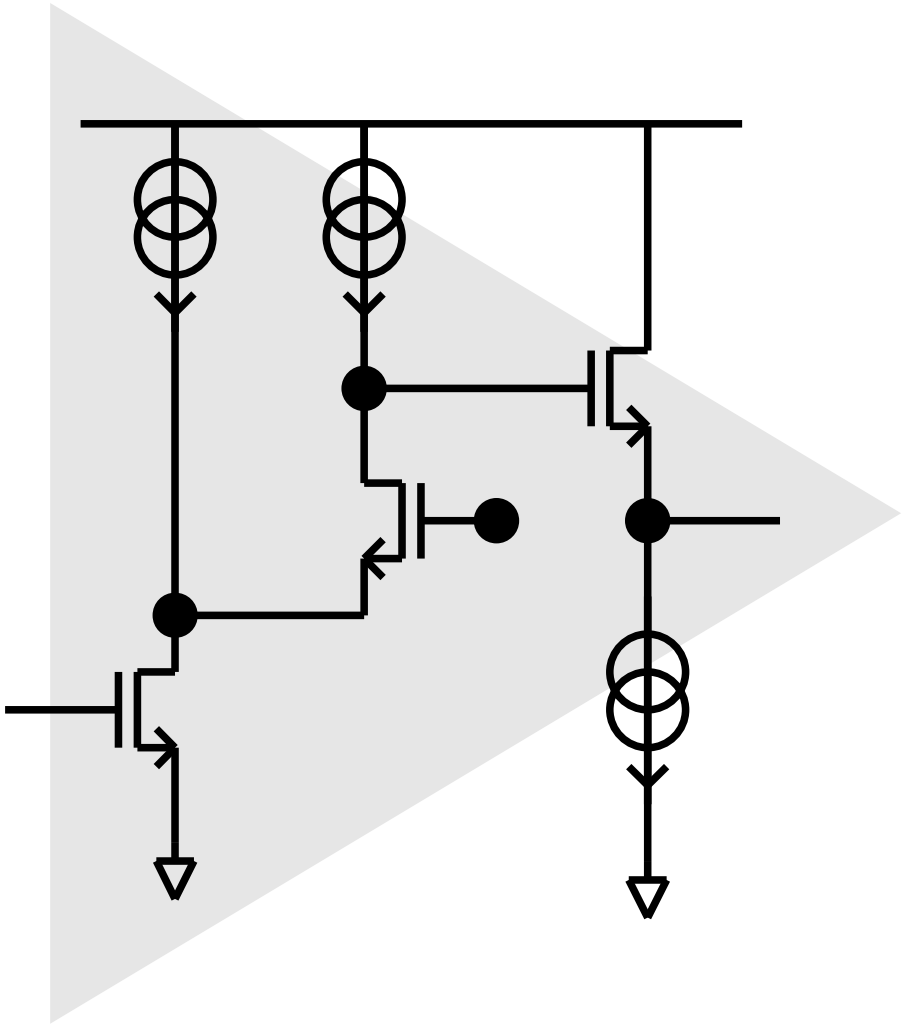
- Preamplifier with PZ-canceling O'Connor MOS feedback
- 2nd order shaper with two real poles:
  - Good matching required
  - But: Matching only between components of the same type!
- Circuit is optimized for positive charges (N-MOS feedback)
- Chosen shaping time is 80ns (200kΩ, 400fF)

Only one amplifier-cell is used for both, preamplifier and shaper.

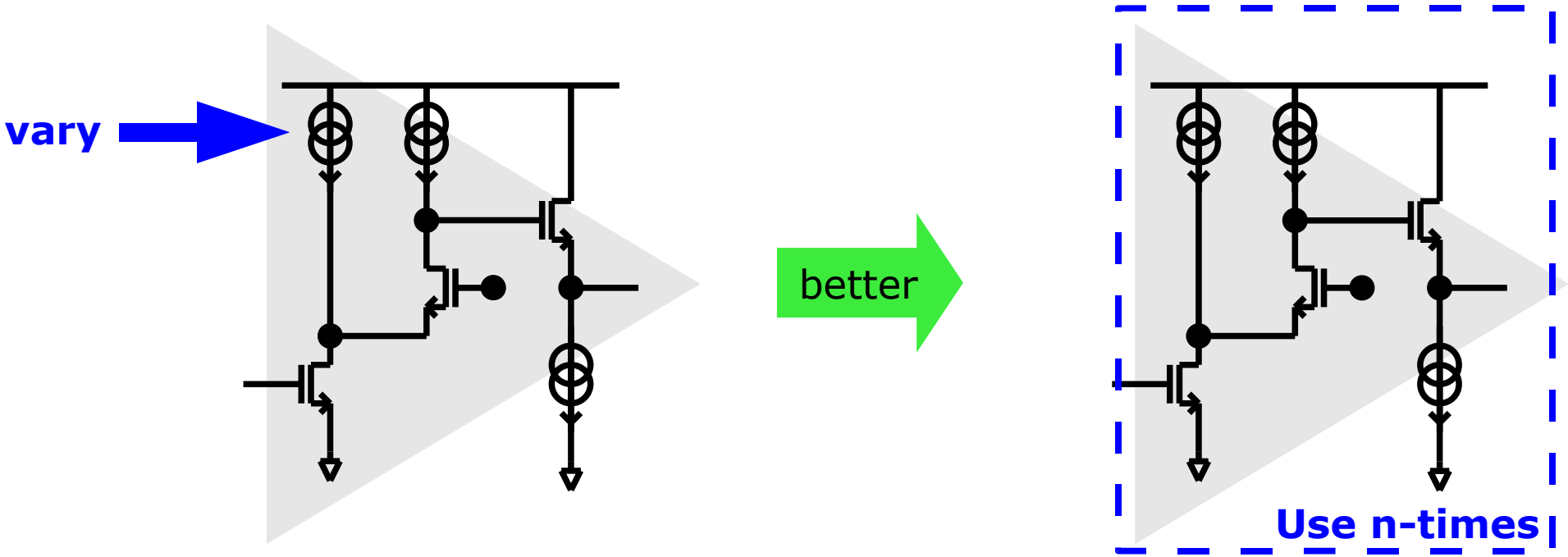
Preamplifier uses n parallel instances of same amplifier-cell (cell is scaled).

Voltage Amplifier Cell (VAC)

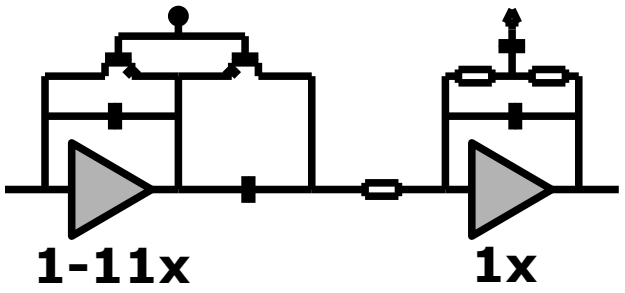
- **Gain stage with straight cascode**
  - Cascode faces upwards to maximize current through input MOS
  - NMOS input for maximum gm (flicker noise in simulation not significant)
  - Transconductance of input MOS ~ 3.1mS/instance
  - Typical power (adjustable): 0.3mW/instance
- **Source follower** is used as level shifter and unity gain buffer
- **Miscellaneous**
  - Compact layout, the cell has been designed for easy scaling
  - The cell has been used for the preamplifier (scaled) and for the shaper => same input DC-levels
  - All bias voltages are decoupled in cell



Scaling of Voltage Amplifier Cell (VAC)



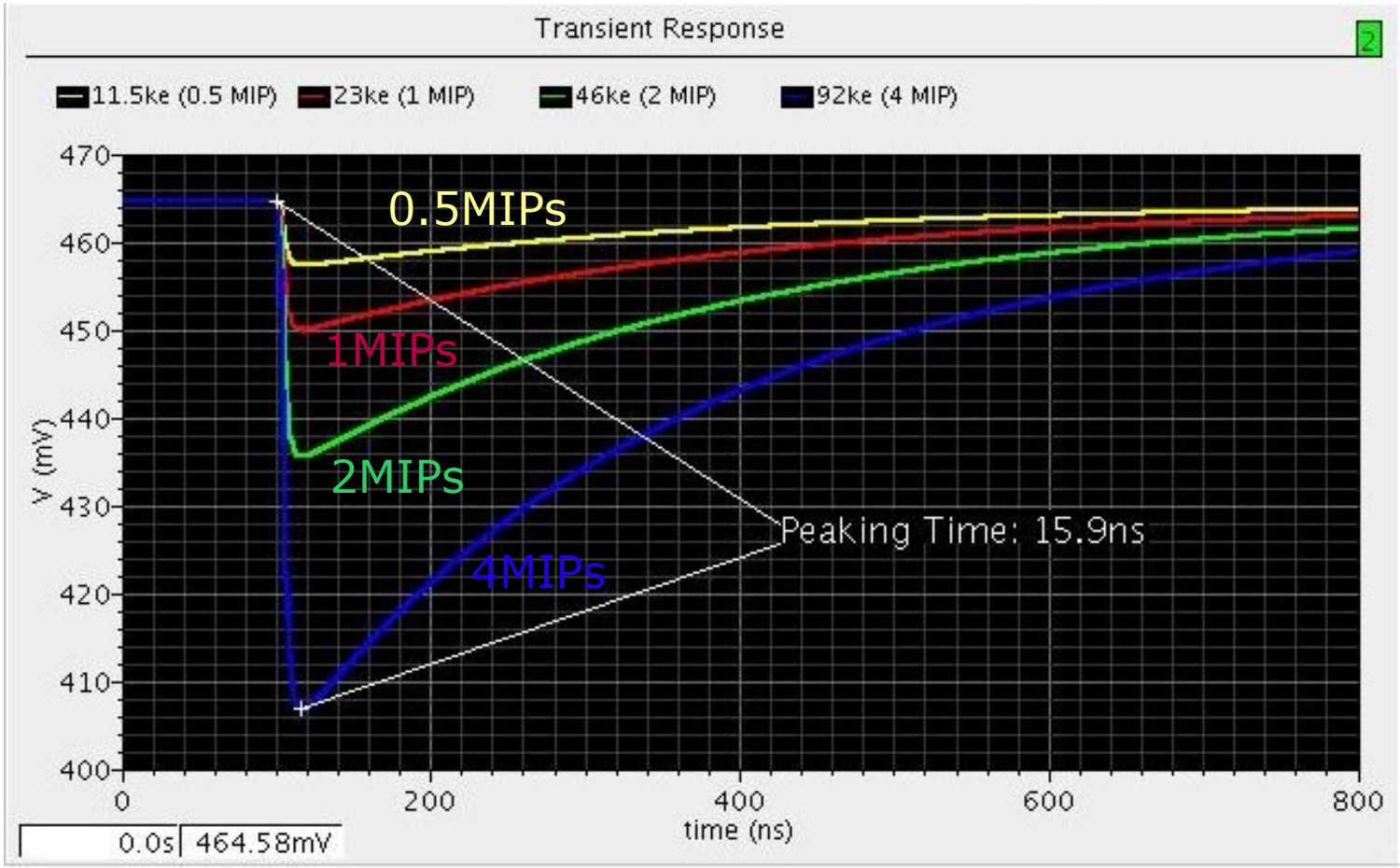
- We want to figure out: How does noise depend on power?
- Simple method: Variation of bias currents
  - But: this also shifts the operating points
- It's probably better to use the same cell n-times
  - But: this also scales input capacitance, layout size, ...



Both "methods" available on this chip

- 20 "normal" channels - preamp: 11x VAC, shaper: 1x VAC
- 6 test channels - preamp: 1,3,5,7,9,11x VAC, shaper: 1x VAC

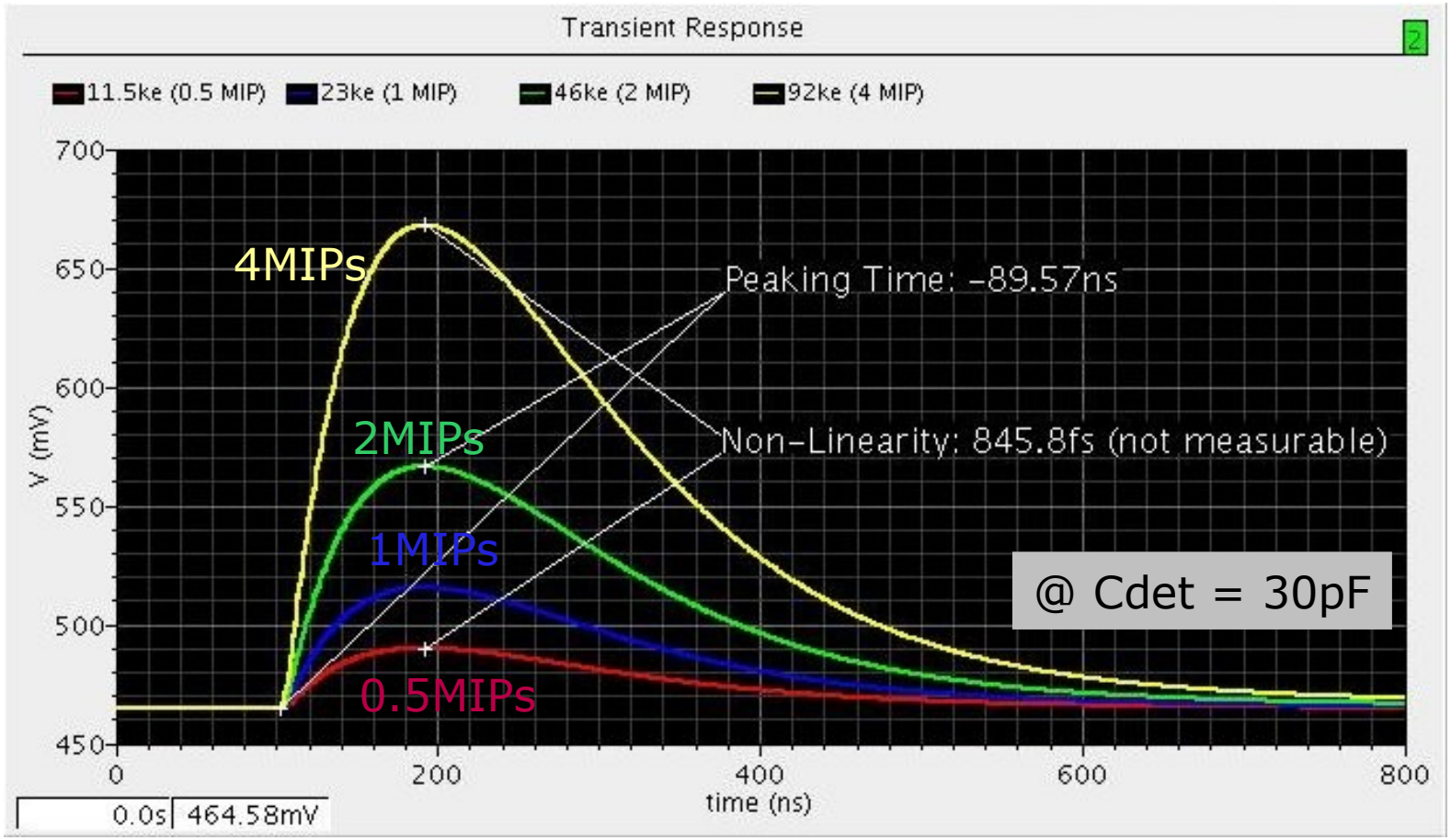
Transient Simulation Preamplifier



From simulation (11x VAC-instances, 3.3mW, Cdet = 30pF):

- Peaking time (0% - 100%): ≈16ns
- Rise-Time (10%-90%): ≈9ns
- Pulse length adjustable (current DAC -> bias for O'Connor FB)

Transient Simulation Shaper

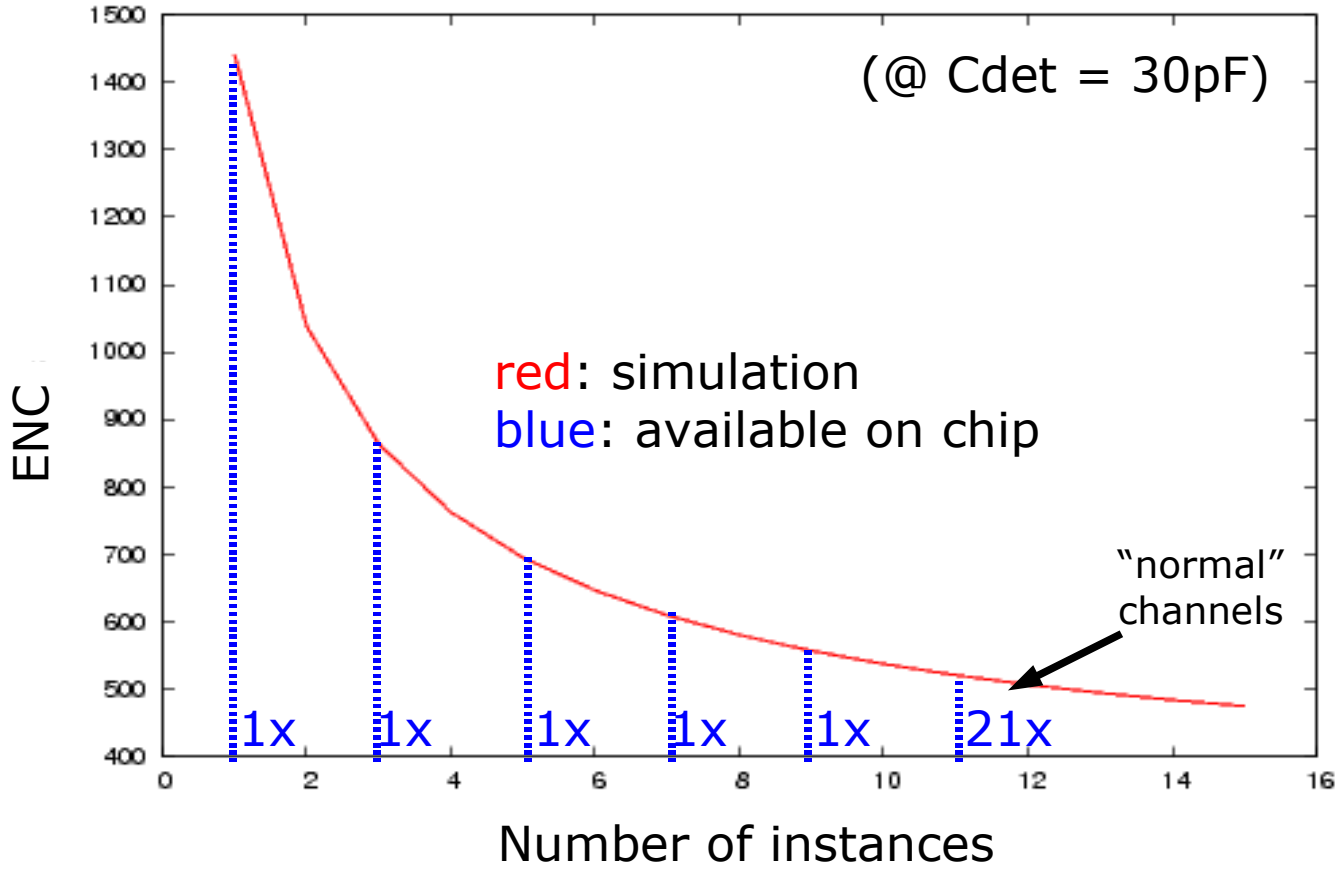


- Peaking time (0% - 100%): ≈90ns
- Rise-Time (10%-90%): ≈50ns
- High linearity, **range up to 13 MIPs** (a 23ke)
- Gain: 13.8mV/fC (=> amplitude for MIP ≈50mV)

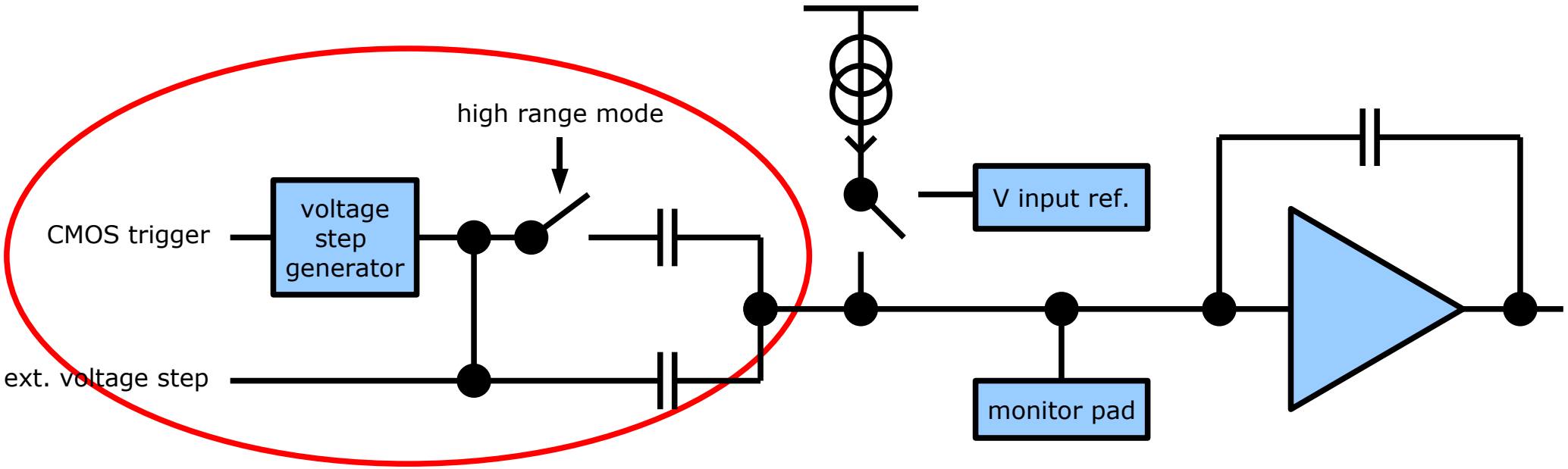
Noise Simulation

Simulated noise (ENC): 138e + 11.36e/pF (=> e.g. 479e @ 30pF)
(for preamp with 11x voltage amplifier cell (VAC), 3.3mW)

Noise vs. number of VAC instances (in preamplifier):

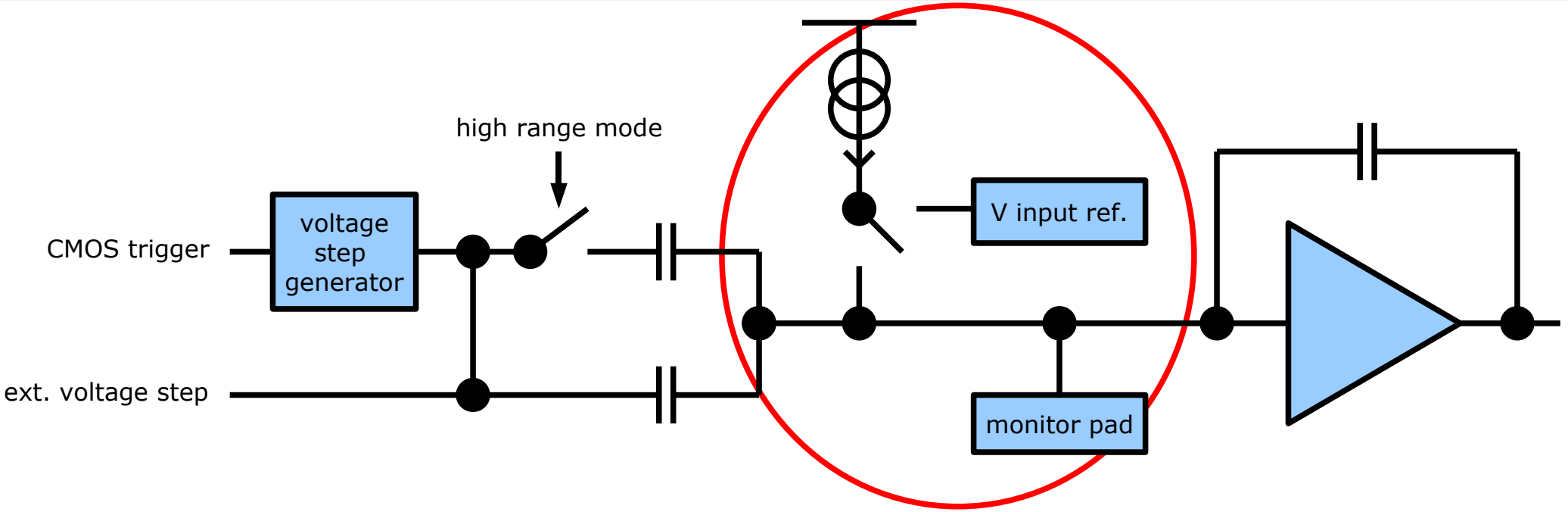


Injection Circuit 1/2



1) **Internal voltage step injection** (pos. and neg. charge)
   - Voltage step generator is triggered by external C-MOS signal
   - Low and high range mode:
     - Up to 1.2MIPs with higher granularity
     - Up to 12 MIPs with lower granularity
   - Short pulses (~ 3ns)
2) **External voltage step injection** (pos. and neg. charge)
   - Same range like internal voltage step injection
   - Pulse-length depends on rise-time of external voltage step

Injection Circuit 2/2



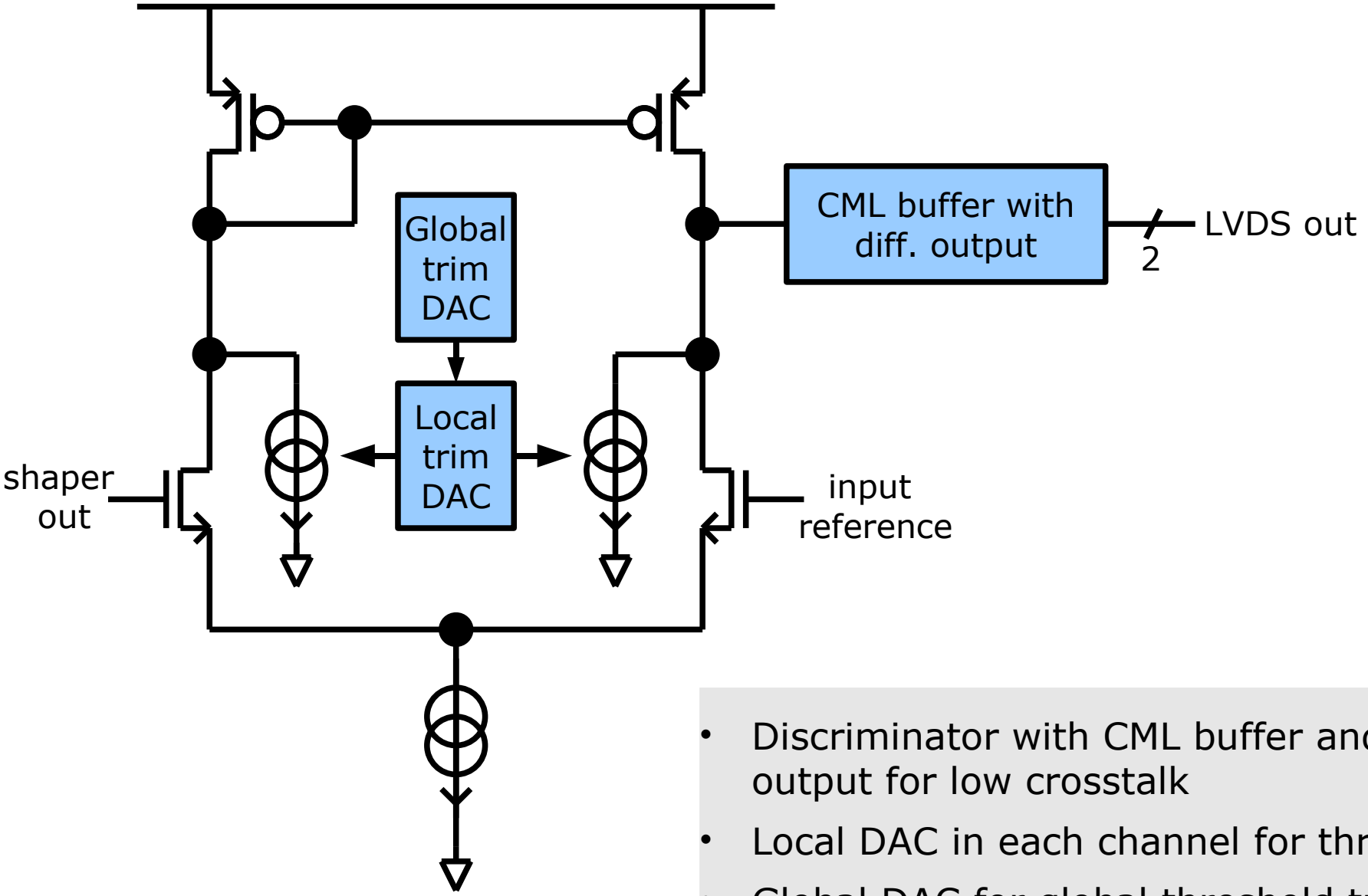
3) **Internal current pulse injection** (pos. charge only)

- Current source is switched between input reference voltage and amp. input node
- External differential control signal required
- Pulse length depends on switching speed
- No upper limit for magnitude of injected charge

Features

- Monitoring pad for calibration, measurements or even direct injection
- Every part can be enabled/disabled by internal control register (not sketched here)

Discriminator



- Discriminator with CML buffer and LVDS output for low crosstalk
- Local DAC in each channel for threshold trim
- Global DAC for global threshold trim

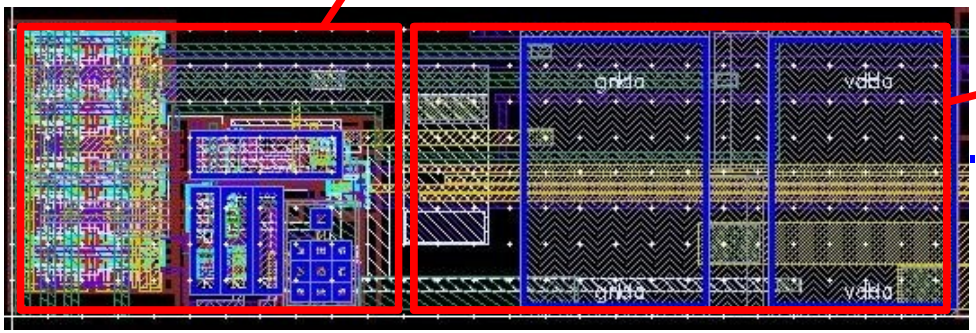
Miscellaneous

- **Different detector capacitors** are distributed over channels
  - The det. caps. are on the die (place-consuming) for exact measurements
  - Values of 0..20pF and 40pF are directly connected to different channel inputs
  - Some channel inputs are connected to input pads instead -> to connect external devices (capacitors, diodes, detectors, ...)
- **Monitoring**
  - All bias voltages are routed to pads -> decoupling and monitoring
  - Monitor buses for preamplifier and shaper inputs/outputs
  - The outputs of all injection methods can be monitored
- Additional circuits for measurement of detector and injection capacitors (based on charge pump)
- Chip needs only 2 external non-power bias voltages

Layout Channel

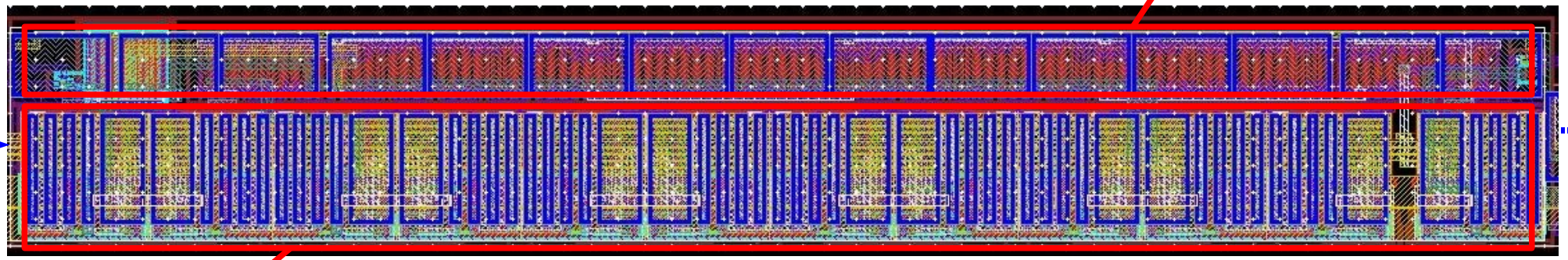
Injection + Register

40 µm



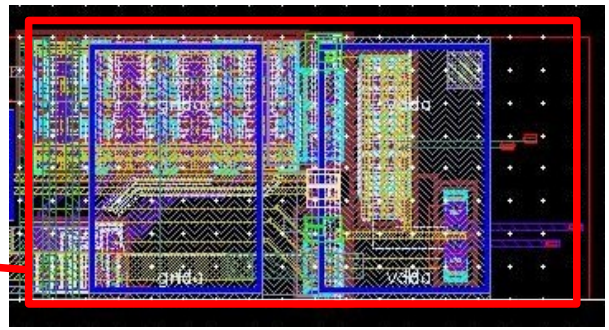
Buses (M5+M6 not visible here)

FB-devices:
NMOS, resistors, capacitors

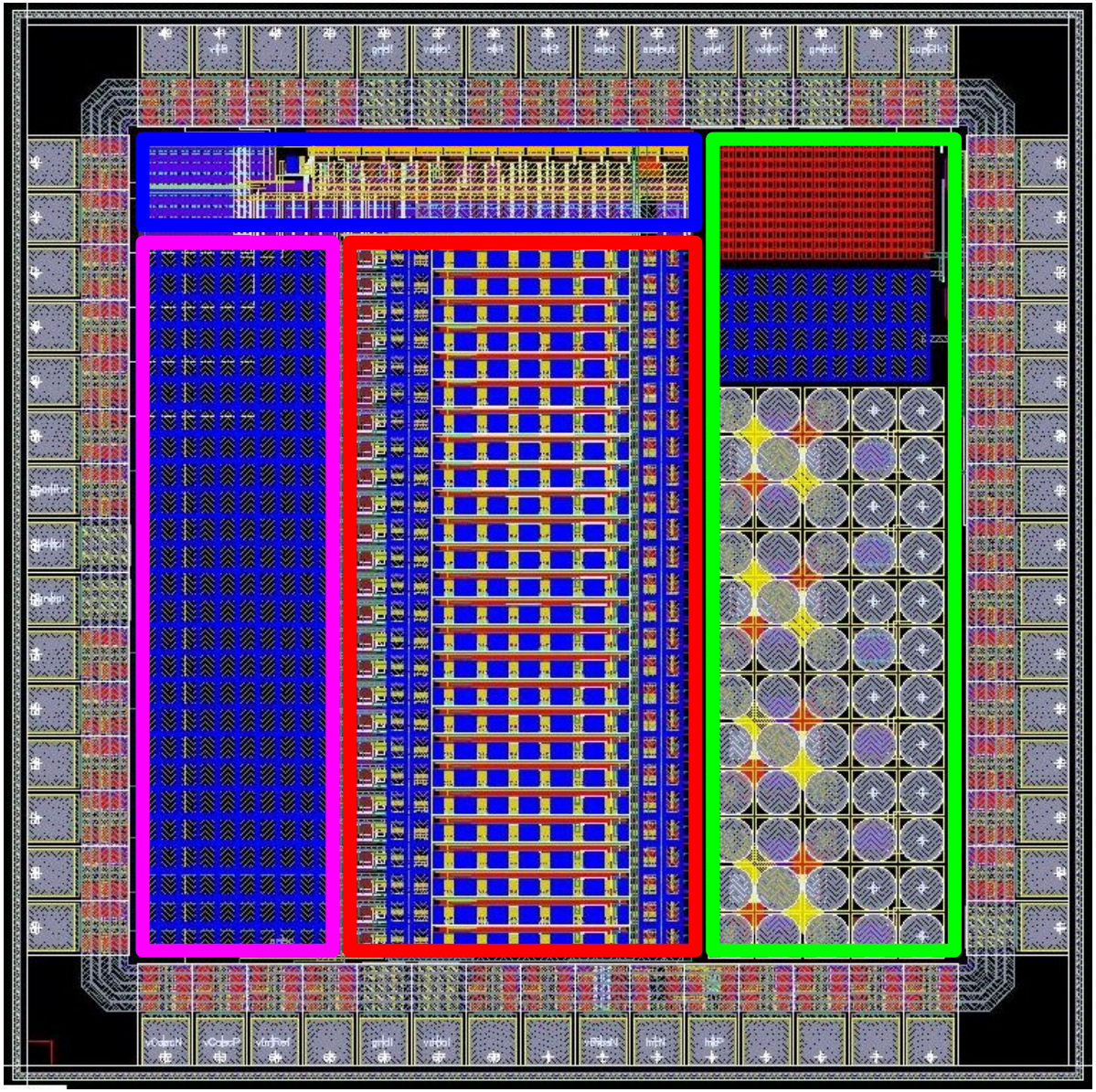


12x Voltage Amplifier Cell
(11x preamp + 1x shaper)

Discriminator, buses,
LVDS output buffer



Layout Chip



- Inj. / preamp. / shaper / disc.
  - 26 channels
  - 517µm x 1040µm
- Bias
  - DACs
  - Diodes
  - Decoupling
- Detector capacitors
  - 0pF – 20pF, 40pF
  - 290µm x 1040µm
- Test structures

Summary

26 channel csa test chip, submitted on 29th September 2008

- Design highlights
  - 2nd order shaper
  - 3-way test injection
  - CML-discriminator with threshold trim
  - Compact layout (Channel size: 40µm x 517µm)
  - Most bias generation is on-chip (33 8-bit-DACs)
- Typical values (30pF detector cap., 11x VAC)
  - Power consumption: 3.6mW/channel
  - Gain: ≈14mV/fC
  - Shaping Time: 80ns
  - Noise (ENC): 480e
  - Rise-Time Shaper: 50ns
  - Input range: 0 - 13MIPs (0 - 47.8fC)

First measurement will be available in the beginning of 2009...

Thank you!