UNIVERSITÄT HEIDELBERG

TR1: First Results

First Results of the 26 Channel CSA Readout Chip

Schaltungstechnik und Simulation

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CBM-XYTER Family Planning Workshop

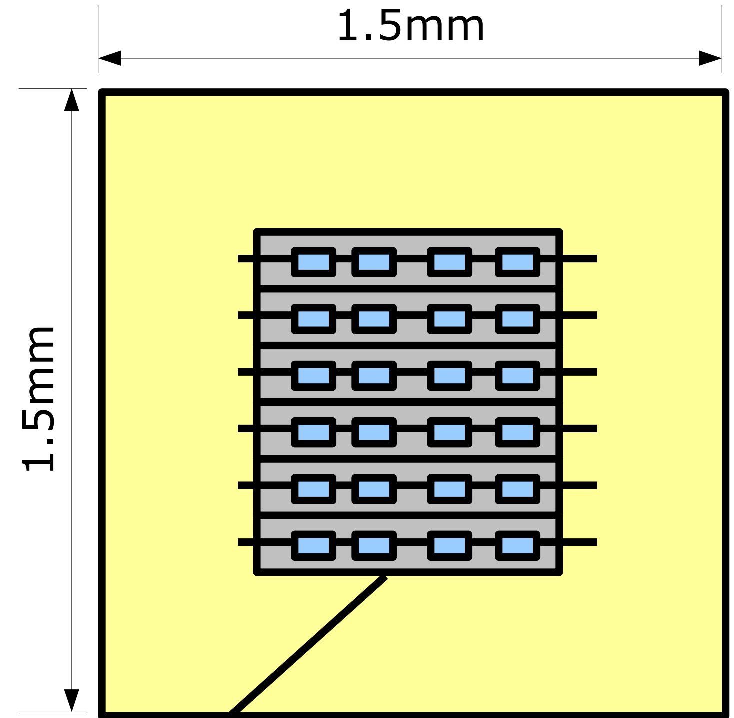
05.12.2008

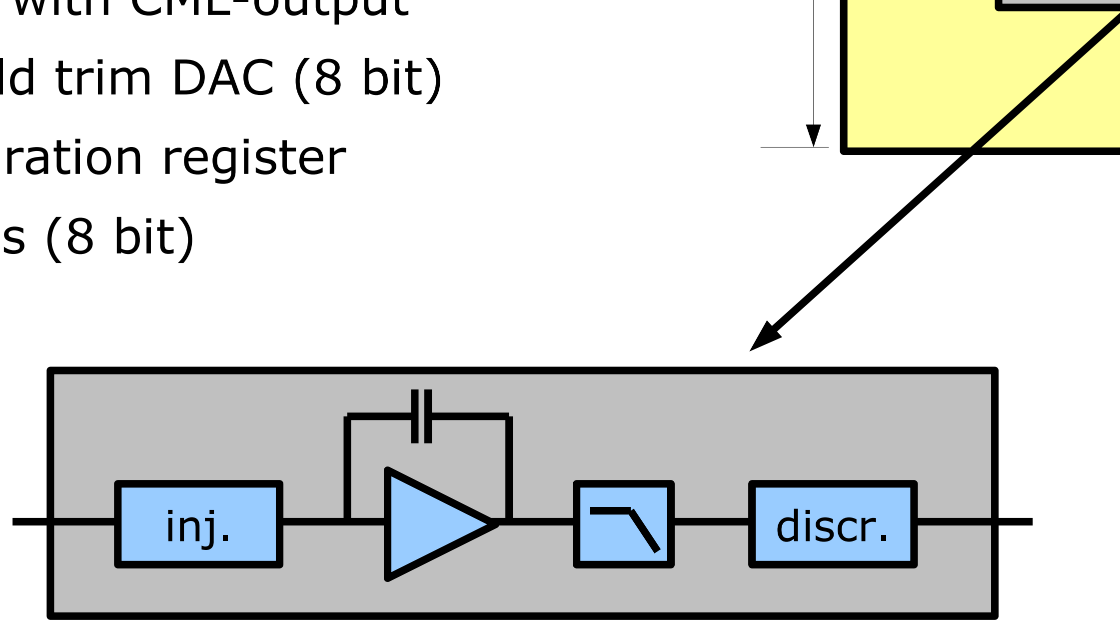
Chip Summary (rush through...)

Overview 2^{nd} CSA Test Chip

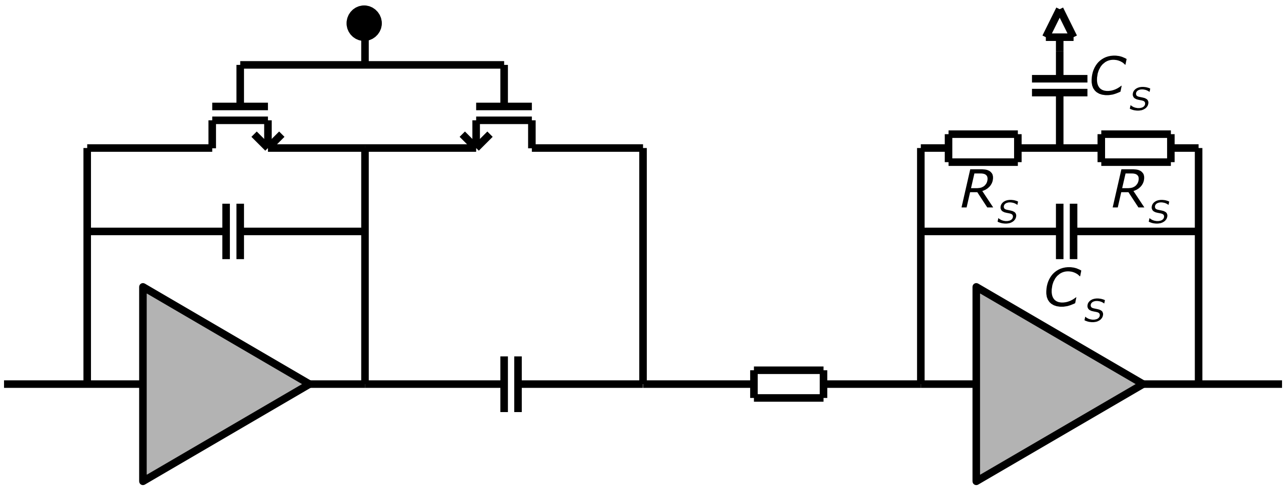
UMC018 MPW Mini@sic (1525µm x 1525µm)

- 26 channels
- 40 µm channel pitch
- Each channel consists of
  - Injection circuit
  - Preamplifier
  - 2^{nd} order shaper
  - Discriminator with CML-output
  - Local threshold trim DAC (8 bit)
  - 15 bit configuration register
- 7 global bias DACs (8 bit)





Preamplifier/Shaper Circuit



with $H(s) \approx \frac{A_{DC}}{(1+sR_SC_S)^2}$

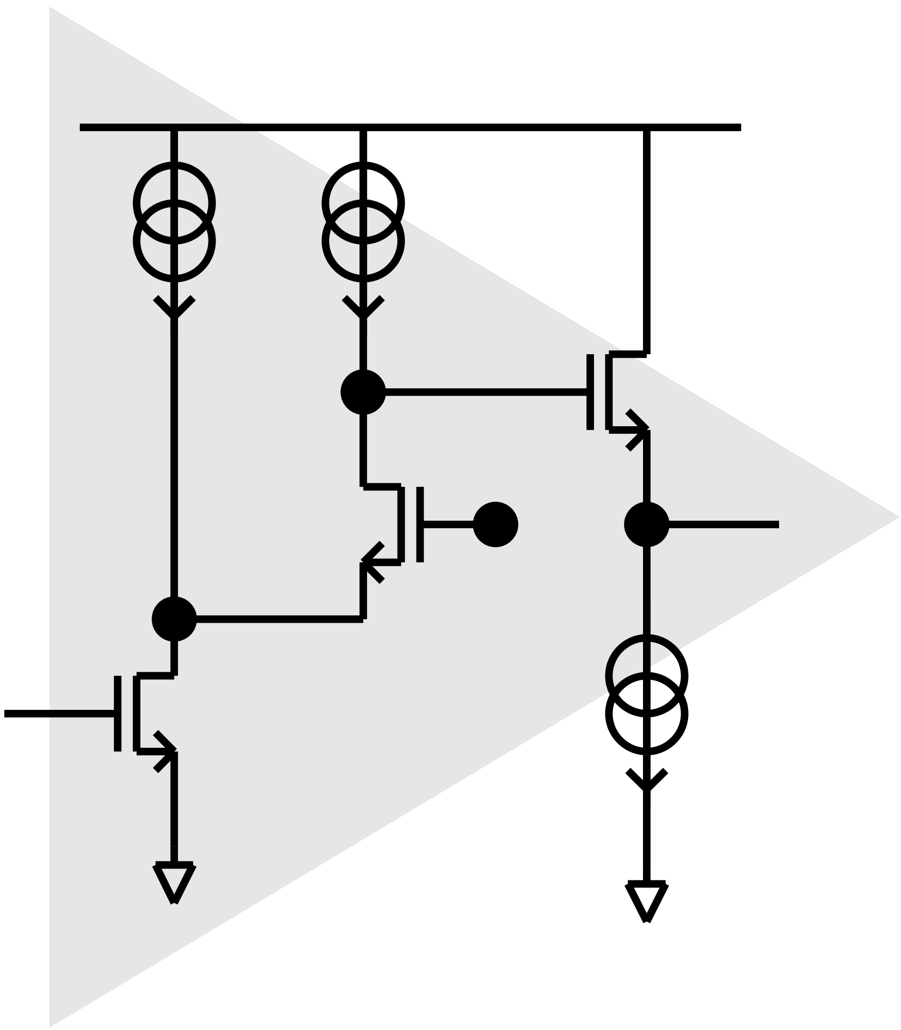
- Preamplifier with PZ-canceling O'Connor MOS feedback
- 2nd order shaper with two real poles:
  - Good matching required
  - But: Matching only between components of the same type!
- Circuit is optimized for positive charges (N-MOS feedback)
- Chosen shaping time is 80ns (200kΩ, 400fF)

Only one amplifier-cell is used for both, preamplifier and shaper.

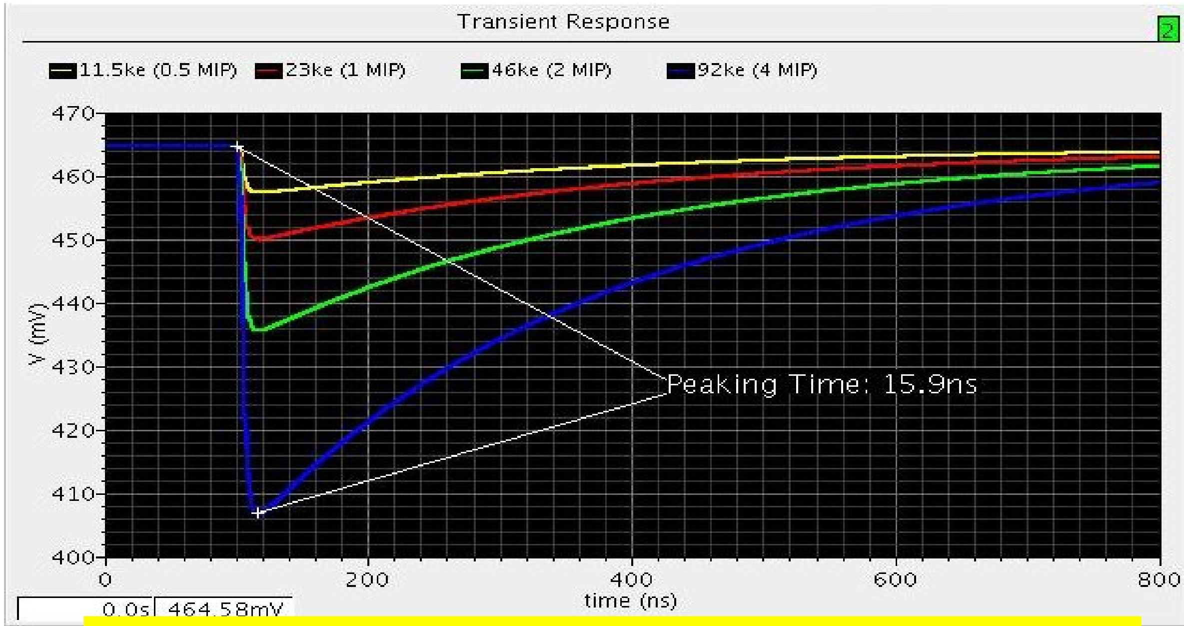
Preamplifier uses n parallel instances of same amplifier-cell (cell is scaled).

Voltage Amplifier Cell (VAC)

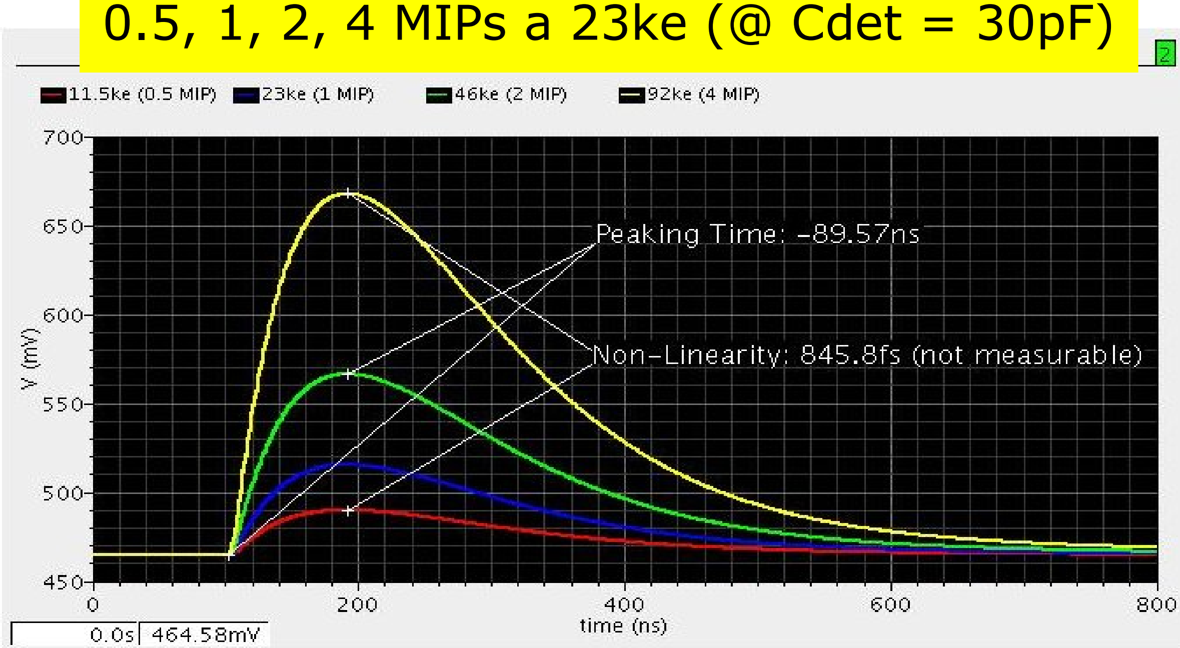
- **Gain stage with straight cascode**
  - Cascode faces upwards to maximize current through input MOS
  - NMOS input for maximum gm (flicker noise in simulation not significant)
  - Transconductance of input MOS ~ 3.1mS/instance
  - Typical power (adjustable): 0.3mW/instance
- **Source follower** is used as level shifter and unity gain buffer
- **Miscellaneous**
  - Compact layout, the cell has been designed for easy scaling
  - The cell has been used for the preamplifier (scaled) and for the shaper => same input DC-levels
  - All bias voltages are decoupled in cell



Transient Simulation Preamplifier/Shaper Part



0.5, 1, 2, 4 MIPs a 23ke (@ Cdet = 30pF)



Results from simulation:

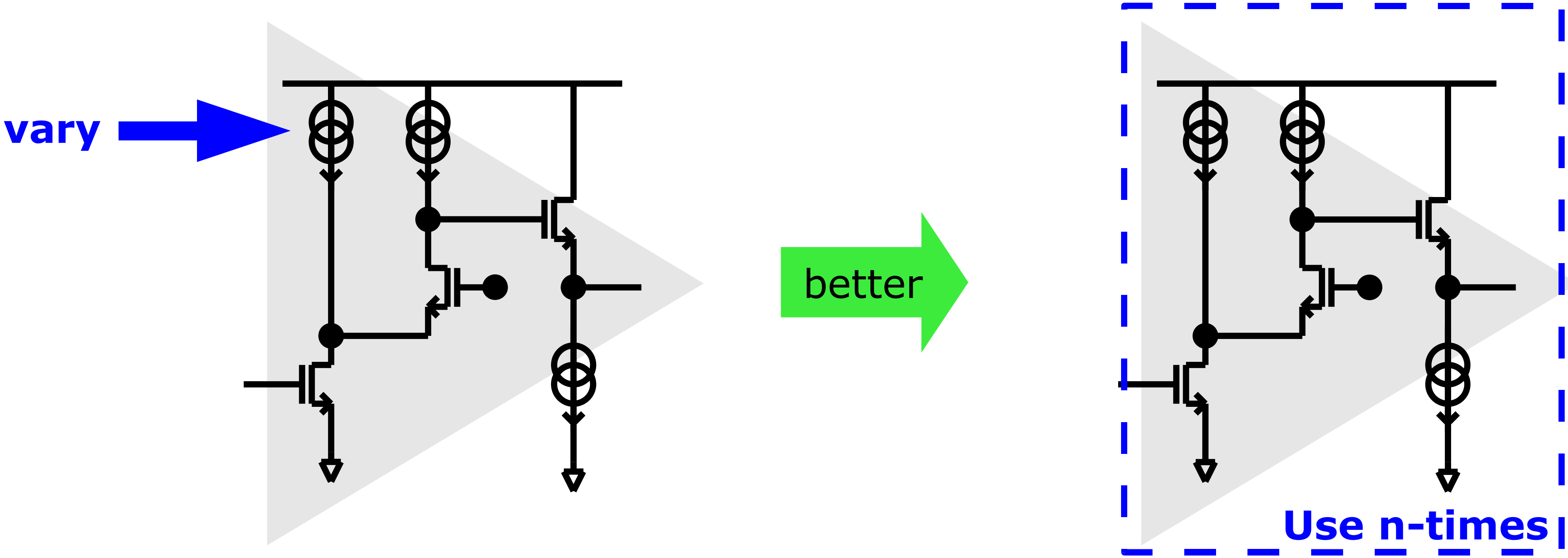
Preamplifier output

- Peaking-Time (0% - 100%): ≈16ns
- Rise-Time (10%-90%): ≈9ns
- Pulse length adjustable

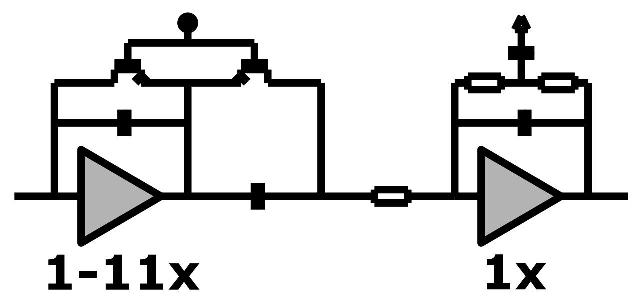
Shaper output (2^{nd} order)

- Peaking time (0% - 100%): ≈90ns
- Rise-Time (10%-90%): ≈50ns
- High linearity, high range up to 13 MIPs (23ke/MIP)
- Gain: 13.8mV/fC (=> amplitude for MIP ≈50mV)

Scaling of Voltage Amplifier Cell (VAC)



- We want to figure out: How does noise depend on power?
- Simple method: Variation of bias currents
  - But: this also shifts the operating points
- It's probably better to use the same cell n-times
  - But: this also scales input capacitance, layout size, ...



Both “methods” available on this chip

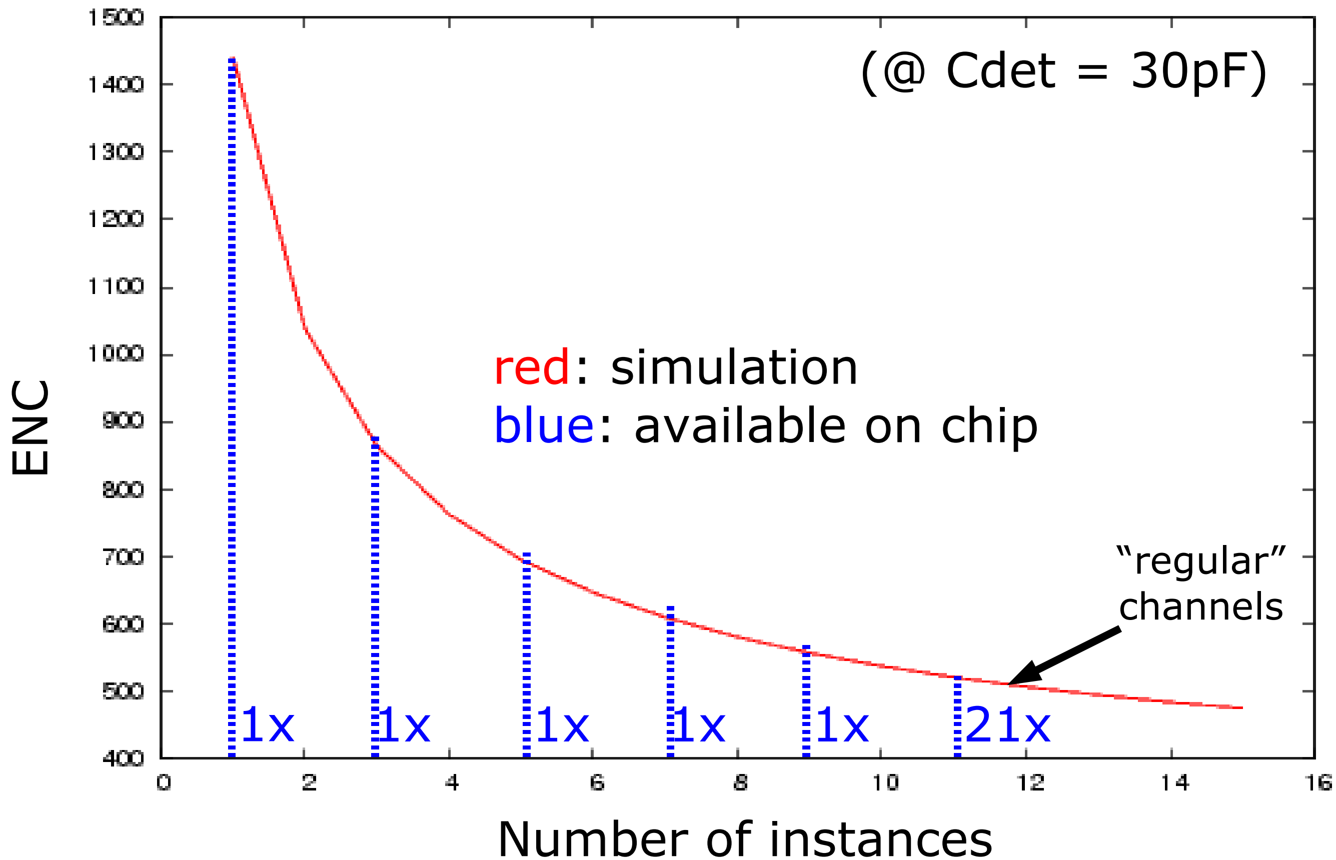
- 20 “normal” channels - preamp: 11x VAC, shaper: 1x VAC
- 6 test channels - preamp: 1,3,5,7,9,11x VAC, shaper: 1x VAC

Noise and Power Consumption of 2nd CSA TC

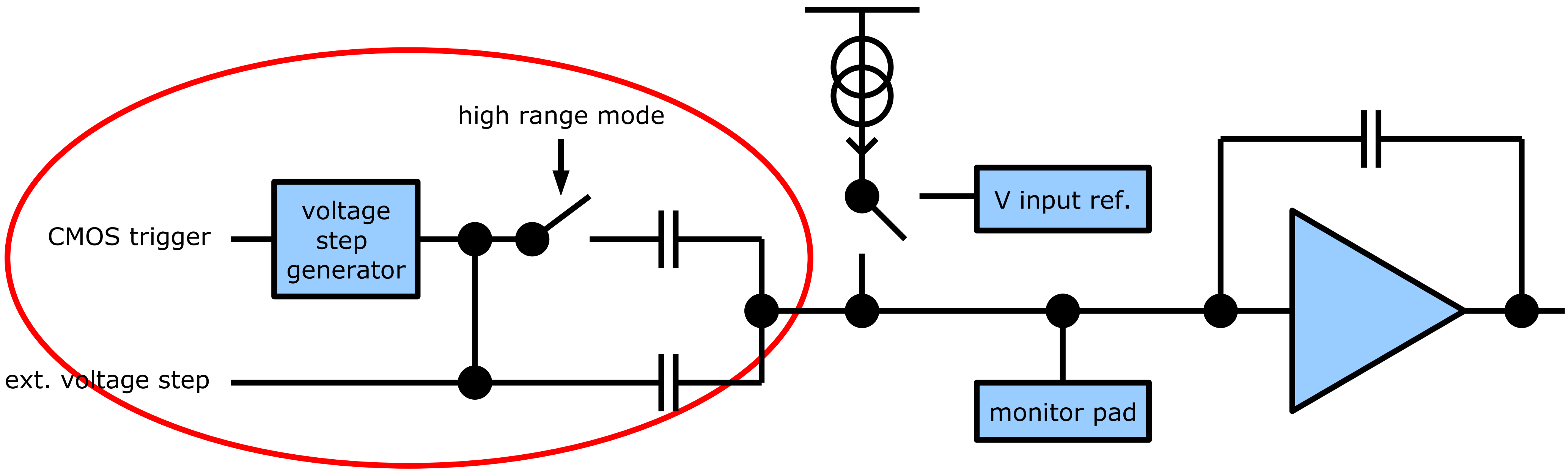
Typical simulated noise (ENC): 138e + 11.36e/pF (=> e.g. **479e @ 30pF**)
(for preamp with 11 amplifier cells, consuming **3.3mW**)

Feature/Simple Trick: Preamplifier is made of n parallel connected amplifier cells. N is varied over different channels to study how noise depends on power.

Noise vs. number of amp. instances (= vs. power):

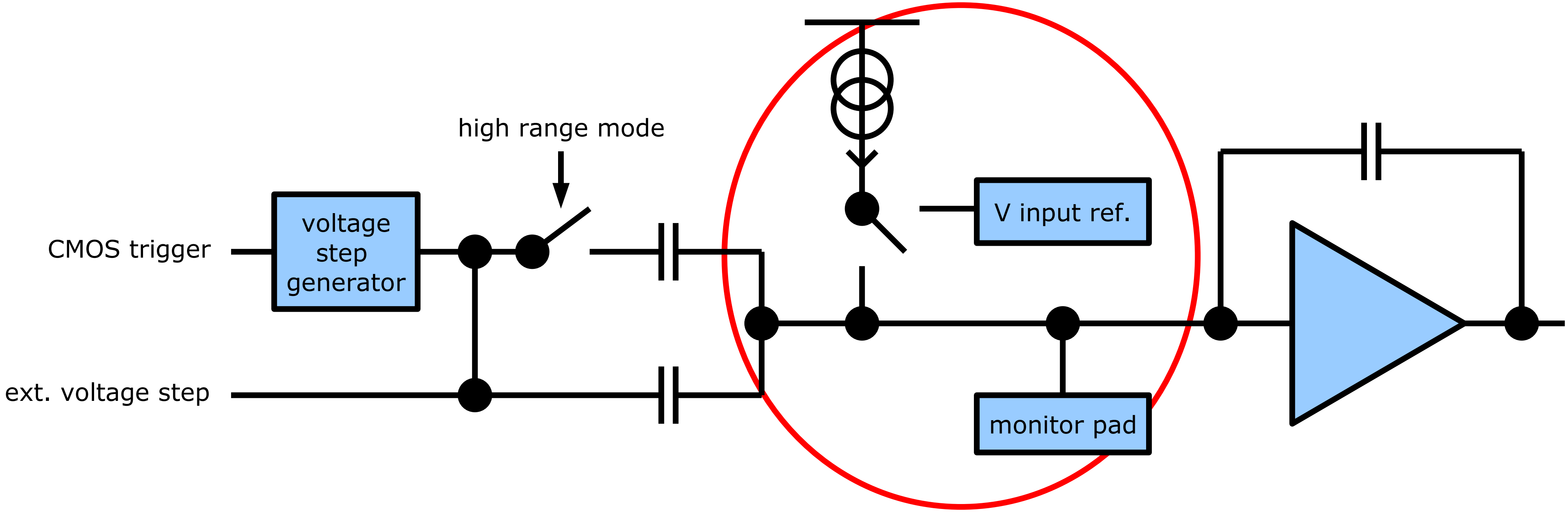


Injection Circuit 1/2



1) **Internal voltage step injection** (pos. and neg. charge)
   - Voltage step generator is triggered by external C-MOS signal
   - Low and high range mode:
     - Up to 1.2MIPs with higher granularity
     - Up to 12 MIPs with lower granularity
   - Short pulses (~ 3ns)
2) **External voltage step injection** (pos. and neg. charge)
   - Same range like internal voltage step injection
   - Pulse-length depends on rise-time of external voltage step

Injection Circuit 2/2



3) **Internal current pulse injection** (pos. charge only)

- Current source is switched between input reference voltage and amp. input node
- External differential control signal required
- Pulse length depends on switching speed
- No upper limit for magnitude of injected charge

Features

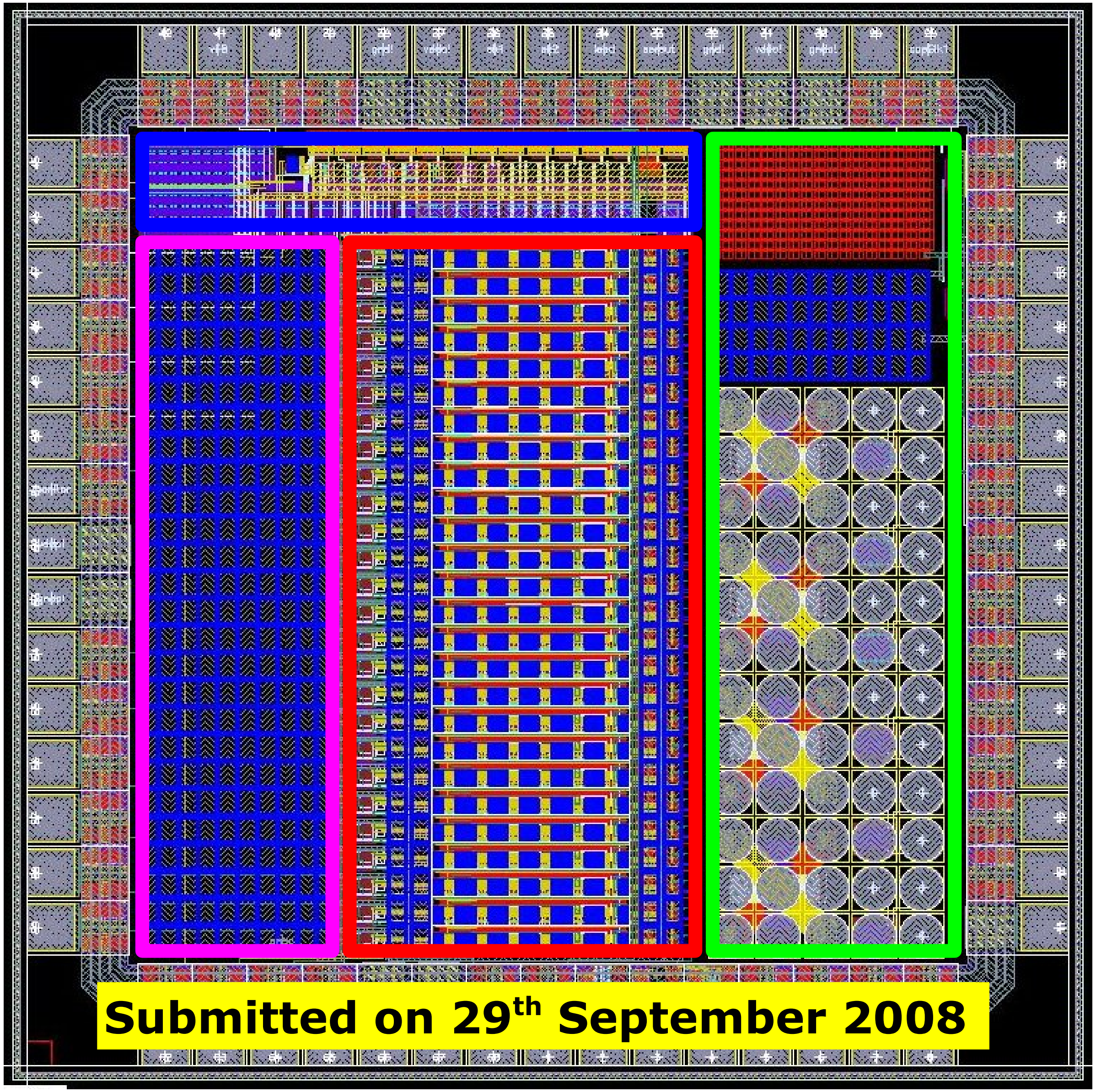
- Monitoring pad for calibration, measurements or even direct injection
- Every part can be enabled/disabled by internal control register (not sketched here)

Additional Features 2nd CSA TC

- 3-way internal test charge injection circuit in each channel
  - Fast and slow pulse generation
  - High and low range mode (up to 12 MIPs in low granularity)
- Advanced discriminator
  - locally adjustable thresholds (via DACs)
  - CML output
- 7 global bias DACs
- Many monitoring possibilities
- Different on-chip detector capacitors distributed over channel inputs
- Capacitor measurement/calibration test circuits
- ...

=> Most of the CSA parameters (shaping times, noise, power, ...) are **well adjustable**, we now **need a more detailed specification** for/from TRD (pulse polarization, noise-limit, power-limit, radiation doses, detector capacitances, timing requirements, ...)

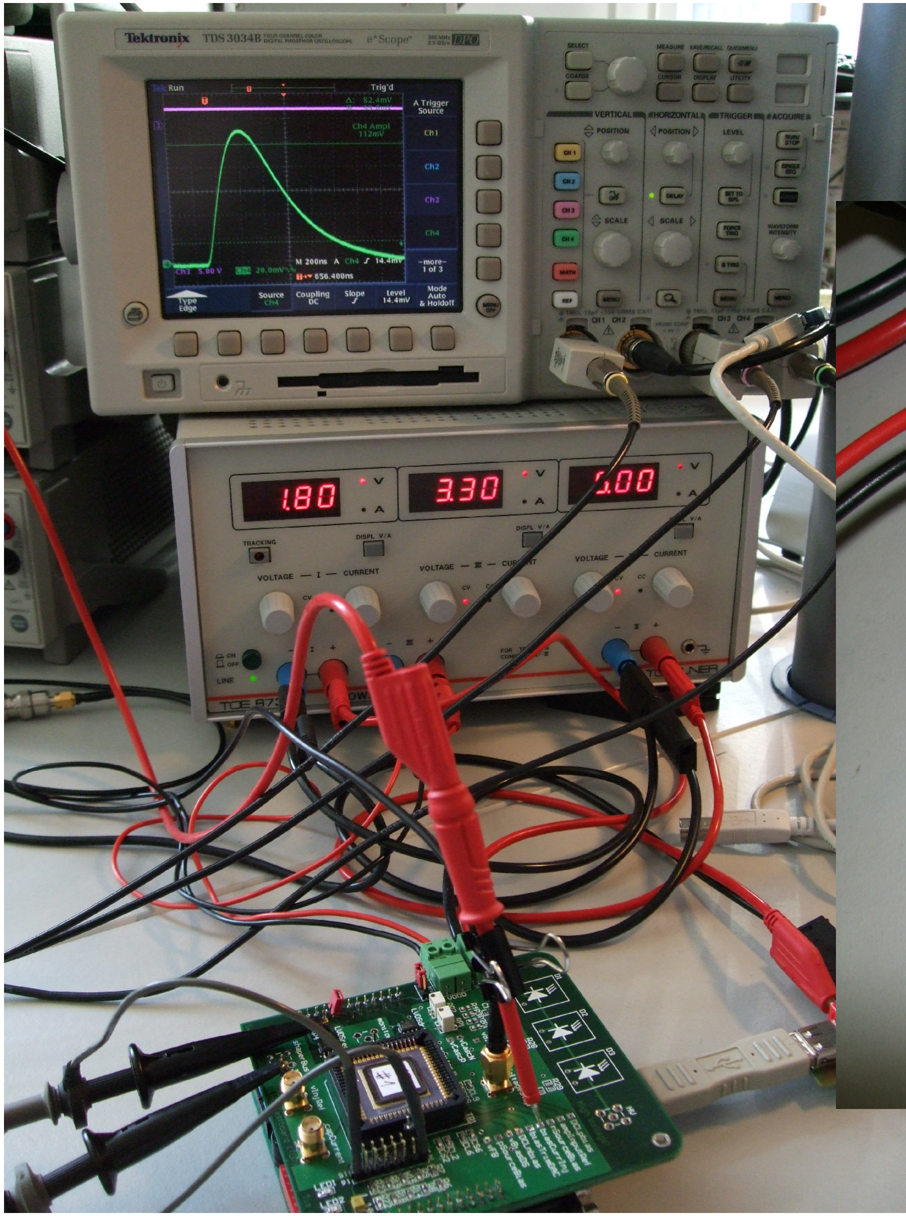
Layout Chip 2nd CSA TC



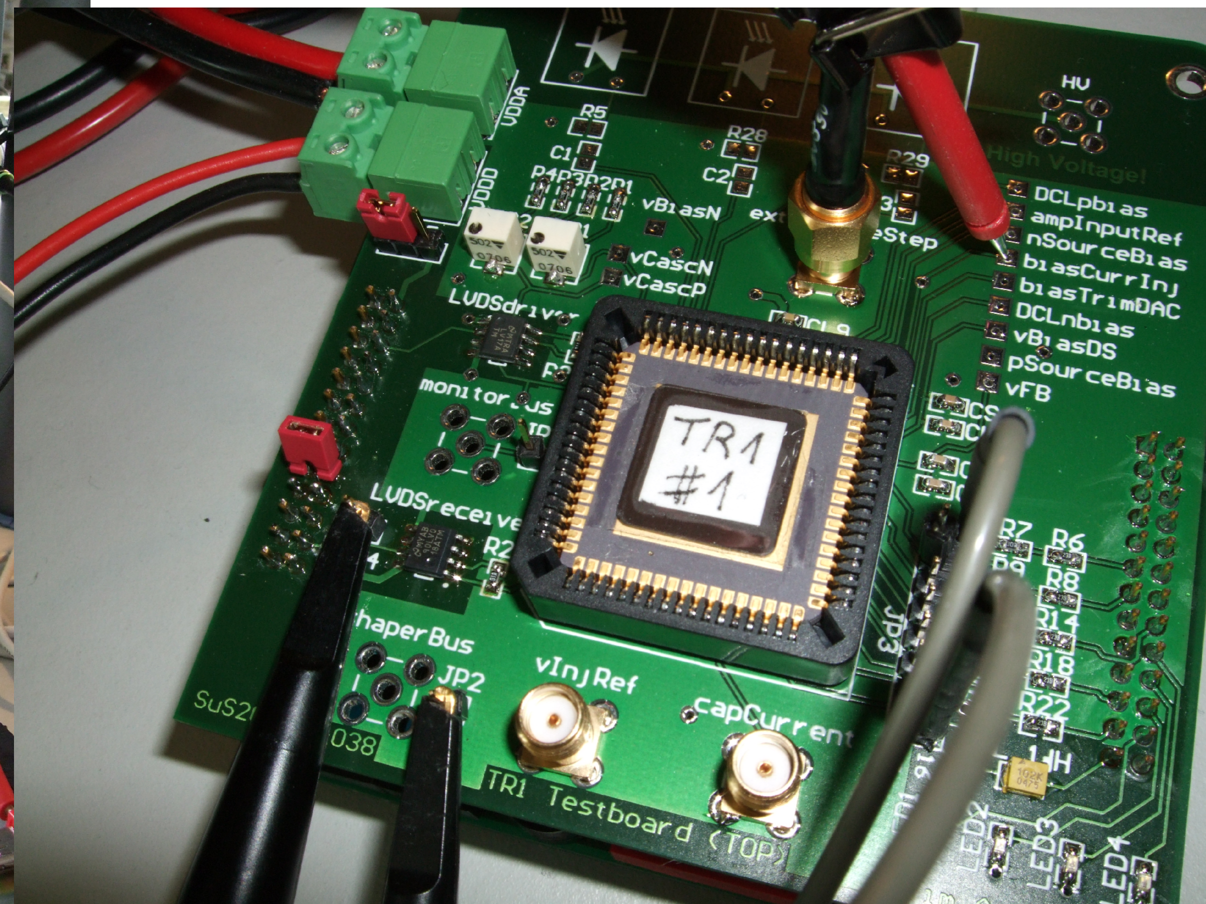
- Inj. / preamp. / shaper / disc.
  - 26 channels
  - 517µm x 1040µm
- Bias
  - DACs
  - Diodes
  - Decoupling
- Detector capacitors
  - 0pF – 20pF, 40pF
  - 290µm x 1040µm
- Test structures

Measurement Results

Test Setup

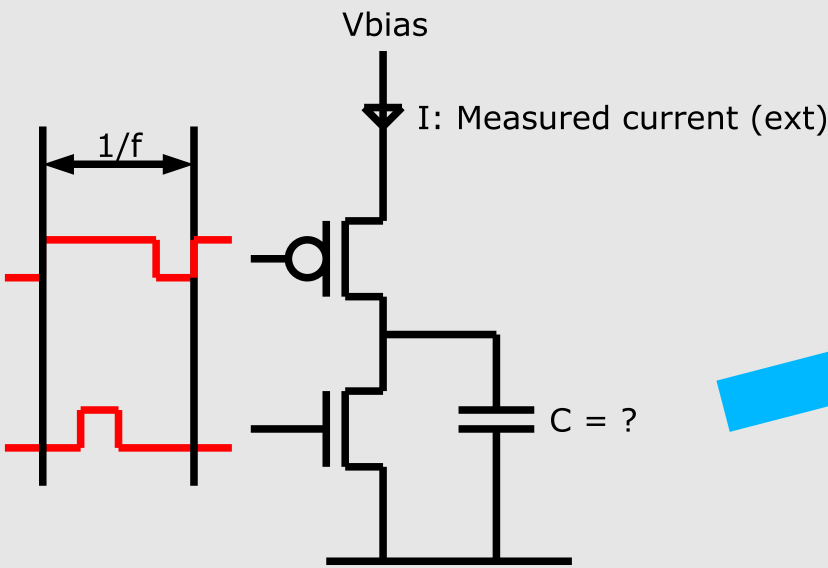


Tektronix
TDS 3034B
1.80
3.30



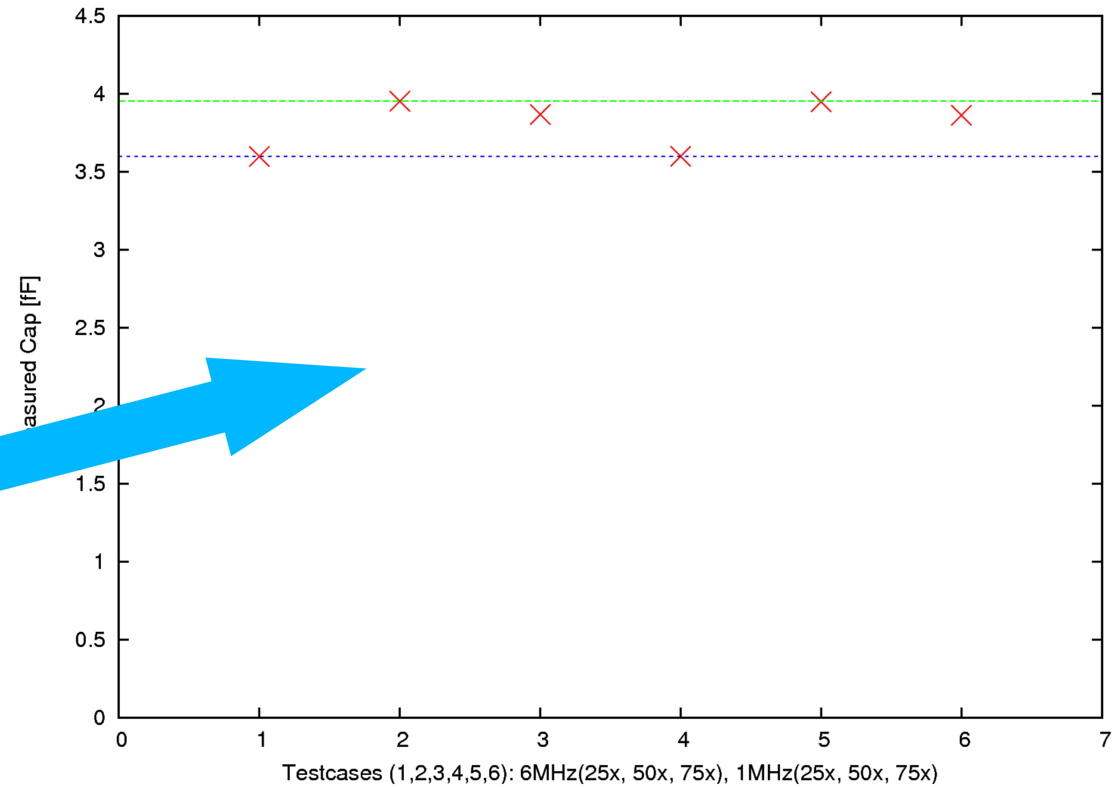
VDDA
VDDD
HV
High Voltage!
DCLpbias
ampInputRef
nSourceBias
biasCurrInj
biasTrimDAC
DCLnbias
vBiasDS
pSourceBias
vFB
vBiasN
vCascN
vCascP
LVDSdriver
monitorBus
LVDSreceiver
haperBus
JP2
JP3
vInjRef
capCurrent
TR1 Testboard (TOP)
TR1
#1
R5
C1
R28
C2
R29
R7
R6
R9
R8
R14
R18
R22
LED3
LED4

Calibration of Injection Capacitance



Simple charge pump circuit on chip
=> C = avg(I) / (Vbias * f)

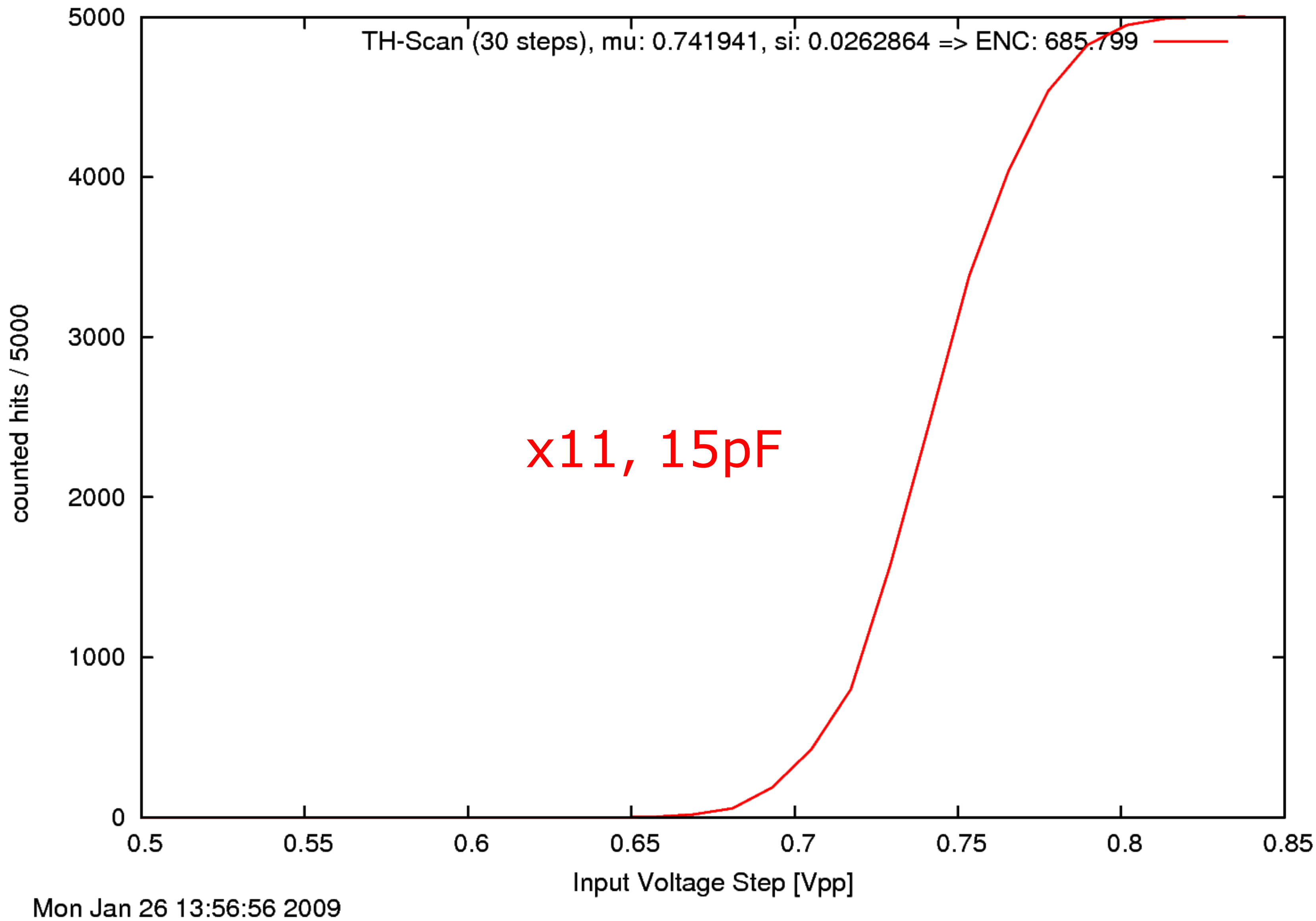
Corner cases:
- Variate f and Vbias
- 4 circuits: 0, 25, 50, 75 * C



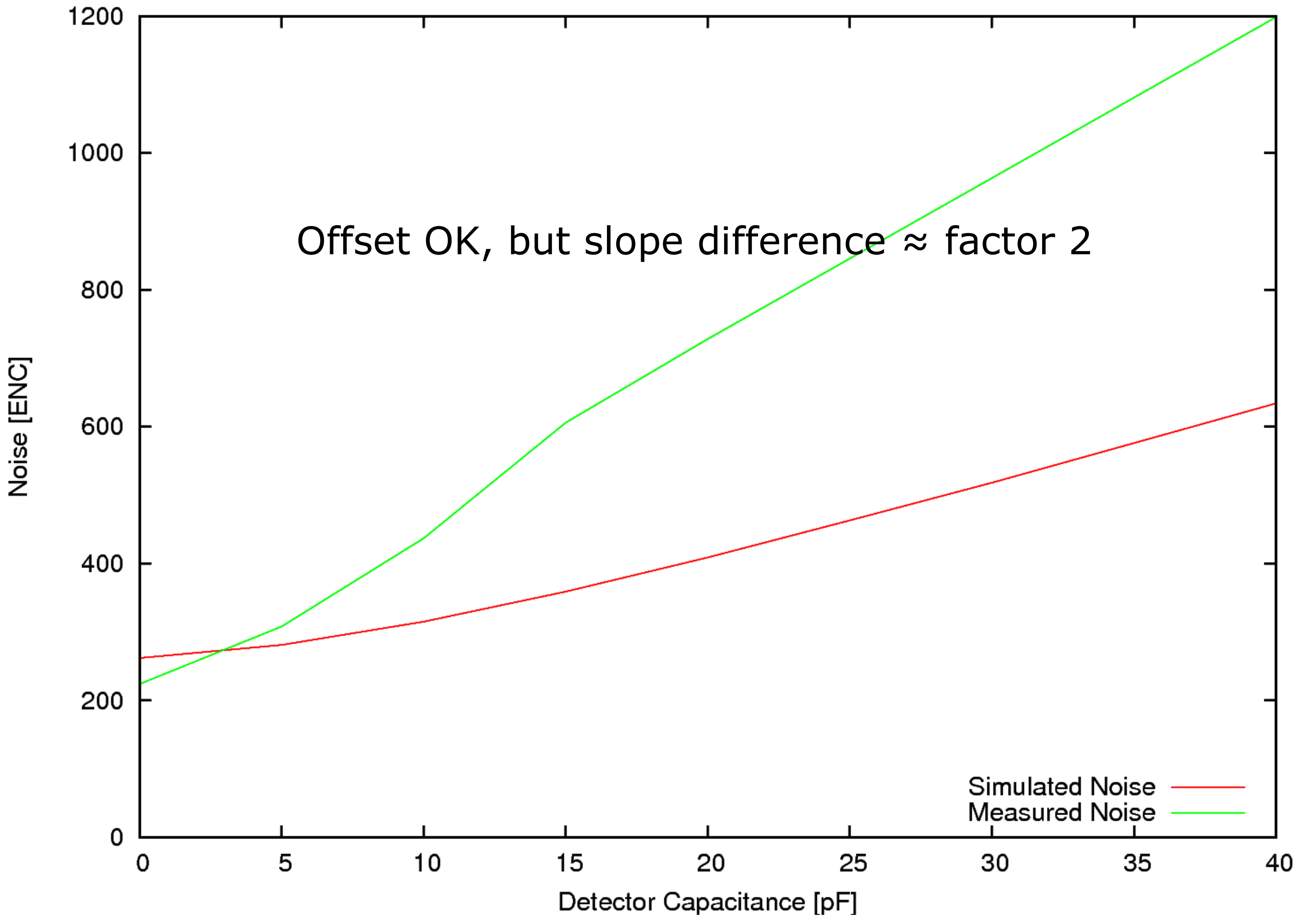
Expected: 4.18fF
Measured Mean Value: 3.80fF

=> Difference ≈ 9.1%

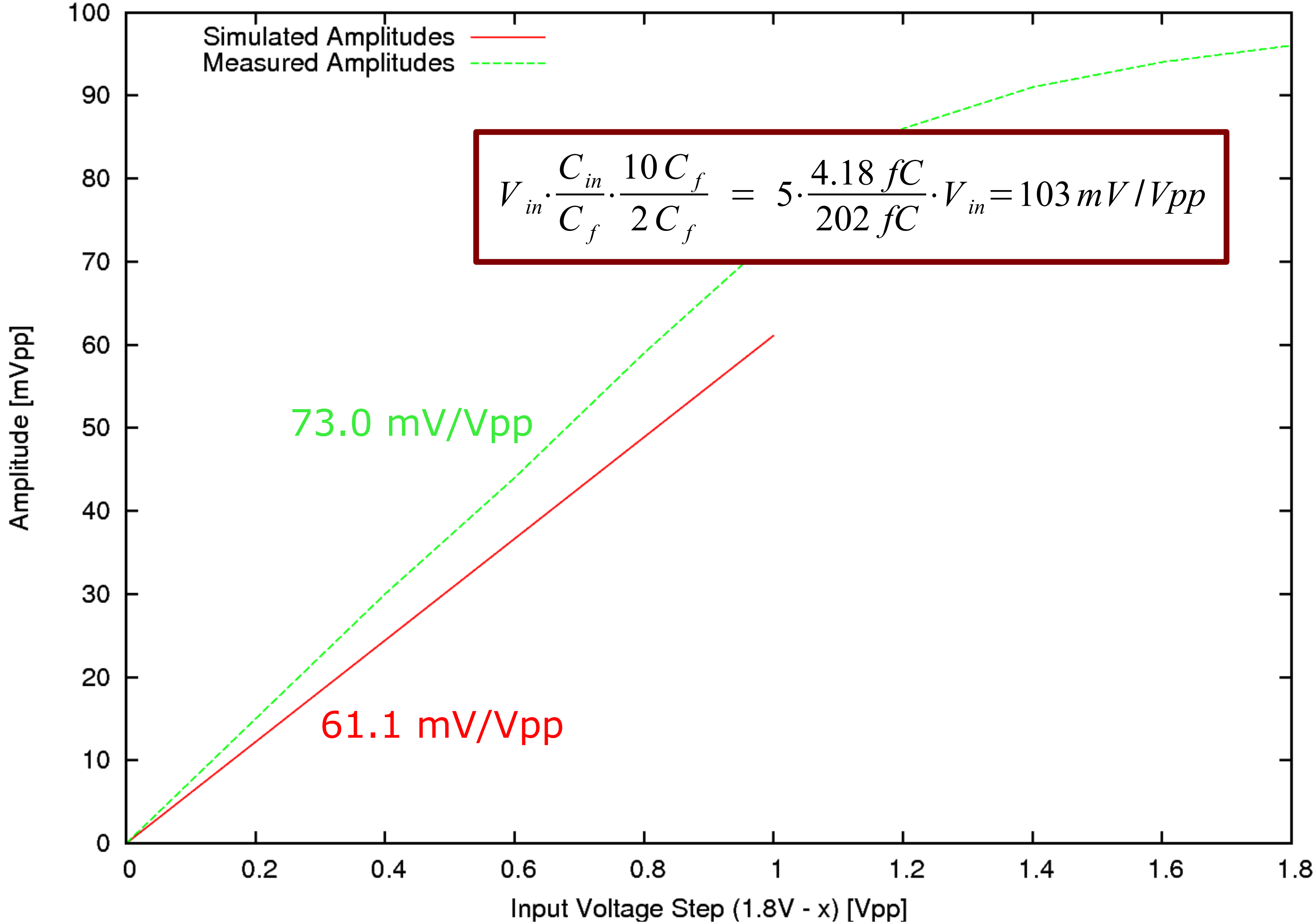
S-Curve Scans



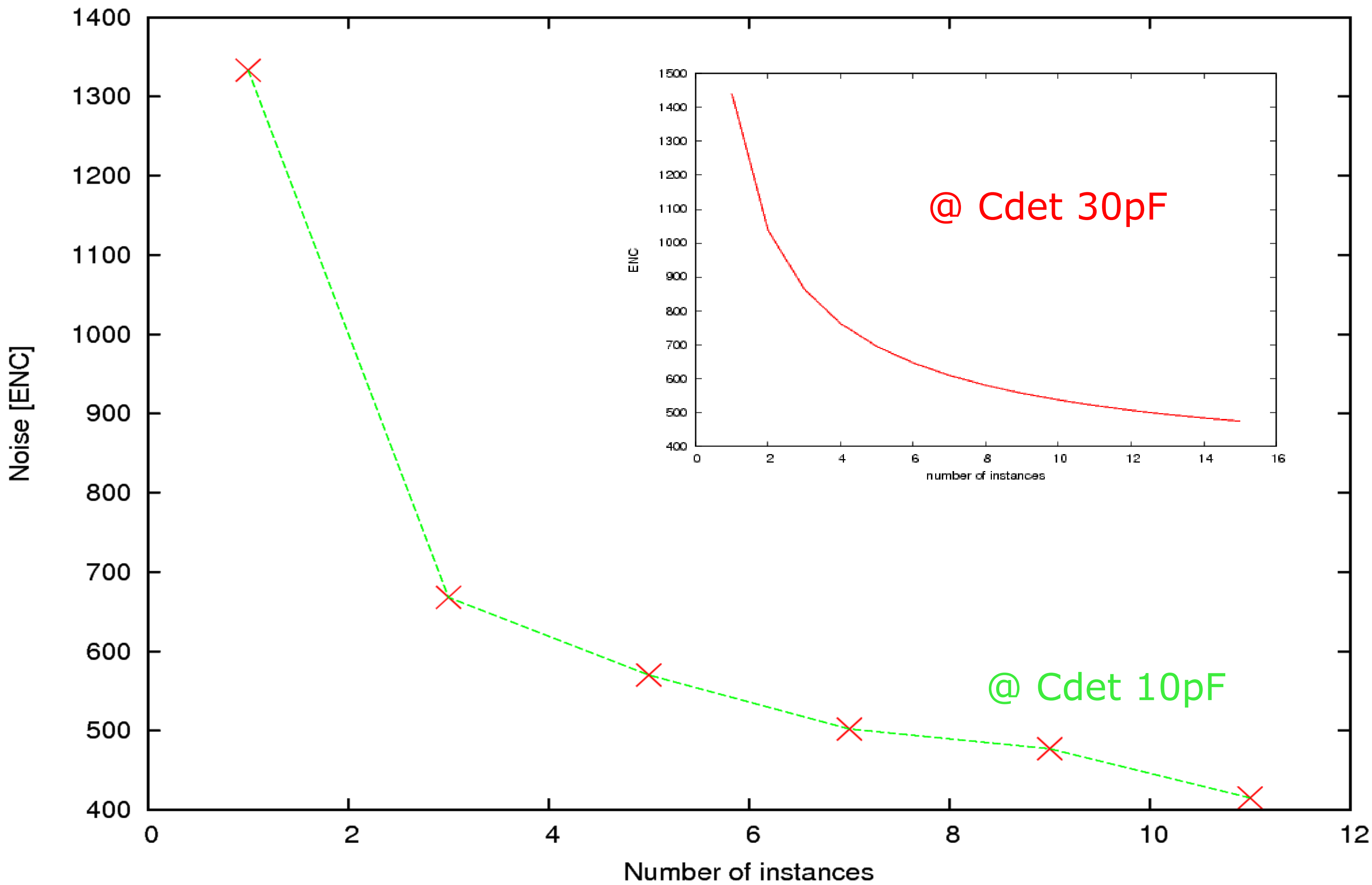
Noise vs. Detector Capacitance



Amplifier Closed Loop Gain



Noise vs. Number of Instances



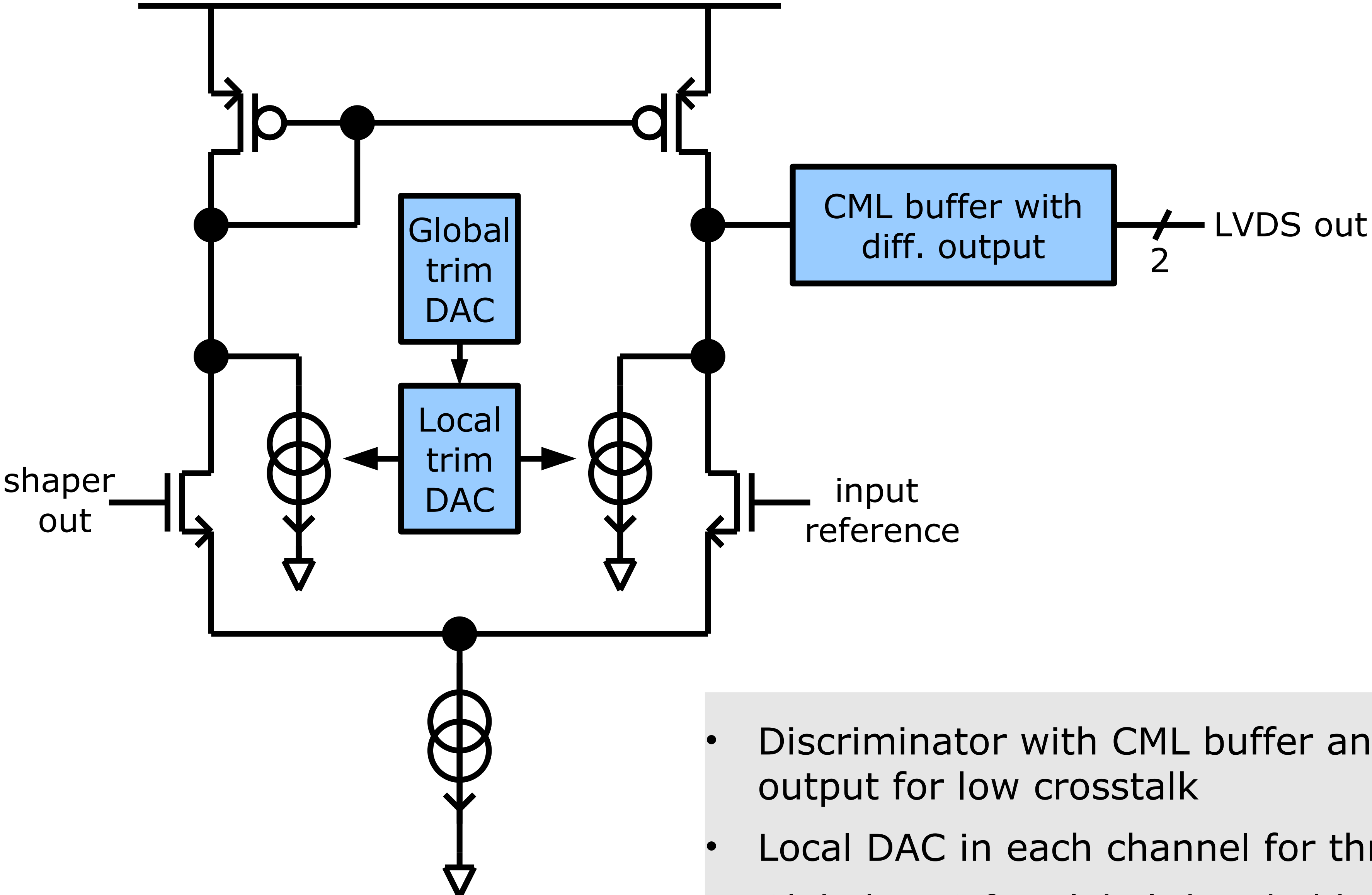
:-)

Summary

26 channel csa test chip, submitted on 29th September 2008

- Design highlights
  - 2nd order shaper
  - 3-way test injection
  - CML-discriminator with threshold trim
  - Compact layout (Channel size: 40µm x 517µm)
  - Most bias generation is on-chip (33 8-bit-DACs)
- Typical values (30pF detector cap., 11x VAC)
  - Power consumption: 3.6mW/channel
  - Gain: ≈14mV/fC
  - Shaping Time: 80ns
  - Noise (ENC): 480e
  - Rise-Time Shaper: 50ns
  - Input range: 0 - 13MIPs (0 - 47.8fC)

First measurement will be available in the beginning of 2009...

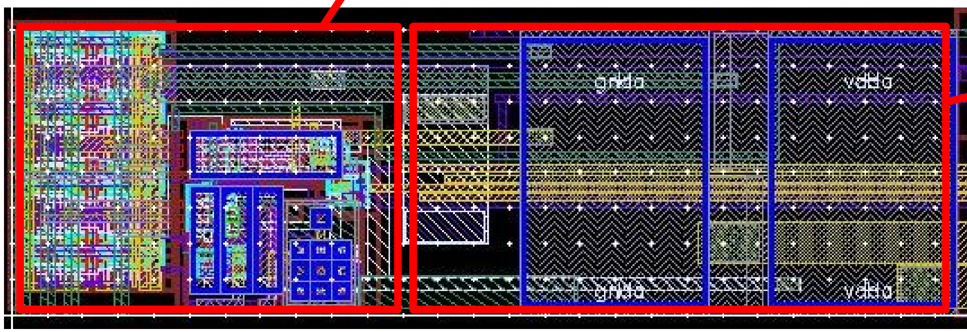


- Discriminator with CML buffer and LVDS output for low crosstalk
- Local DAC in each channel for threshold trim
- Global DAC for global threshold trim

Layout Channel

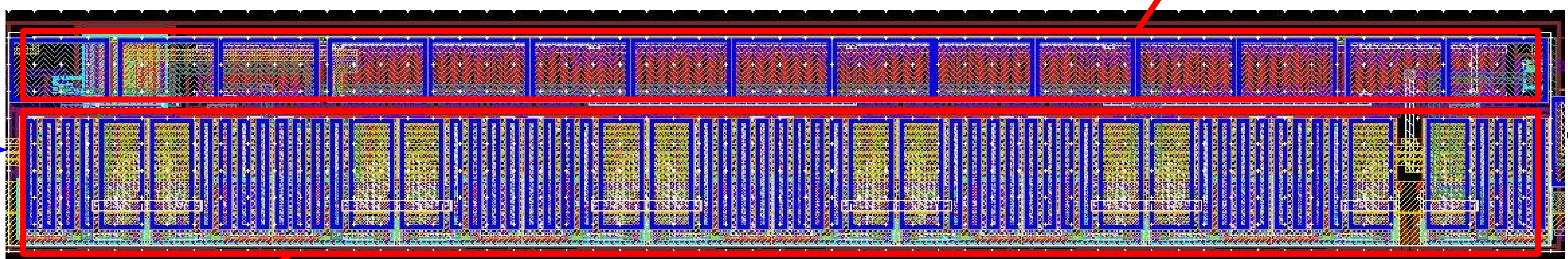
Injection + Register

40 µm



Buses (M5+M6 not visible here)

FB-devices:
NMOS, resistors, capacitors



12x Voltage Amplifier Cell
(11x preamp + 1x shaper)

Discriminator, buses,
LVDS output buffer

Miscellaneous

- **Different detector capacitors** are distributed over channels
  - The det. caps. are on the die (place-consuming) for exact measurements
  - Values of 0..20pF and 40pF are directly connected to different channel inputs
  - Some channel inputs are connected to input pads instead -> to connect external devices (capacitors, diodes, detectors, ...)
- **Monitoring**
  - All bias voltages are routed to pads -> decoupling and monitoring
  - Monitor buses for preamplifier and shaper inputs/outputs
  - The outputs of all injection methods can be monitored
- Additional circuits for measurement of detector and injection capacitors (based on charge pump)
- Chip needs only 2 external non-power bias voltages