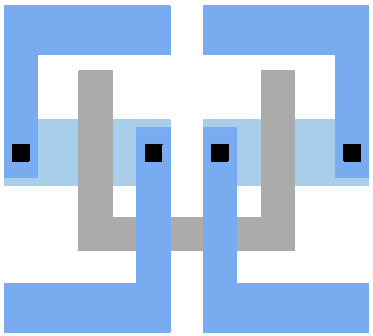
UNIVERSITÄT HEIDELBERG

CSA Test Results

Measurement Results of the 26 Channel CSA Readout Chip



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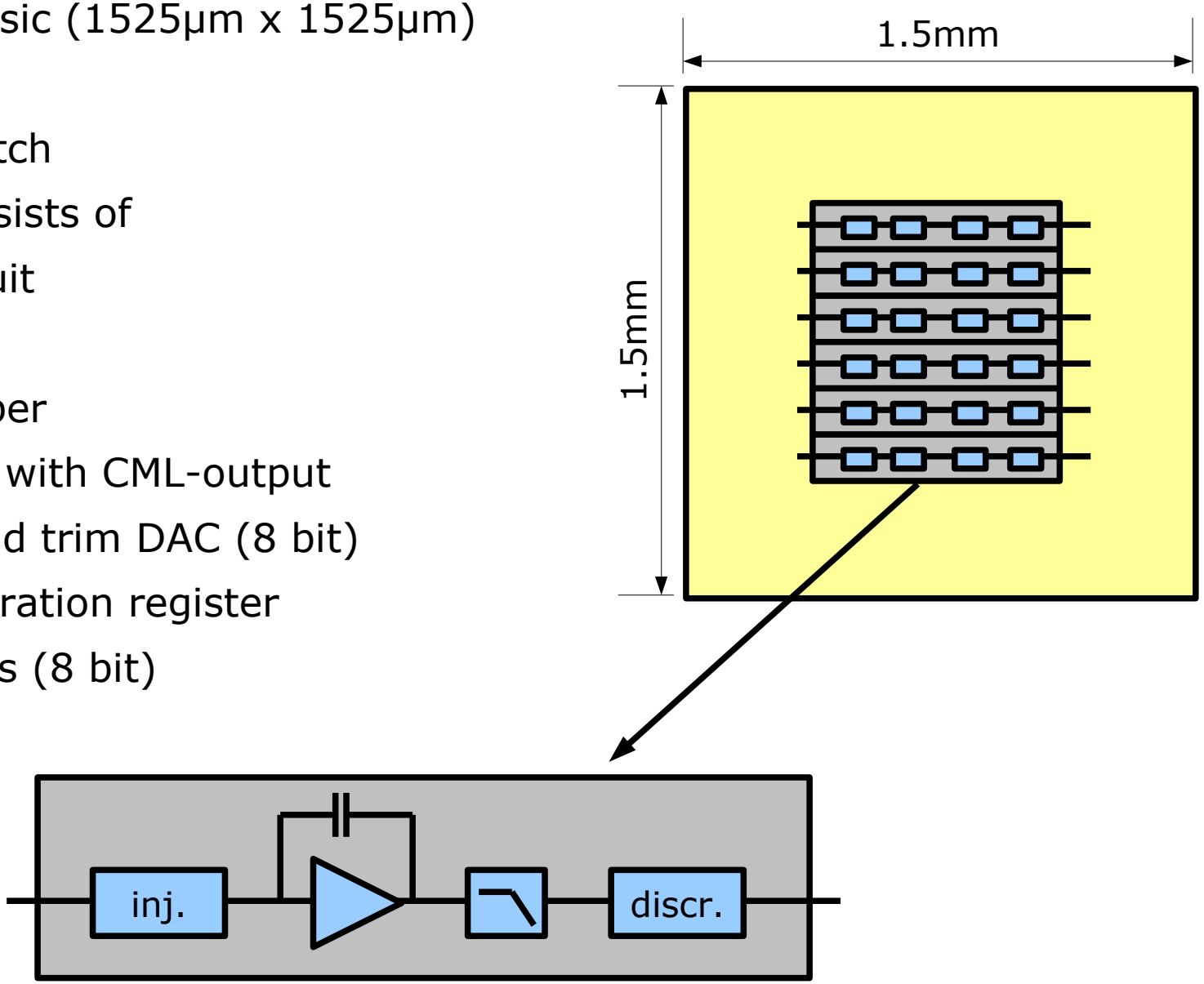
13th CBM CM Darmstadt

12.03.2009

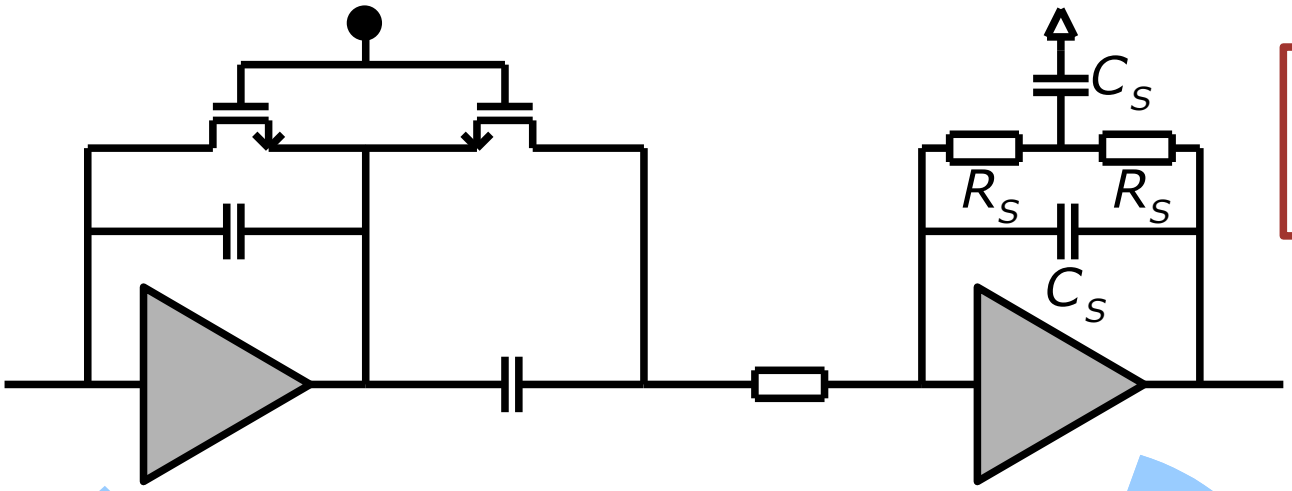
Reminder: Overview 2nd CSA Test Chip

UMC018 MPW Mini@sic (1525µm x 1525µm)

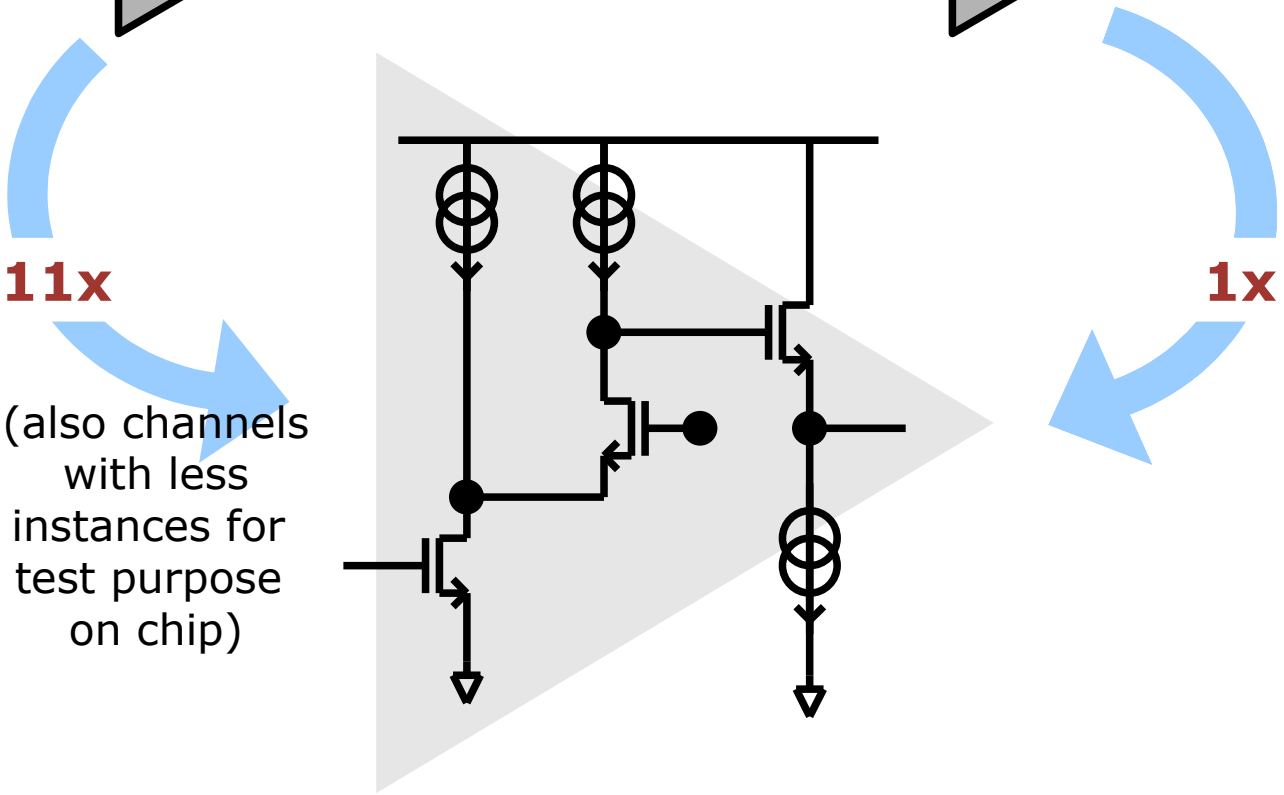
- 26 channels
- 40 µm channel pitch
- Each channel consists of
  - Injection circuit
  - Preamplifier
  - 2nd order shaper
  - Discriminator with CML-output
  - Local threshold trim DAC (8 bit)
  - 15 bit configuration register
- 7 global bias DACs (8 bit)



Reminder: Preamplifier/Shaper Circuit

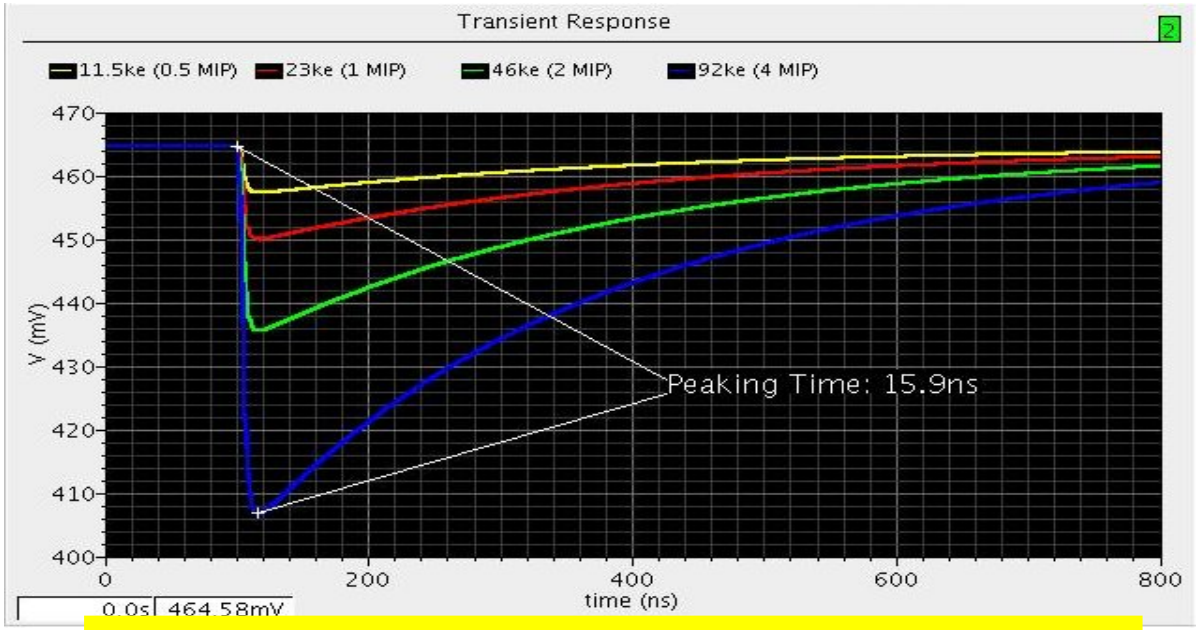


$$H(s) \approx \frac{A_{DC}}{(1+sR_SC_S)^2}$$



- O'Connor FB
- 2nd order shaper
- Shaping time: 80ns
- Unified amplifier cell
- N-MOS input
- Input range up to 47.8fC
- ≈ 3.6mW/channel

Reminder: Transient Simulation Preamplifier/Shaper



0.5, 1, 2, 4 MIPs a 23ke (@ Cdet = 30pF)

Results from simulation:

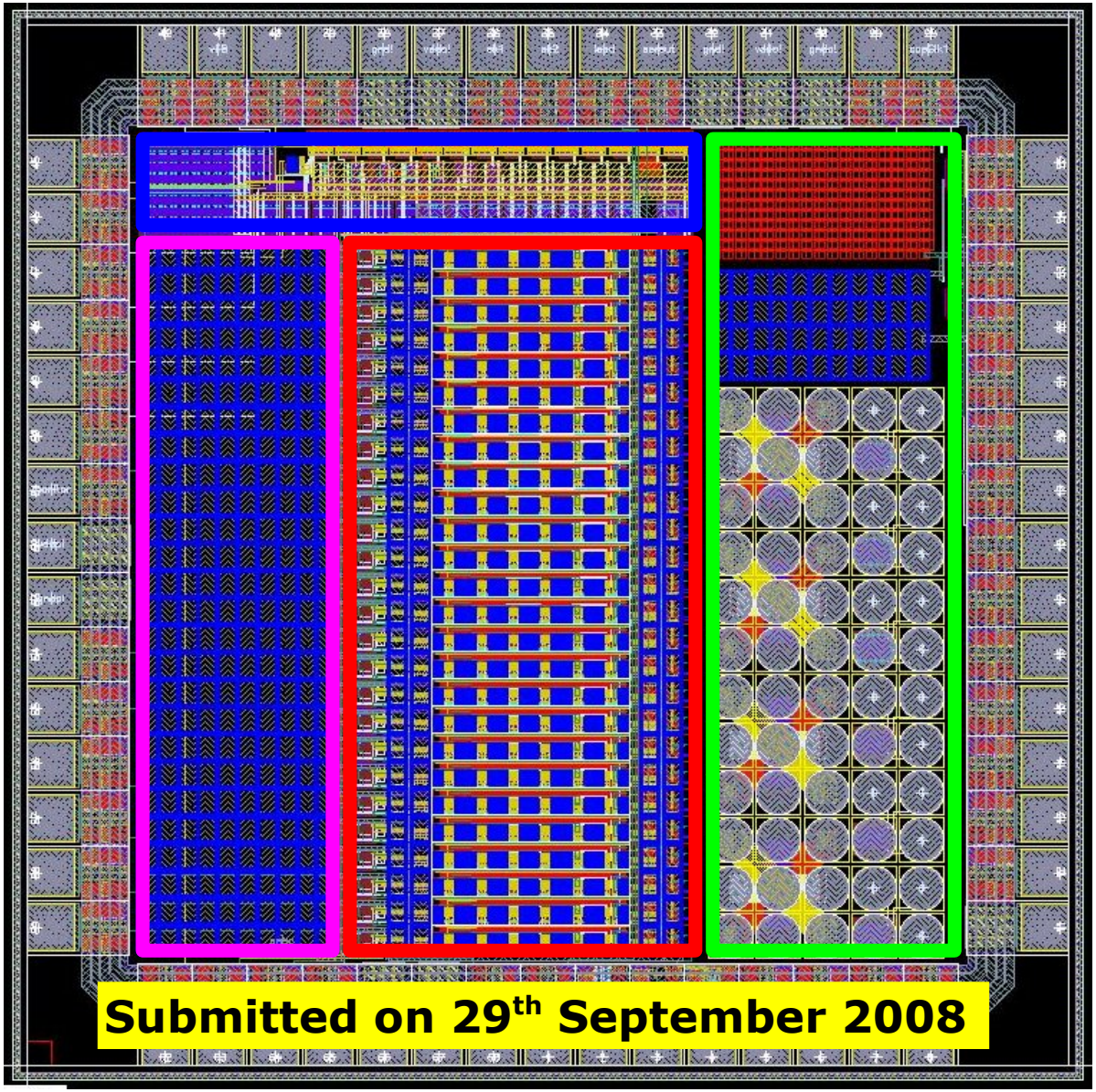
Preamplifier output

- Peaking-Time (0% - 100%): ≈16ns
- Rise-Time (10%-90%): ≈9ns
- Pulse length adjustable

Shaper output (2nd order)

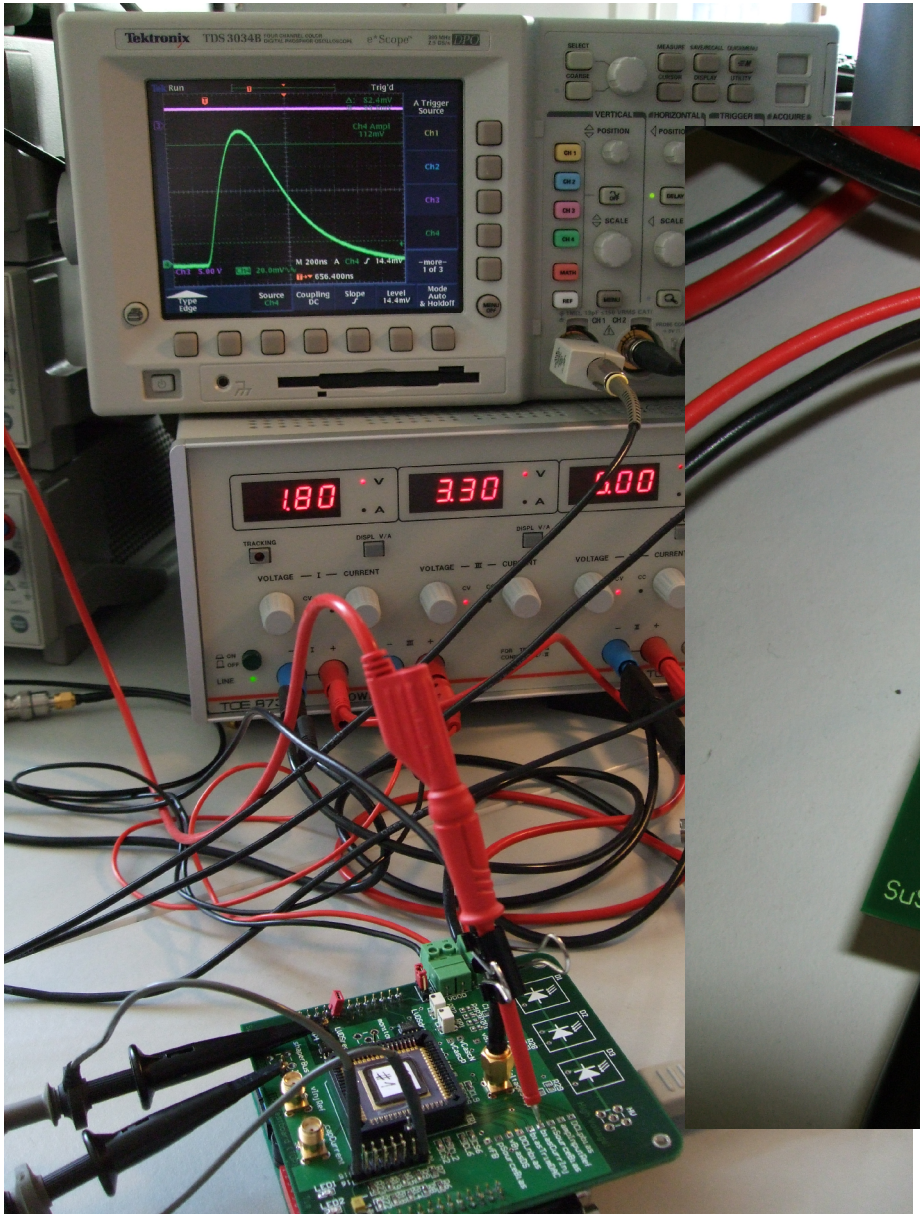
- Peaking time (0% - 100%): ≈90ns
- Rise-Time (10%-90%): ≈50ns
- High linearity, high range up to 13 MIPs (23ke/MIP)
- Gain: 13.8mV/fC (=> amplitude for MIP ≈50mV)

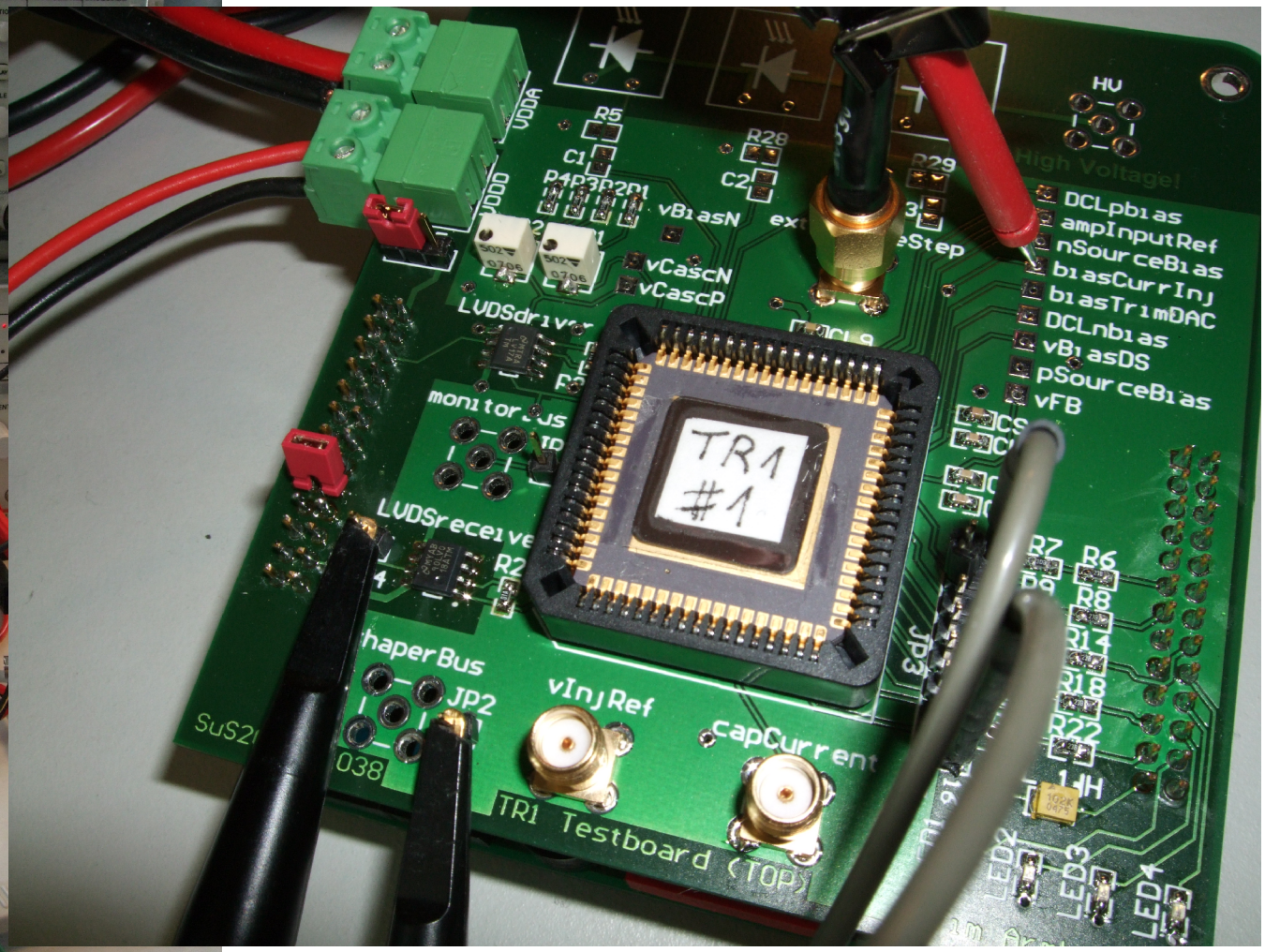
Layout Chip 2nd CSA TC



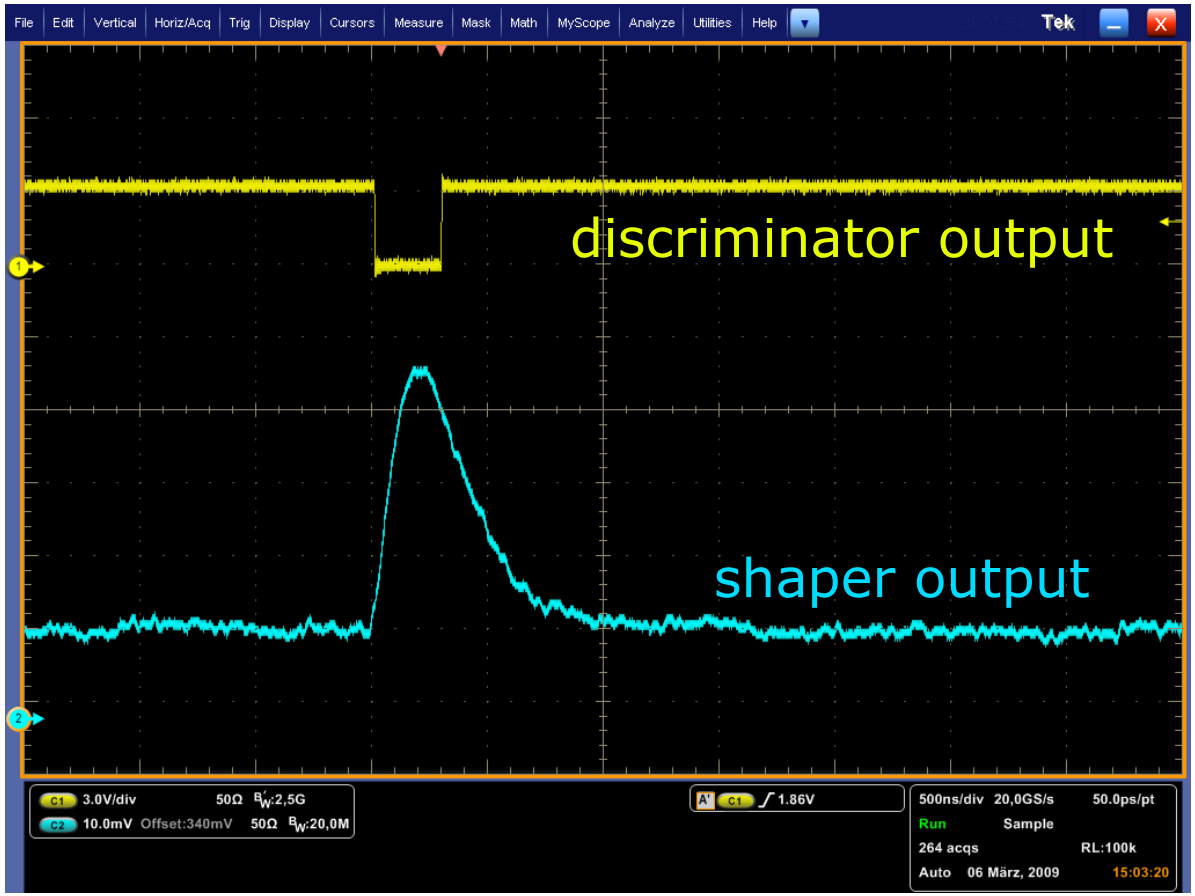
- Inj. / preamp. / shaper / disc.
  - 26 channels
  - 517µm x 1040µm
- Bias
  - DACs
  - Diodes
  - Decoupling
- Detector capacitors
  - 0pF – 20pF, 40pF
  - 290µm x 1040µm
- Test structures

Test Setup


Tektronix
TDS 3034B
1.80
3.30
5.00


TR1
#1
HV
High Voltage!
DCLpbias
ampInputRef
nSourceBias
biasCurrInj
biasTrimDAC
DCLnbias
vBiasDS
pSourceBias
vFB
vBiasN
vCascN
vCascP
LVDSdriver
LVDSreceiver
monitorBus
shaperBus
JP2
vInjRef
capCurrent
TR1 Testboard (TOP)

Transient Signals



Checklist

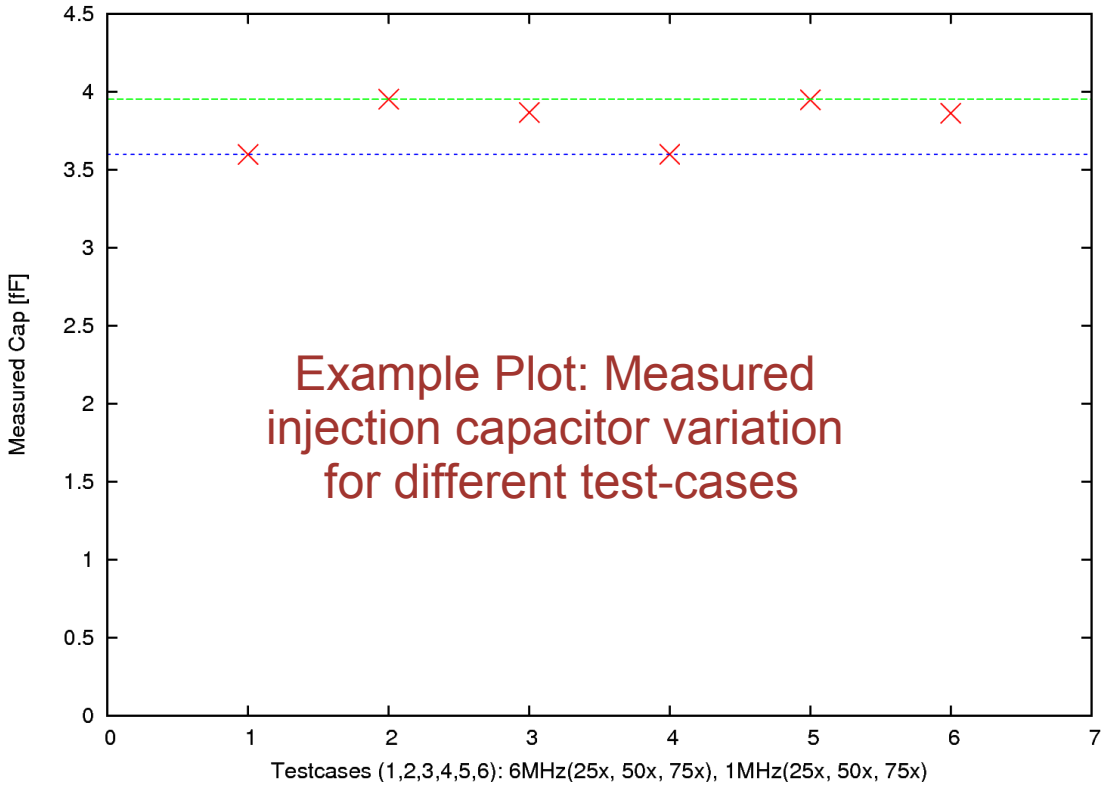
- Power consumption ok
- Bias current/voltages ok
- Shift register ok
- Test injection ok
- Software ok
- ...

Transient signal measurement:

- Shaper output is connected via monitor bus -> cannot see the “real” shape
- Discriminator is differential on chip, plot shows the hit signal after the conversion to CMOS

=> All 26 channels operate, the hole chip works, no critical bugs!

Calibration of Capacitors

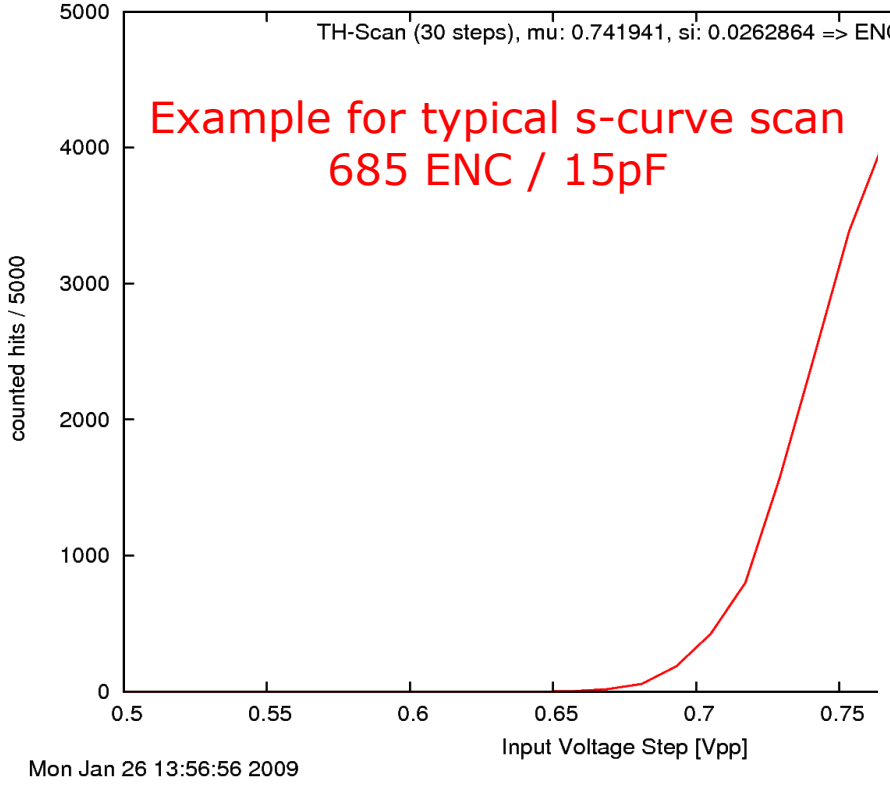


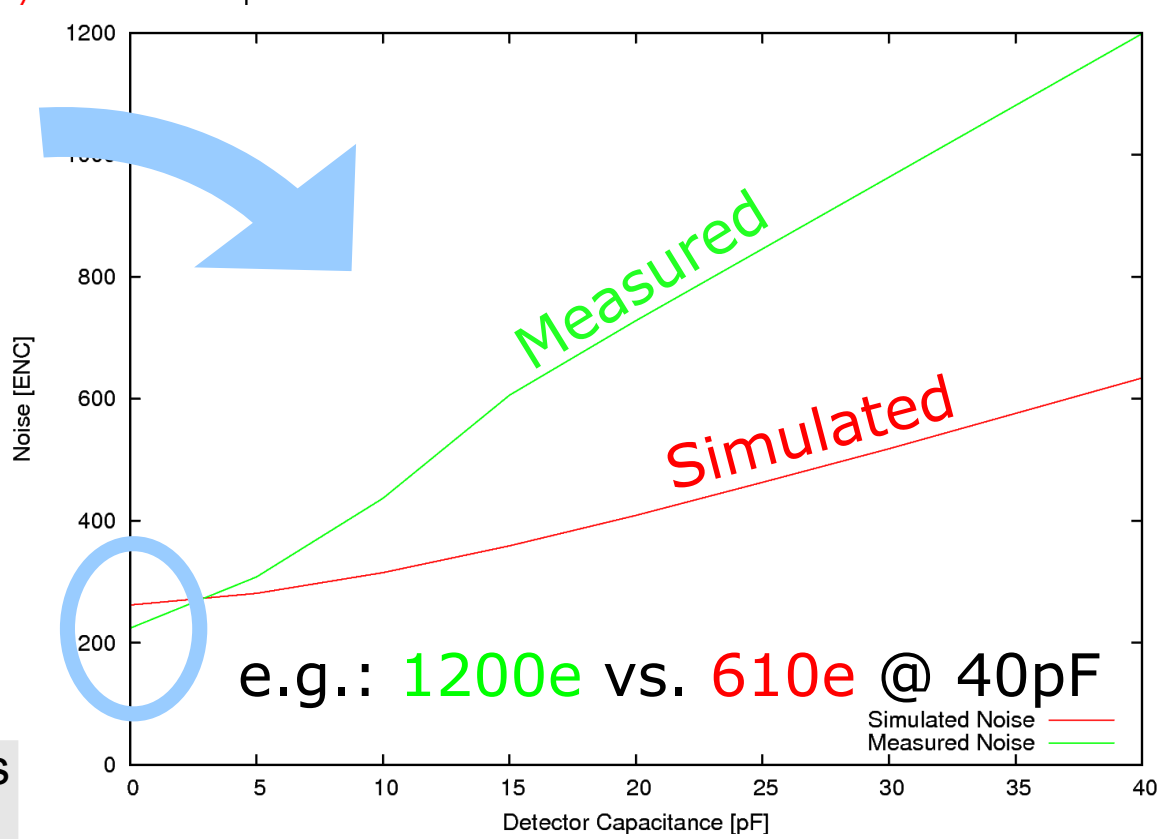
Capacitor measurement circuits on chip:

- Injection capacitor ~9% smaller than simulated/layouted (3.8fF instead of 4.18fF)
- Detector capacitors match very well with the simulated (~1pF/block)

=> All noise critical capacitors well known/calibrated

Noise Results via S-Curve Scan





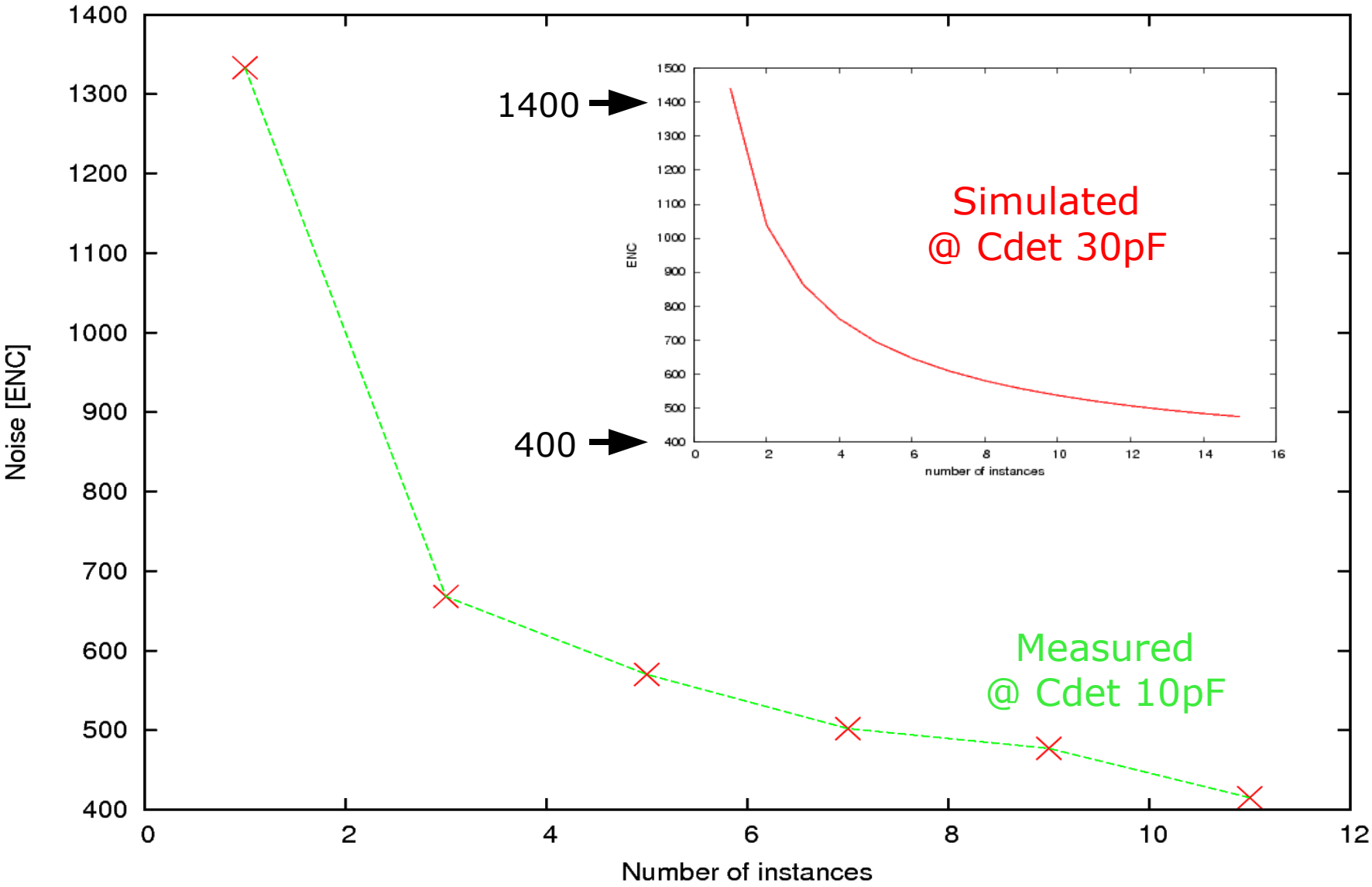
- Noise measurements via s-curve scans by using the discriminator
- Different test-cases on chip (0 - 20pF and 40pF detector capacitors)

=> Noise baseline even better than simulated but slope is factor 2 worse

Casual research still in progress – hard task

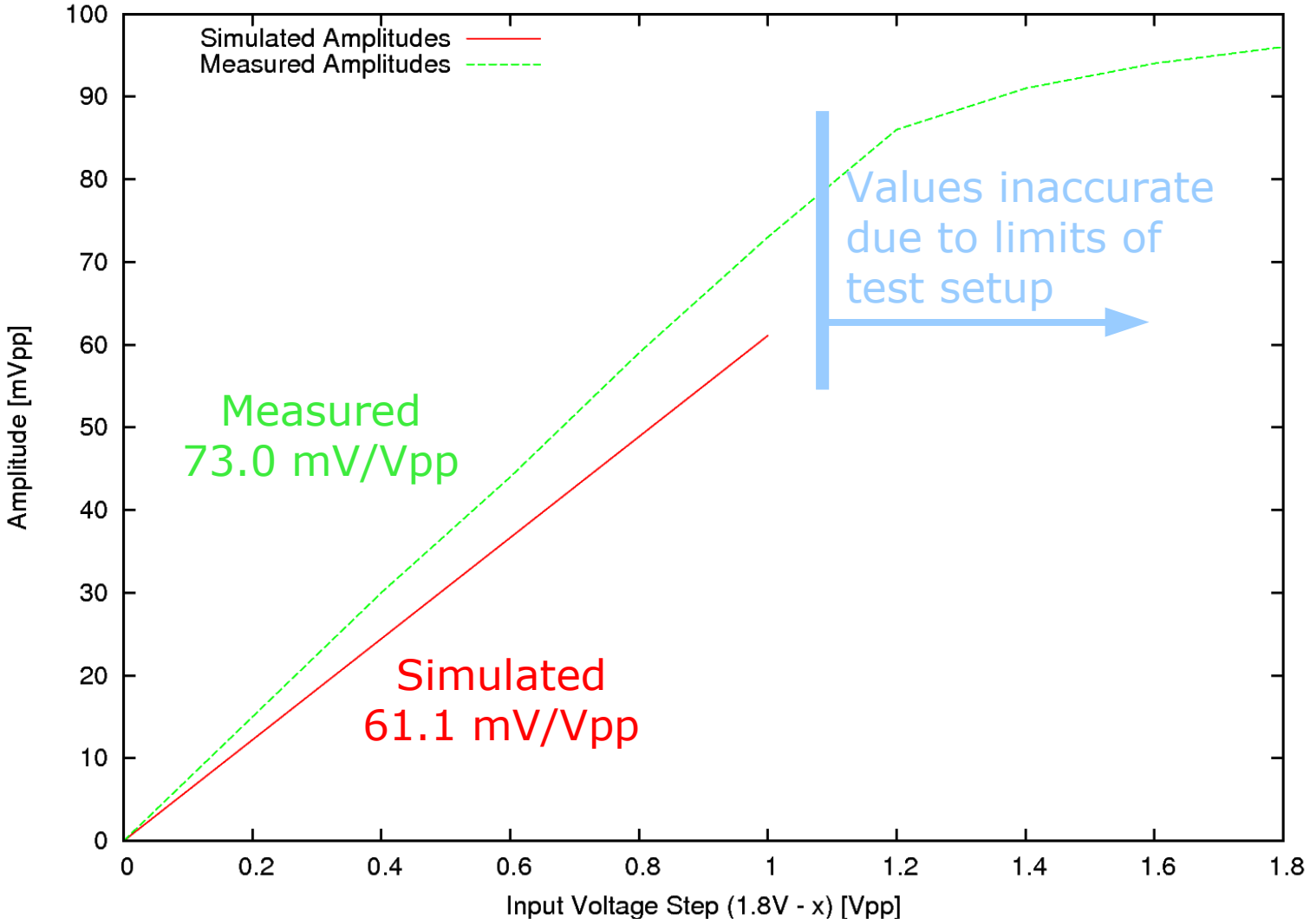
- Flicker noise? (Behavior would fit)
- Design problem? (None could be found until now)
- ...

Noise vs. Number of Amplifier-Instances



=> Shape/Behavior as predicted, but noise also worse.

Amplifier Closed Loop Gain



=> Amplitude gain (shaper output amplitude / input voltage step) is even higher than simulated -> ok!

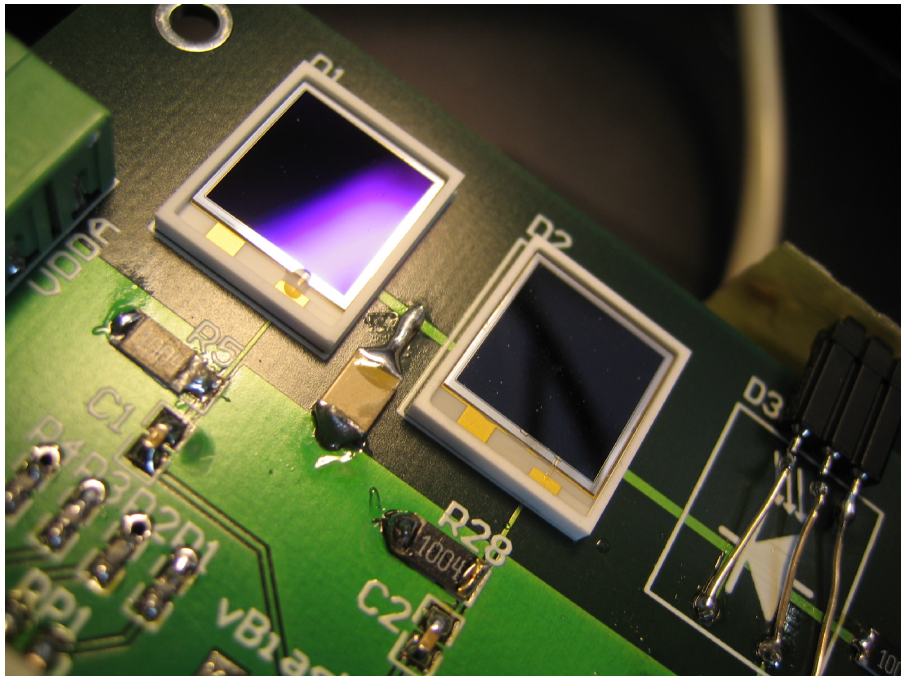
Radiation-Spectrum Measurements

The activity of an iron-source (Fe55) has been observed (with a 5pF Si-diode attached to the chip, an X-ray particle from Fe55 has ≈6keV and injects ≈1700e)

But: Amplitude/energy measurement only with low resolution possible:

- Shaper output signal is deformed due to test-bus
- Noise of test-bus is much higher than "real" noise at shaper output
- TOT with the gaussian shaper pulses very non-linear

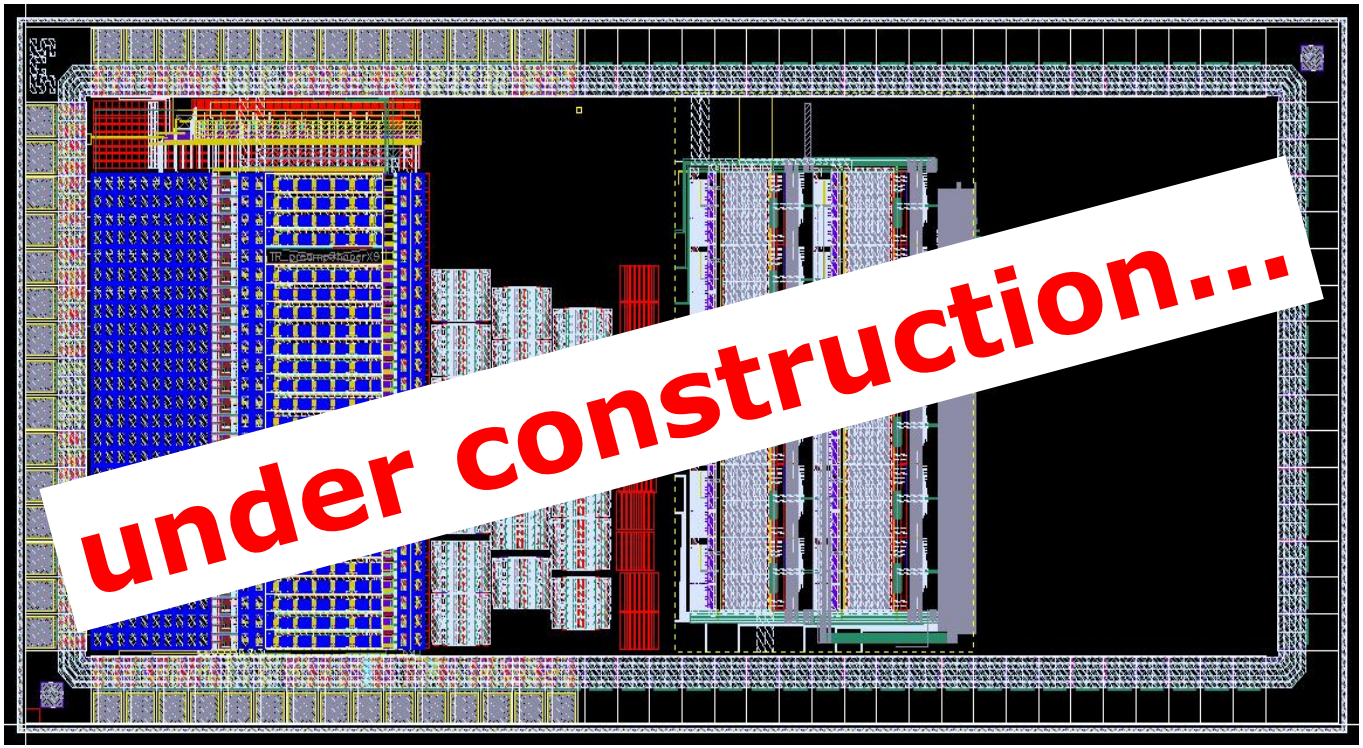
Nevertheless, spectra of Co60 and Na22 could be measured – but I'm not sure, how they should look like... (so they are not shown here)



Next Steps

The next iteration of the CSA-testchip has nearly been finished:

- Improvements of layouts and schematics: only minor changes, but many of them
- New test-channel with non-minimal channel-length (L): lower flicker noise?
- New Pipeline ADCs connected to the channel outputs, see separate talk
- Larger die: 2x1 Mini@sics (3240µm x 1525µm)
- **Submission on March the 23th**



Thank you!

Summary (Simulation)

26 channel csa test chip, submitted on 29th September 2008

- Design highlights
  - 2nd order shaper
  - 3-way test injection
  - CML-discriminator with threshold trim
  - Compact layout (Channel size: 40µm x 517µm)
  - Most bias generation is on-chip (33 8-bit-DACs)
- Typical values (30pF detector cap., 11x VAC)
  - Power consumption: 3.6mW/channel
  - Gain: ≈14mV/fC
  - Shaping Time: 80ns
  - Noise (ENC): 480e
  - Rise-Time Shaper: 50ns
  - Input range: 0 - 13MIPs (0 - 47.8fC)