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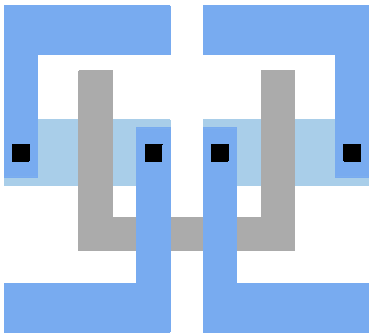
Algorithmic Pipeline ADC

Ivan Perić's new current-mode ADC design



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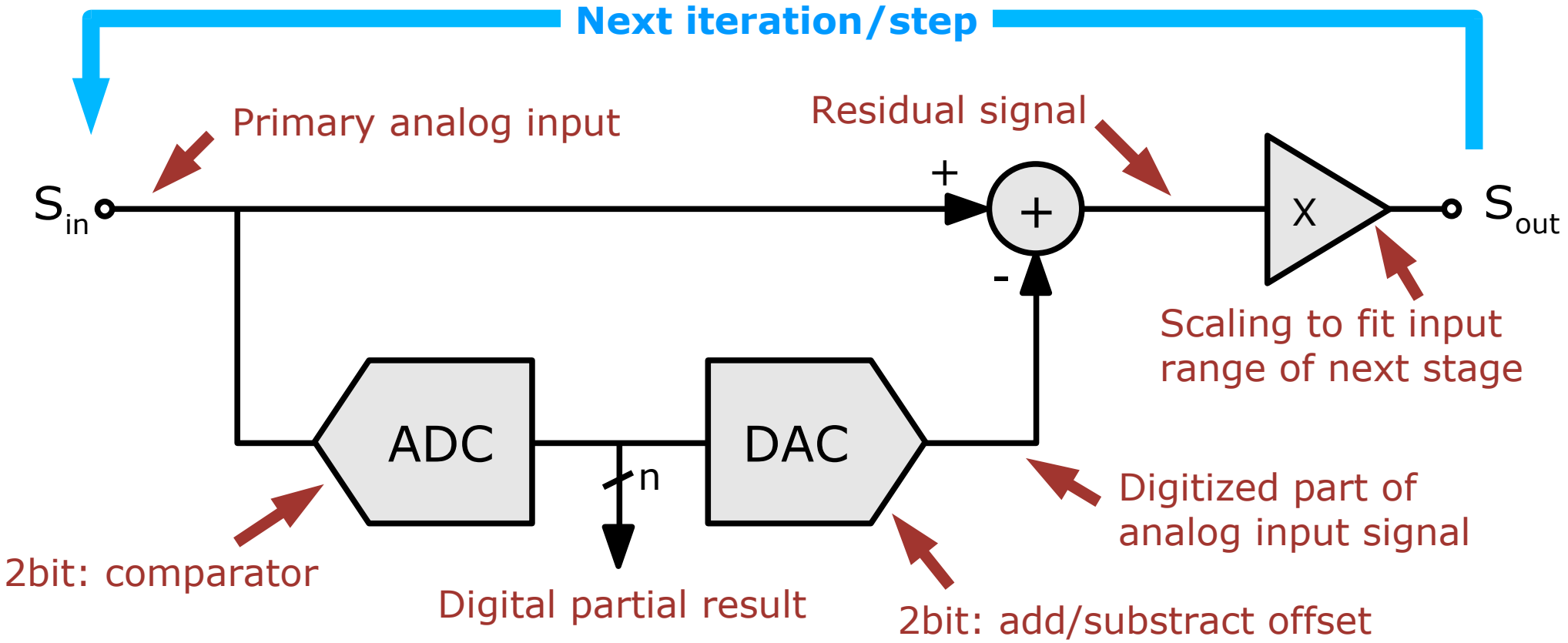
ADC Overview and Application

- Ivan Perić's ADC
  - Algorithmic ADC with pipeline structure
  - UMC018 design
  - Radiation hard layout
  - Current-mode architecture based on new current-memory cell
  - ≈ 9bit @ 25MS/s, 4.5mW
  - Cyclic version already established (in other projects)
- ADC is being integrated into next CSA test-chip iteration
  - ≈ 8 ADC connected to preamp outputs intended
  - Readout logic: dynamic shift register matrix feeds parallel adder
  - Design of ADC and readout logic has been finished
  - Submission: March the 23th

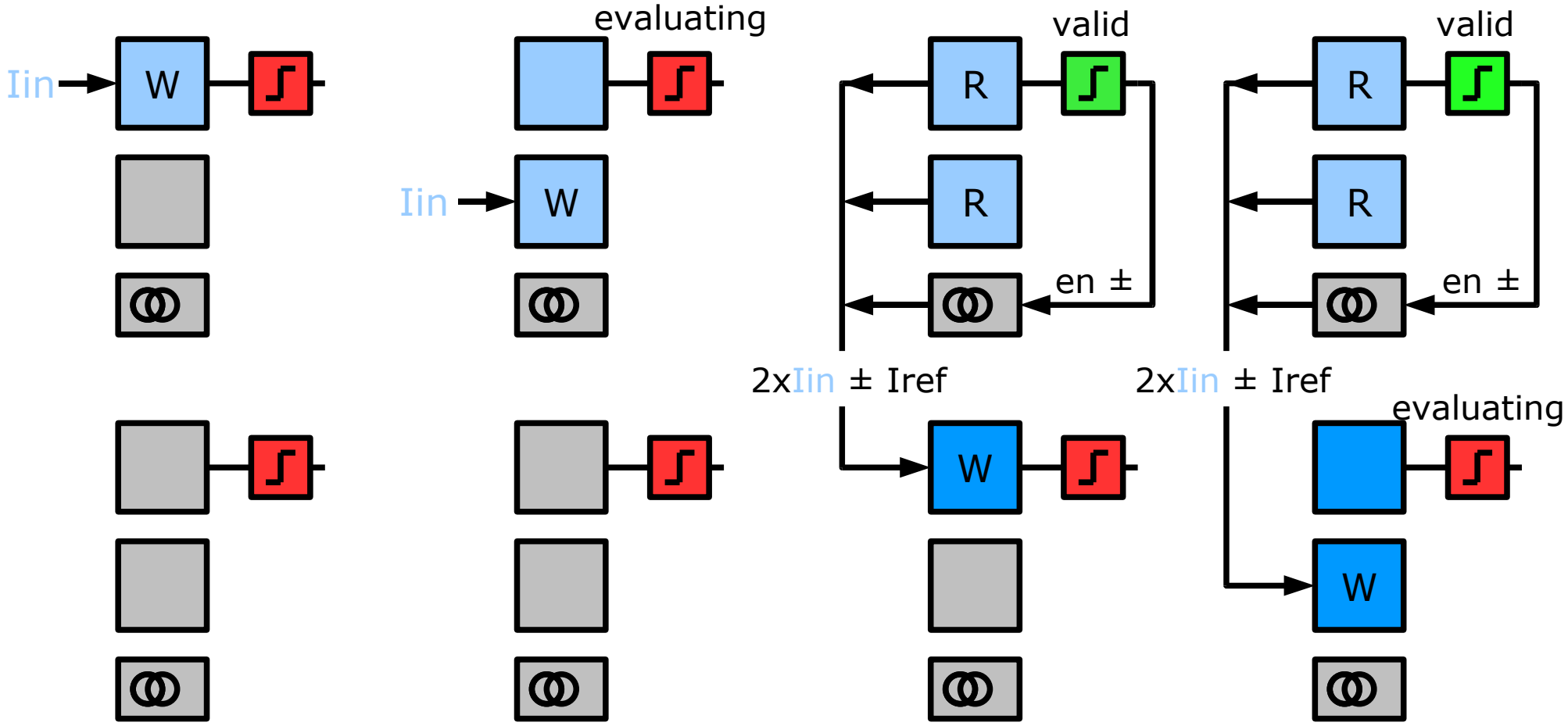
Algorithmic Idea



- Typical case: 2bit per stage/iteration (“1.5bit method”)
- Evaluation logic needed (adder)

=> 4 building blocks required: **(simple) ADC, (simple) DAC, adder, multiplier**

Current Based Realization (1/2) – Cyclic Method



Step 1
- Write cell 1

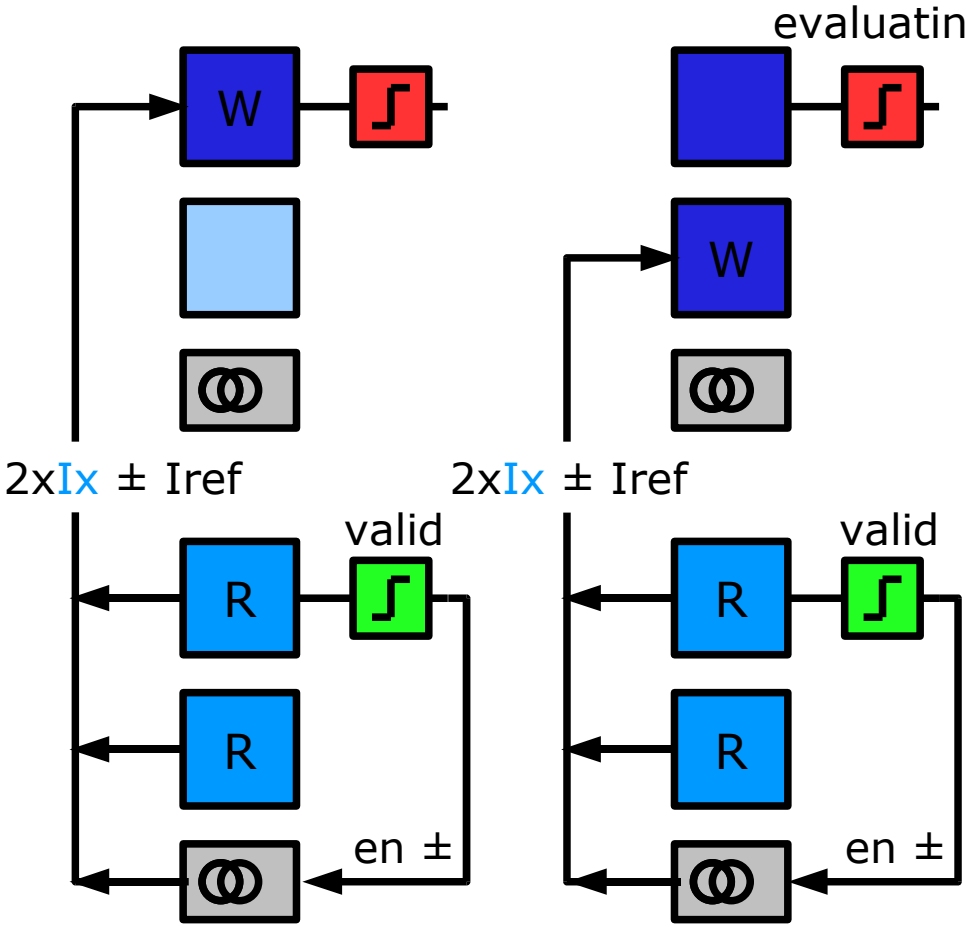
Step 2
- Write cell 2
- Comp. 1 is eval.

Sampling

Step 3
- Read cell 1+2
- Comp. 1 is valid
- Write cell 3

Step 4
- Read cell 1+2
- Comp. 1 is valid
- Write cell 4
- Comp. 2 is eval.

Current Based Realization (2/2) – Cyclic Method



Step 5
- Read cell 3+4
- Comp. 2 is valid
- Write cell 1

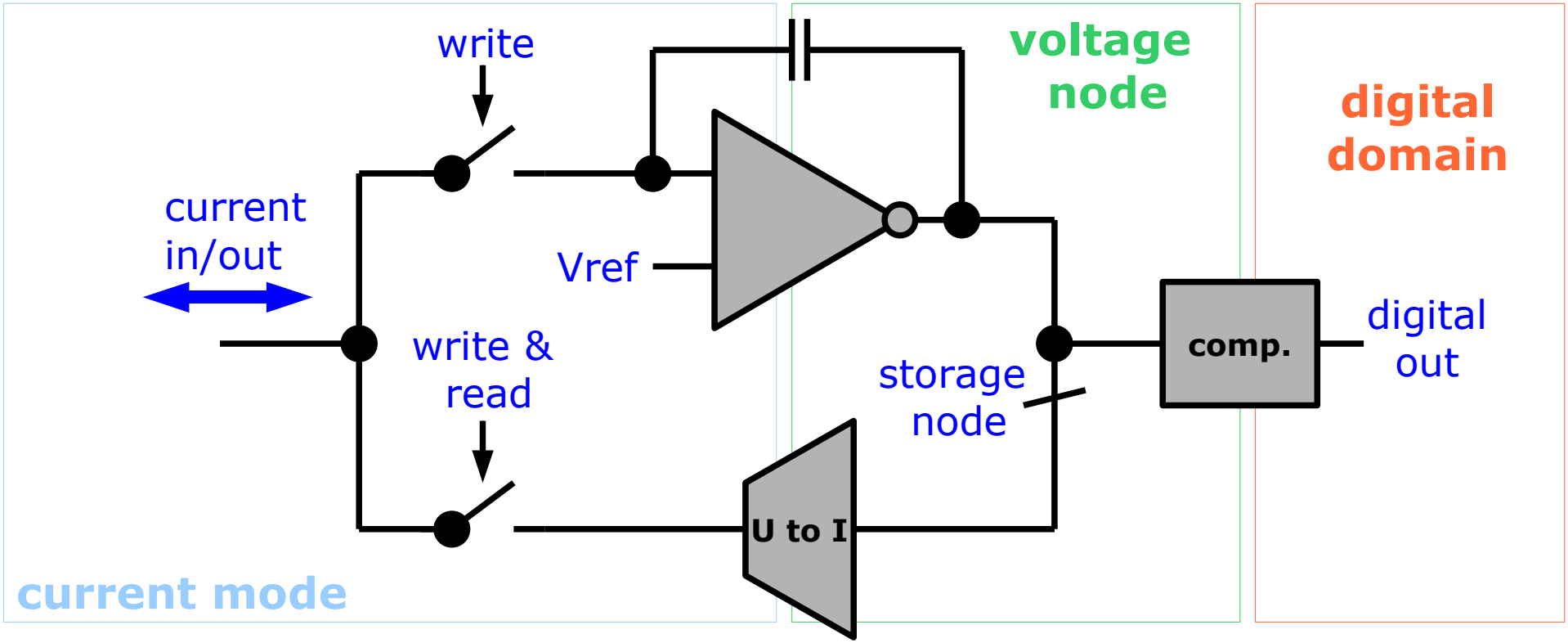
Step 6
- Read cell 3+4
- Comp. 2 is valid
- Write cell 2
- Comp. 1 is eval.

Note: Cyclic method sketched here -> parallel ADC copies current from stage to stage

Necessary building blocks:

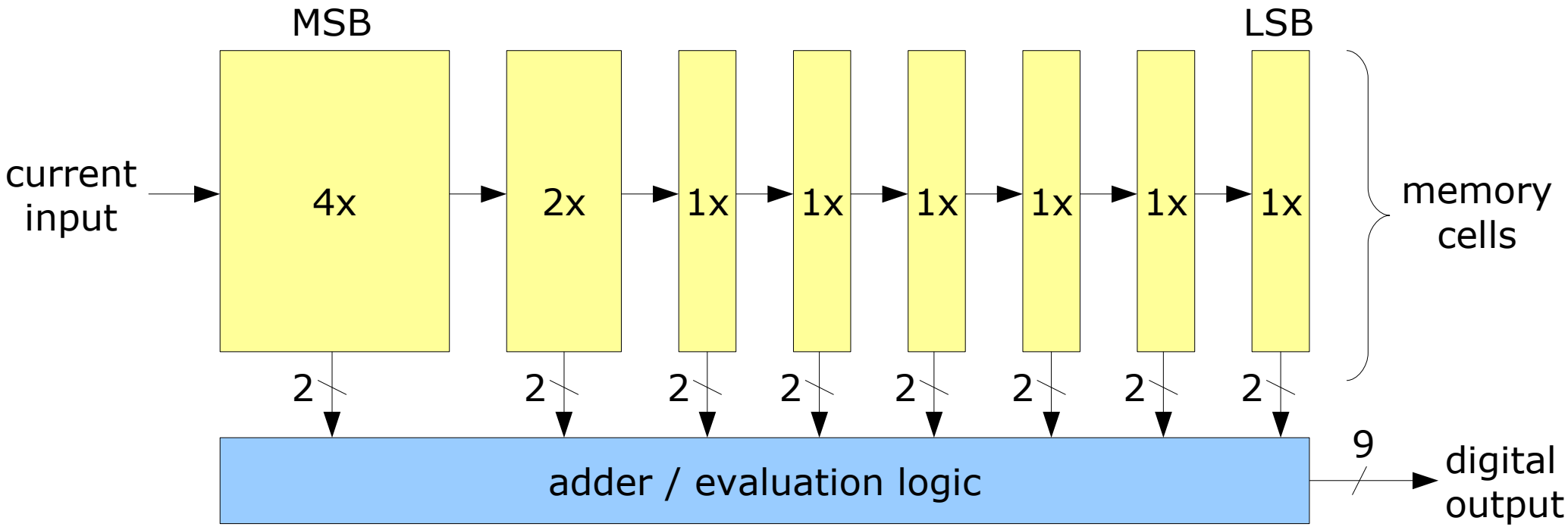
- **Multiplication** is done by writing the same current twice into different cells
- The comparator represents the 1.5-bit **ADC**, it's result equals the partial conversion result of the algorithmic-ADC
- The 1.5-bit **DAC** is realized using current sources that add or subtract a fixed reference current
- Due to the use of currents, the **adder** is "for free".

Current Memory Cell (simplified)



- Write: integrator output voltage increases until current flowing into cell is compensated by the transconductor output current
- Read: transconductor provides the stored current
- Current mode: input/output voltage DC-levels are always at Vref
- Good: comparator can be connected to voltage-storage-node

Realized Pipeline Structure

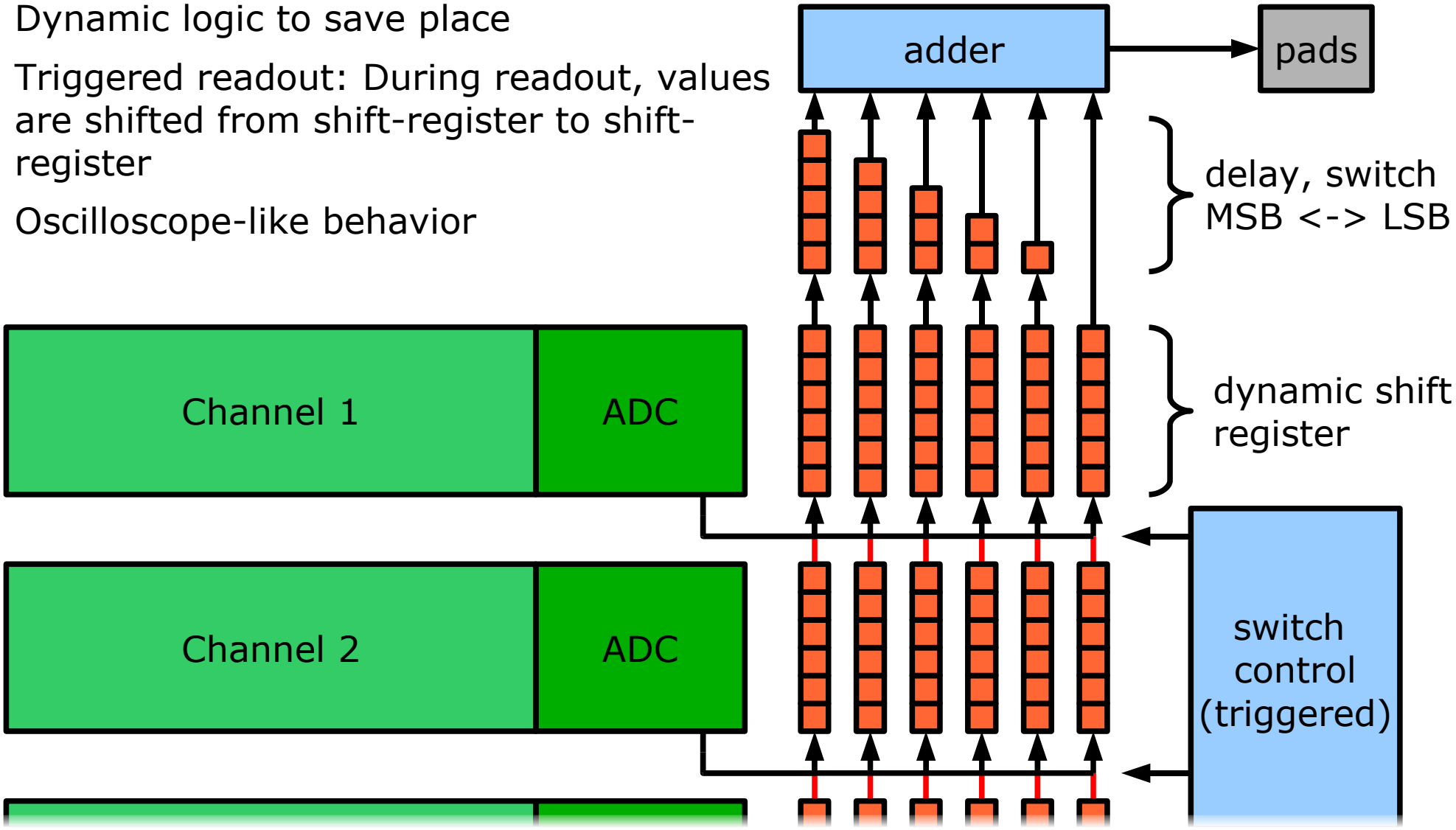


- Pipeline with 8 stages providing a 9bit resolution
- First two stages are scaled to minimize noise
- 8x2bit @ 25MHz - bits in redundant signed binary (RSD) representation (-1,0,+1)
- Output comes MSB first -> wrong order for adder
- Parallel adder with delay stairways needed

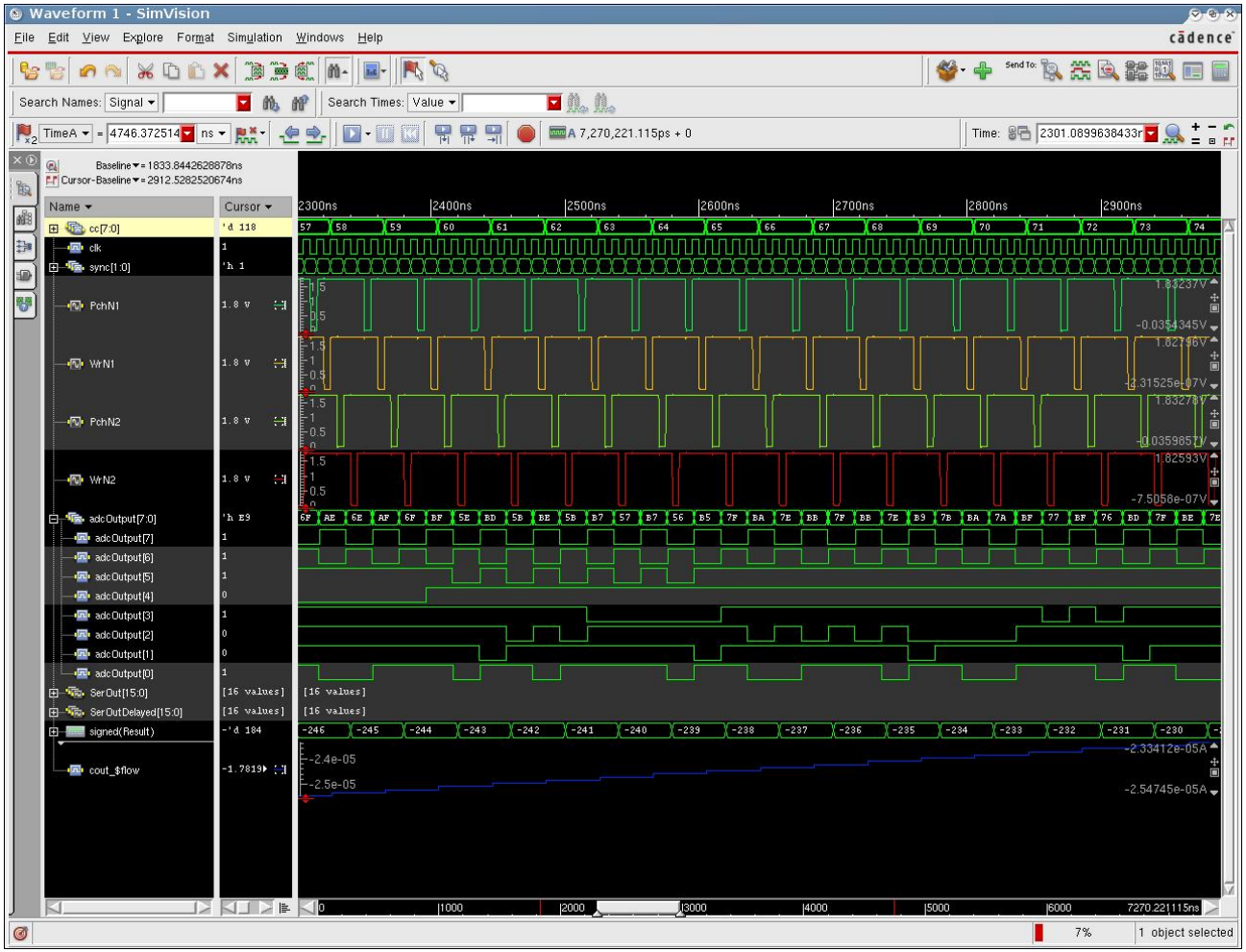
ADC Readout in next CSA test-chip

Easy readout for test-chip:

- Dynamic logic to save place
- Triggered readout: During readout, values are shifted from shift-register to shift-register
- Oscilloscope-like behavior

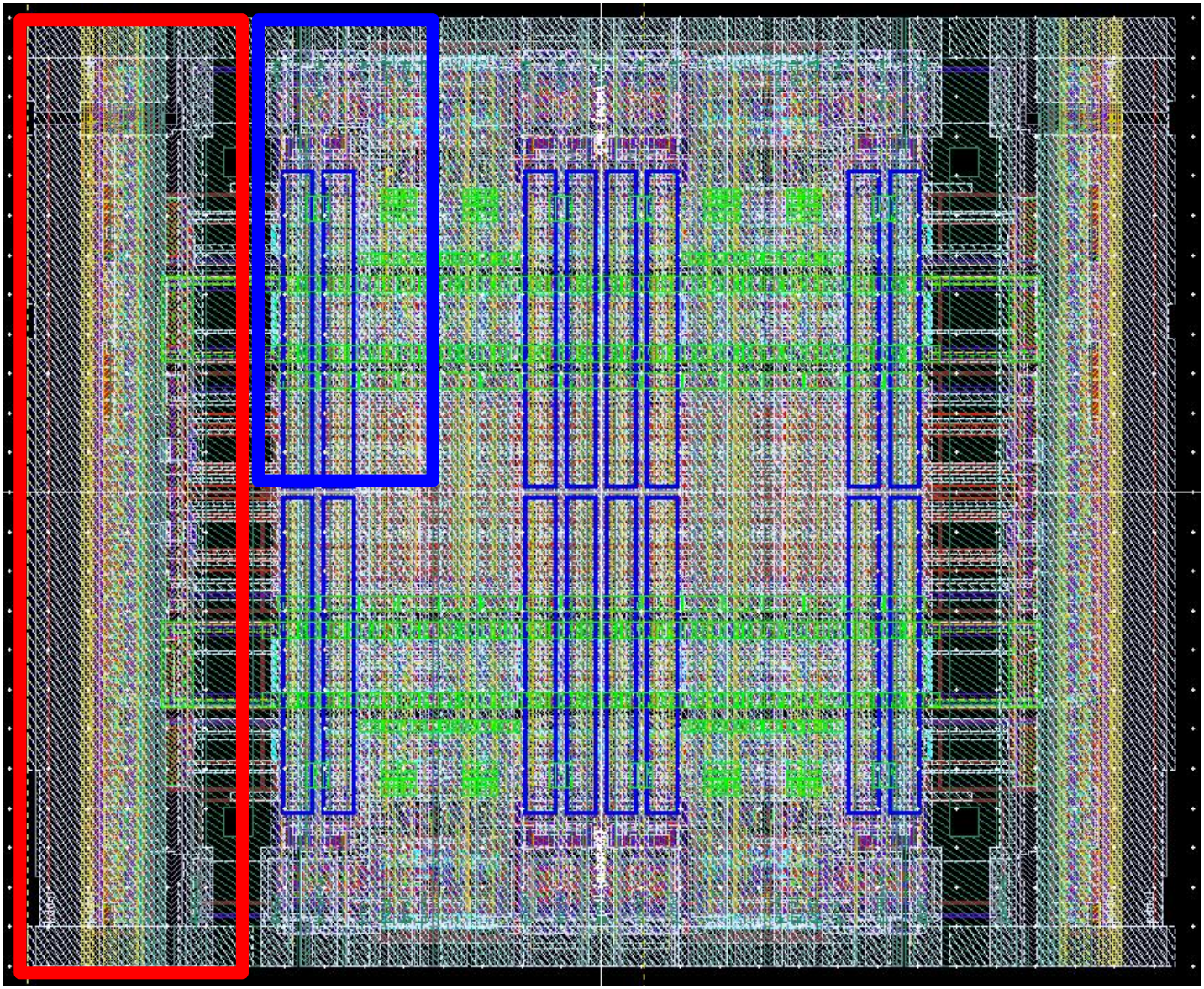


Mixed-Mode Simulation



- Complex ADC design + confusing readout logic => predestinated for a mixed-mode simulation
- Just to show you: it works :-)

Layout Complete ADC



- 110µm x 140µm
- Control logic (redundant)
- 4 current memory cells, 2 comparators = 1 stage

Thank you!