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Status of CBM-XYTER Development

Latest Results of the CSA/ADC Test-Chip

Schaltungstechnik
und Simulation

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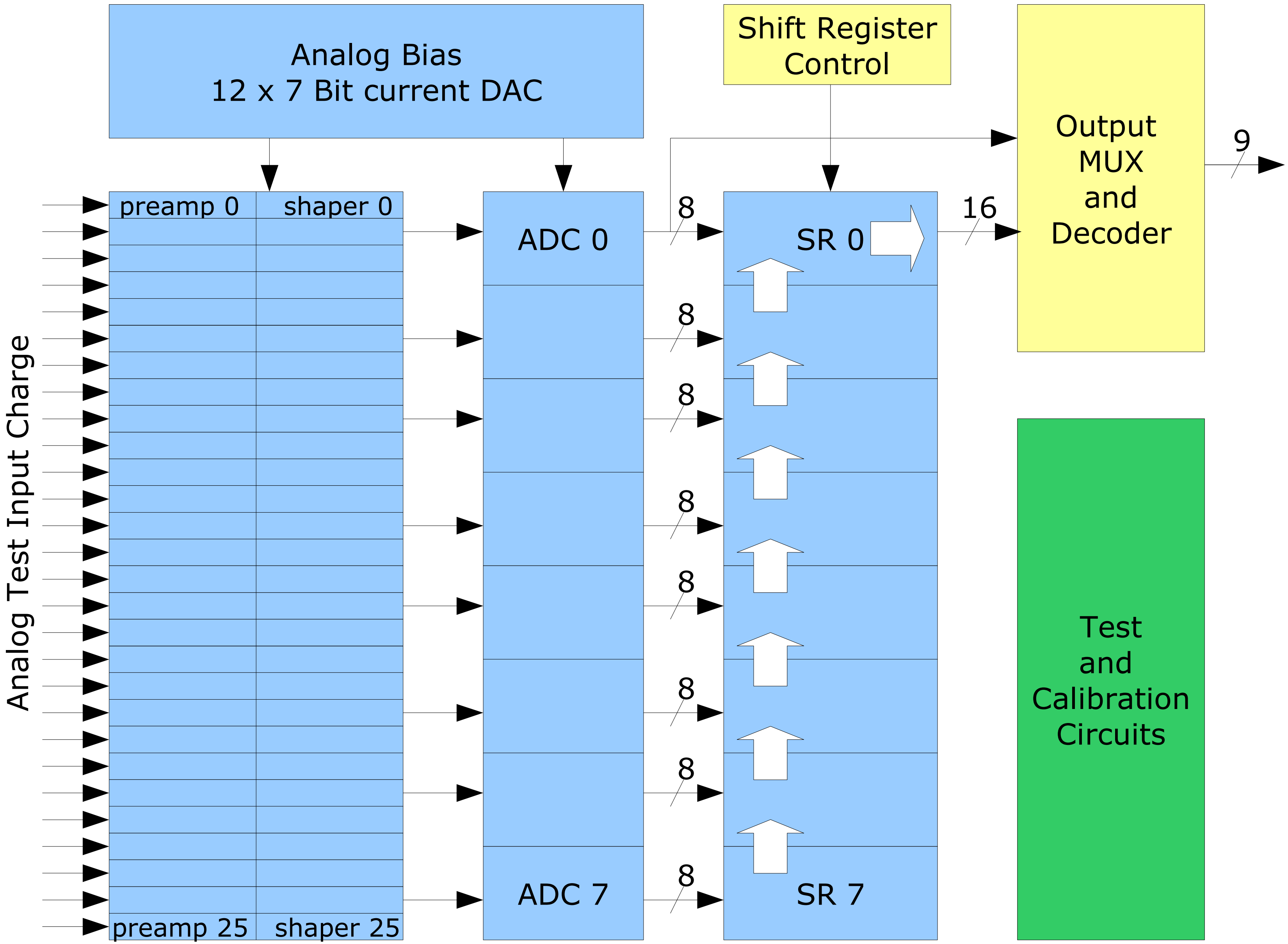
14th CBM CM Split

October 2009

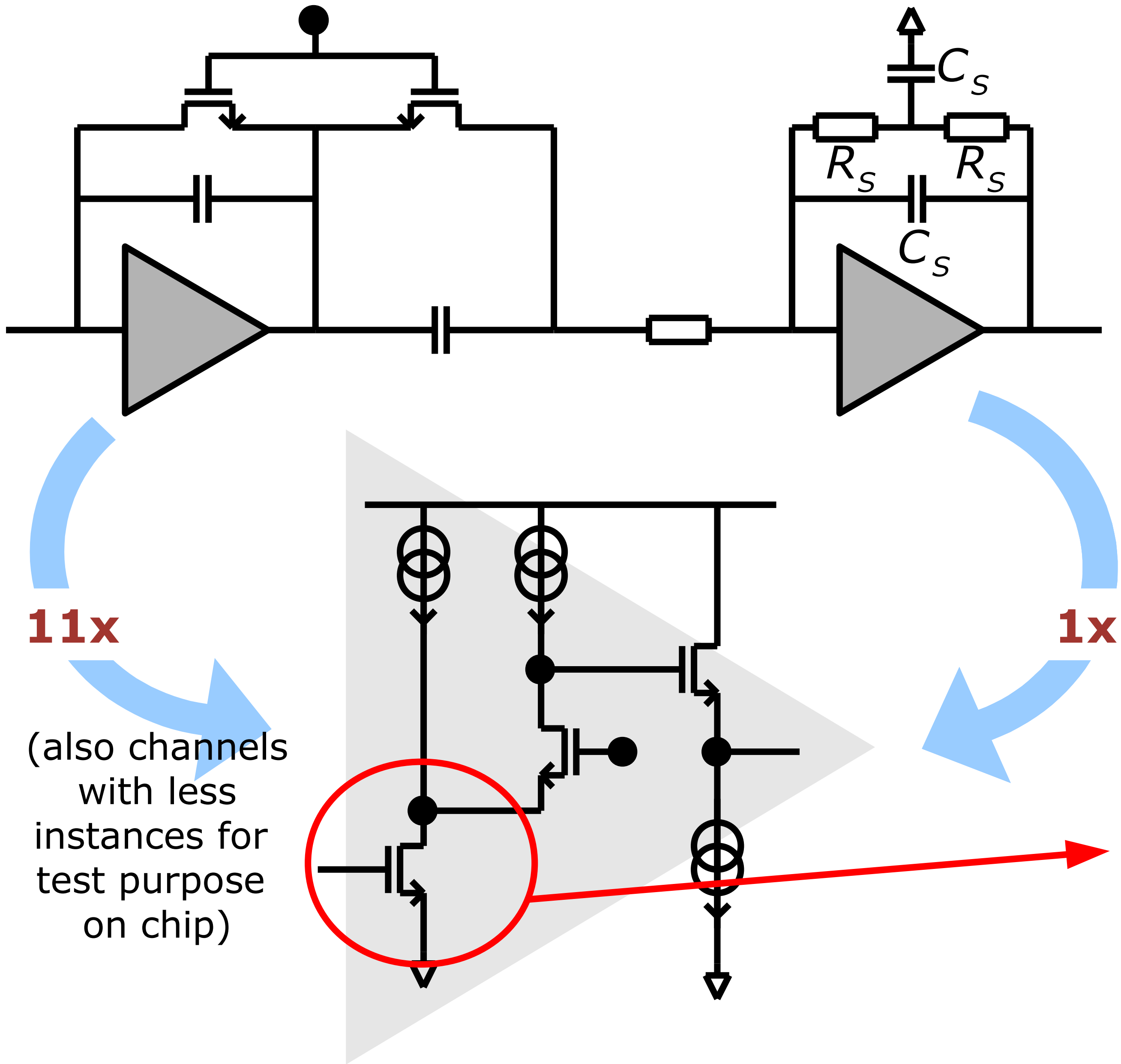
Introduction

- Reminder: Last Test-Chip
  - 1x1 Mini@sic blocks (1.5 x 1.5 mm²), UMC 0.18µm
  - 26 channels (injection, preamp/shaper, discriminator)
  - Results: power, bias, pulse-shapes, ... good, but measured noise much worse than in simulation
- This talk: Design + results of the new prototype ASIC
  - 1x2 Mini@sic blocks (1.5 x 3.2 mm²), UMC 0.18µm
  - 26 channels (injection, preamp/shaper, discriminator)
    - Refined layout + smaller schematic improvements
    - 3 different types of input N-MOS (normal, no-triwell, long)
  - New: 8 pipelined 9 Bit ADCs
    - Algorithmic processing based on novel current storage cell
    - Dynamic 3 transistor storage cell matrix
    - Synthesized readout logic and decoder

Current Prototype: Architecture Overview



Reminder: Preamplifier/Shaper Circuit



(also channels with less instances for test purpose on chip)

$$H(s) \approx \frac{A_{DC}}{(1+sR_S C_S)^2}$$

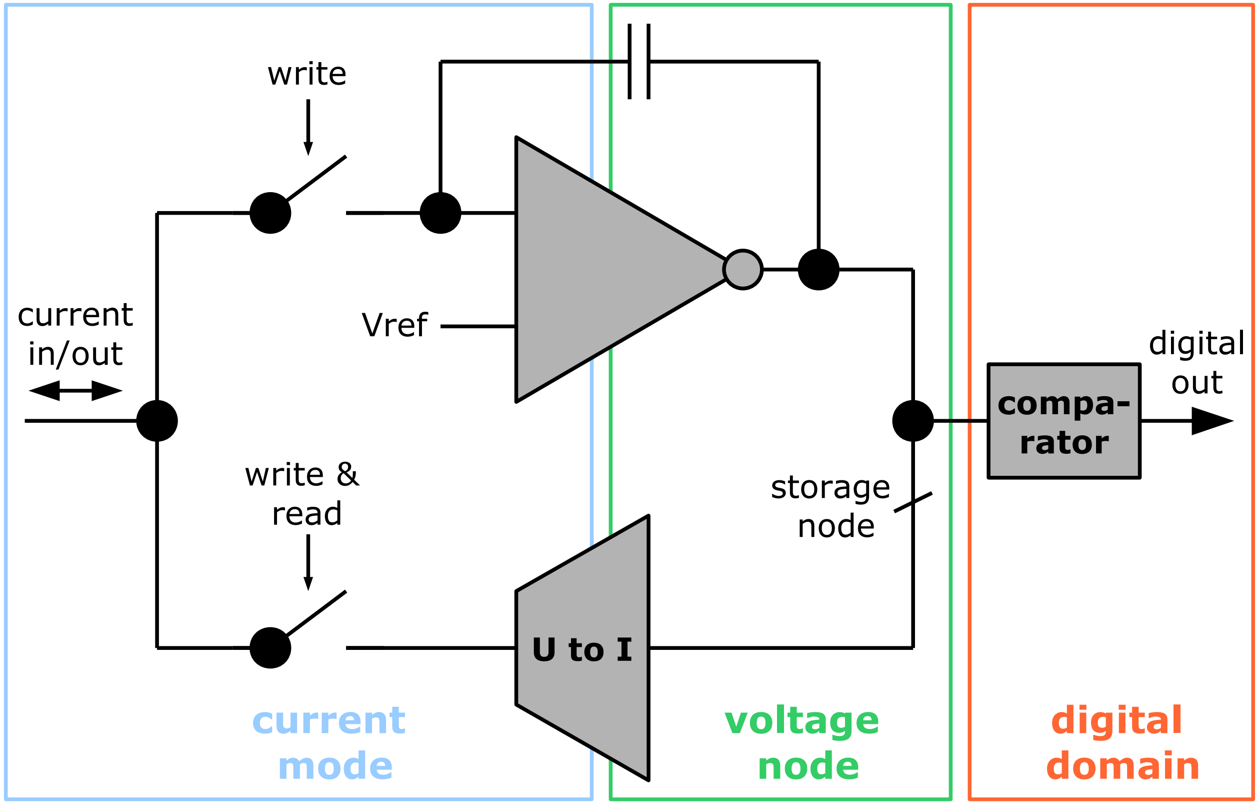
- O'Connor FB
- 2^{rd} order shaper
- Shaping time: 82 ns
- Unified amplifier cell
- N-MOS input
- ≈ 3.6 mW/channel

New: For noise analysis: 3 different input NMOS types

- normal: NMOS, triwell, 180nm length
- no-triwell: NMOS, no-triwell, 180nm length
- long: NMOS, triwell, 320nm length

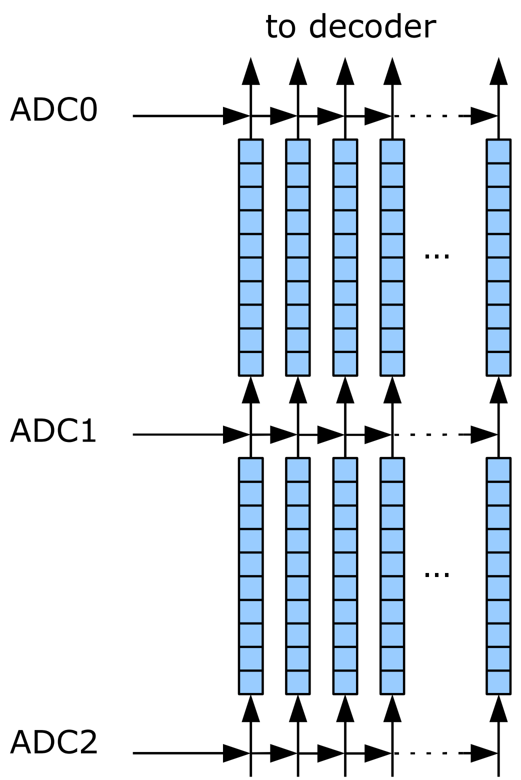
Ivan's Algorithmic ADC Design

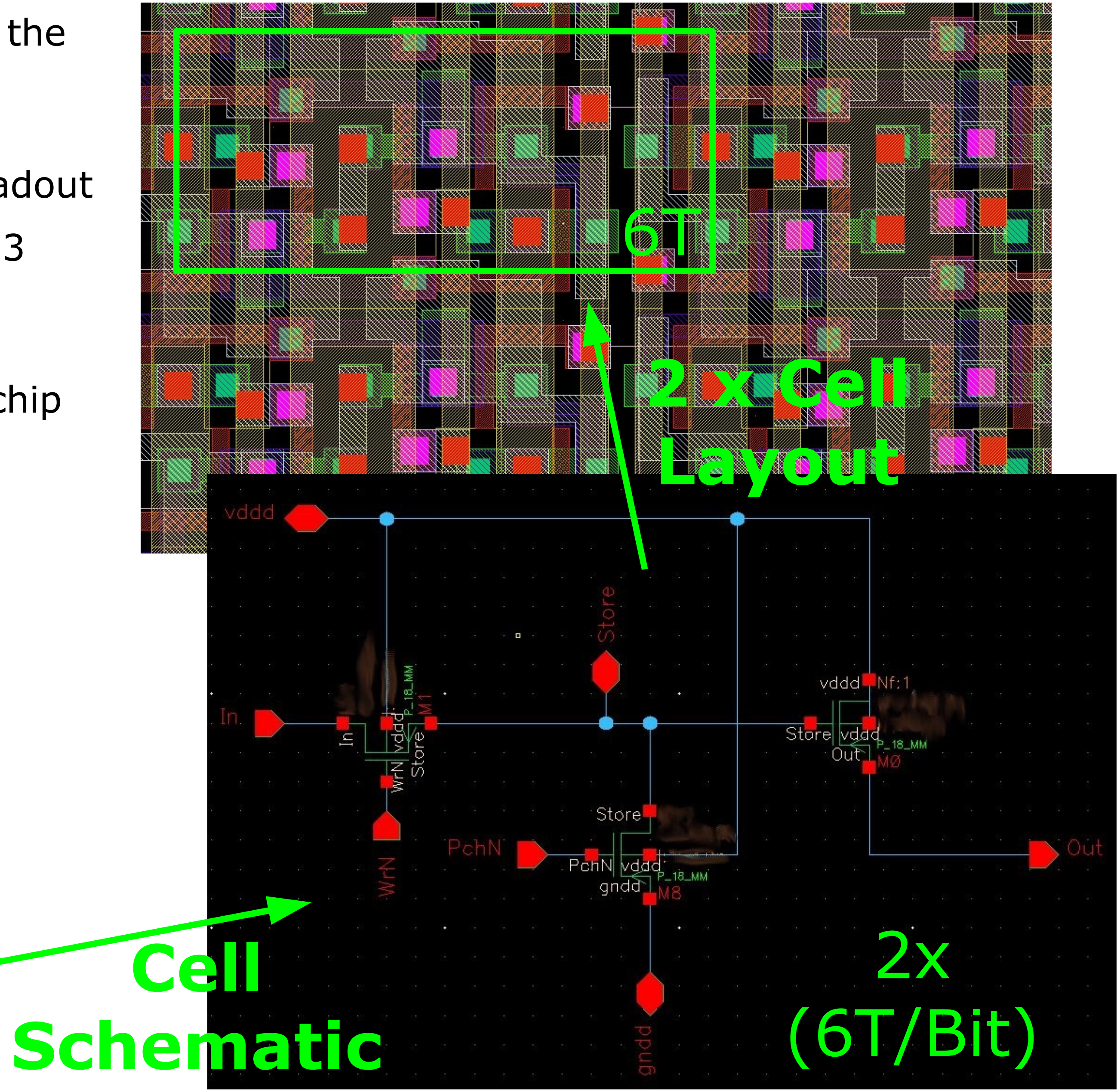
- 8 (scaled) pipeline stages, therefore 9 Bit design
- Algorithmic working principle (“1.5 redundant Bits” / conversion step)
- 25 MSamples/s, layout only 130x120 µm², power consumption 4.5 mW
- Core unit: Novel current storage cell:

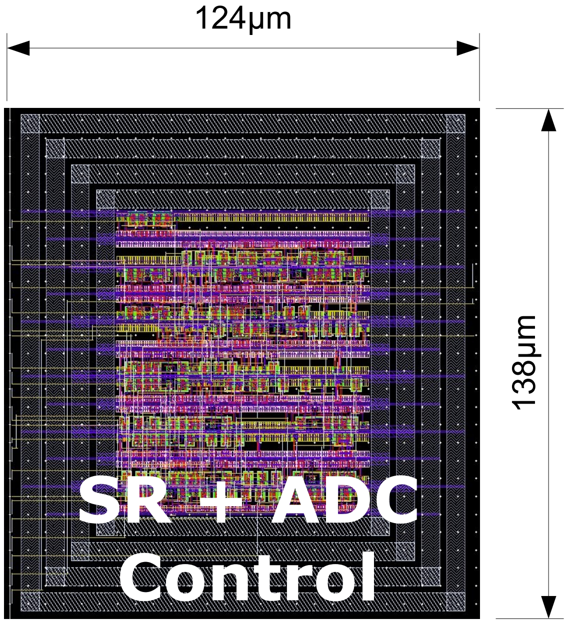


Readout Buffer: Shift Register Matrix

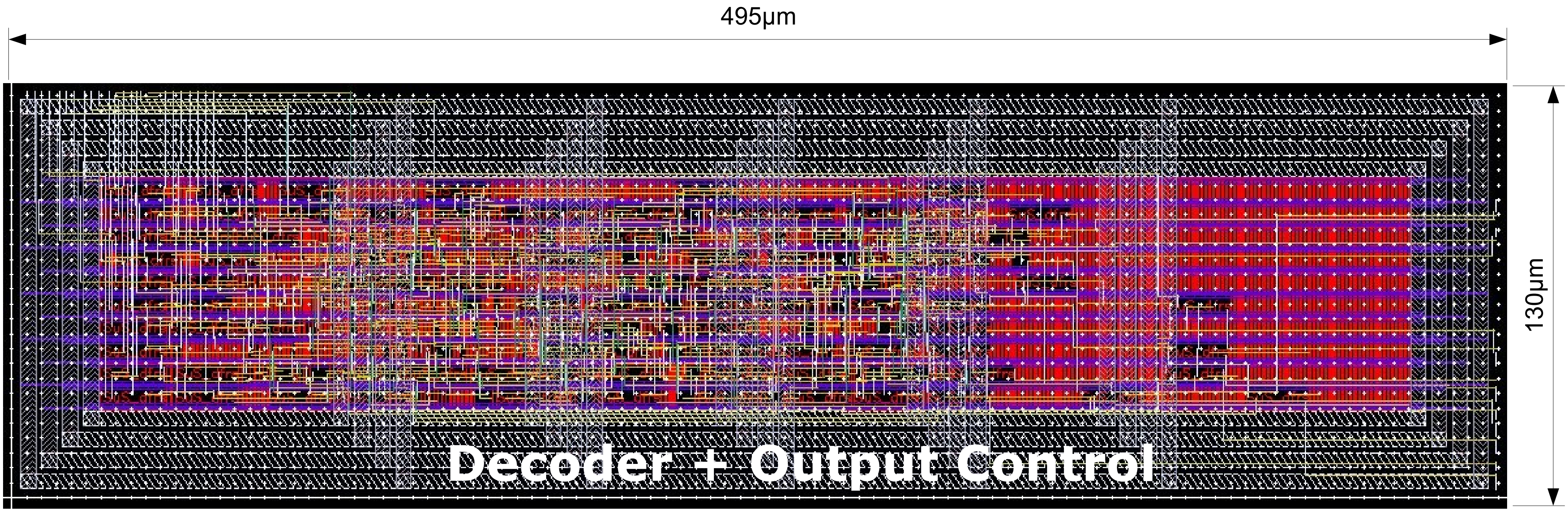
- Shift register matrix can hold the last 40 ADC output values
- Shift registers of all ADCs connected in series during readout
- Small and compact: dynamic 3 transistor storage cell, only 6 transistors per SR-Bit
- Total memory of 5.3 kBit on chip



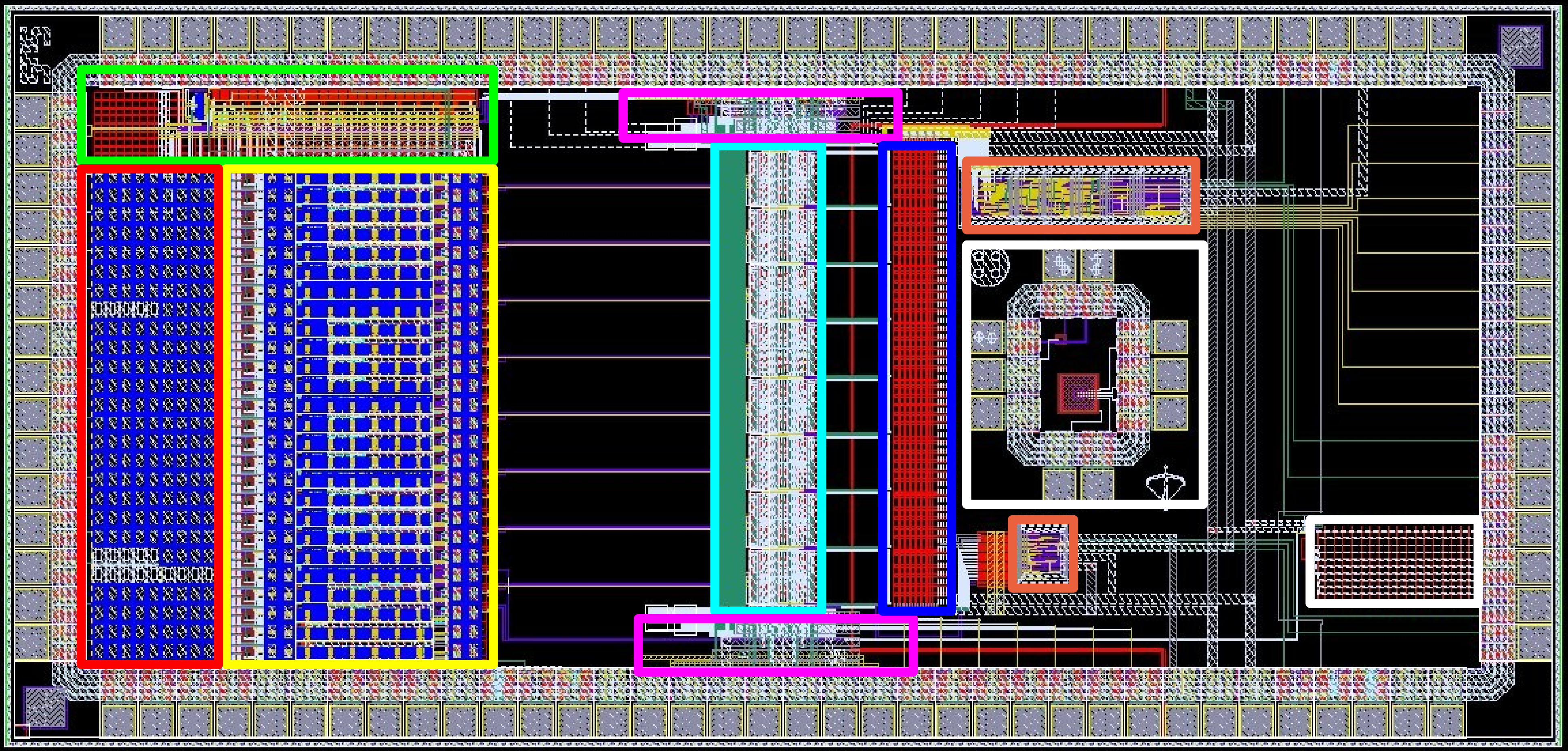




- Two synthesized blocks using our radiation-tolerant standard cell library
- Main CLK frequency is 200 MHz
- Shift Register + ADC Control: Several ADC + SR control signals and hit trigger logic
- Decoder + Output Control: redundant signed binary to signed binary converter, output multiplexer,...



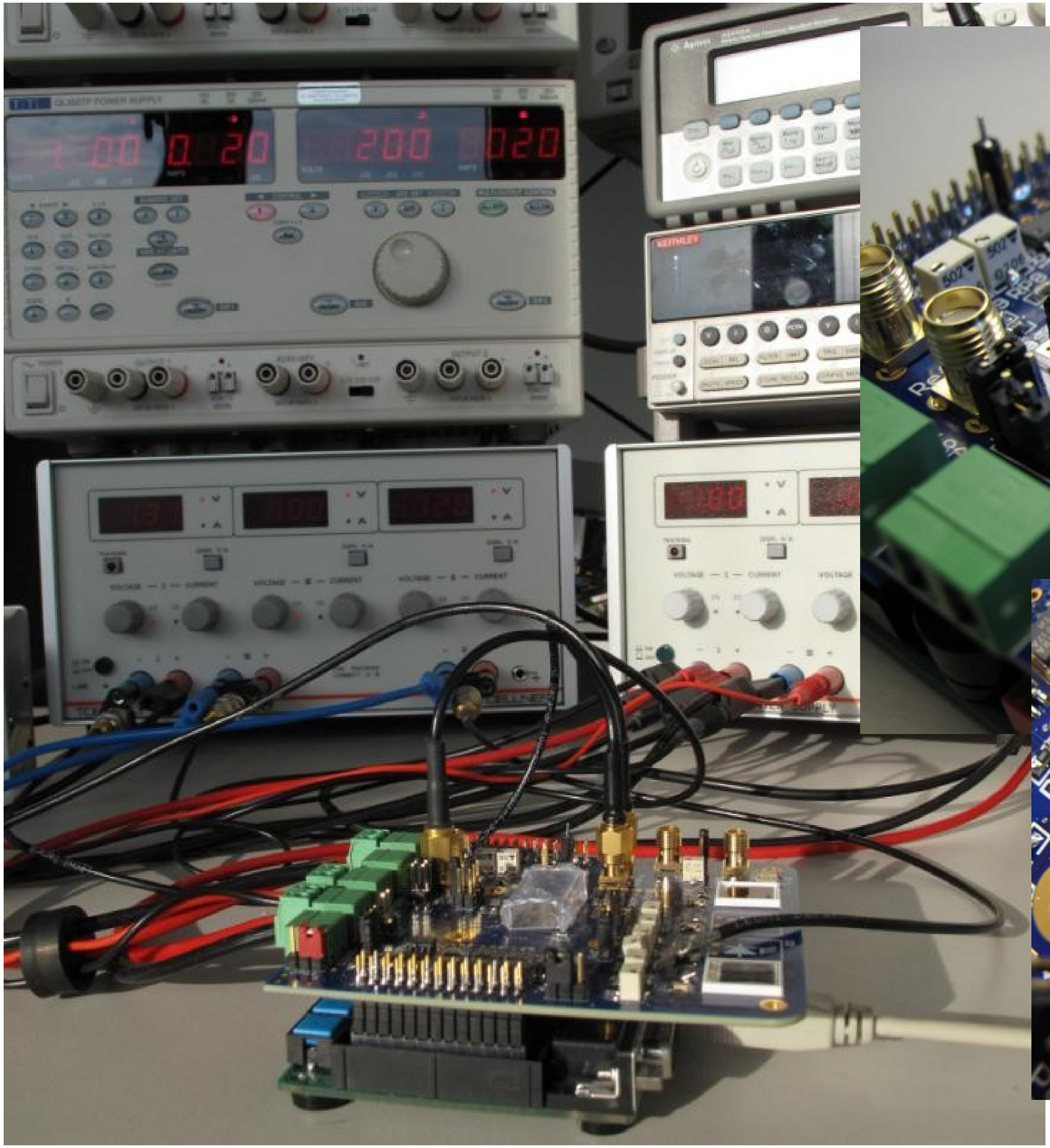
Layout

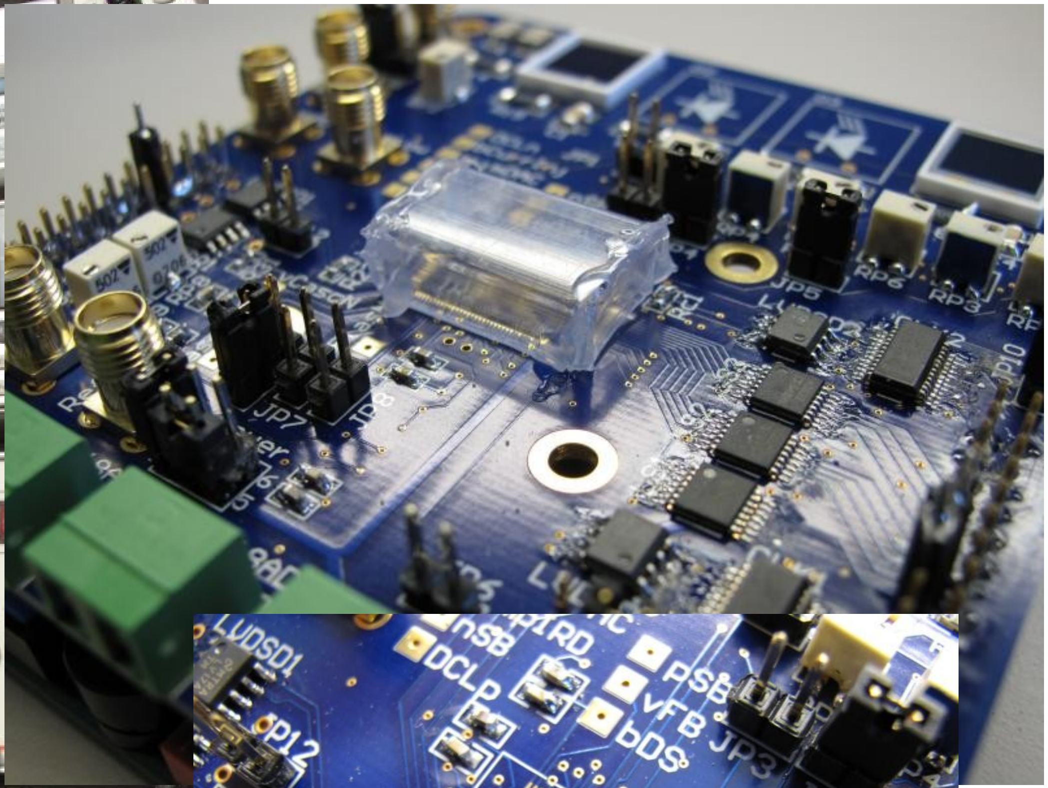


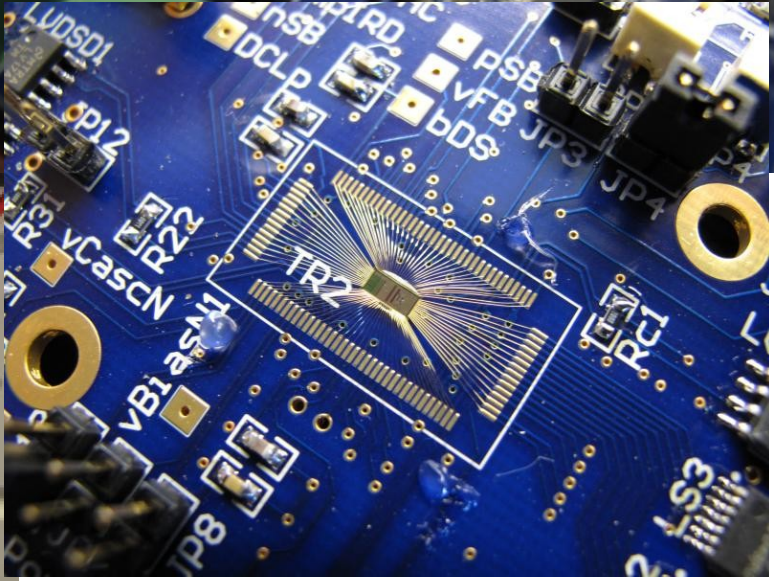
Bias circuitry (12 current DACs)
26 preamp/shaper channels
Detector capacitors (5pF per block)
8 pipelined ADCs

ADC control + bias
5.2 kBit shift register matrix
Control + readout/decoder logic blocks
Test circuits

Test Setup

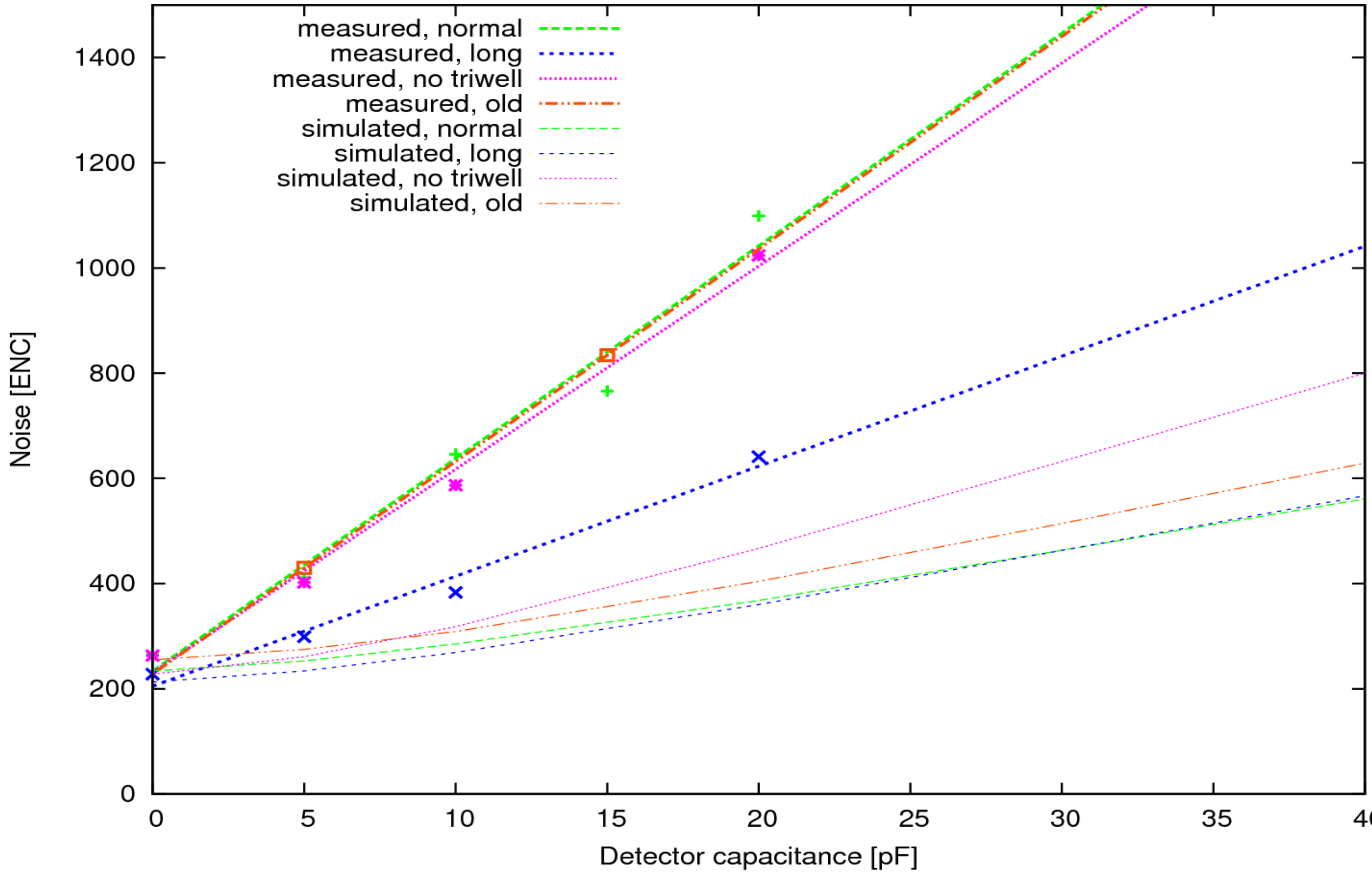





LVDSD1
nSB
DCLP
PSB
vFB
bDS
JP3
JP4
R31
vCascN
R22
TR2
Rc1
JP8
LS3

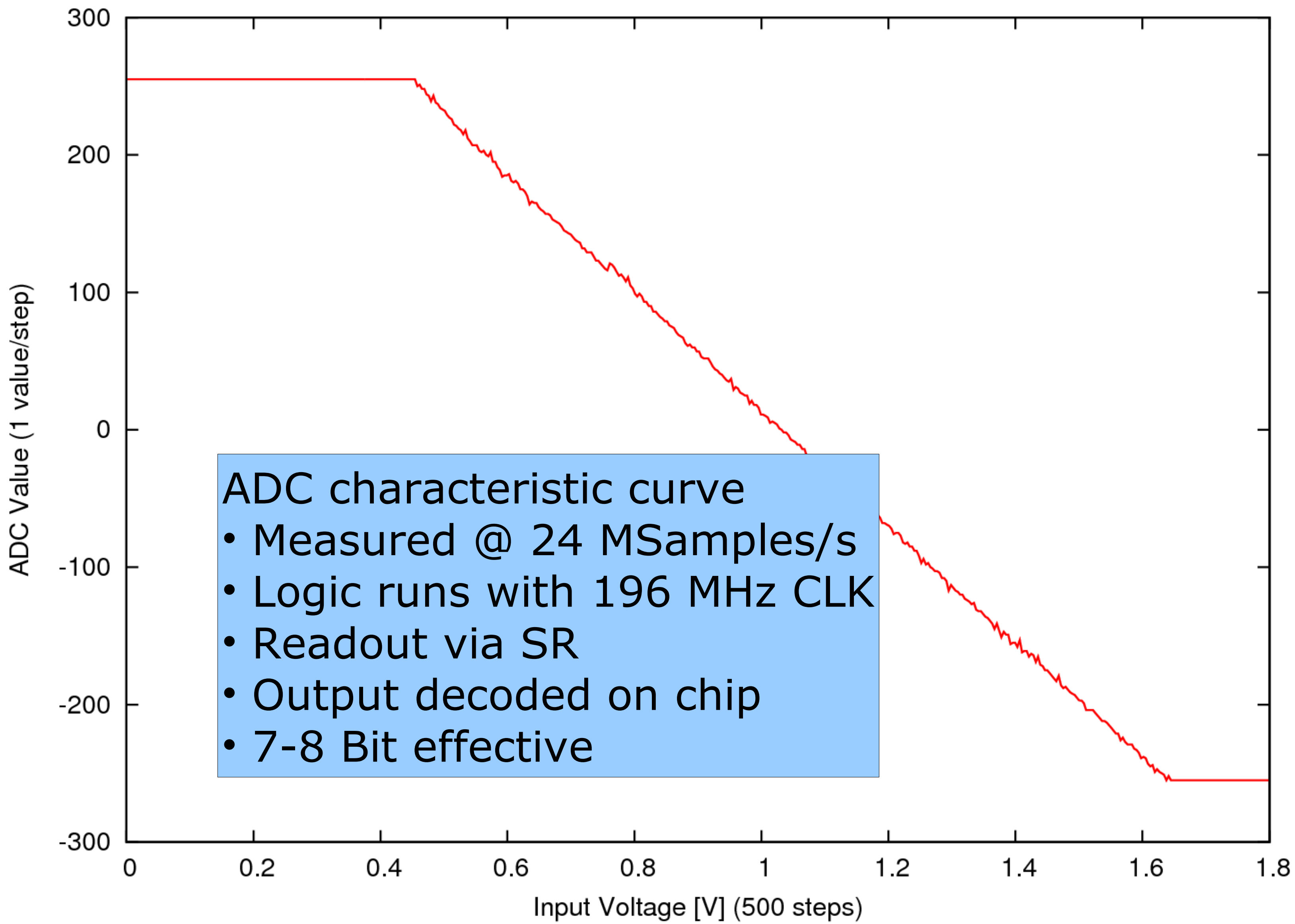
Preamp/Shaper Results

- Noise was measured with s-curve scans using the discriminator
- Injection capacitor calibrated via test circuit
- 4 different preamplifier types: old, normal, no triwell, long

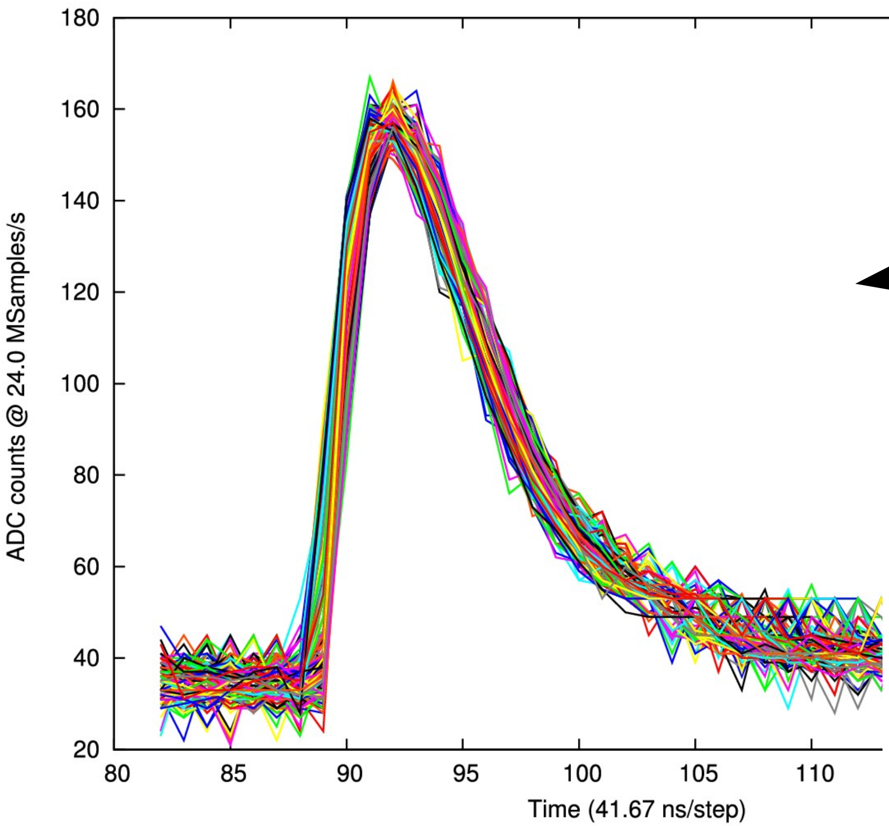


- Results:
  - Noise values of normal (triwell NMOS input, minimal length) and no triwell (NMOS without triwell, minimal length) channel show <u>no significant difference compared to the old channel</u> => values still much worse than simulated
  - Noise slope of long (triwell NMOS input, 320 nm length) channel about <u>two-times smaller</u> => about 800 e ENC @ 30 pF achievable, still worse than simulation

ADC Results


300
200
100
0
-100
-200
-300
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
ADC Value (1 value/step)
Input Voltage [V] (500 steps)
ADC characteristic curve
• Measured @ 24 MSamples/s
• Logic runs with 196 MHz CLK
• Readout via SR
• Output decoded on chip
• 7-8 Bit effective

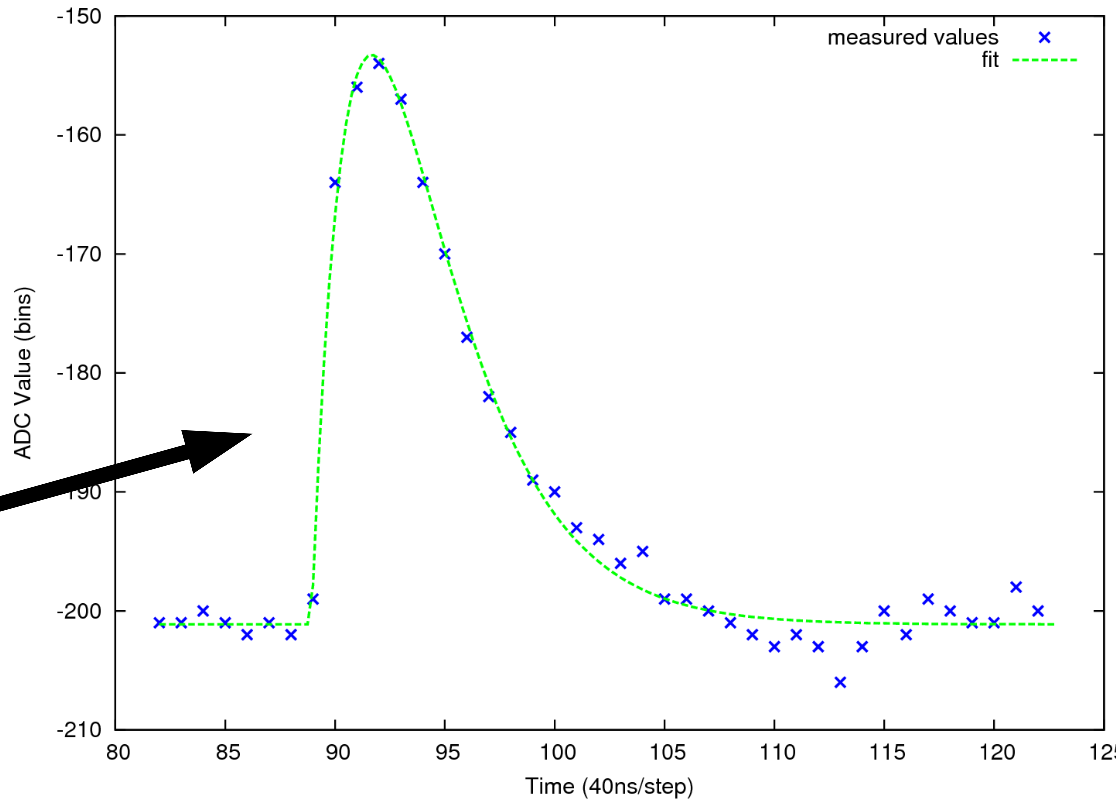
System: Shaper Output connected to ADC



Some ADCs can be connected to shaper outputs → digitization of shaper pulses possible (1000 hits shown here)

Theoretic and measured pulse shapes match well

(fitted with x * exp(-x))



Summary

1x2 Mini@sic 0.18 µm UMC 1P6M Test-Chip (1.5x3.2 mm²)

- 26 preamp/shaper channels
  - 40 µm channel pitch (540 µm length)
  - 3.8 mW per channel
  - Shaper output pulse peaking-time 95 ns
  - 800 e ENC @ 30 pF detector capacitance (long channel)
- 8 pipelined ADCs
  - 9 Bit design, 7-8 Bit effective
  - 4.5 mW per ADC
  - 130x120 µm²
  - 24 MSamples/s (has not been tested at faster speed yet)
- 5.3 kBit dynamic readout shift register matrix operates correctly
- 2 synthesized control and decoder blocks run with 196 MHz CLK
  - radiation-tolerant standard cells
  - “home-made” library

=> Whole chip works well!

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Outlook: CBM/TRD Readout Chip V1.0

Ideas for the first complete readout chip

Schaltungstechnik
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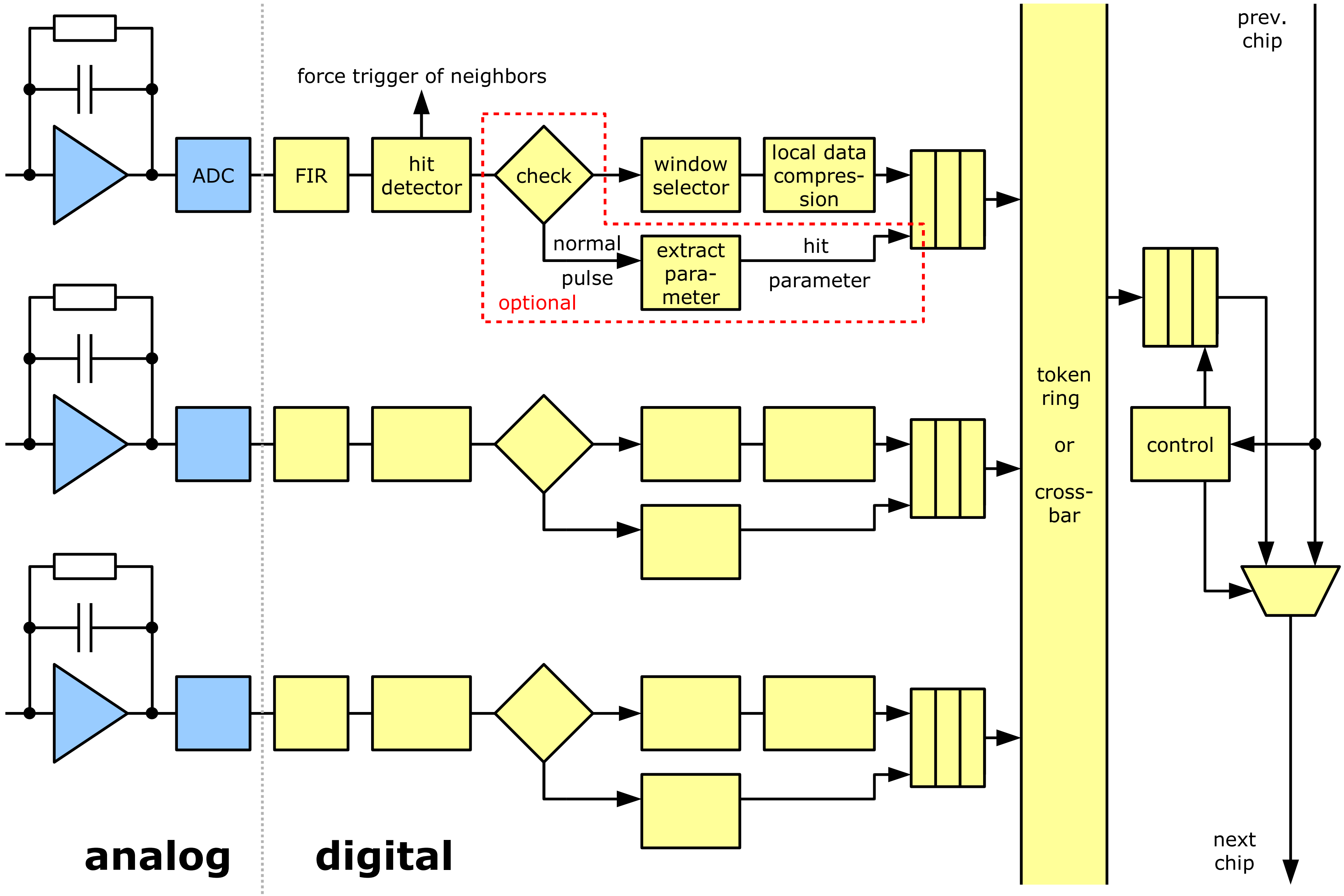
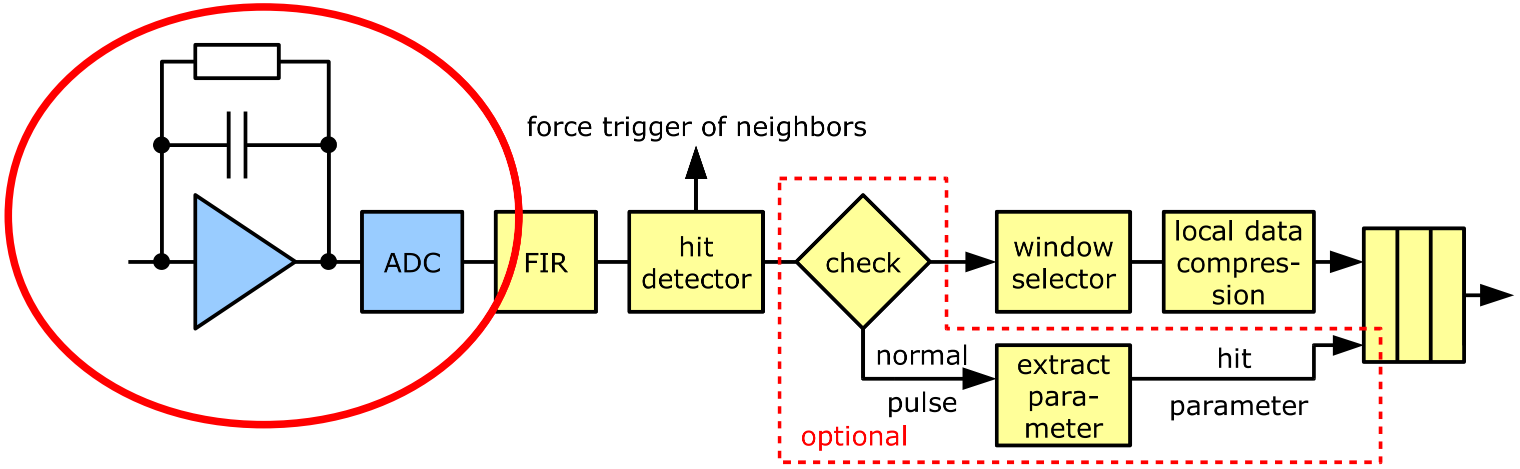
Preliminary Block Diagram



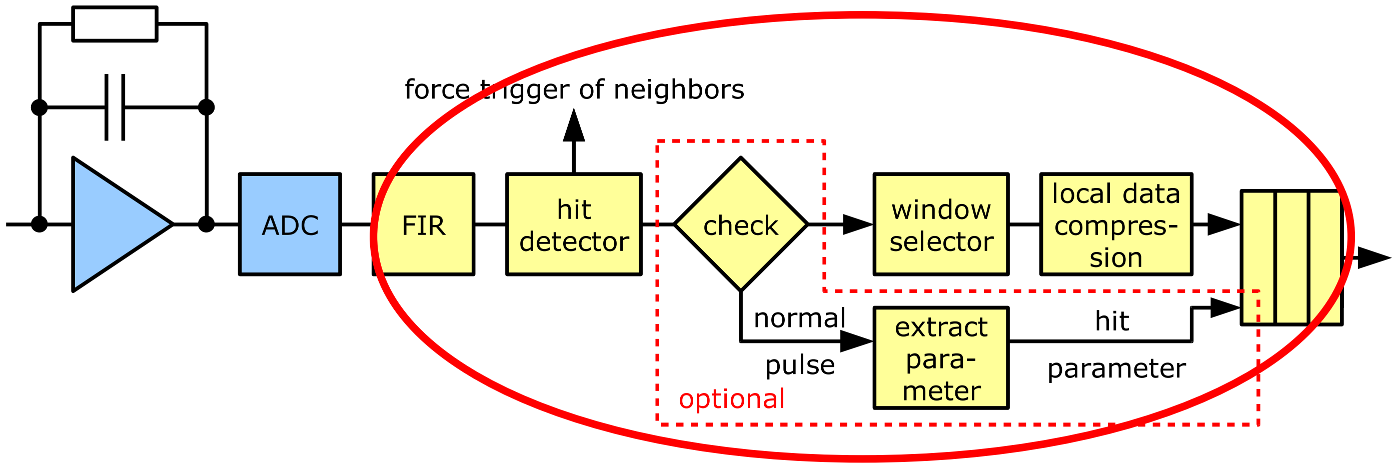
Analog Front-End

- Preamp/Shaper
  - Design as presented in previous talk(s), probably new layout needed to adjust pitch (benefit: more compact channels should be less sensitive to process variations)
  - Intended new feature: Switchable number of preamp-cells (adjustable tradeoff between amplifier noise and power consumption)
- ADC
  - Pipeline design mostly as presented in previous talk (8 Bit effective, 25 MSamples/s)
  - Control logic must be (re-)integrated into digital block

=> Detailed specification proposal will be finished soon



Digital Data Processing



- FIR filter stage, different tasks possible, for example:
  - 3rd/4th analog shaper
  - under/overshoot correction
- Hit detection unit ("digital discriminator")
  - detects valid hits, triggers packet generation
  - force trigger: force readout of neighbor channels
- Window selector
  - choose minimal but sufficient series of sample values
- Local data compression
  - due to high data rates data compression very reasonable (see next slides)
- Dynamic buffer / FIFO

Data-Rate Calculation (1/2)

Some estimated numbers:

- 32 channels / chip
- 250 kHz event rate / channel (one hit every 4 µs)
- 8 Bit ADC resolution
- 10 samples / event
- 12 Bit time-stamp / event (epoch length 164 µs @ 25MSamples/s ADC speed)
- 5 Bit channel ID

$$R_{chip} = \underbrace{\frac{250k\,events}{channel \cdot s} \cdot 32\,channels}_{hit\,rate\,chip} \cdot \left(\underbrace{\frac{8\,bit}{sample} \cdot \frac{10\,samples}{event}}_{hit\,data} + \underbrace{\frac{17\,bit}{event}}_{time-stamp+ID} \right) = \frac{776\,Mbit}{s}$$

=> Conservative estimation: <u>about 100 Bits/hit!</u>

=> One 2.5 Gbit/s LVDS link could only be shared between 3 chips

But: Corner chips may produce much less than 250k events/s

Simple data compression unit reasonable

=> Epoch counter + forward error correction overhead <u>not considered here!</u>

Data-Rate Calculation (2/2)

Possible strategies for data-rate reduction:

- Reduction of data
  - (Nearly) fixed: number of channels, event rate, ADC resolution (8-9 Bit), time-stamp resolution (10-12 Bit), channel ID
  - Potentially reducible: waveform data
    - 10 Samples/hit → 80 Bits/hit (8 Bit ADC) → main fraction of hit data
    - For curve fitting, less than 10 Samples/s may be sufficient. This depends strongly on curve shape and therefore on application/detector.
- Data compression
  - Further investigation on data compression strategies must be done
  - Compression potential due to data structure probably small

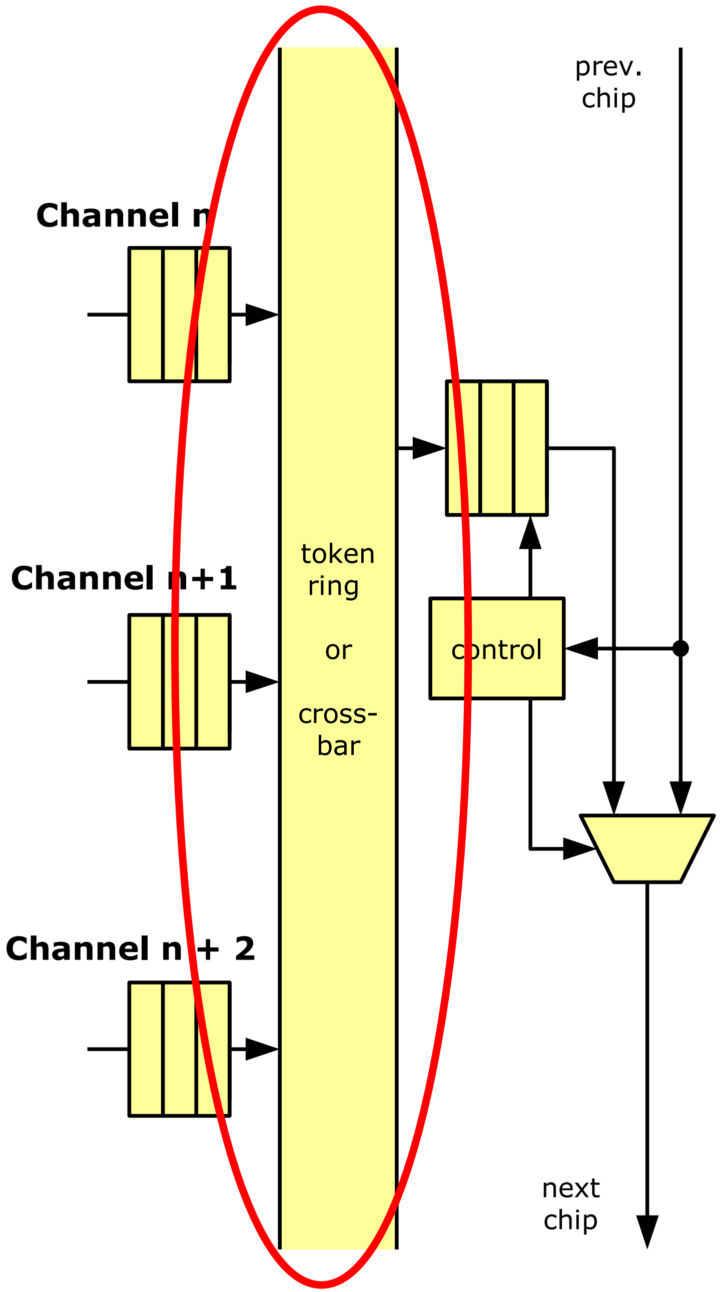
=> Very optimistic estimation (lower limit):

4 Samples/hit, data compression factor 80%

→ Still about 50 Bits/hit

→ 12.5MBit per second and channel

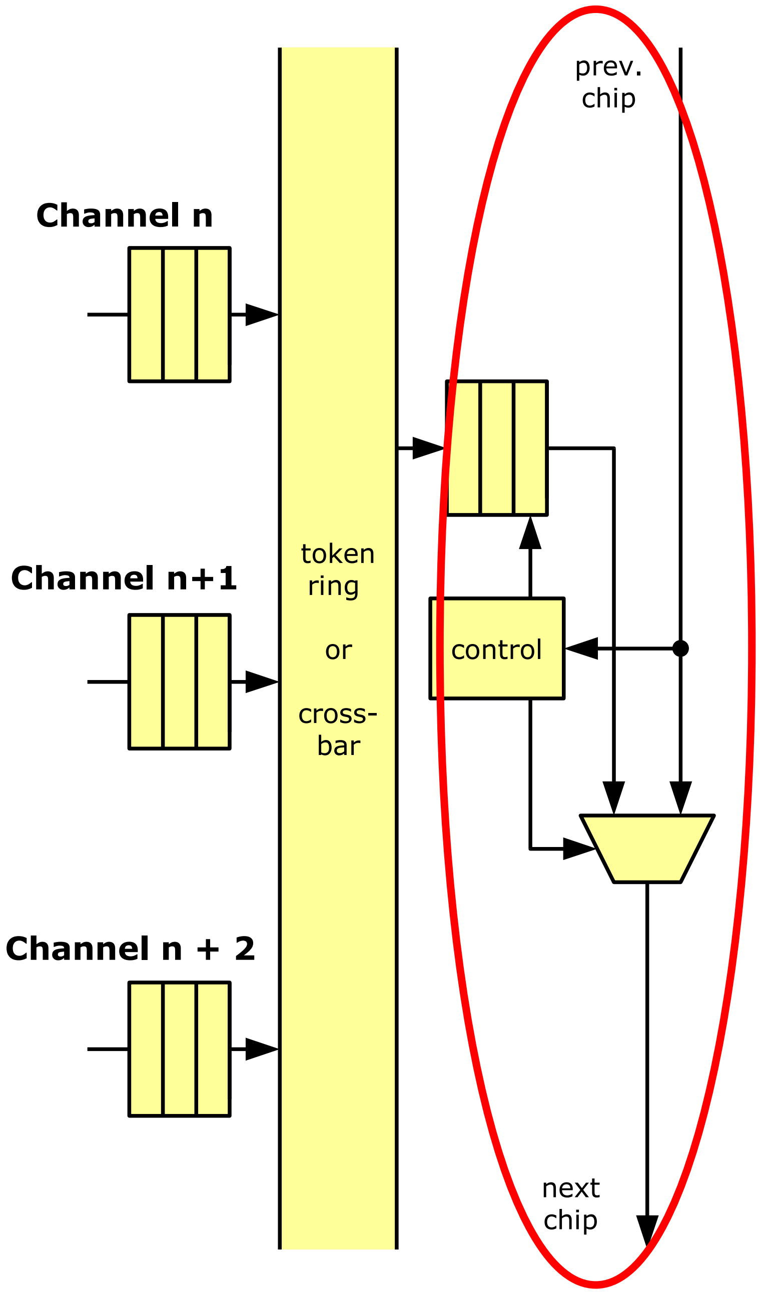
Inter-Channel Network



Data transfer <u>from channels to output logic</u>

- Token ring network seems to be "fairest" solution
- n-XYTER serves as good example
- Think about subdividing one large ring in several smaller rings (e.g. two rings, 16 channels each):
  - small maximal token delay
  - simple arbiter/multiplexer between the small token rings should be easy to design, could be used for some additional load balancing
  - short(er) data buses
  - parallel design: token would have more time to "choose" next channel, could think about some kind of simple priority mechanism

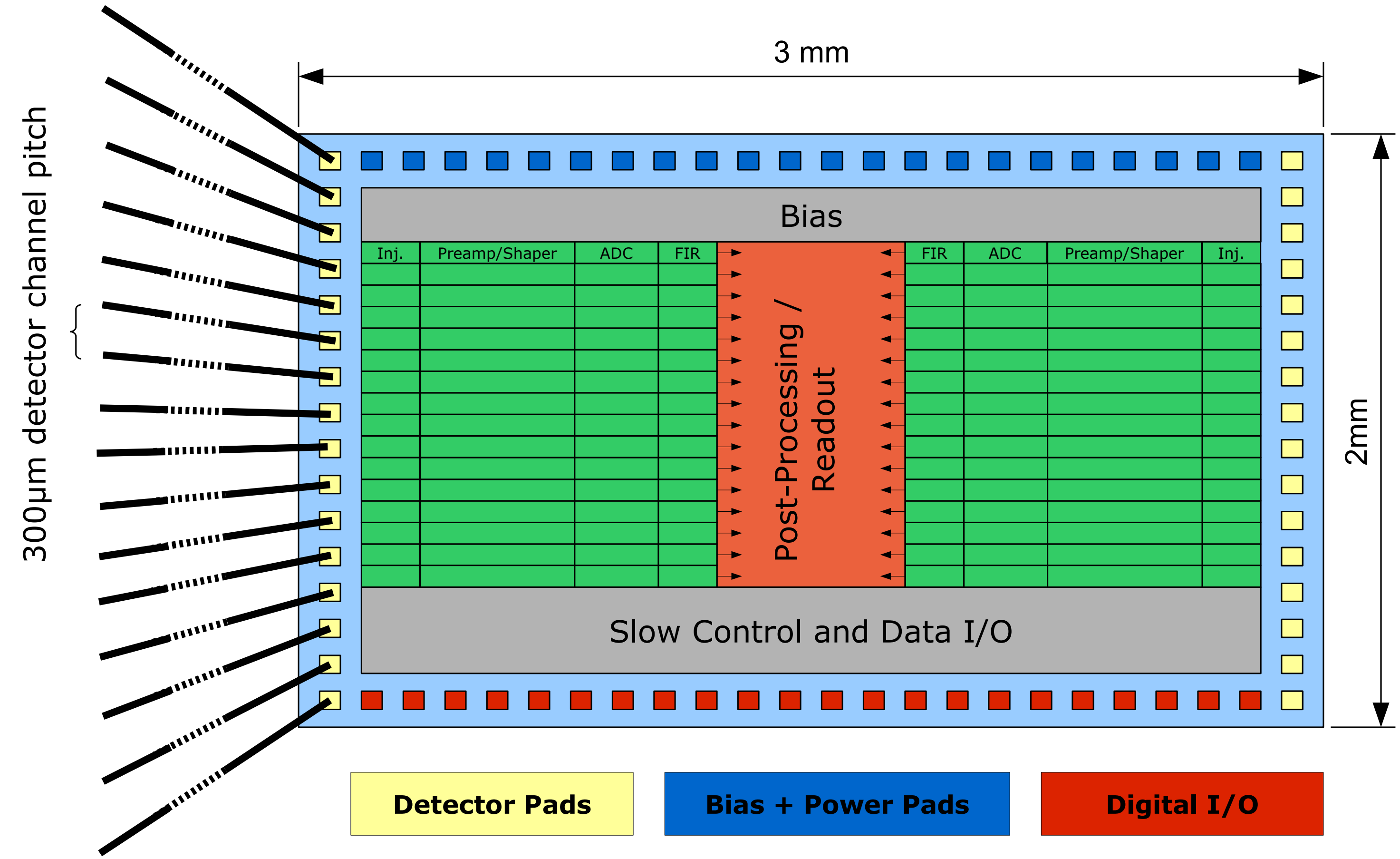
Inter-Chip Network



Data transfer in-between chips and from chip to the outer world

- Data rates of one chip smaller than typical data-rate of common LVDS link (e.g. 2.5 GBits/s) → share one LVDS driver cell between several chips
- Simple proposal:
  - Connect n chips in series
  - First chip (initial mode): Loop: Create and send n-1 empty packets, send 1 data package, ... (LVDS driver in low strength / low power mode)
  - Middle chip (pass mode): Loop: Pass n-1 packets, replace one empty packet with data, ... (LVDS driver in low strength mode)
  - Last chip (driver mode): Loop: Pass n-1 packets, replace last empty packet with own data, ... (LVDS driver in high strength mode) → last chip drives transmission line

Preliminary Floorplan



- 3 x 2 mm² estimated die size
- 32 channels, 40-80µm pitch, (mostly) symmetric layout, low(er) IR-drops
- Detector connection-pads on two sides (chips will probably be attached to back of detector-module, this relaxes routing/spacing)
- Next/first (very important) step: Find good pin and power routing strategy

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Simple electric data transmission

Or: How far can we go with copper?

Schaltungstechnik
und Simulation

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Motivation

The question arose some time ago: Why not using copper cables for data transmission from front-end chips to DAQ?

=> Big advantages:

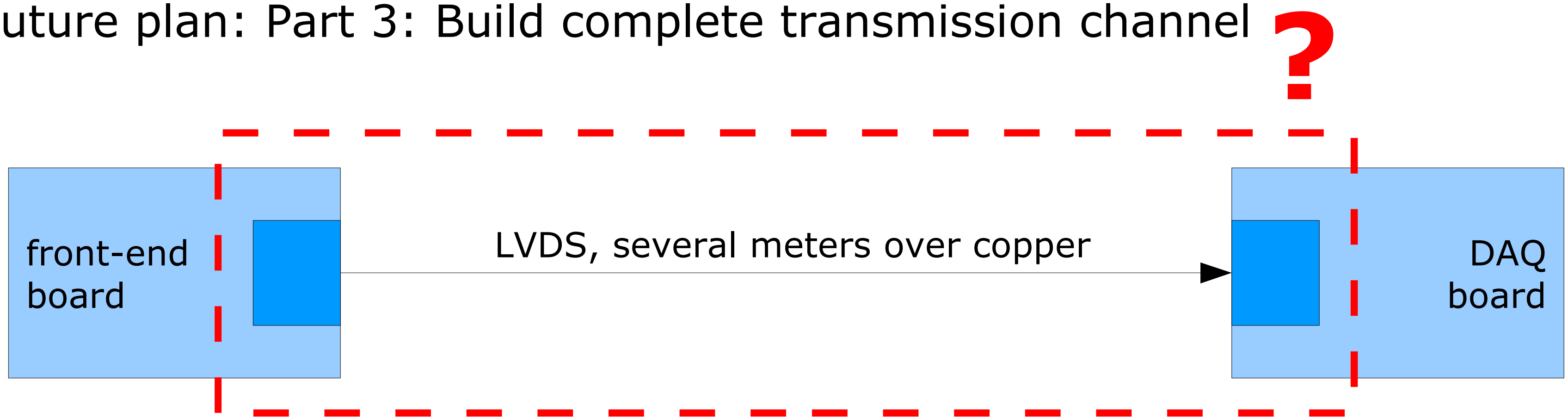
- No need of large and non-radhard optical transceiver modules
- Much simpler to connect and handle front-end devices
- ...

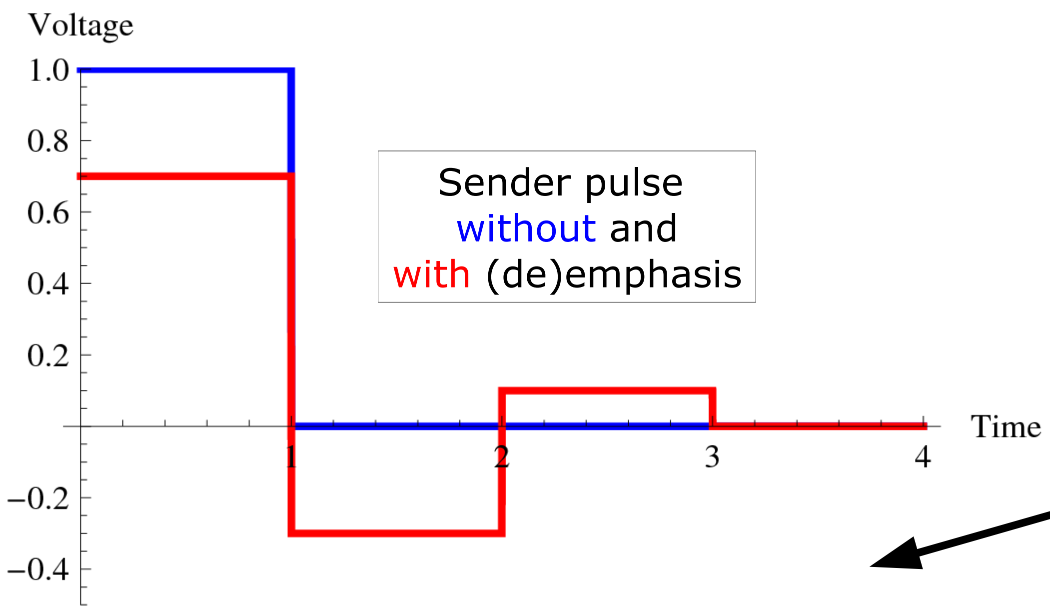
Therefore we've started a study to figure out how far we can go with moderate effort.

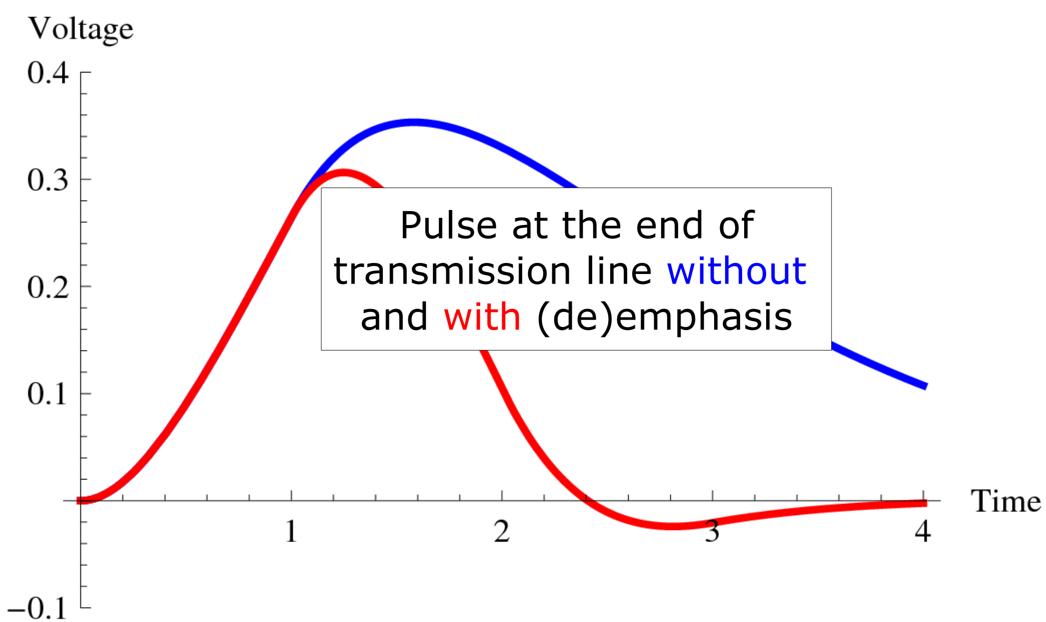
Project goal: Build a simple UMC018 transmitter cell which encodes to a minimal Xilinx Aurora protocol and which is able to drive over some meters of copper (into a Xilinx multi gigabit transceiver (MGT)).

Stoyan Todorov's and Marco Oster's Diploma Thesis

- Part 1 (Stoyan Todorov): Design of a minimal Aurora protocol cell
  - Verilog modules have been finished and tested successfully via FPGA
  - Aurora module has been synthesized and submitted (not tested yet)
- New: Part 2 (Marco Oster): Physical design space exploration
  - Gain experience in modeling and simulating simple transmission lines
  - Gather information about available cable types and their behavior
  - Study different emphasis/equalization techniques
  - Build and submit a simple LVDS transmission circuit
  - Evaluate chip results (still in progress)
- Future plan: Part 3: Build complete transmission channel

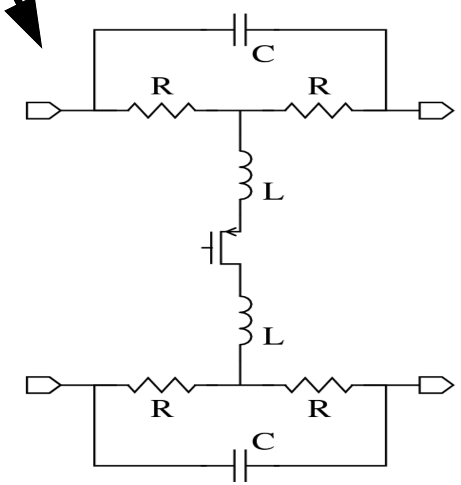






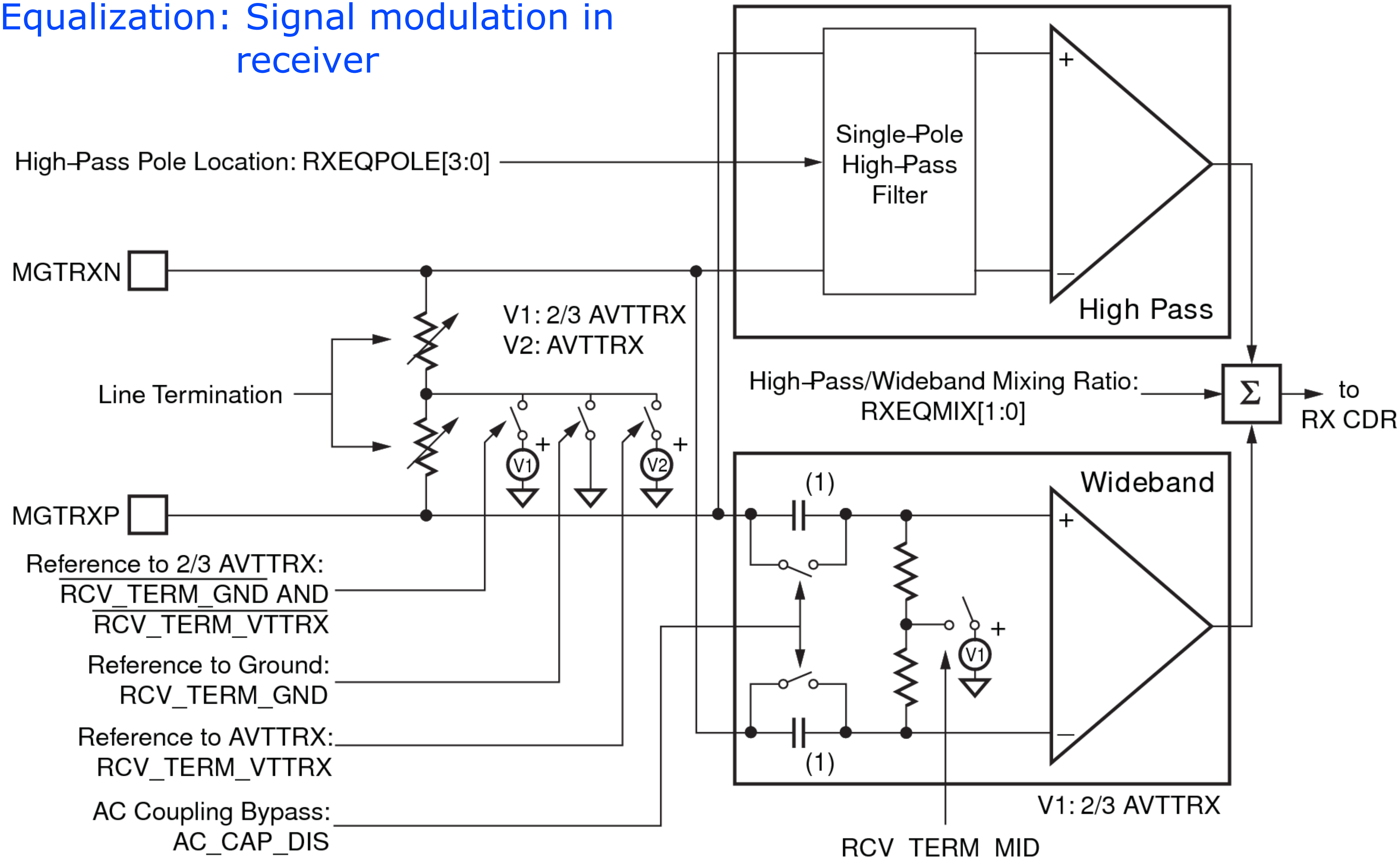
Emphasis: Signal modulation in sender

- With little effort, pulse length can be significantly reduced → higher data rates
- Two basic methods:
  - Logical, e.g. via FIR filter
  - Analog, e.g. high frequency boosting by using a passive “RCL” network:

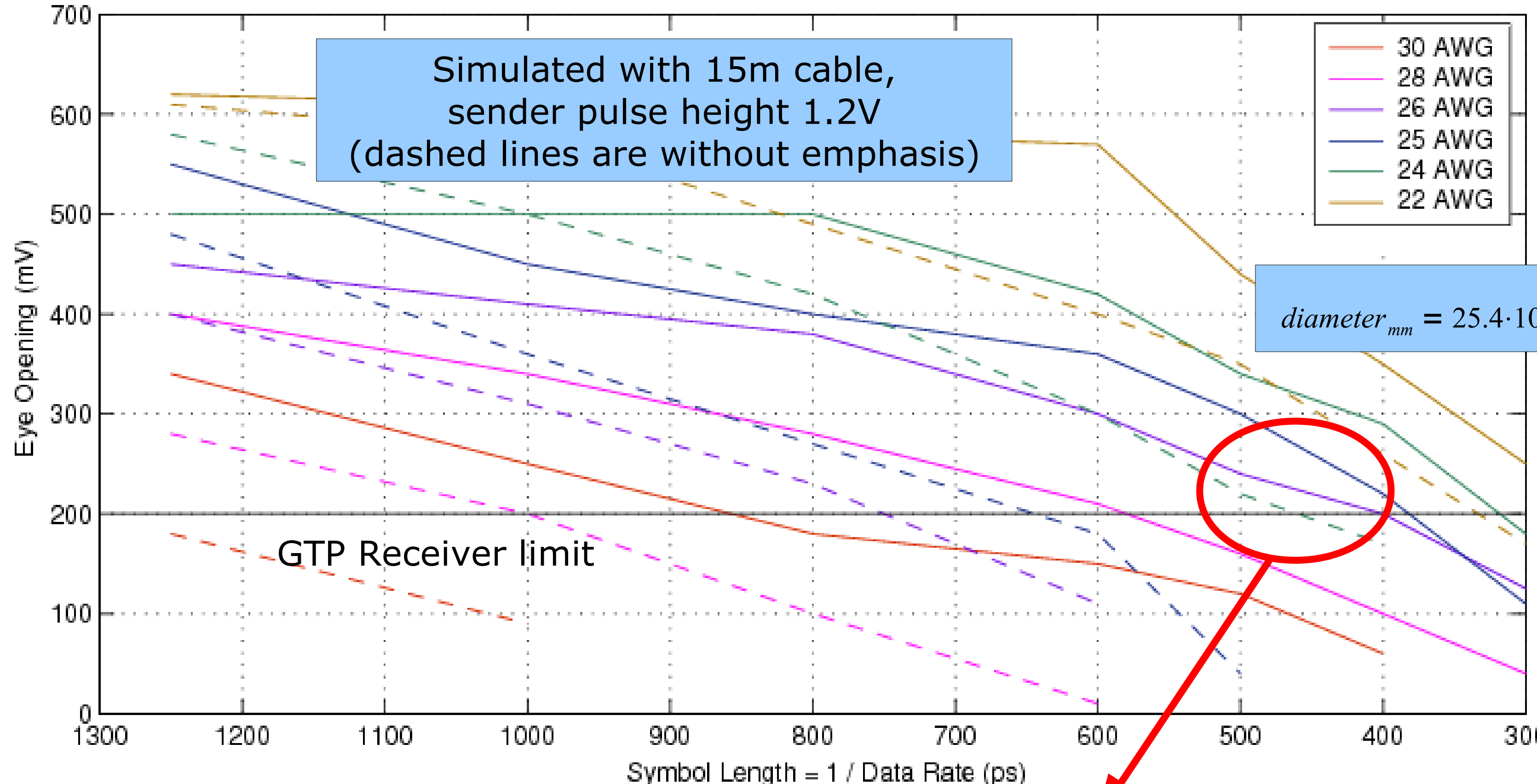


Equalization-Example: GTP/GTX Receiver of Virtex5

Equalization: Signal modulation in receiver



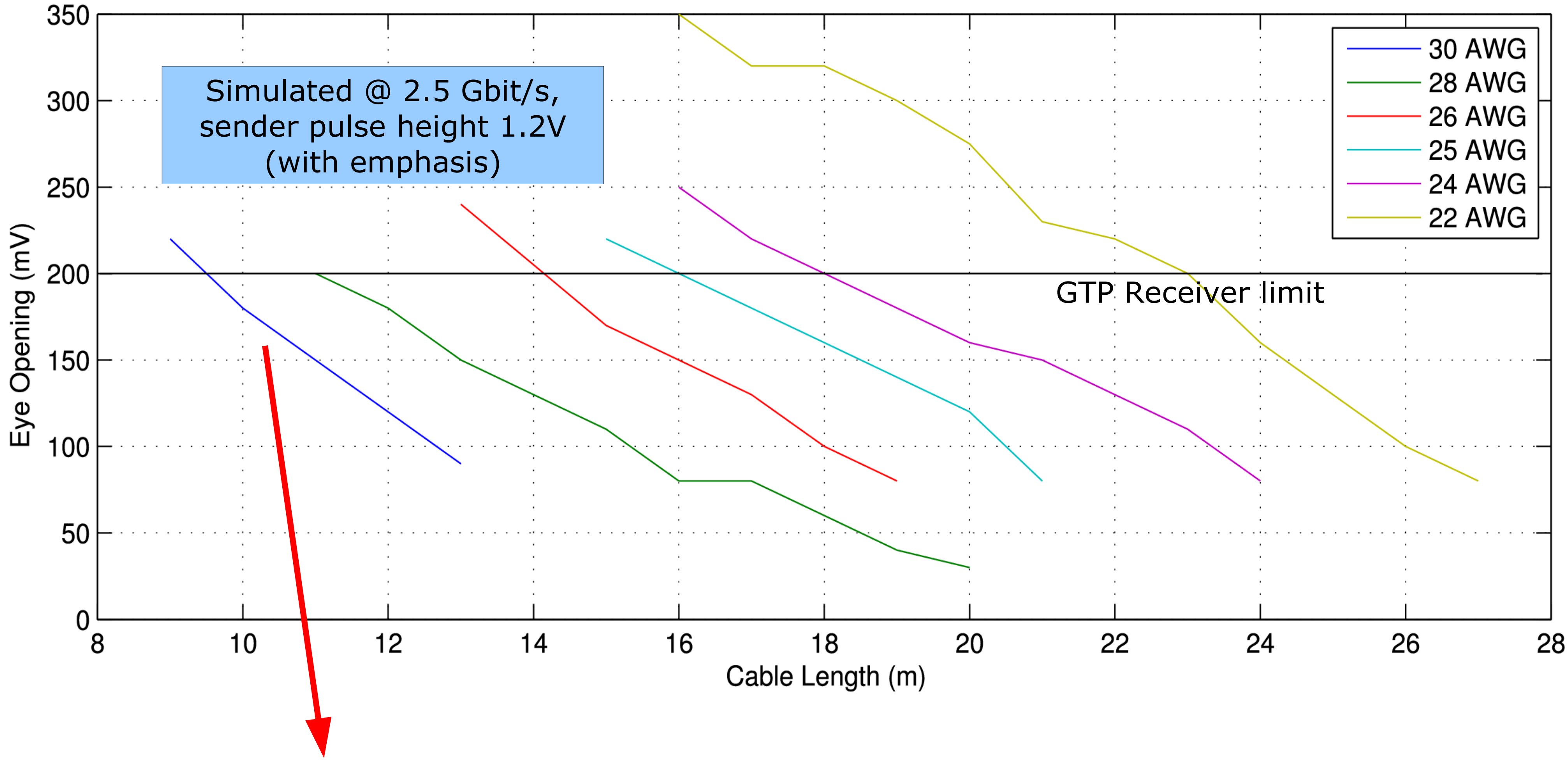
Cable Simulations (1/2)



$$diameter_{mm} = 25.4 \cdot 10^{-\frac{AWG+9,6954}{19,8578}}$$

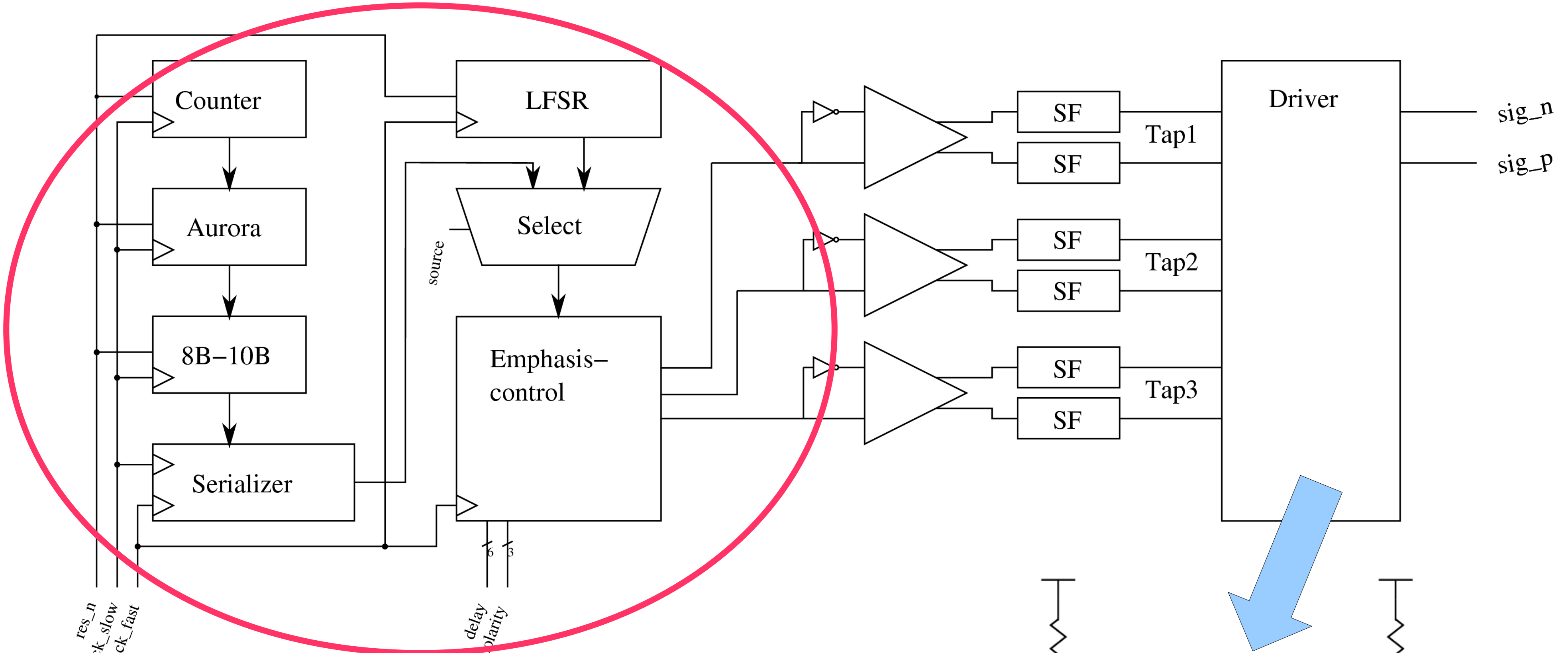
For example: 2GBit/s over 15m with AWG 26 (0.4mm diameter) should be receivable by Xilinx GTP (order of magnitude)

Note: Cable models were fitted using the data sheet parameters



For example: 2.5GBit/s over 10m should already be receivable when using a AWG 28 cable (0.32mm diameter)

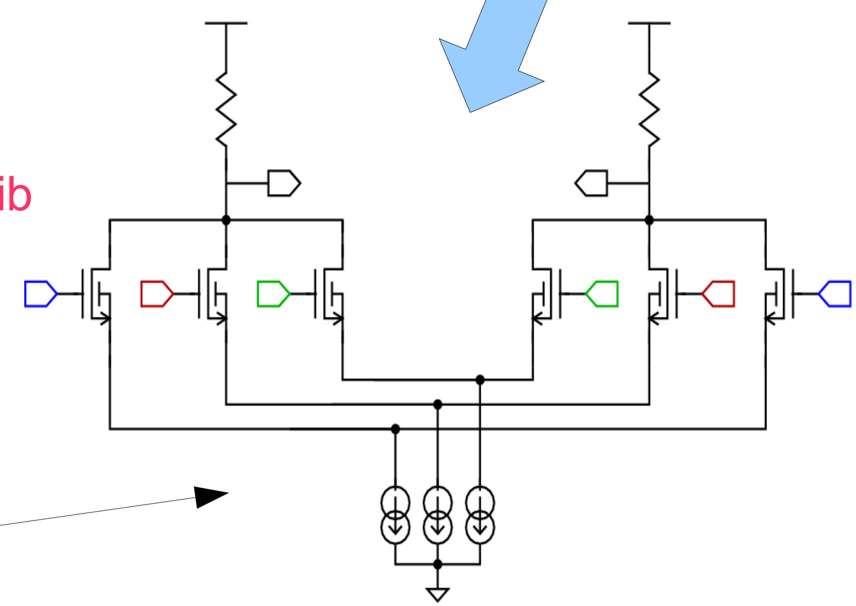
Test Circuit Design Overview (UMC018)



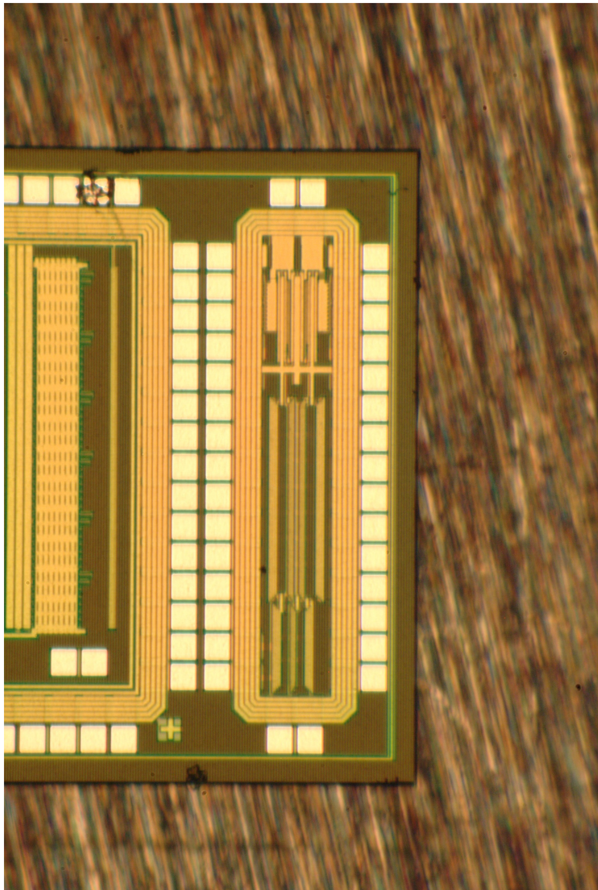
Synthesized using our
rad-hard standard-cell lib

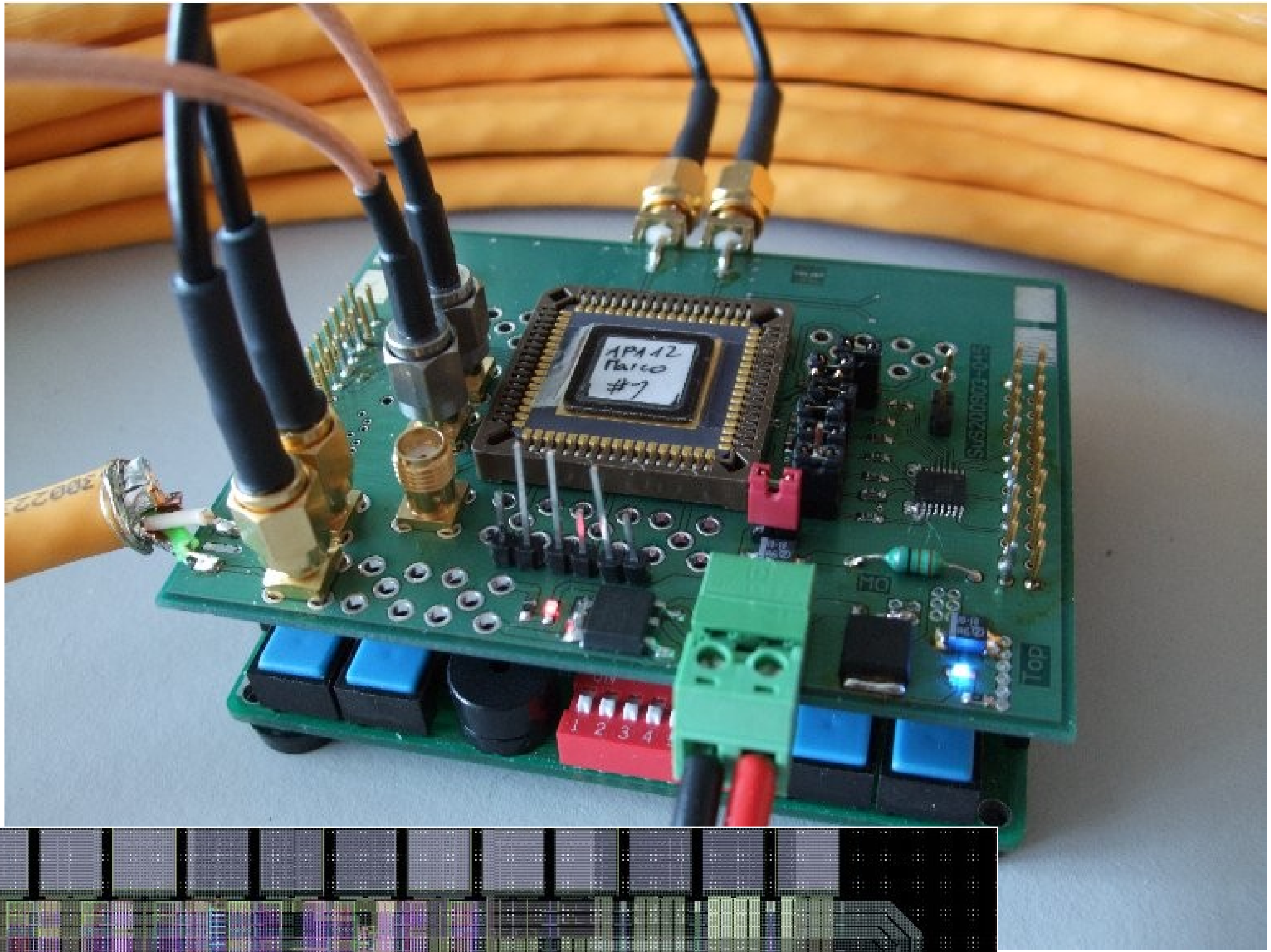
Two test cases:

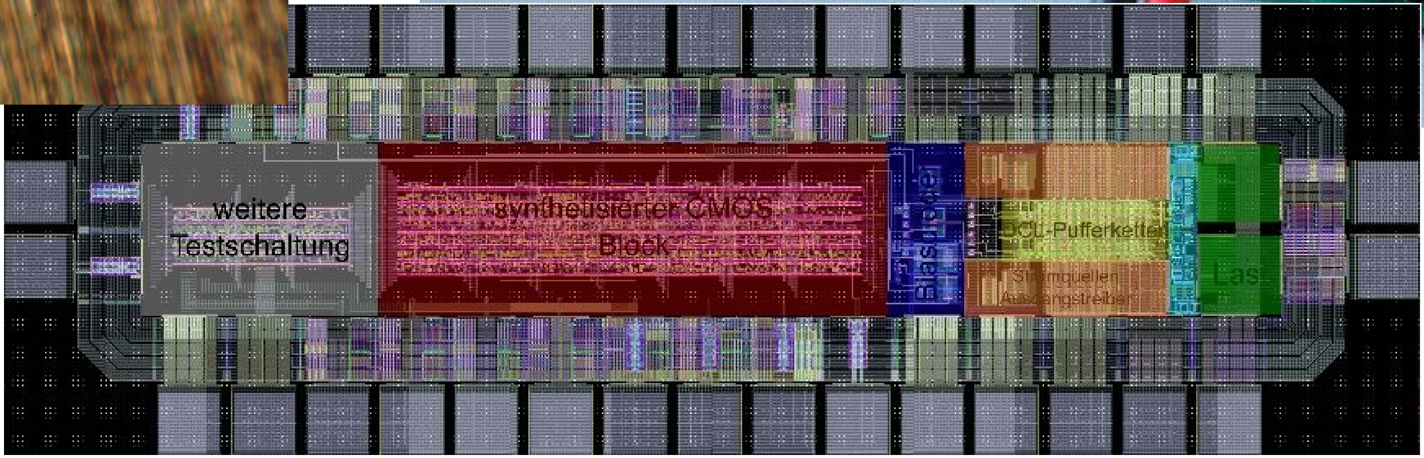
- Simple LFSR
- Counter encoded to Aurora protocol



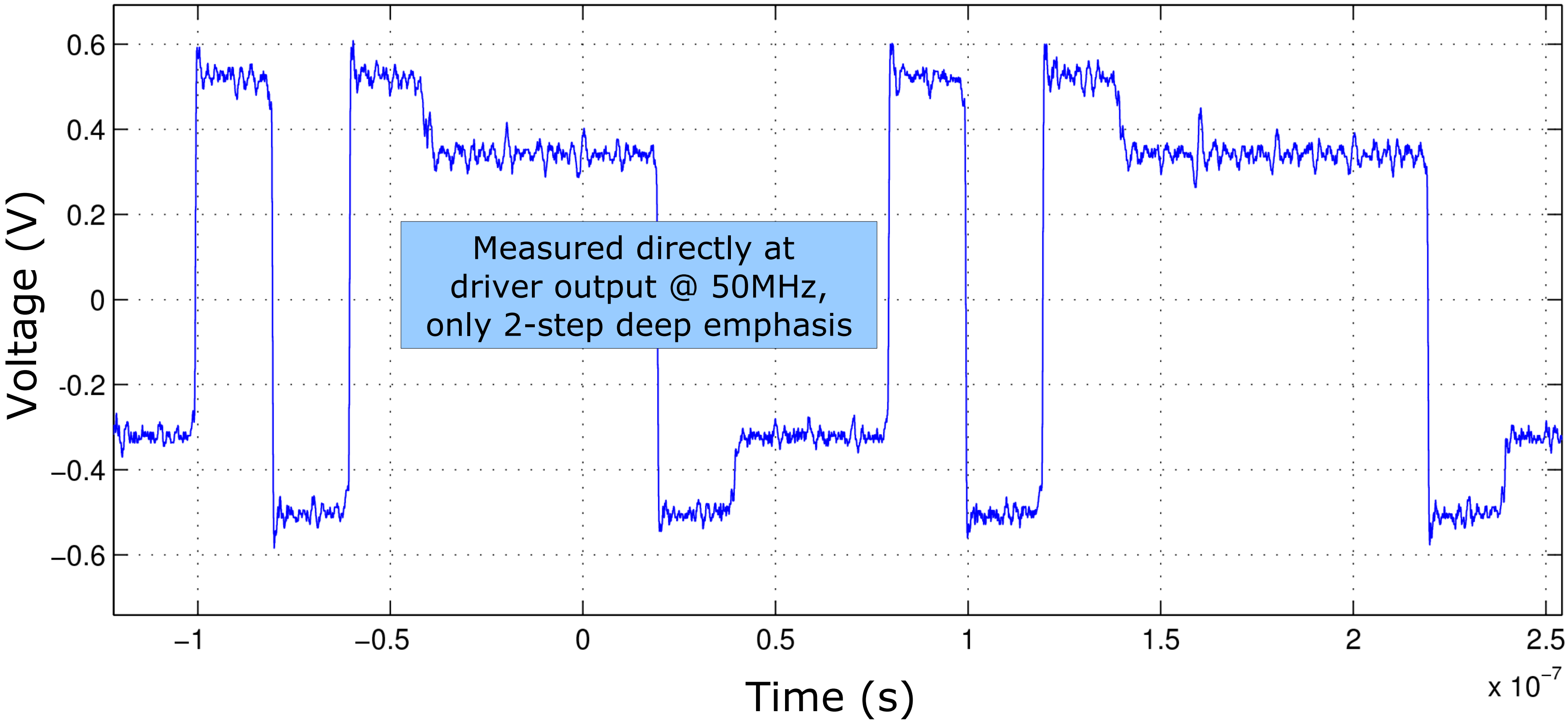
Emphasis realized with three weight
stages (FIR filter implementation)





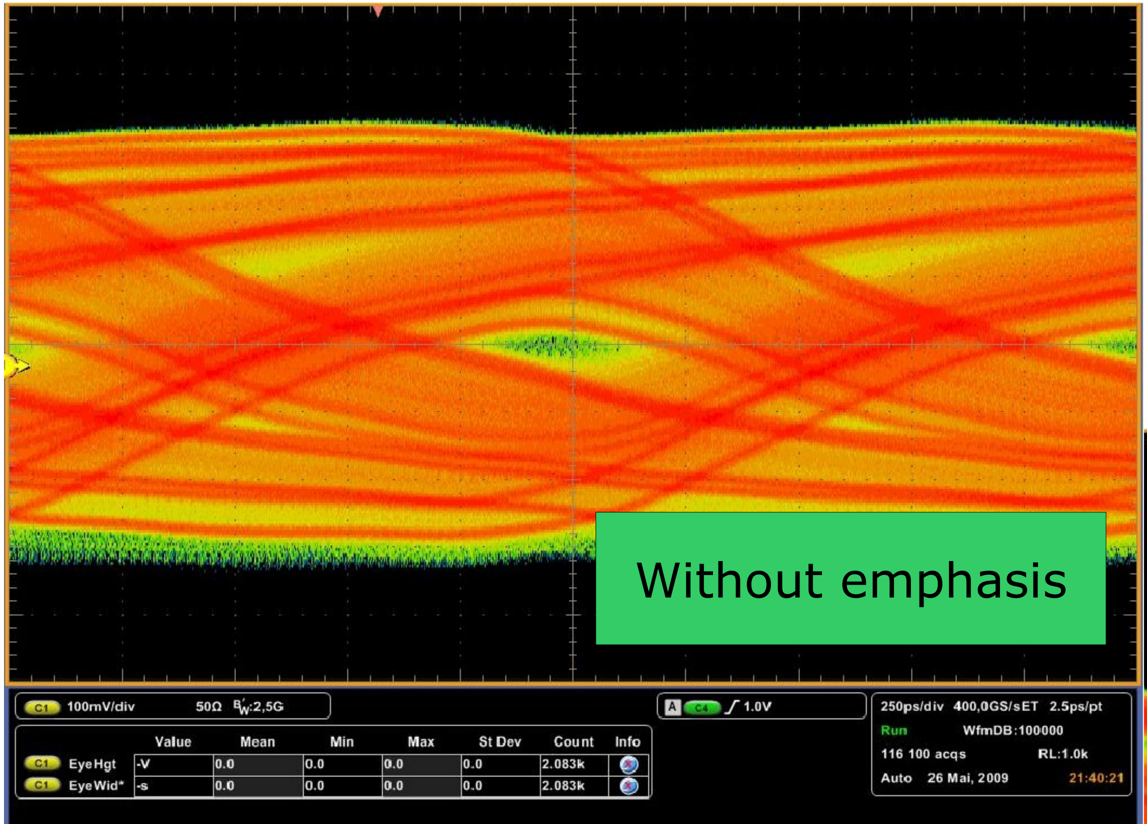

weitere
Testschaltung
synthetisierter CMOS
Block
DCU-Pufferketten

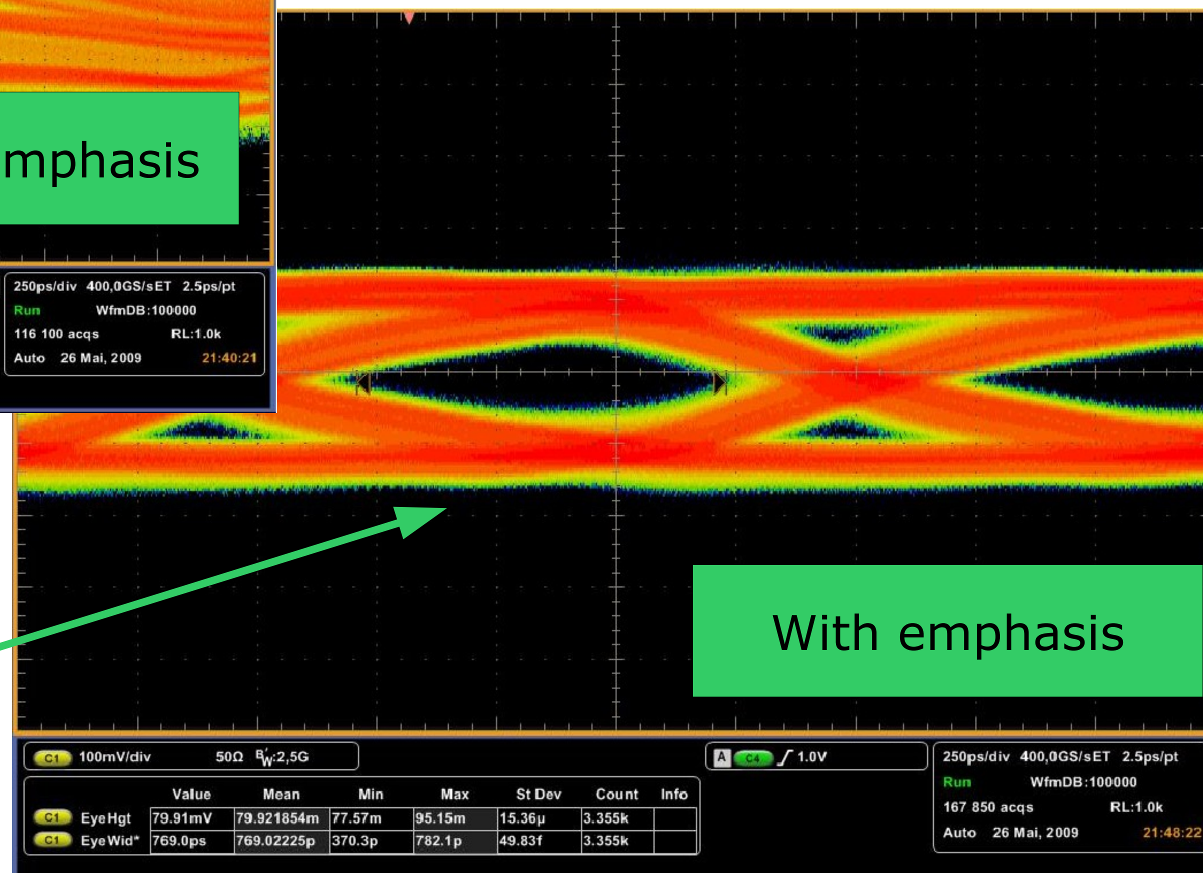
Measured Buffer Output with Deemphasis



First Result: Eye Diagram after 42m

measured with 42m cable @ 750MBit/s





eye opening about 80mV

Summary and Outlook

Aurora protocol

- Minimal encoding block has been designed and simulated successfully
- Synthesized and submitted cell available but not tested yet

Physical transmission

- Gained basic knowledge of transmission techniques
- Several cable models and simulation setups available
- Test-chip/test-driver works but is not fully tested yet
- 2.5GBit/s over 10m should be achievable with moderate effort

=> Copper cable seems to be a reasonable alternative to optical data transmission, further analysis is being performed.

Thank you!