UNIVERSITÄT HEIDELBERG

Status of GAS-XYTER

Latest Results of the Self-Triggered Digitizer Chip

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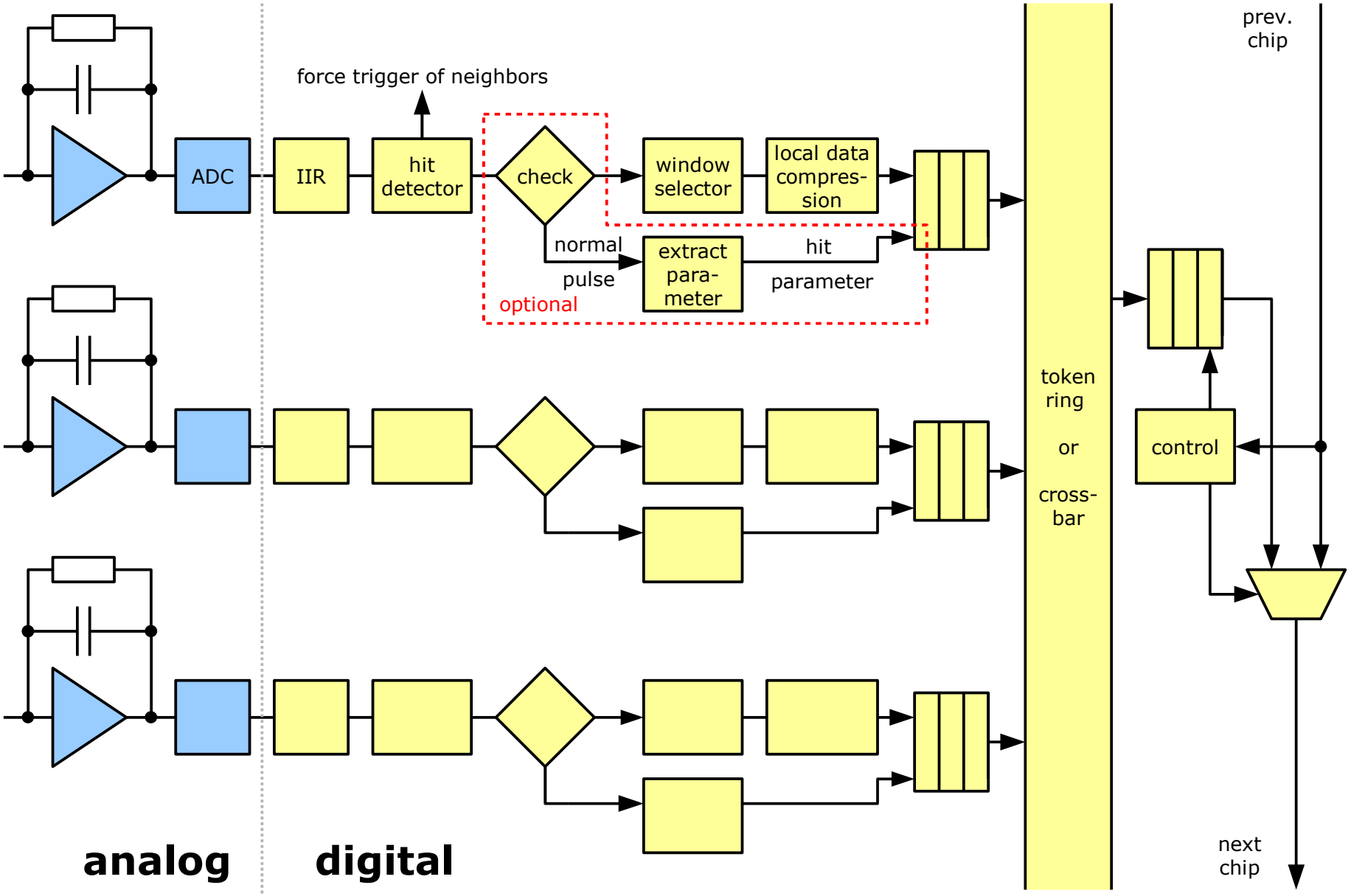
1. Chip Concept

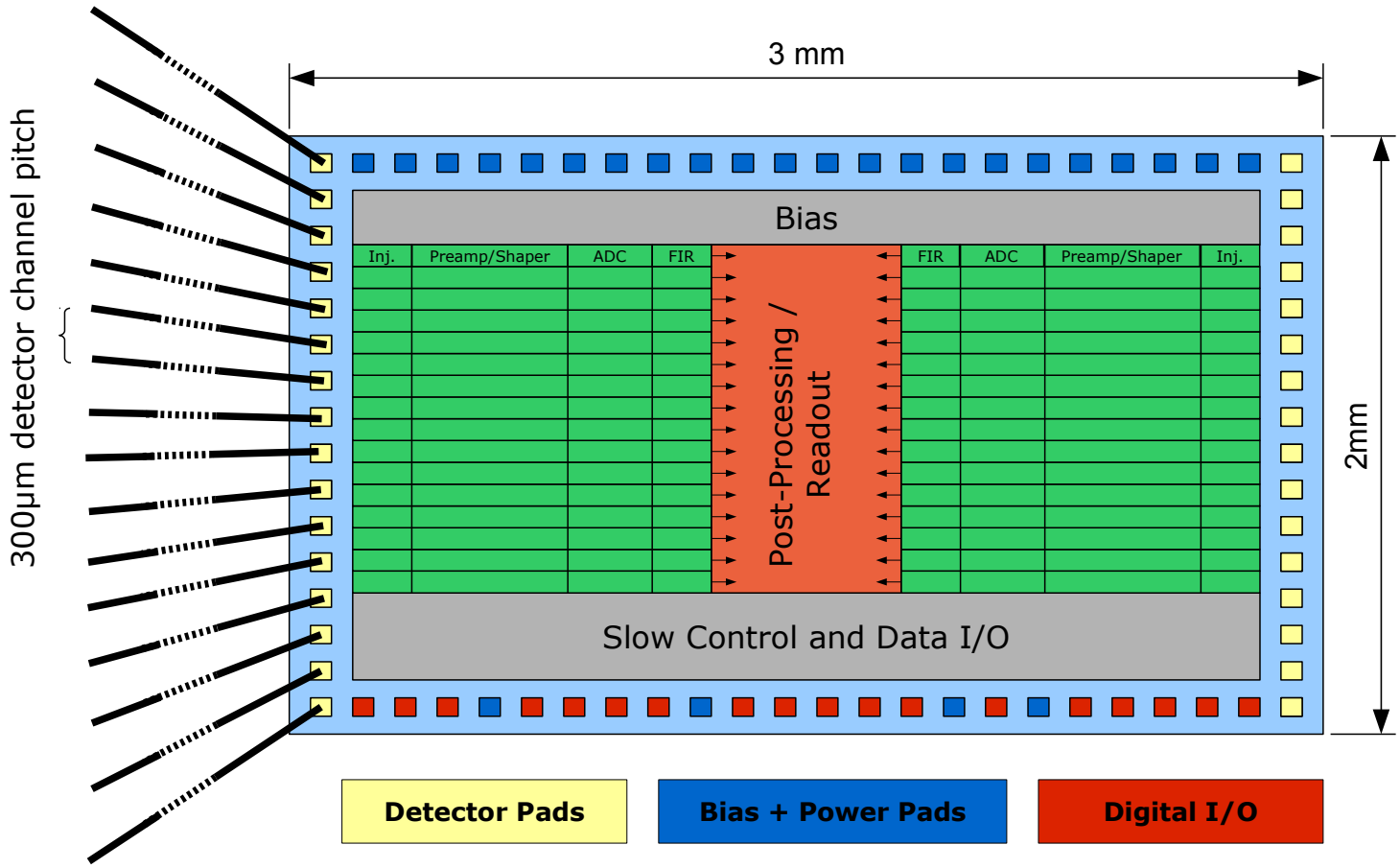
Requirements

- Application:
  - Main task: gas chamber readout for CBM TRD
  - Application in other FAIR detectors also conceivable
- We need a self-triggered readout chip that has:
  - 32-64 mixed-signal channels
  - Low noise & power charge amplification (order of 1000e ENC @ 30pF det.)
  - Bandwidth limitation (2^{nd} order shaper or higher, about 90ns shaping time)
  - Digitization (8-10 bit @ 5-30 MHz)
  - Time stamping (necessary time resolution depends on ADC sample speed)
  - In-channel data processing (ion tail cancellation, baseline correction, ...)
  - Inter-channel network (e.g. token ring network)
  - High-speed data transmitter (up to 1 Gbps LVDS)
  - Inter-chip bandwidth sharing protocol (e.g. daisy chain topology)

Preliminary Block Diagram

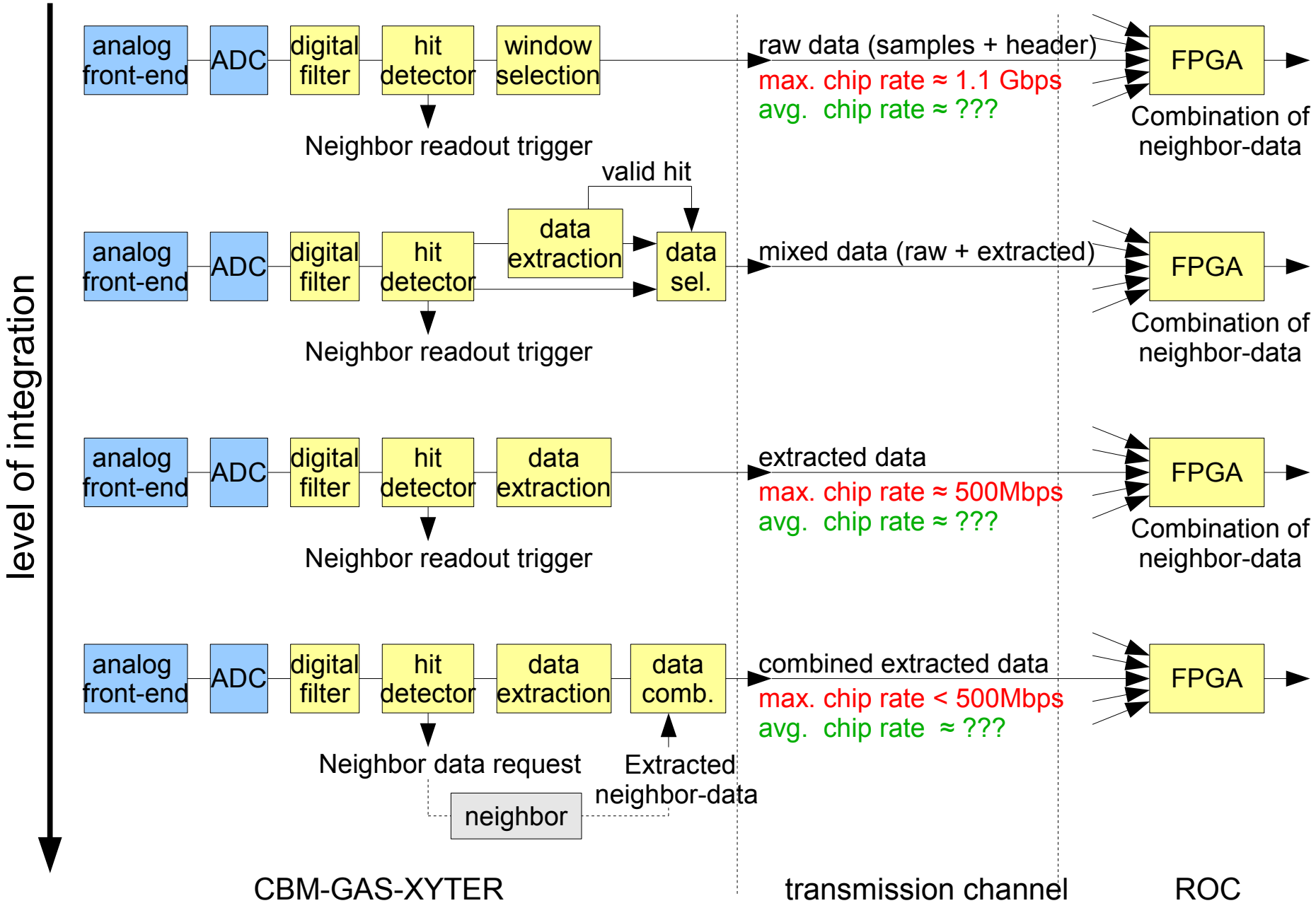


Floorplan Proposal



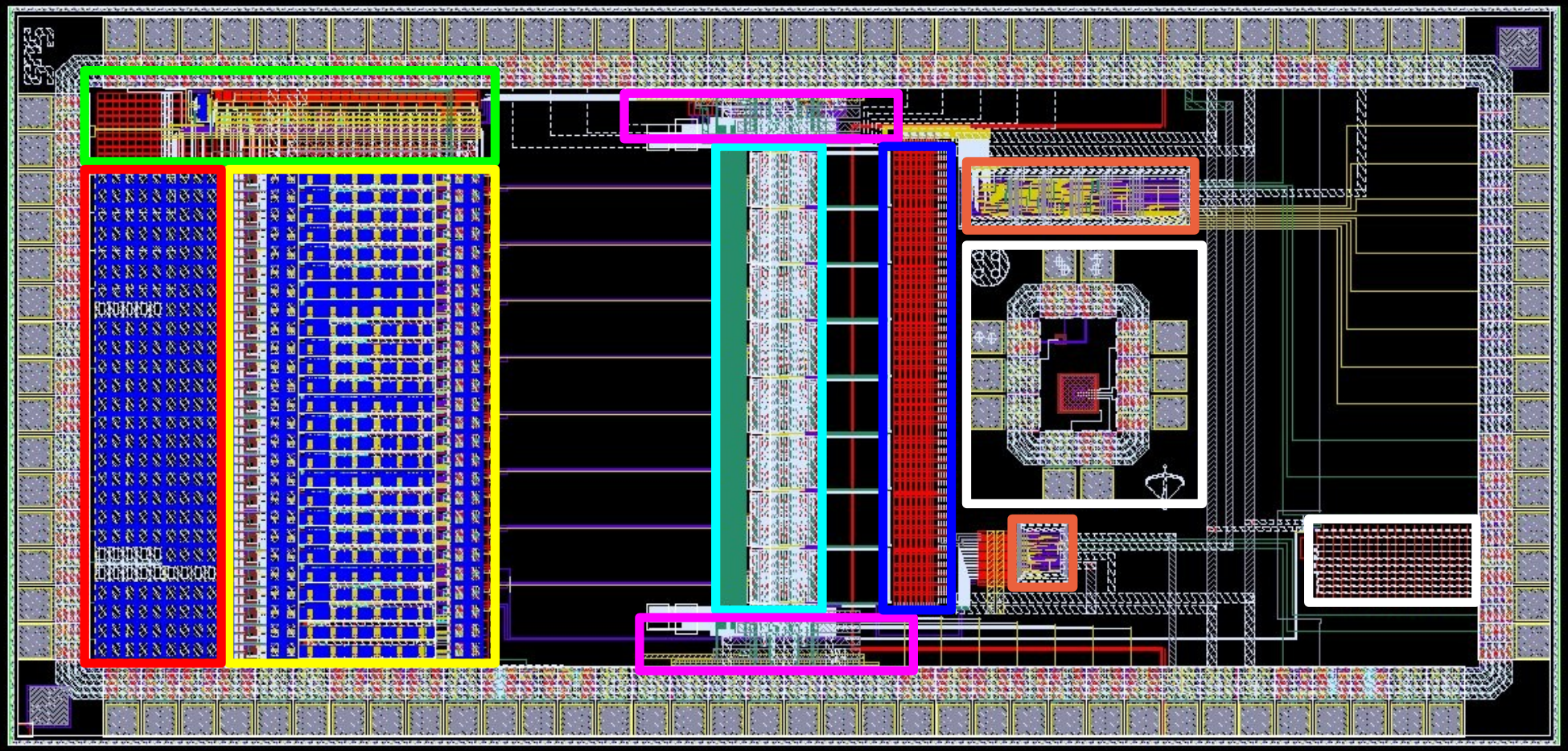
- 3 x 2 mm² estimated die size
- 32 channels, 40-80µm pitch, (mostly) symmetric layout, low(er) IR-drops
- Detector connection-pads on two sides (chips will probably be attached to back of detector-module, this relaxes routing/spacing)

Raw Data vs. Extracted Data: System Options



2. Status of Development

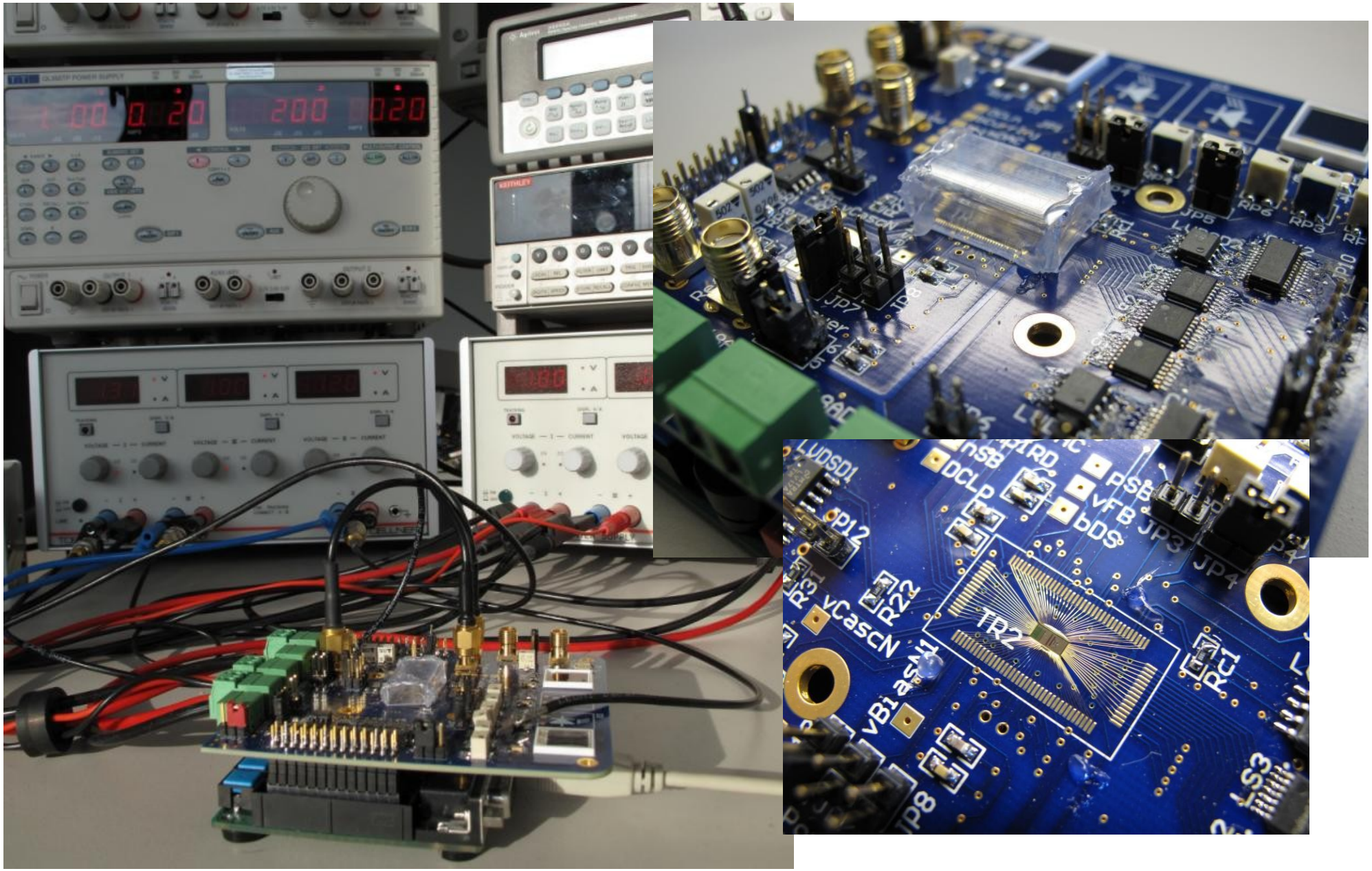
Next to last Test-Chip: Layout



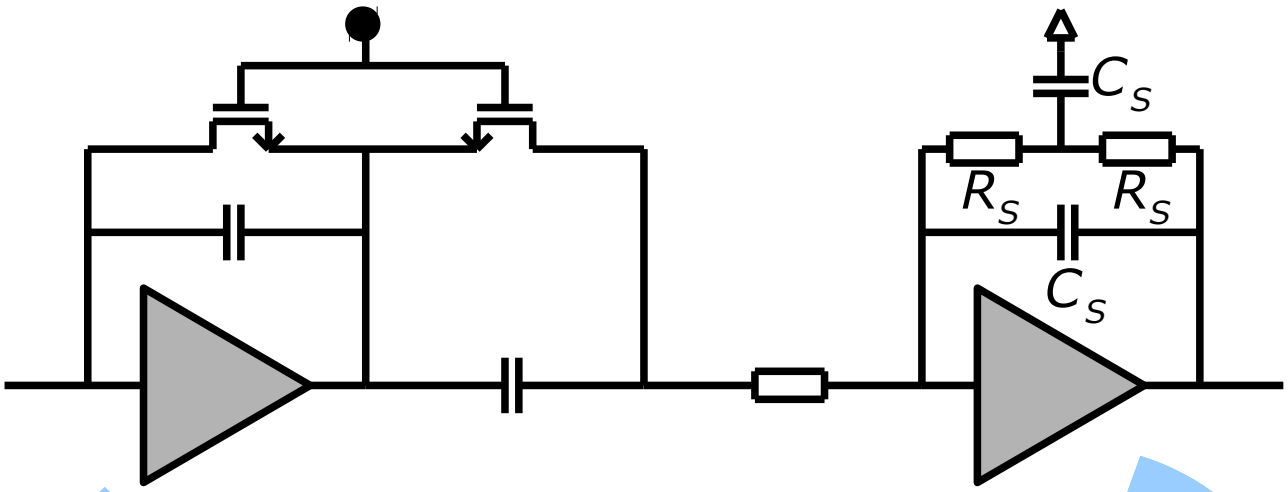
Bias circuitry (12 current DACs)
26 preamp/shaper channels
Detector capacitors (5pF per block)
8 pipelined ADCs

ADC control + bias
5.2 kBit shift register matrix
Control + readout/decoder logic blocks
Test circuits

Impression: Test Setup



Reminder: Preamplifier/Shaper Circuit



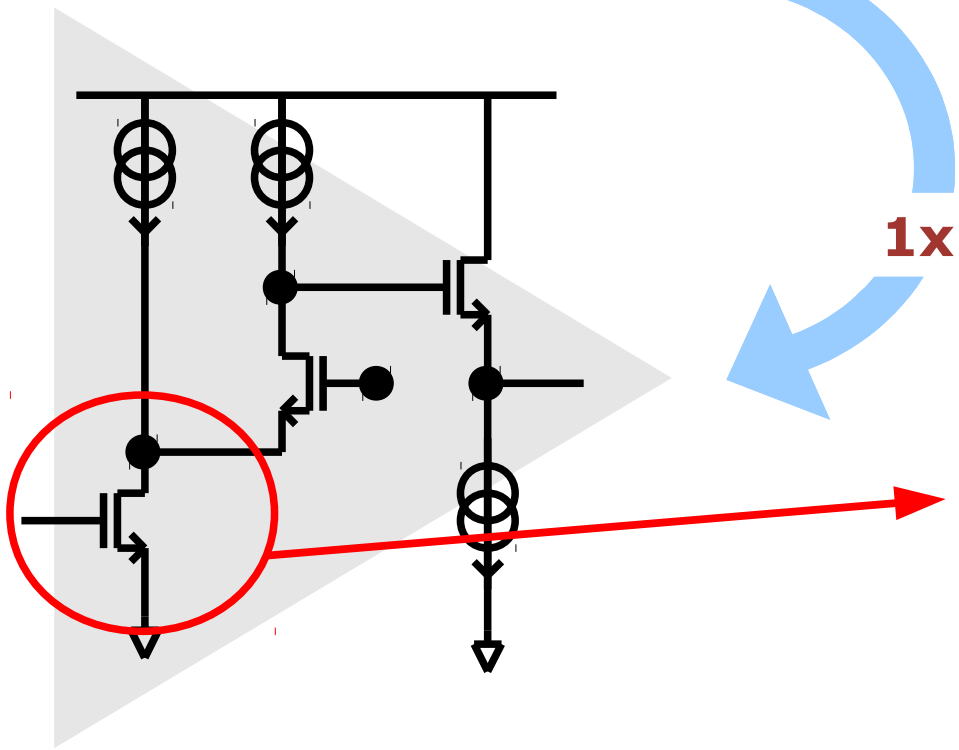
$$H(s) \approx \frac{A_{DC}}{(1+sR_SC_S)^2}$$

- O'Connor FB
- 2nd order shaper
- Shaping time: 82 ns
- Unified amplifier cell
- N-MOS input
- ≈ 3.6 mW/channel

11x

1x

(also channels with less instances for test purpose on chip)

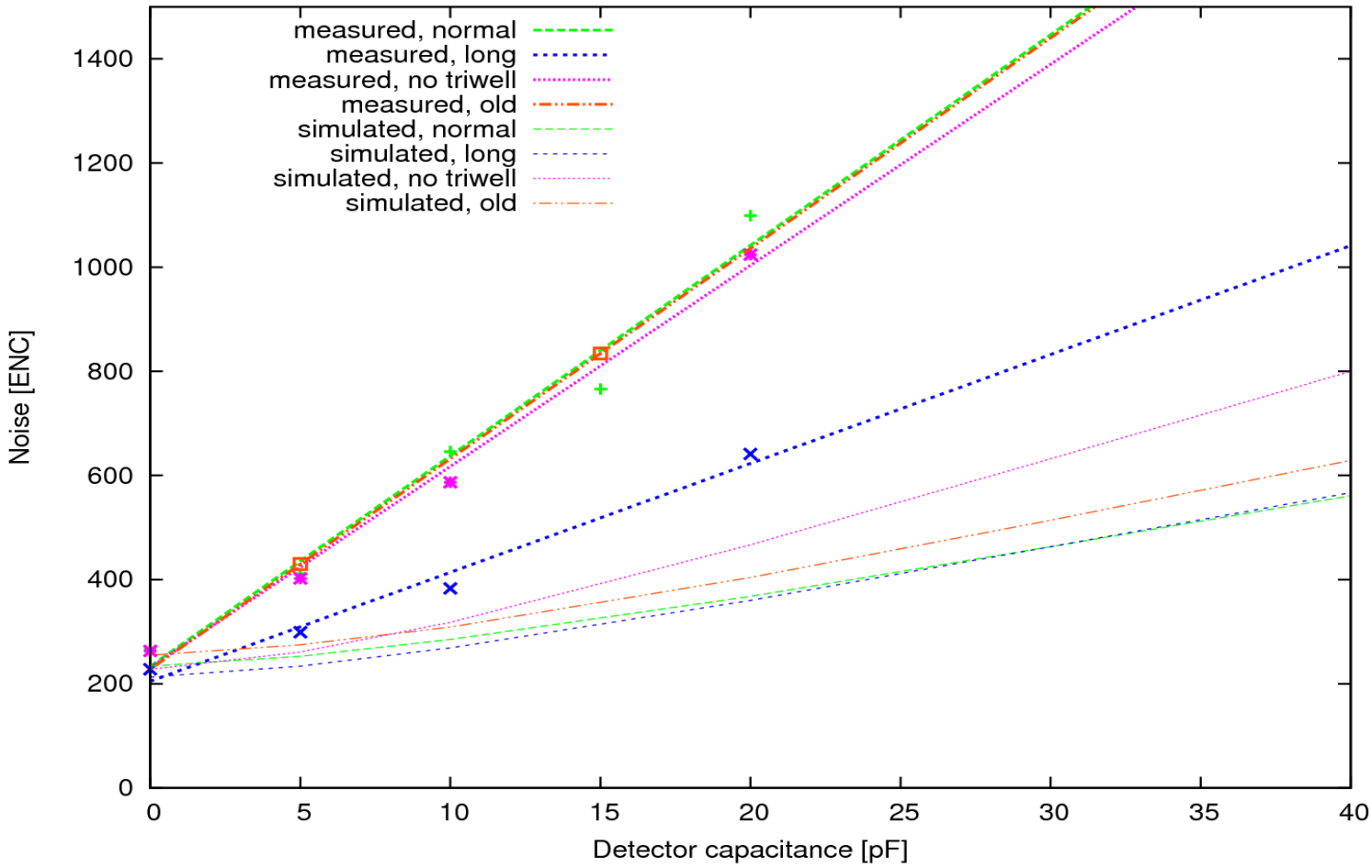


New: For noise analysis: 3 different input NMOS types

- normal: NMOS, triwell, 180nm length
- no-triwell: NMOS, no-triwell, 180nm length
- long: NMOS, triwell, 320nm length

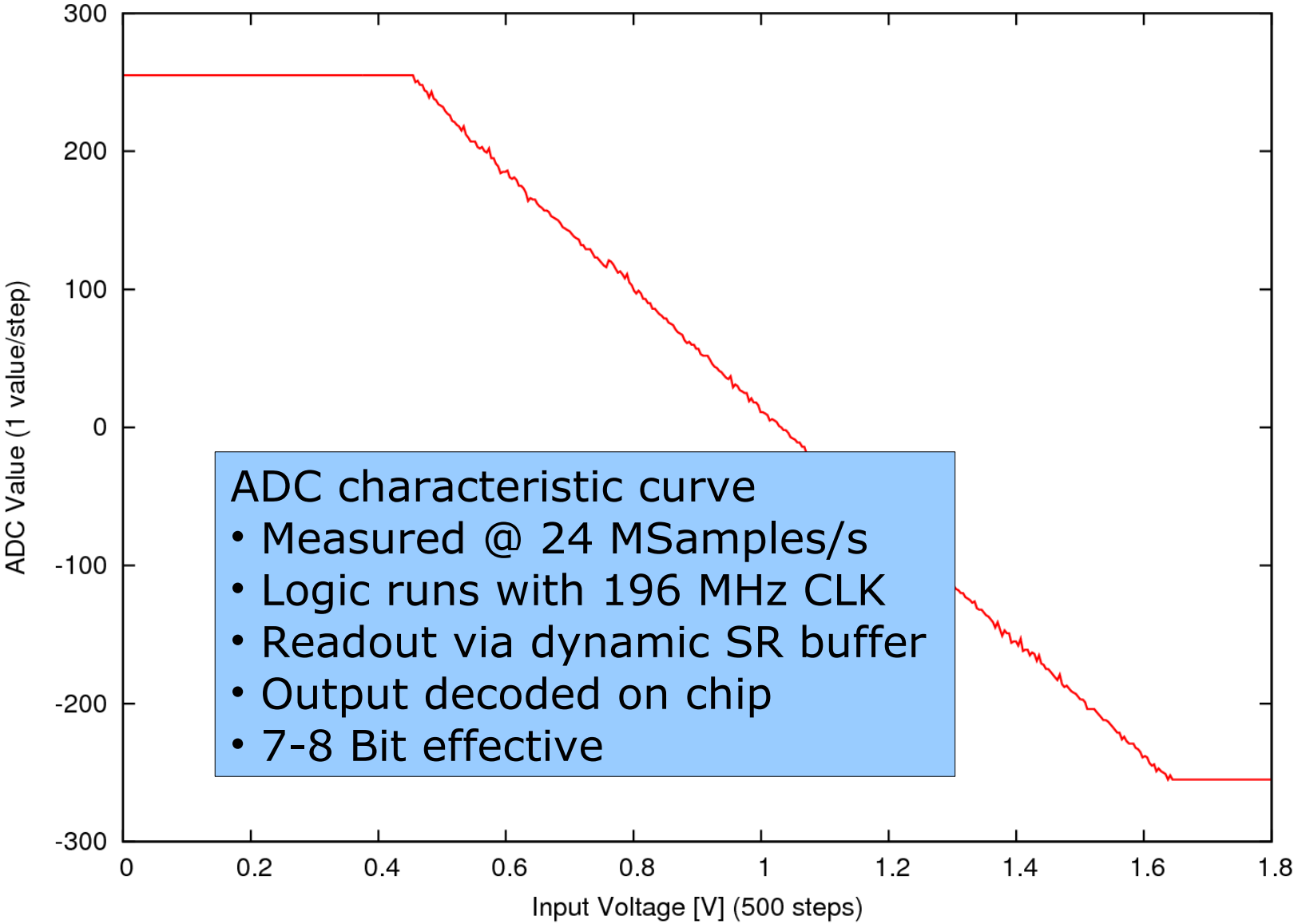
Chip: Preamp/Shaper Results

- Noise was measured with s-curve scans using the discriminator
- Injection capacitor calibrated via test circuit
- 4 different preamplifier types: old, normal, no triwell, long

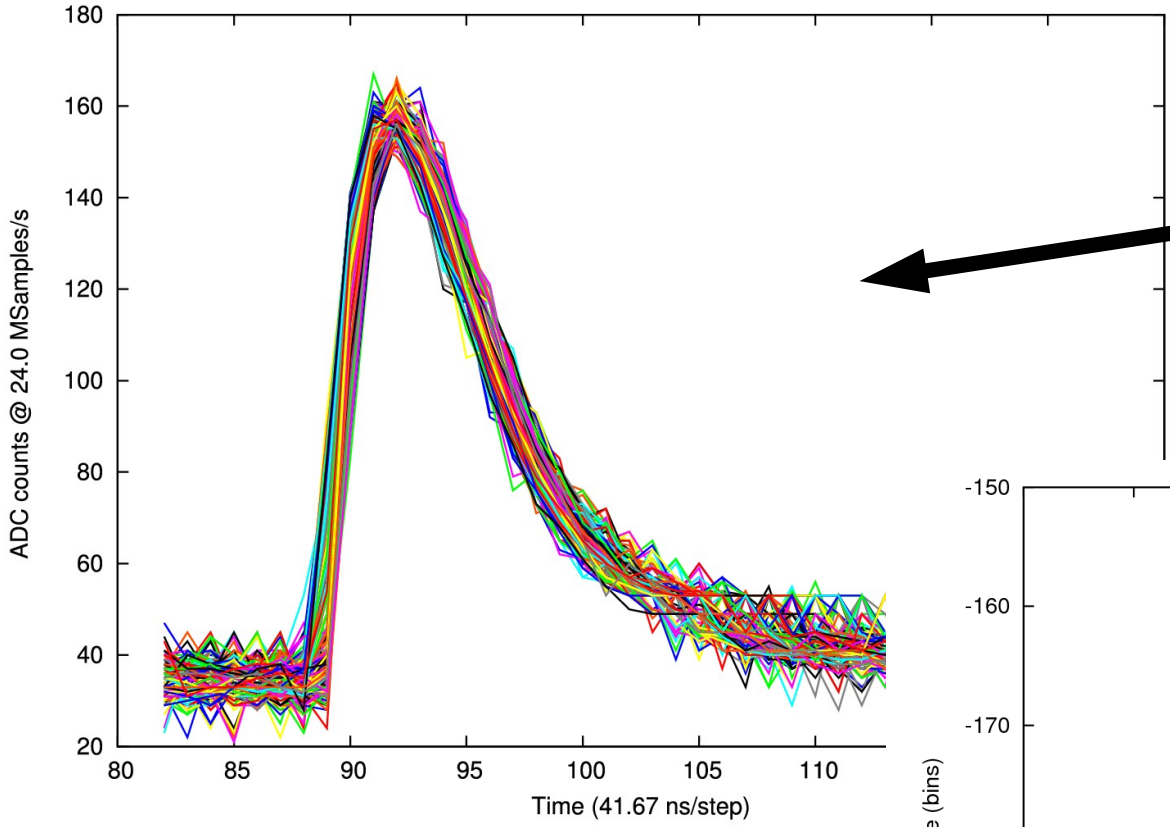


- Results:
  - Noise values of normal (triwell NMOS input, minimal length) and no triwell (NMOS without triwell, minimal length) channel show no significant difference compared to the old channel => values still much worse than simulated
  - Noise slope of long (triwell NMOS input, 320 nm length) channel about two-times smaller => **about 800 e ENC @ 30 pF** achievable, still worse than in simulation

Chip: ADC Results



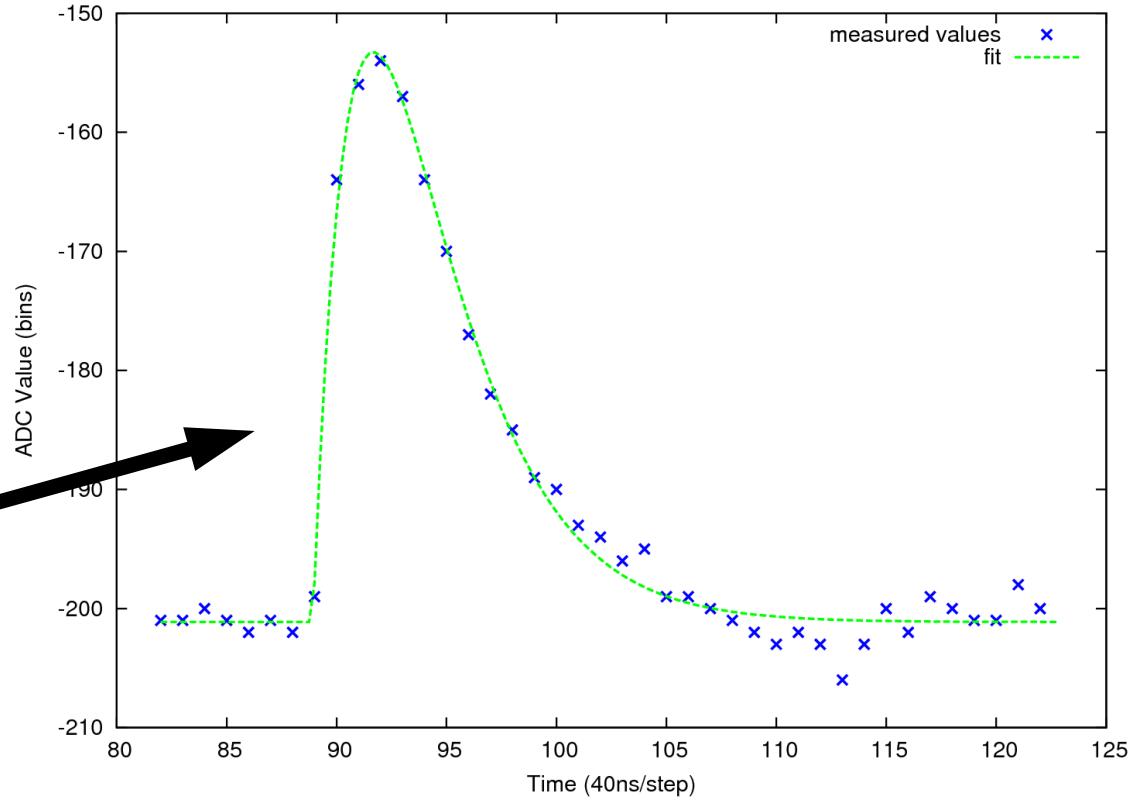
Chip: Shaper Output connected to ADC



Some ADCs can be connected to shaper outputs → digitization of shaper pulses possible (1000 hits shown here)

Theoretic and measured pulse shapes match well

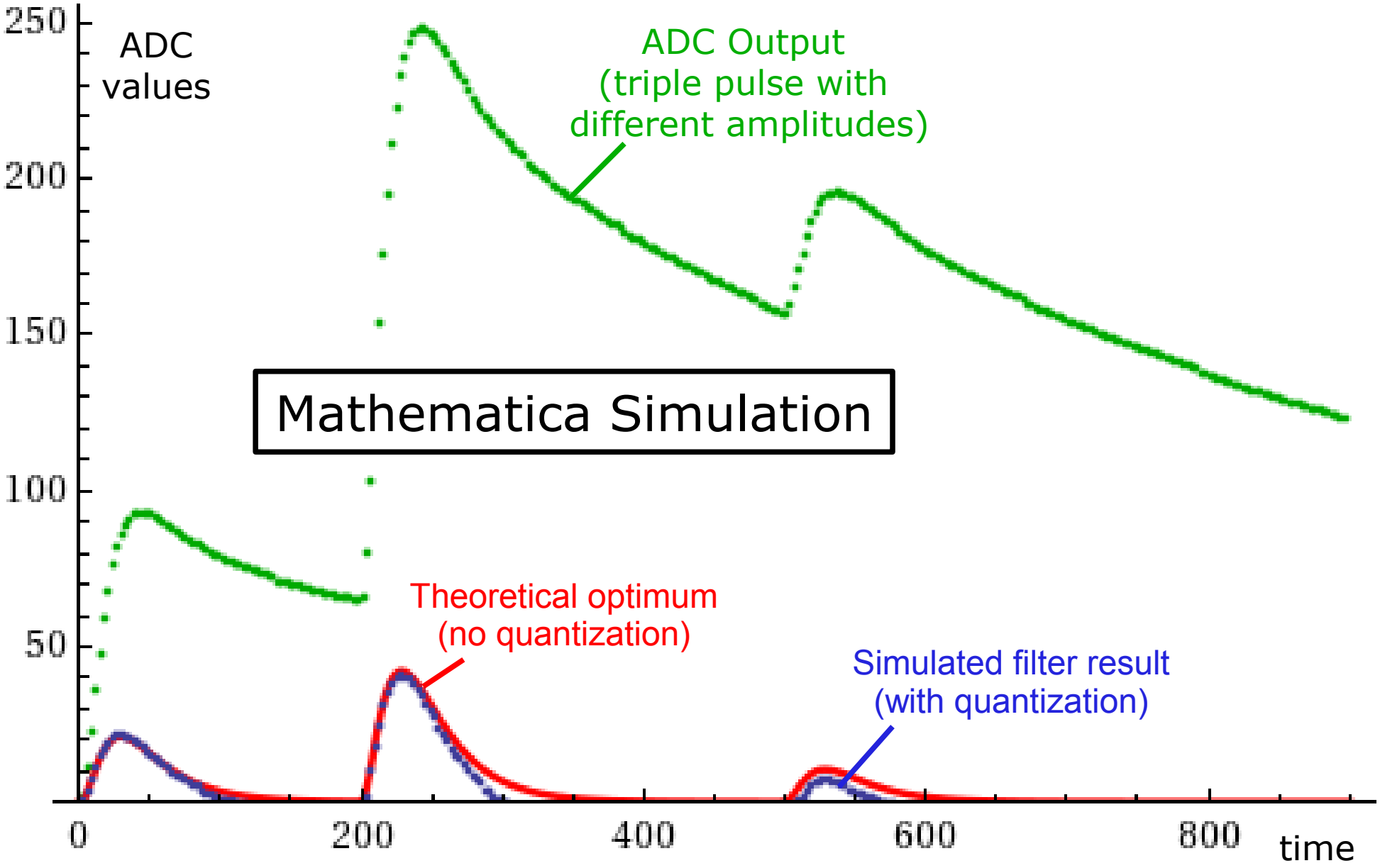
(fitted with x * exp(-x))



New: Simulation of IIR Filter (Ion Tail Cancellation)

- Principle of filter: Cancel several exponential components of the (1/x shaped) ion tail, but keep the exponential component having the fastest time-constant.
- IIR (infinite impulse response) filter needed due to the very long ion tails (influence of FIR filter on data stream would be too limited)
- Design challenges:
  - Choose feasible filter structure and filter order (ALTRO: 3-times 1st order)
  - Find necessary fixed-point resolution: quantization noise limits accuracy (ALTRO: 18 bit internal resolution, 10 bit ADC values)
  - 2's complement decimal point arithmetic is very tricky
  - Build fast fixed-width multiplier, processing time must be small
  - Avoid oscillations (IIR can get unstable, quantization makes it even worse)
- Status:
  - Theoretically well understood (Mathematica-Simulations, see next slide)
  - 0th iteration of Verilog modules available, seems to work (currently under investigation) well, but multiplier currently too slow and large

Simulation: IIR Filter (Ion Tail Cancellation)



Current (but yet untested) Test-Chip

- Results of the next test-chip iteration very soon available
  - **Naked dies lie on my desk** since last week
  - Re-designed PCB finished, fabricated and ready
  - Software improved, adjusted and ready
- Main new features:
  - 8 complete channels with (so far) best preamp type and ADC type, connected to input pads with (new) spark protection → first gas chamber tests hopefully feasible
  - Re-layouted input NMOS of preamps (proposal from Mircea Ciobanu)
  - Varied length of input NMOS (180 … 460nm) due to strange noise results from previous chip
  - Various smaller improvements

Data-Rate Calculation

Some estimated numbers:

- 32 channels / chip
- 250 kHz event rate / channel (one hit every 4 µs)
- 8 Bit ADC resolution
- 10 samples / event
- 12 Bit time-stamp / event (epoch length 164 µs @ 25MSamples/s ADC speed)
- 5 Bit channel ID

$$R_{chip} = \underbrace{\frac{250\,k\,events}{channel \cdot s} \cdot 32\,channels}_{hit\,rate\,chip} \cdot \Big(\underbrace{\frac{8\,bit}{sample} \cdot \frac{10\,samples}{event}}_{hit\,data} + \underbrace{\frac{17\,bit}{event}}_{time-stamp+ID} \Big) = \frac{776\,Mbit}{s}$$

=> Conservative estimation: about 100 Bits/hit!

=> One 2.5 Gbit/s LVDS link could only be shared between 3 chips

But: Corner chips may produce much less than 250k events/s

Simple data compression unit reasonable

=> Epoch counter + forward error correction overhead not considered here!

3. Future Plans and Next Steps

Design: Event Builder and Readout Scheme

- Already available: whole chain from preamp to ADC => focus now on digital parts
- Main digital construction sites:
  - Event builder (currently under investigation)
    - Hit detection logic (extract hit trigger from digital data stream), including neighbor hit logic
    - Time-stamp latch logic (global TS counter, local latches)
    - Meta data generator (header, flags, ID's, …)
    - Dynamic buffers
    - Eventually a data extraction unit (amplitude and high-res. TS)
  - Token ring network
  - Output serializer (will maybe include some data recombination logic)
  - Output LVDS buffer/driver
  - Slow control

Next Measurements / Test Setup Plans

Step 1:

- Measurement of latest test-chip will start at the beginning of March (new student: Lukas Raffelt)

Step 2:

- First gas chamber measurements in cooperation with Frankfurt (Matthias Hartig) can start as soon as basic chip characterization has been finished (end of March).
- Measurements with chamber from Münster (David Emschermann) also feasible!?

Summary

Next to last test-chip:

- 26 preamp/shaper channels, 40 µm pitch (540 µm length)
- 3.8 mW per amplifier
- Pulse peaking-time 95 ns
- 800 e ENC @ 30 pF detector capacitance (long channel)
- 8 pipeline ADCs (9 Bit design, 7-8 Bit effective) @ 24MSamples/s
- 4.5 mW per ADC

Current test-chip, untested

- Further improvements, but conceptually identical to previous chip
- 8 complete digitizer channels with spark protected inputs for real gas chamber tests
- Addresses several noise issues (layout further improved, NMOS length varied)

Current construction sites

- IIR filter, baseline correction, ...
- Digital event builder and readout scheme
- Data output protocol

Thank you!