UNIVERSITÄT HEIDELBERG

Status of CBM-GAS-XYTER

Latest Results of the Self-Triggered Digitizer Chip

Tim Armbruster

tim.armbruster@ziti.uni-heidelberg.de

15th CM @ GSI

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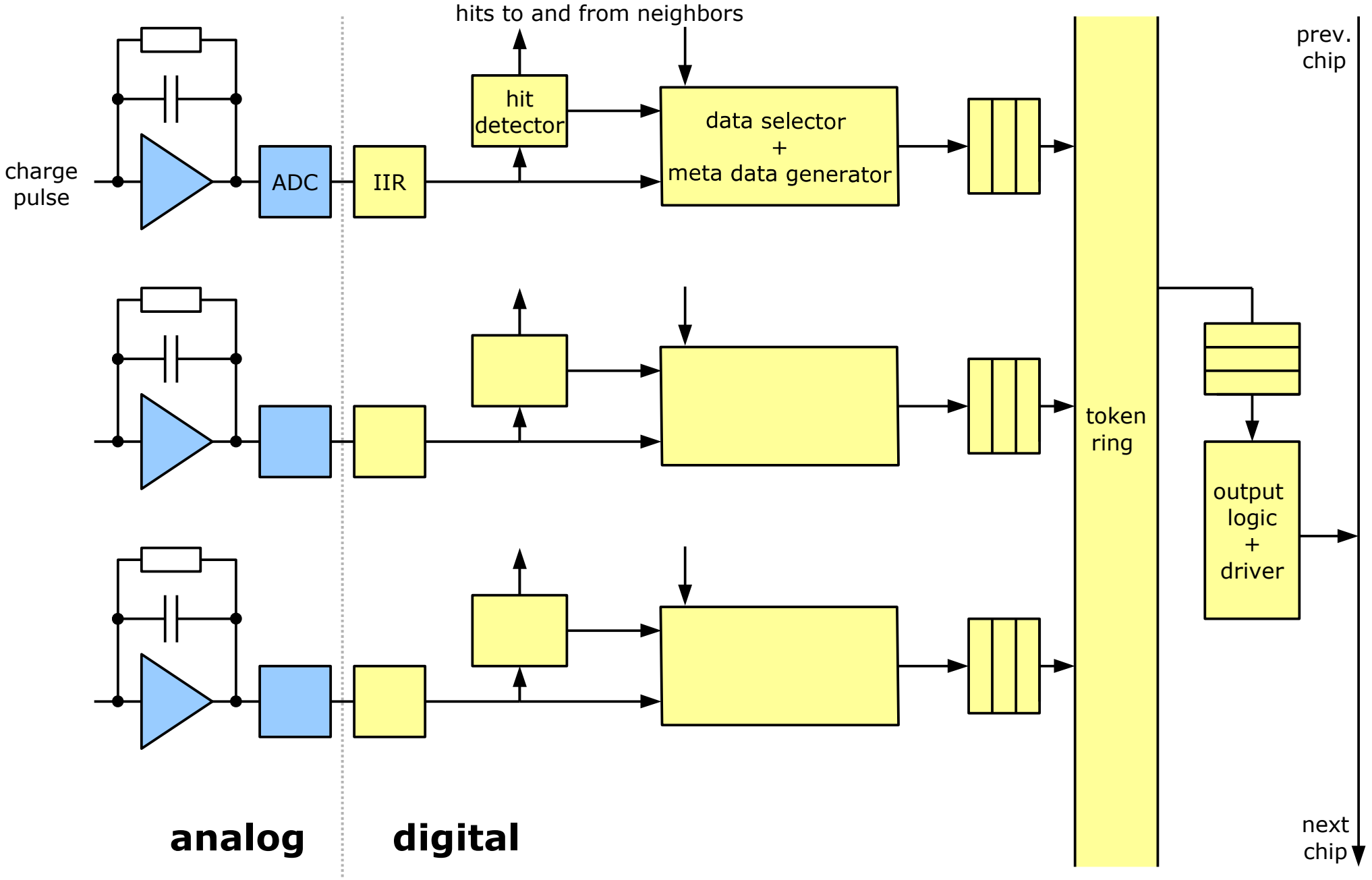
1. Introduction

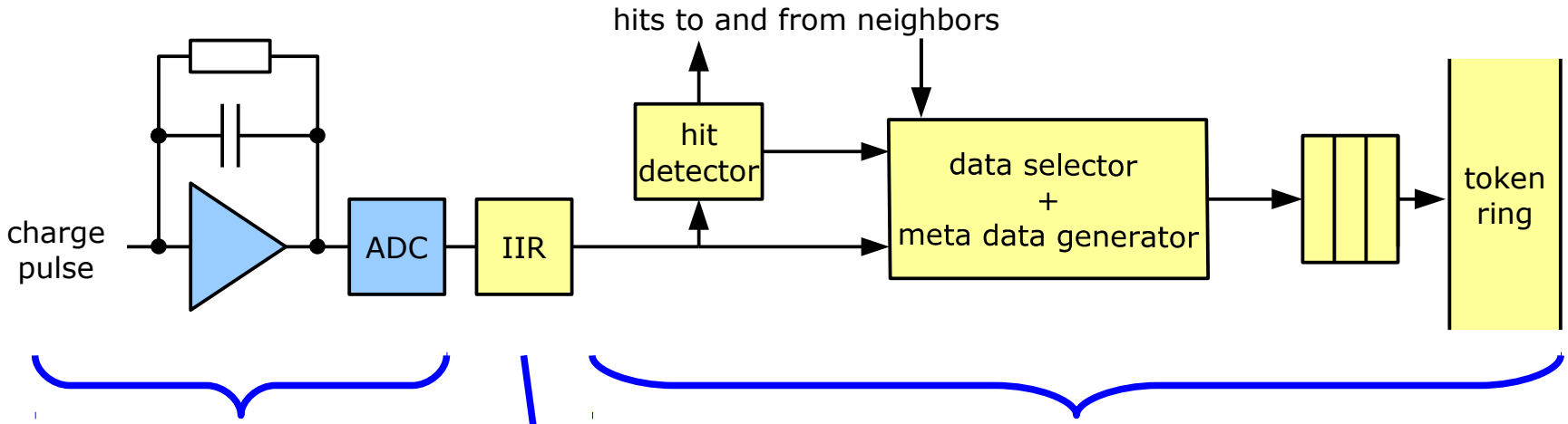
Requirements/Motivation

- Application:
  - Main task: gas chamber readout for CBM TRD
  - Application in other FAIR detectors also conceivable
- We need a self-triggered readout chip that has:
  - 32-64 mixed-signal channels
  - Low noise & power charge amplification (order of 1000e ENC @ 30pF det.)
  - Bandwidth limitation (2^{nd} order shaper or higher, about 90ns shaping time)
  - Digitization (7-10 bit @ 5-30 MHz)
  - Time stamping (necessary time resolution depends on ADC sample speed)
  - In-channel data processing (ion tail cancellation, baseline correction, ...)
  - Inter-channel network (e.g. token ring network)
  - Inter-chip network (pass the data to the next stage)

Conceptual Data Flow Diagram



Status of Development



Preamp, Shaper, ADC

- Several test-ASICs successfully realized
- First test-chip including an ADC (next to last chip) showed promising results as shown in Split
- Preliminary measurement results of current test-chip will be presented

Hit detector, data generator and token ring

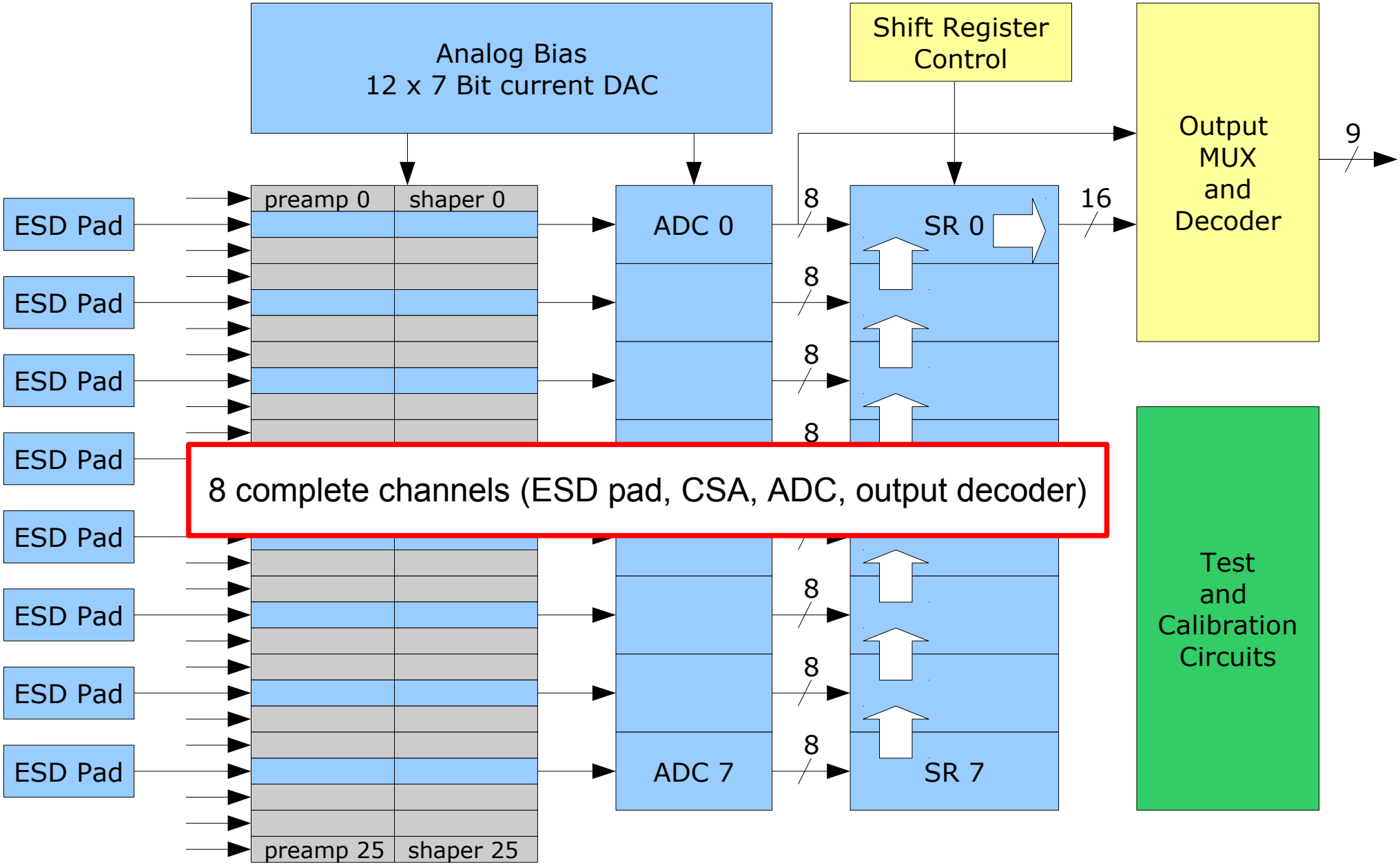
- Design of data flow and control concept completed
- 1st iteration of Verilog description finished
- First simulation results will be presented

Infinite Impulse Response Filter (IIR)

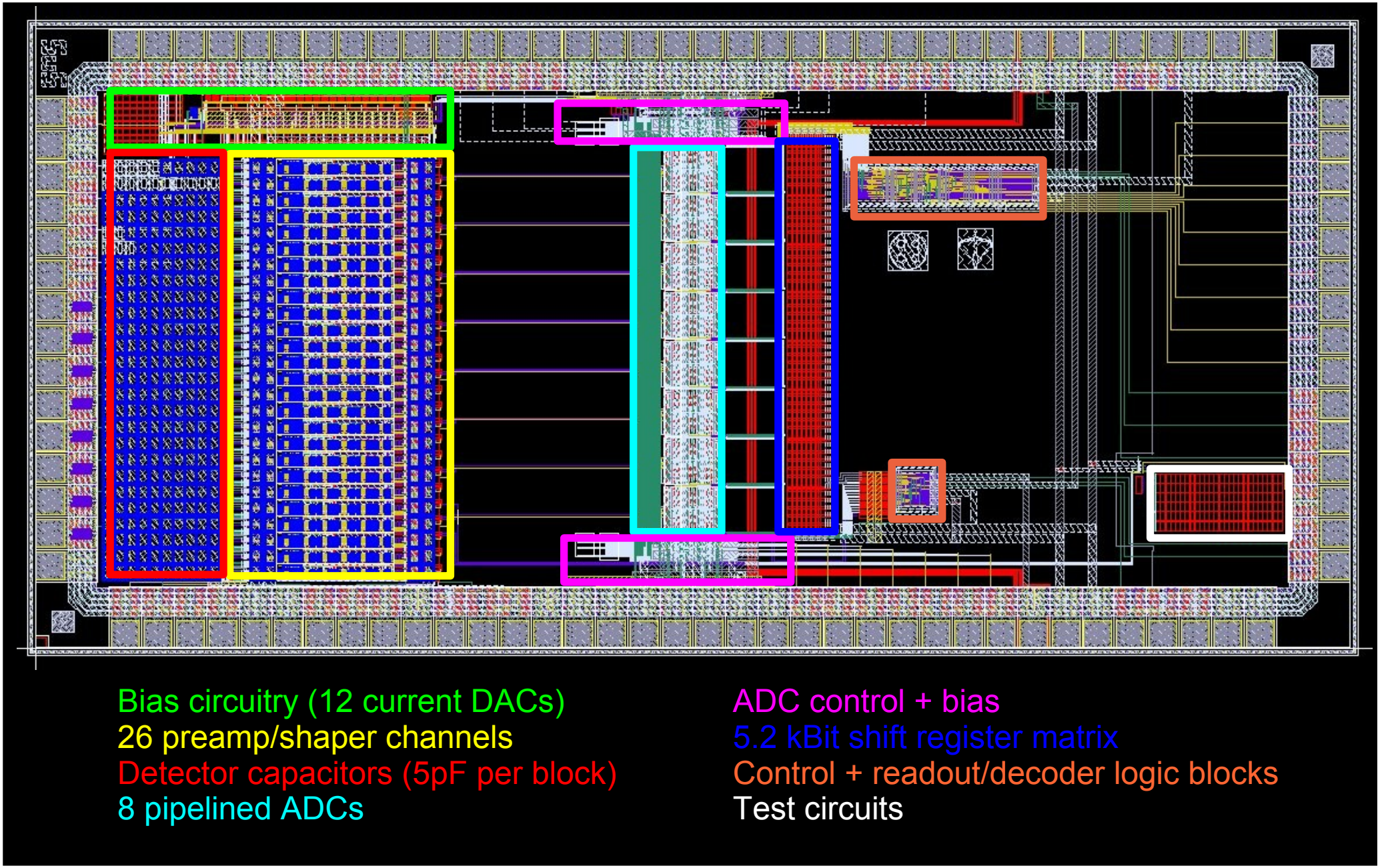
- Theoretically well understood, abstract Mathematica calculations completed
- Simplified Verilog description has been written
- First simulation results will be presented

2. Current Test-Chip Architecture

Block Diagram of Current ASIC



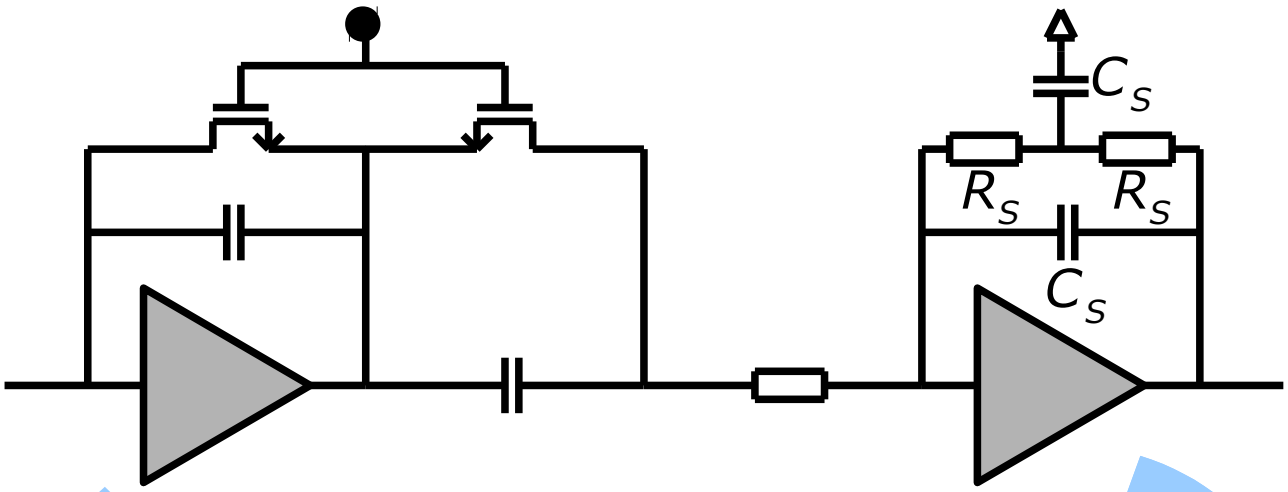
Current Test-Chip: Layout



Bias circuitry (12 current DACs)
26 preamp/shaper channels
Detector capacitors (5pF per block)
8 pipelined ADCs

ADC control + bias
5.2 kBit shift register matrix
Control + readout/decoder logic blocks
Test circuits

Reminder: Preamplifier/Shaper Circuit



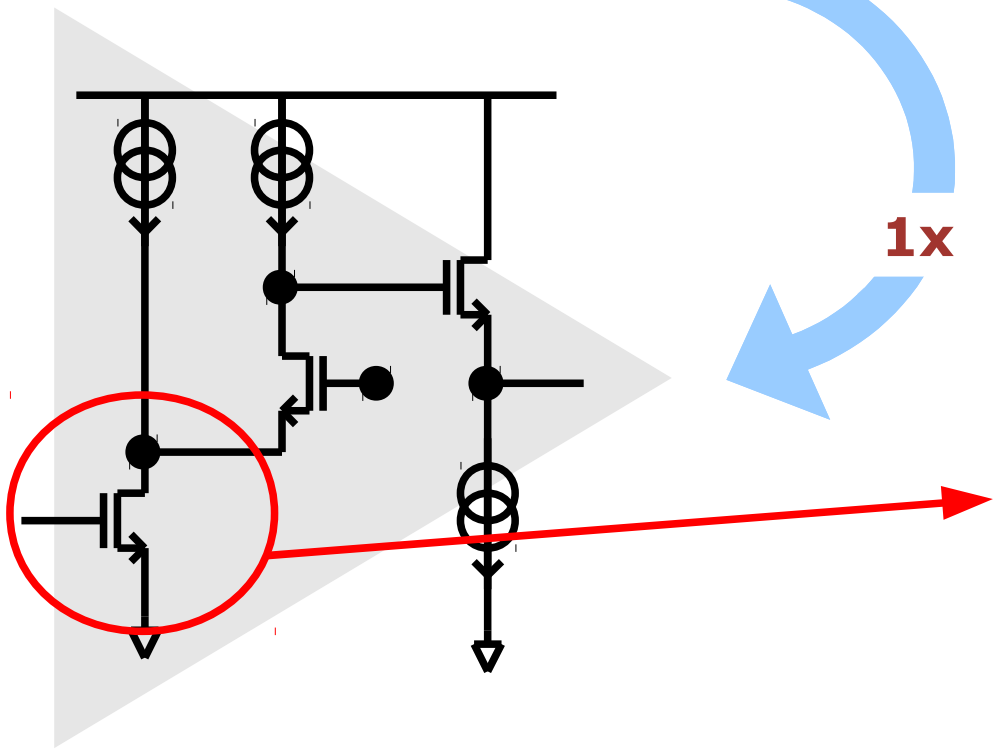
$$H(s) \approx \frac{A_{DC}}{(1+sR_sC_s)^2}$$

- O'Connor FB
- 2nd order shaper
- Shaping time: 82 ns
- Unified amplifier cell
- N-MOS input
- ≈ 3.6 mW/channel

11x

(also channels with less instances for test purpose on chip)

1x

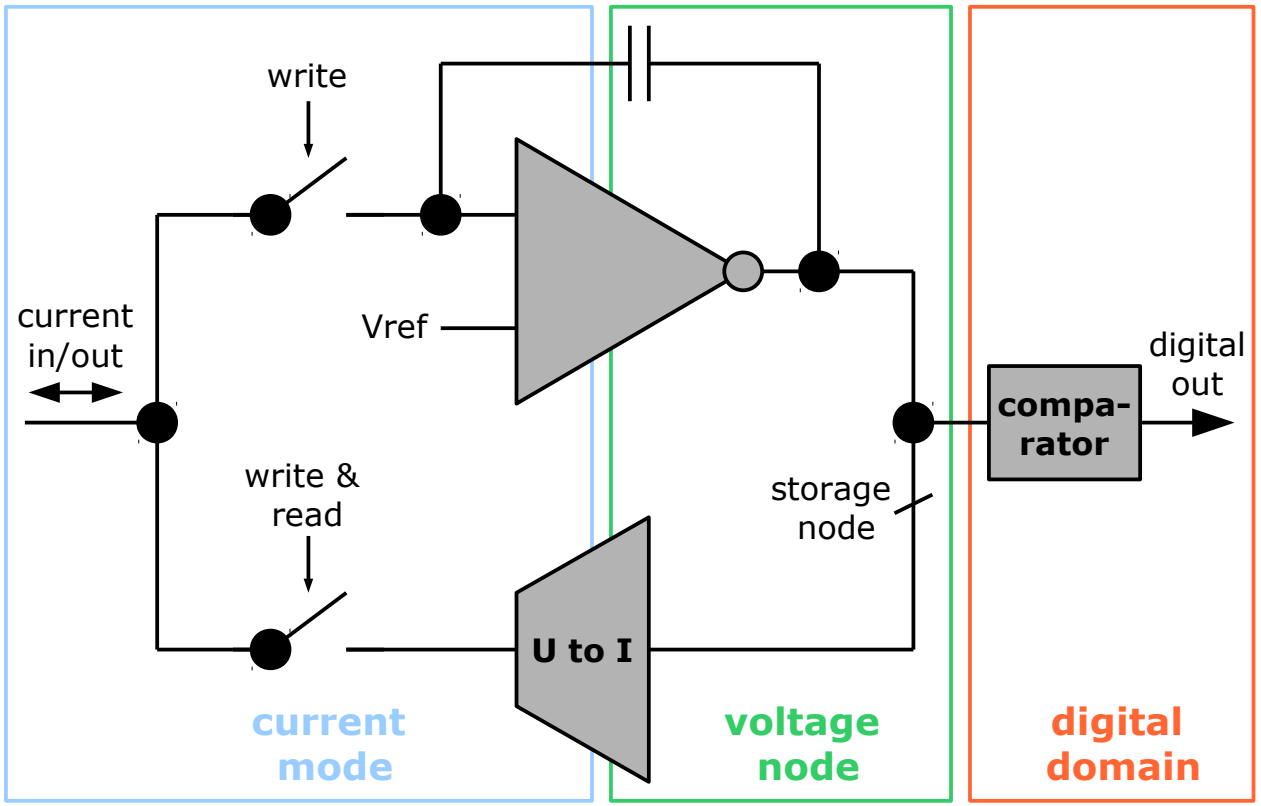


New:

- Scaled lengths of input NMOS (180, 250, 320, 390, 460nm)
- Re-Layout of input NMOS: The (long) gate-fingers have been cut into smaller pieces to decrease gate resistance

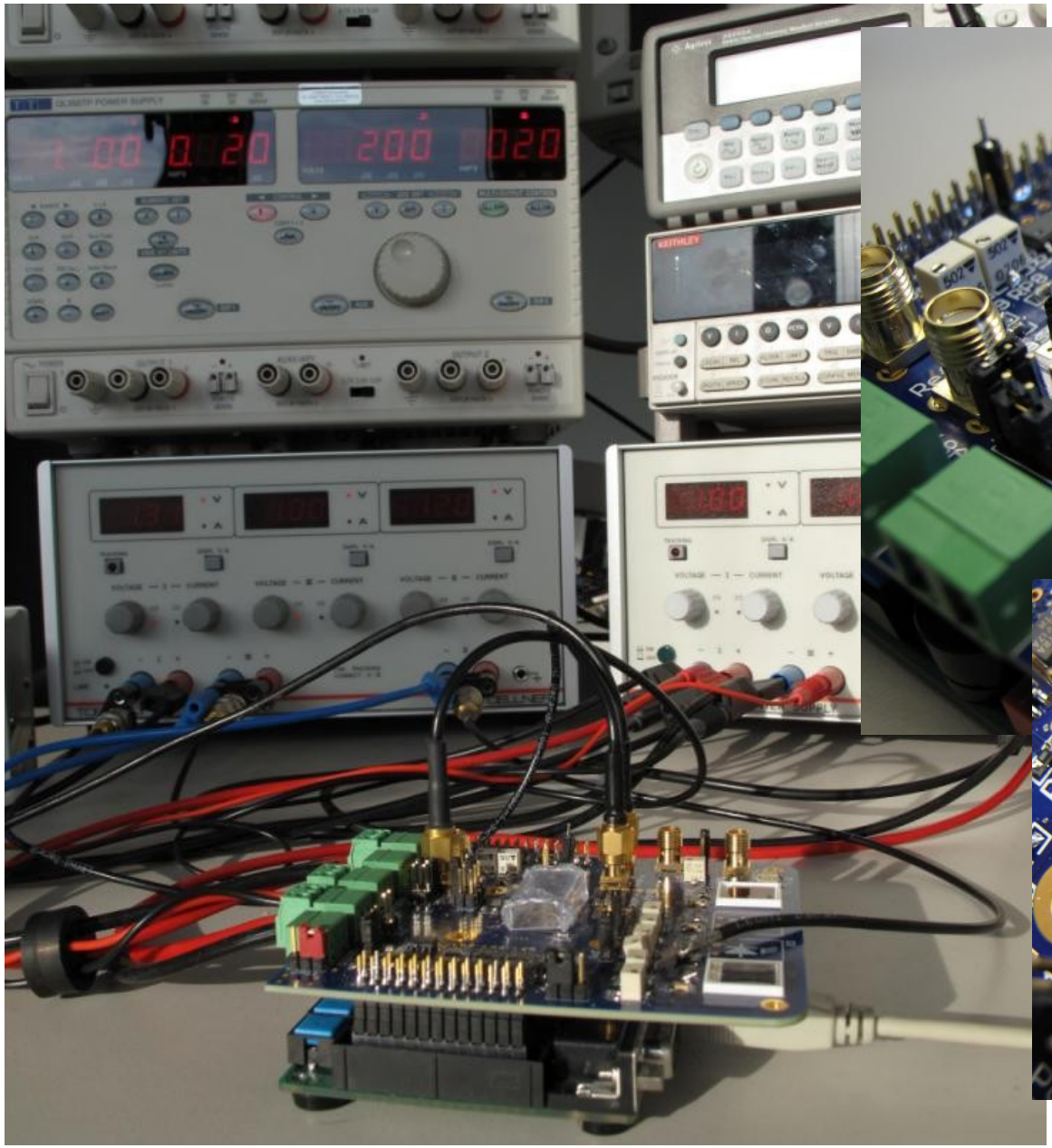
Reminder: Algorithmic ADC Design

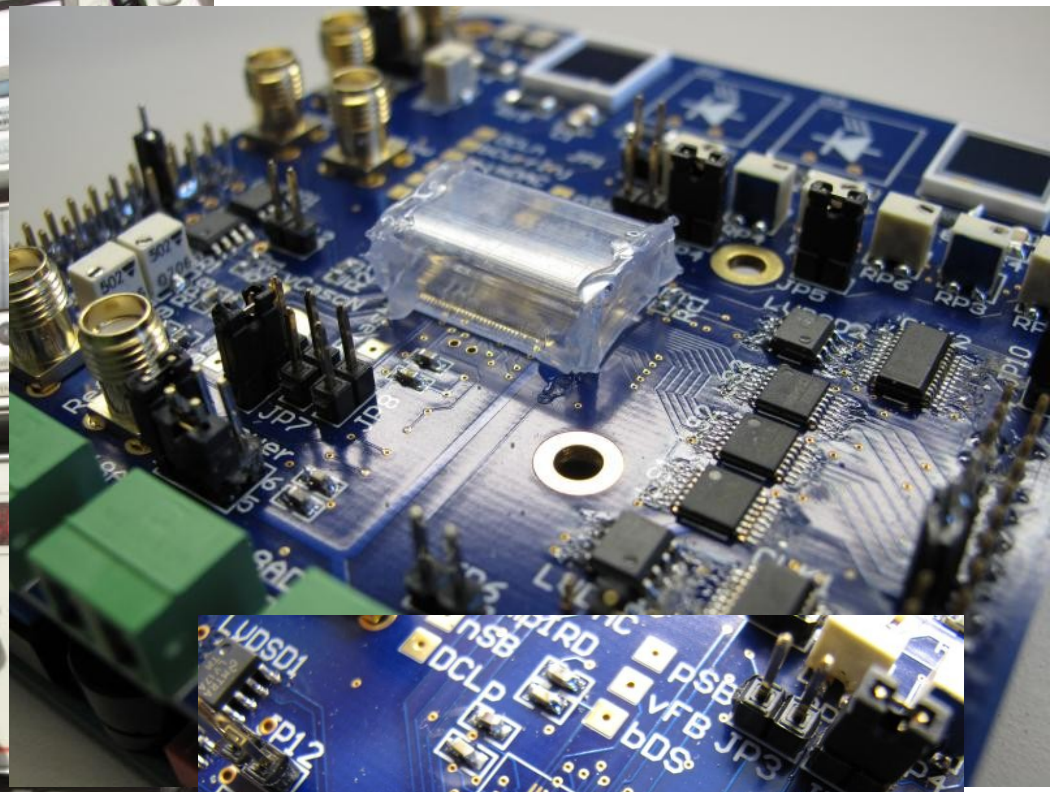
- 8 (scaled) pipeline stages, therefore 9 Bit design
- Algorithmic working principle (“1.5 redundant Bits” / conversion step)
- 25 MSamples/s, layout only 130x120 µm², power consumption 4.5 mW
- Core unit: Novel current storage cell:

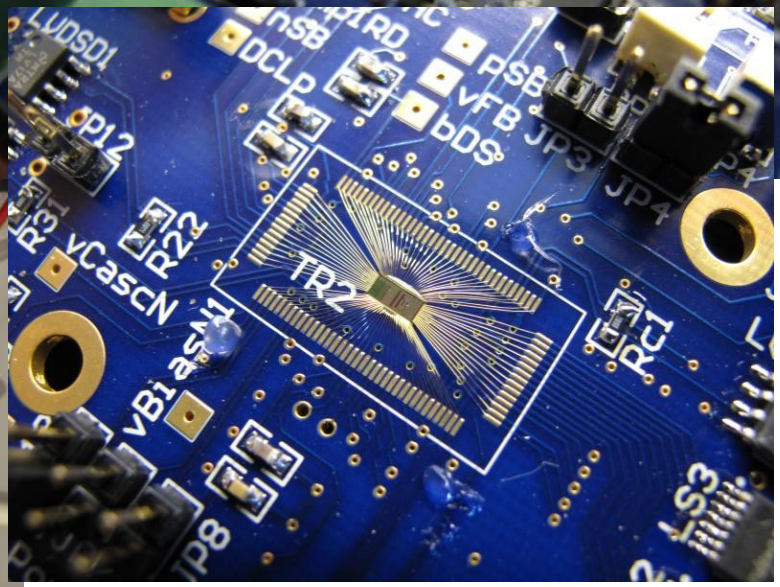


3. Measurement Results

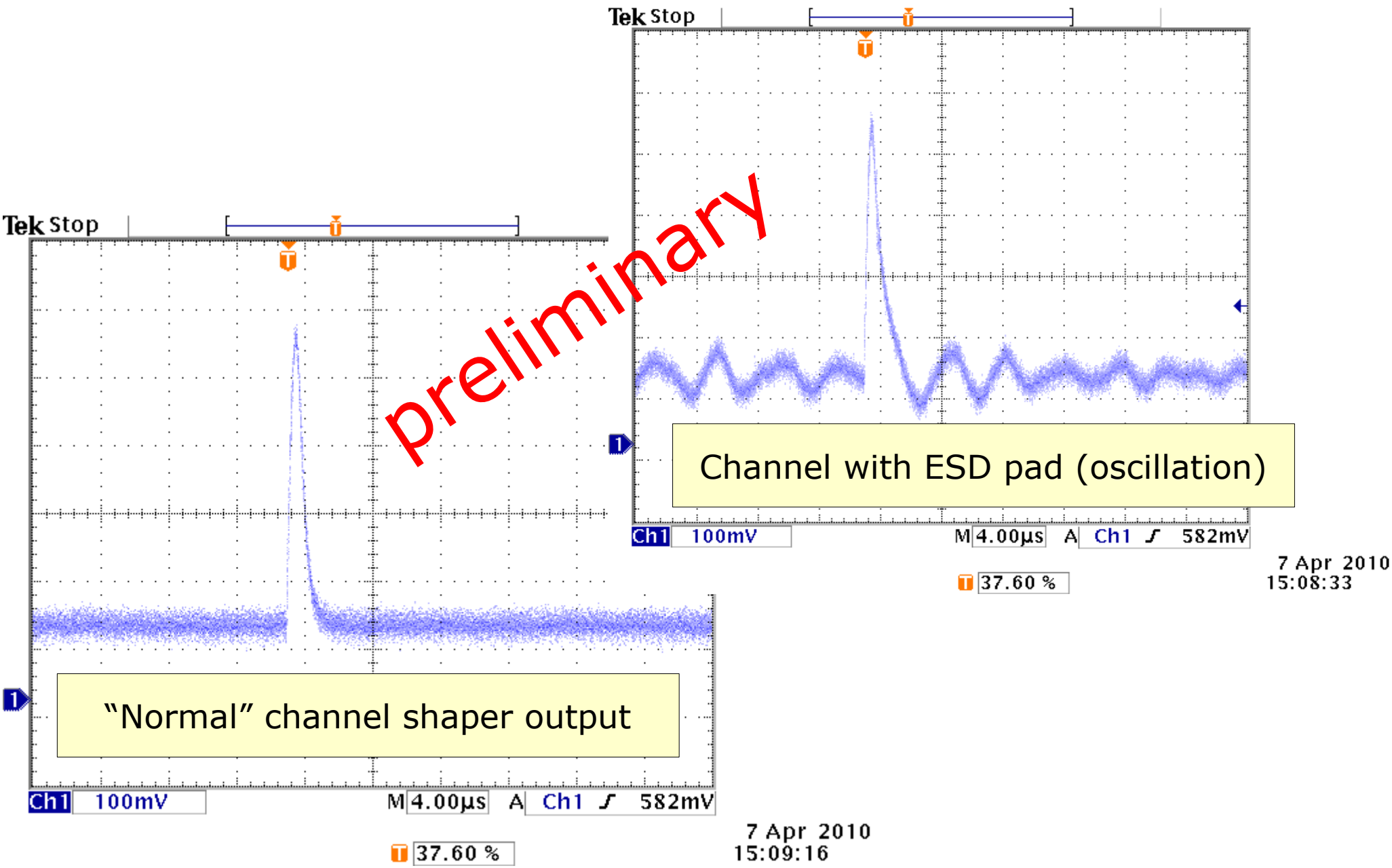
Test Setup



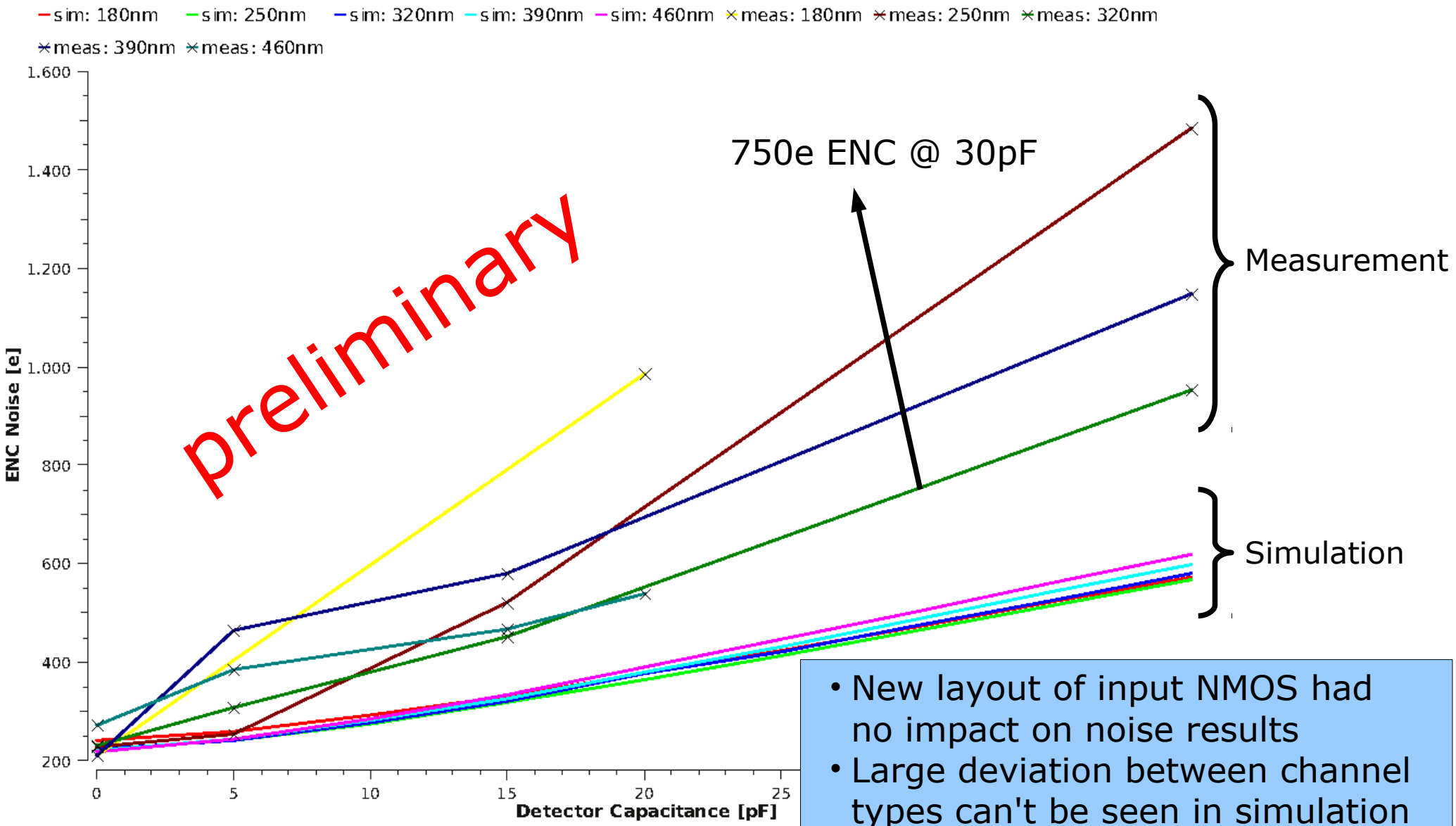

JP5
RP6
RP3
JP7
JP8


LVDSD1
nSB
DCLP
PSB
VFB
bDS
JP3
JP4
RP12
R3
R22
VCascN
TR2
RC1
VB1
JP8
JS3

Shaper Pulse



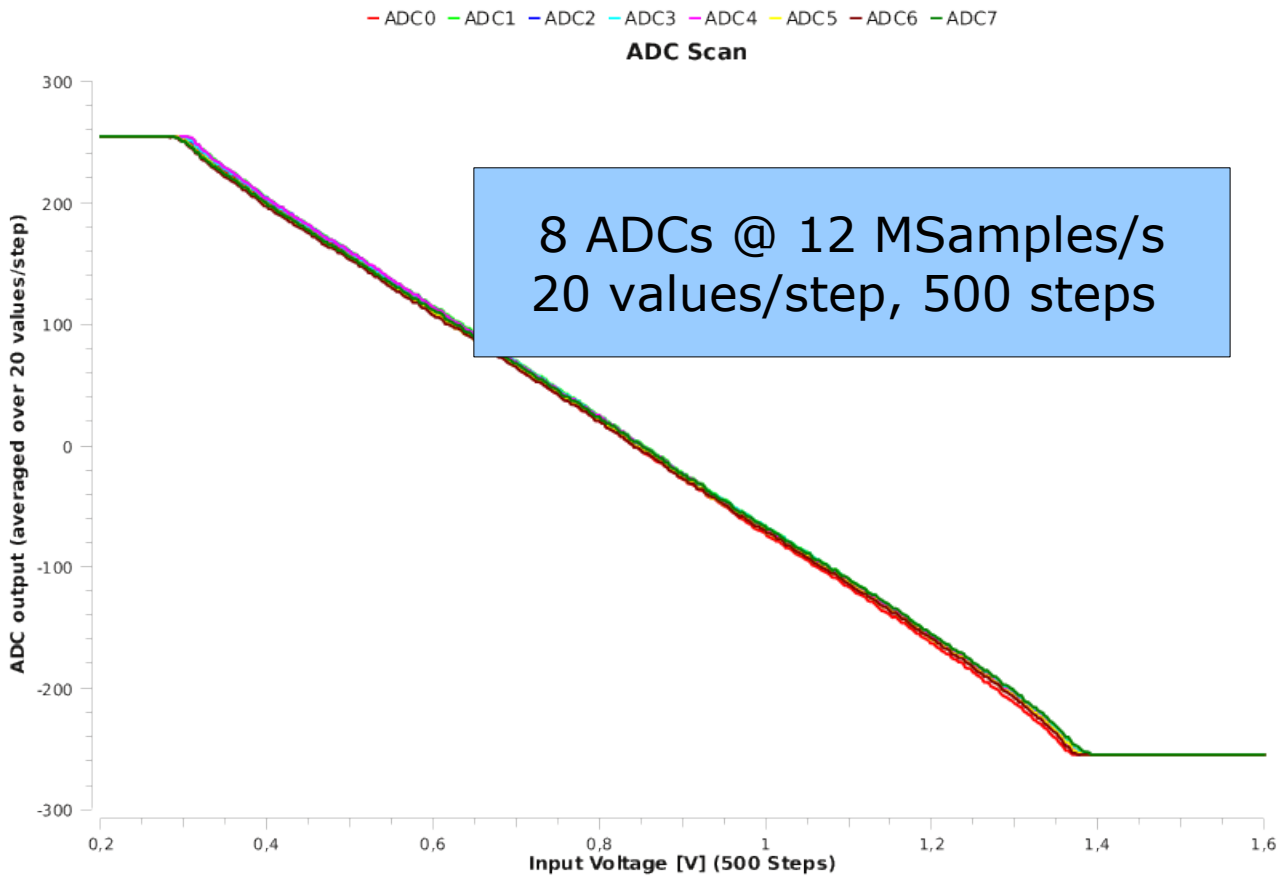
Noise Results



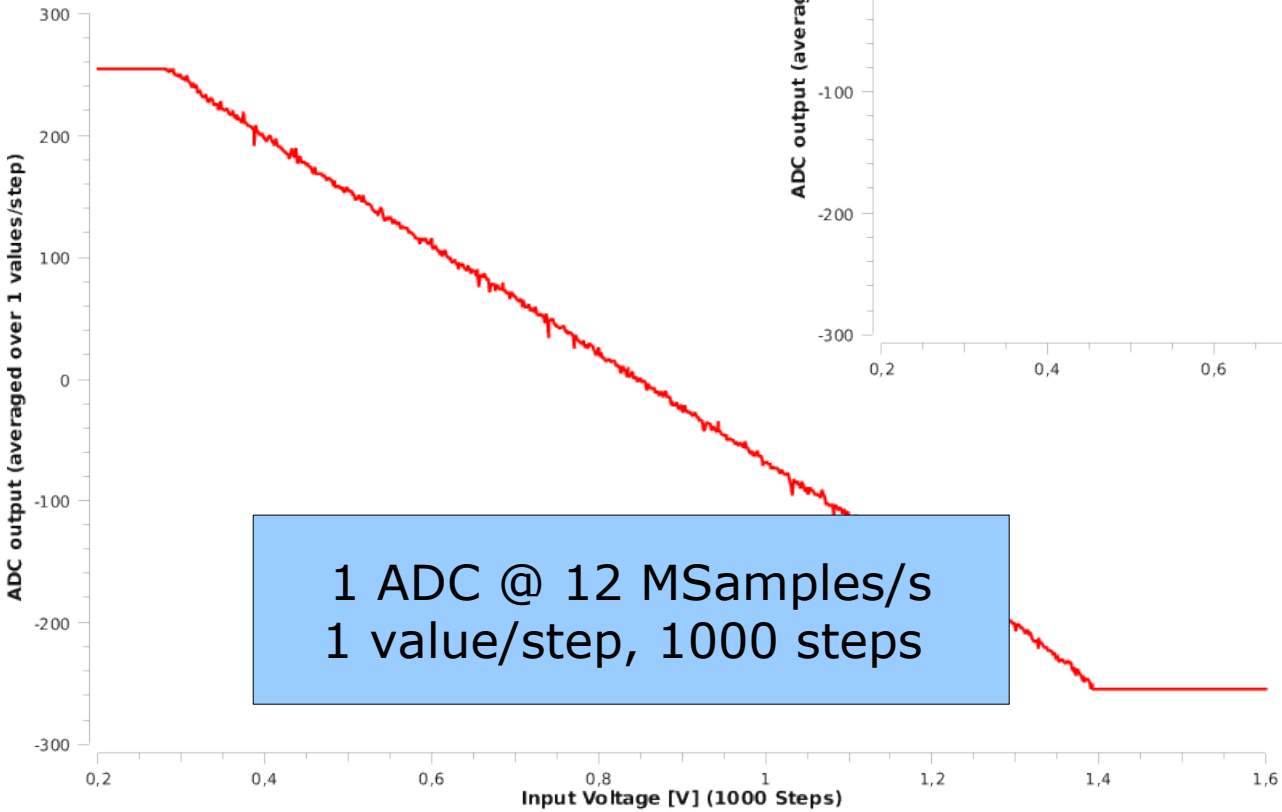
- New layout of input NMOS had no impact on noise results
- Large deviation between channel types can't be seen in simulation
- 320nm is the best choice

Characteristic ADC Curve

preliminary

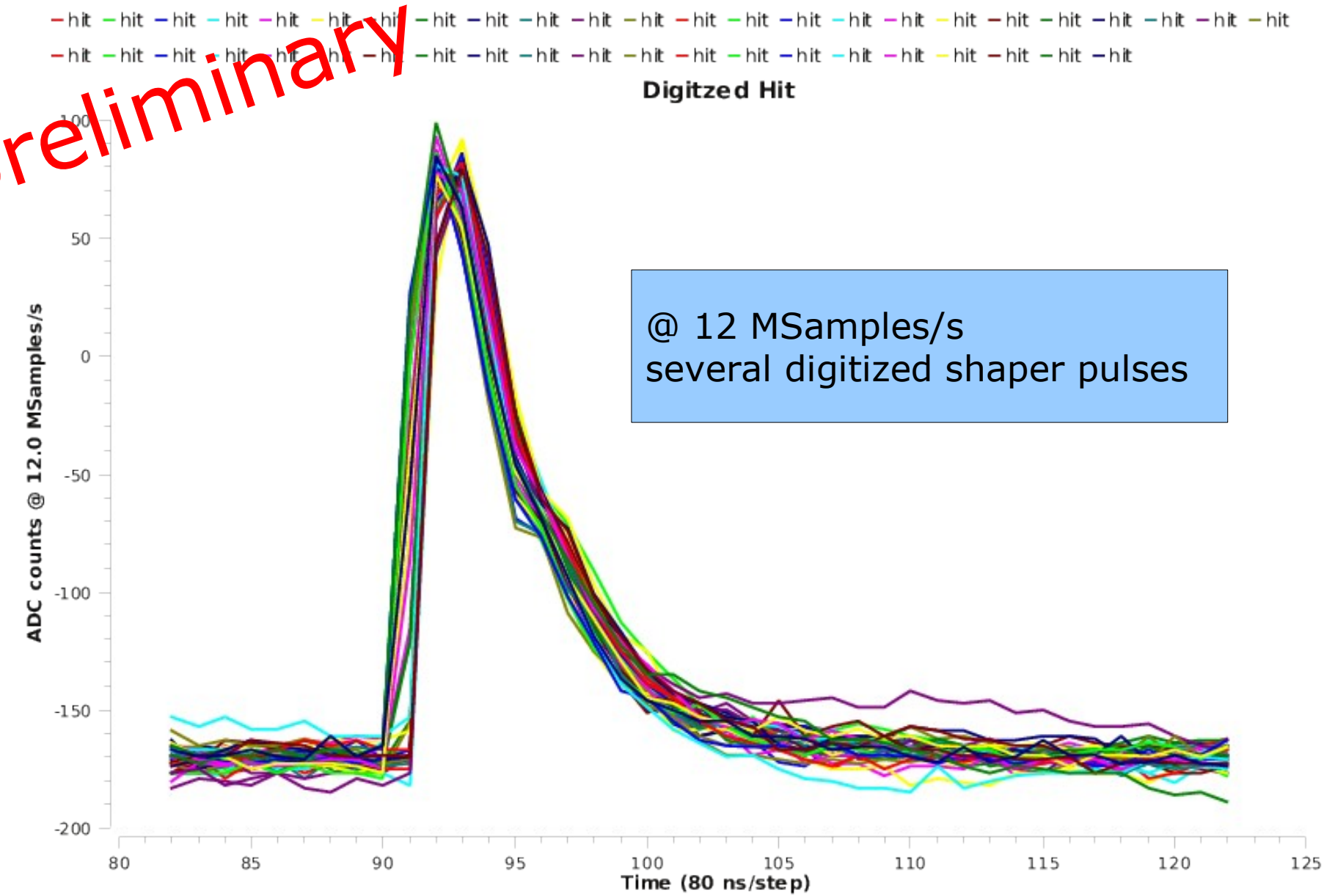


8 ADCs @ 12 MSamples/s
20 values/step, 500 steps



1 ADC @ 12 MSamples/s
1 value/step, 1000 steps

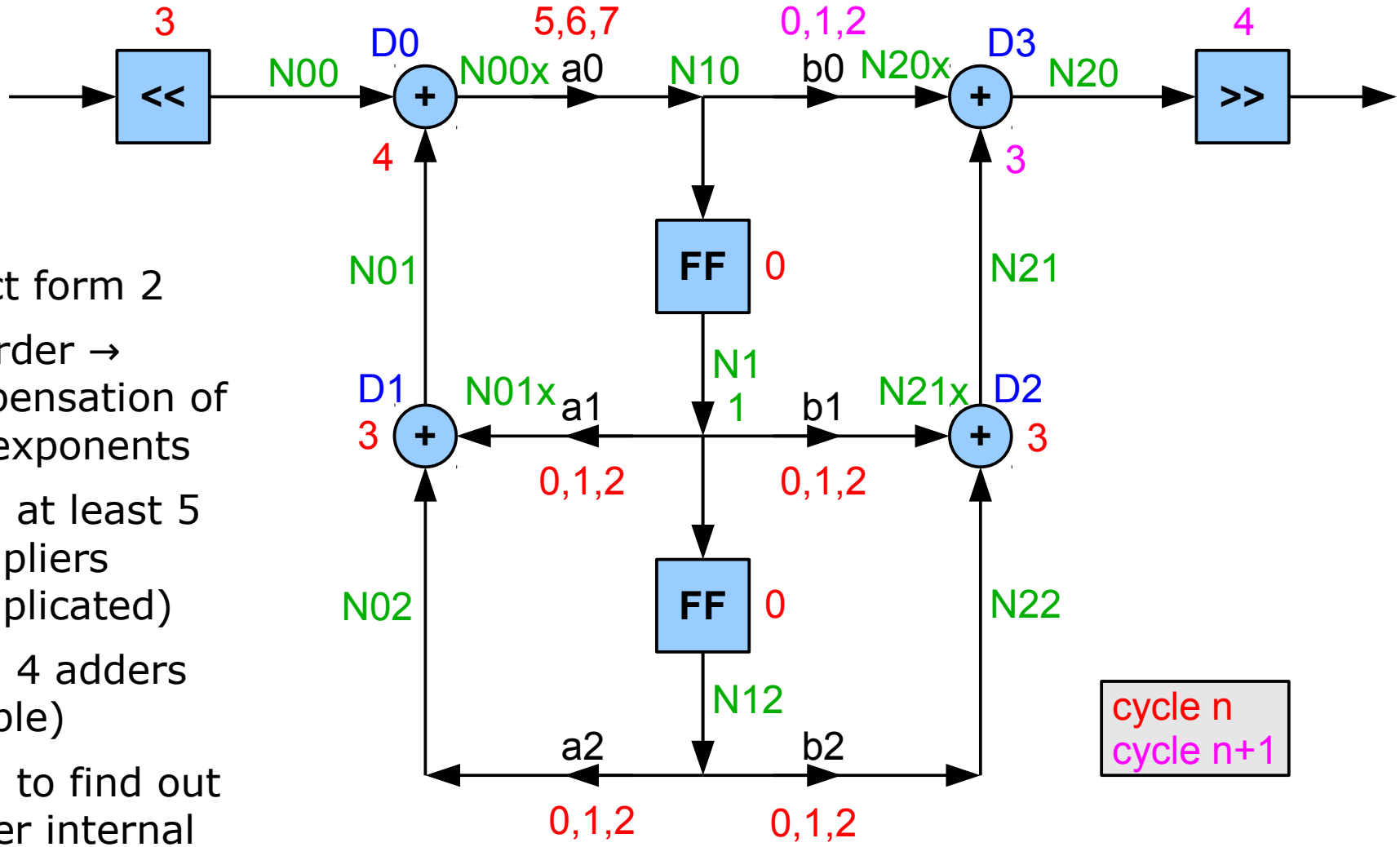
Digitized Pulses



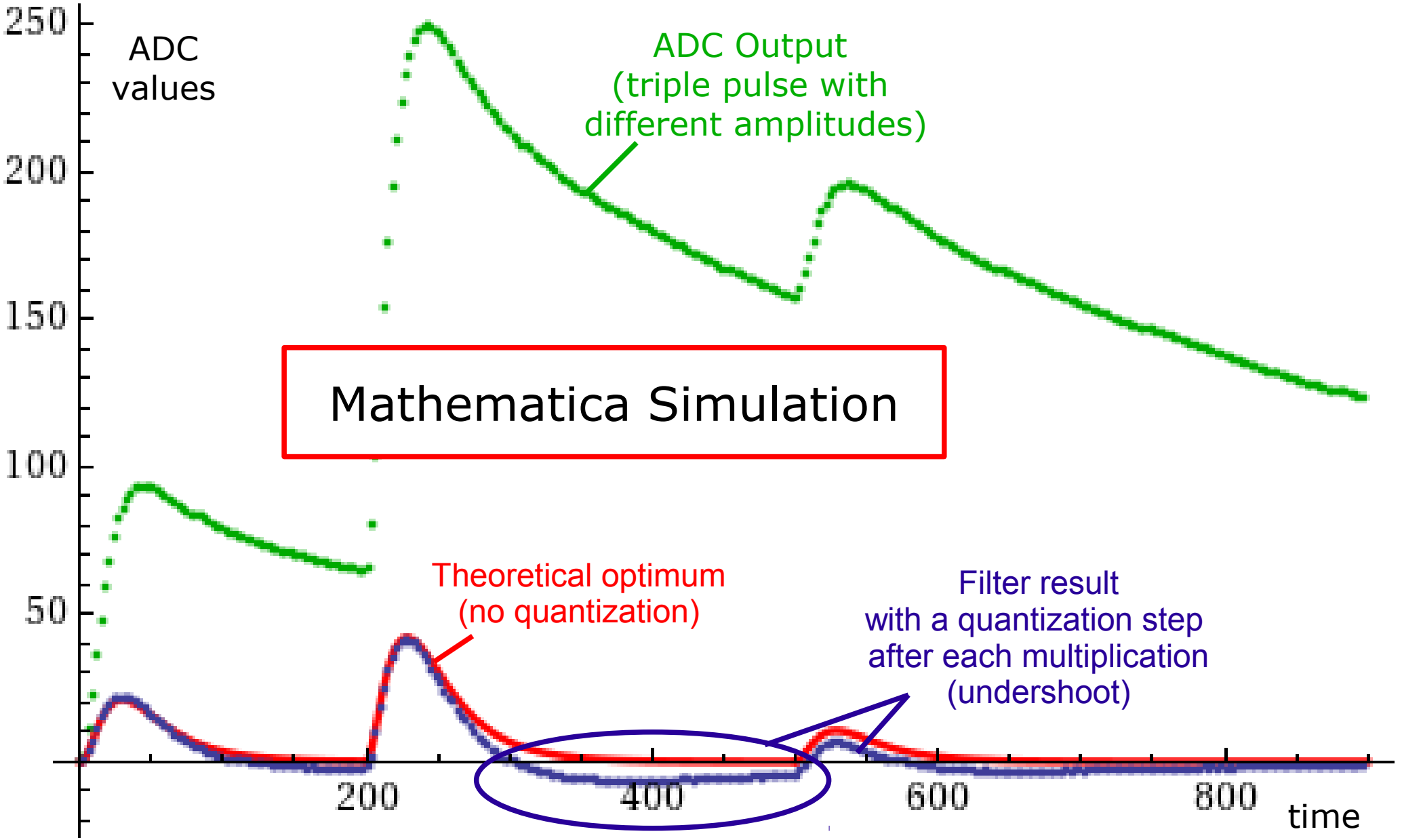
4. Digital Development

IIR Filter (Ion Tail Cancellation) Diagram

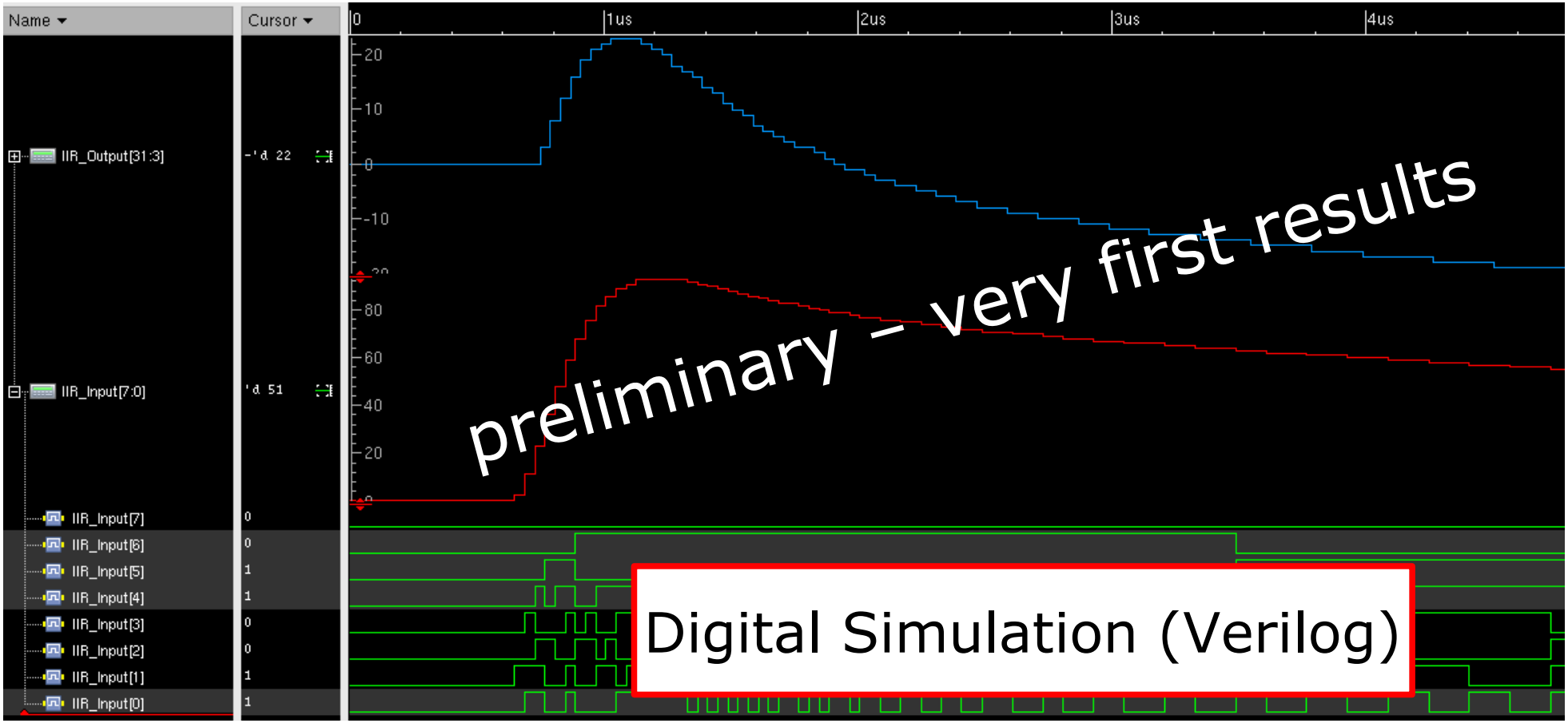
- Direct form 2
- 2nd order → compensation of two exponents
- Need at least 5 multipliers (complicated)
- Need 4 adders (simple)
- Need to find out proper internal resolution



Mathematica: IIR Filter (Ion Tail Cancellation)

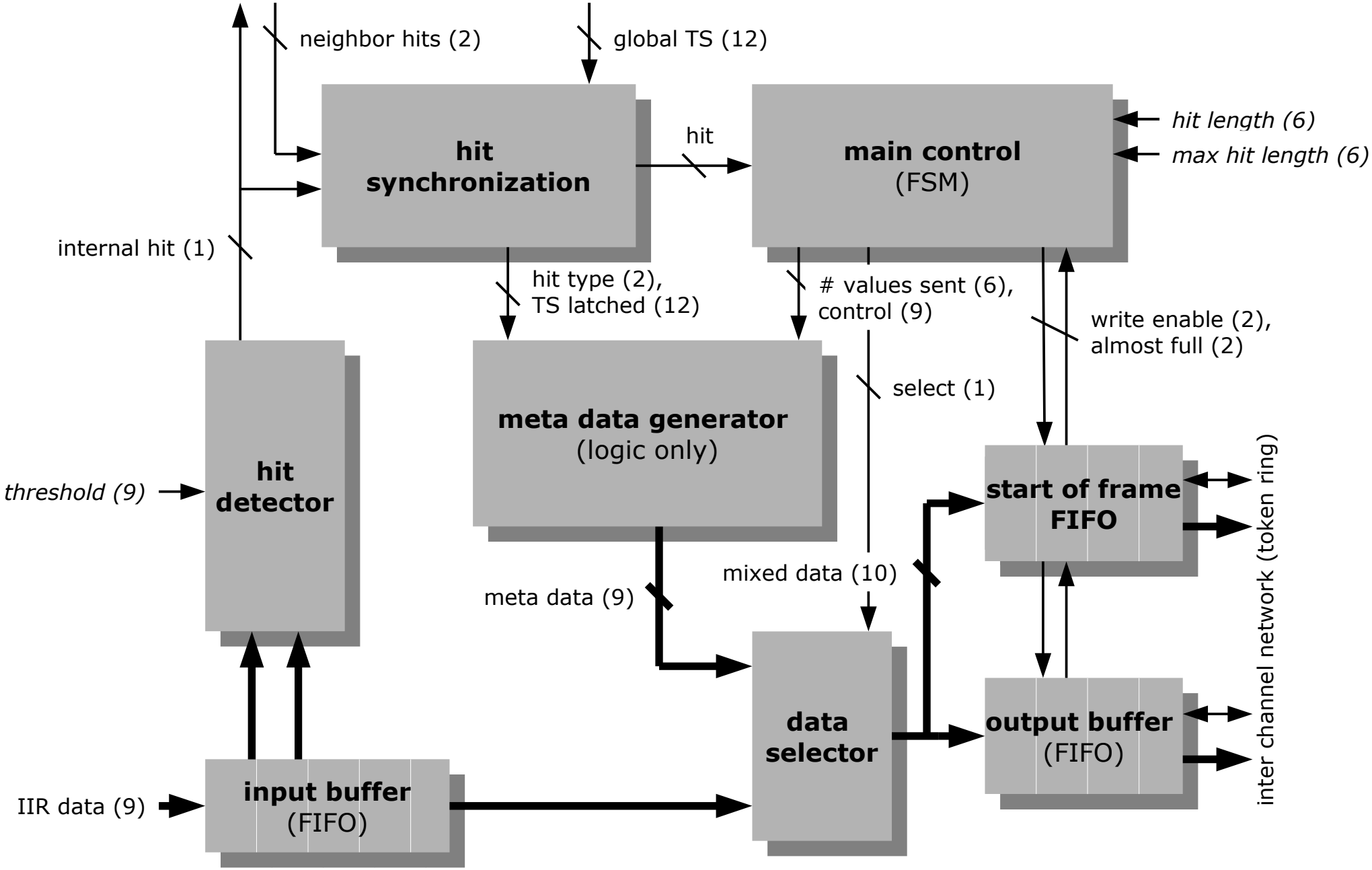


Digital Simulation: IIR Filter (Ion Tail Cancellation)

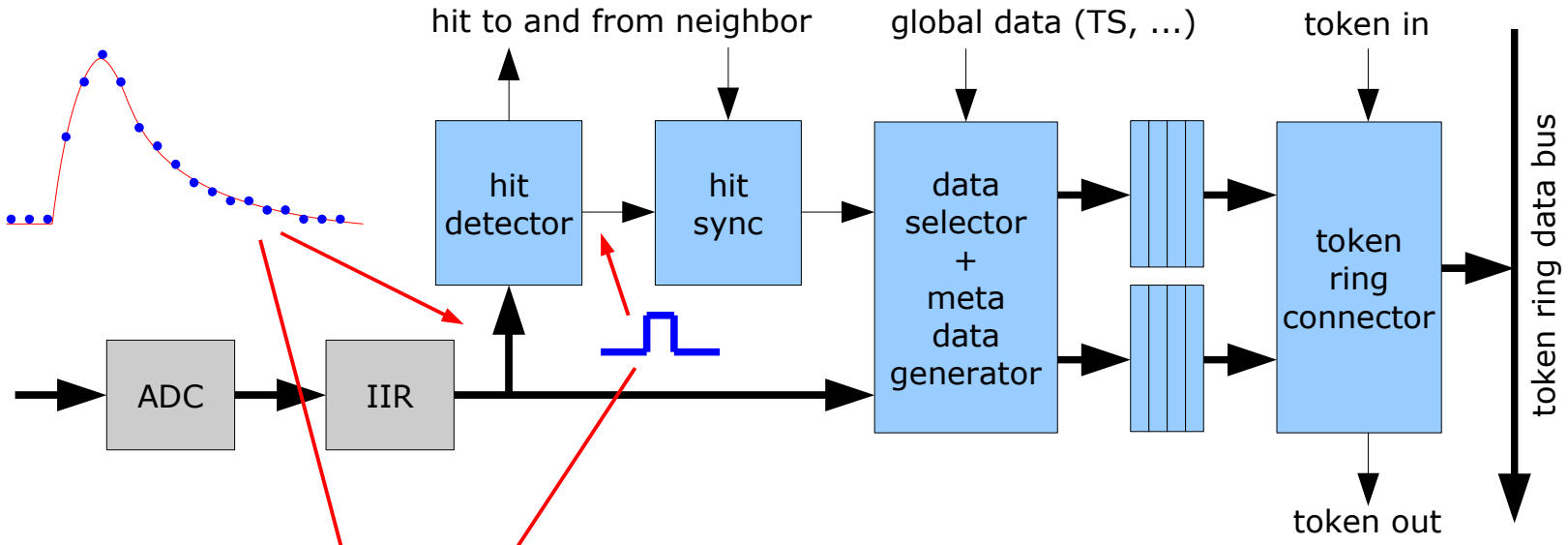


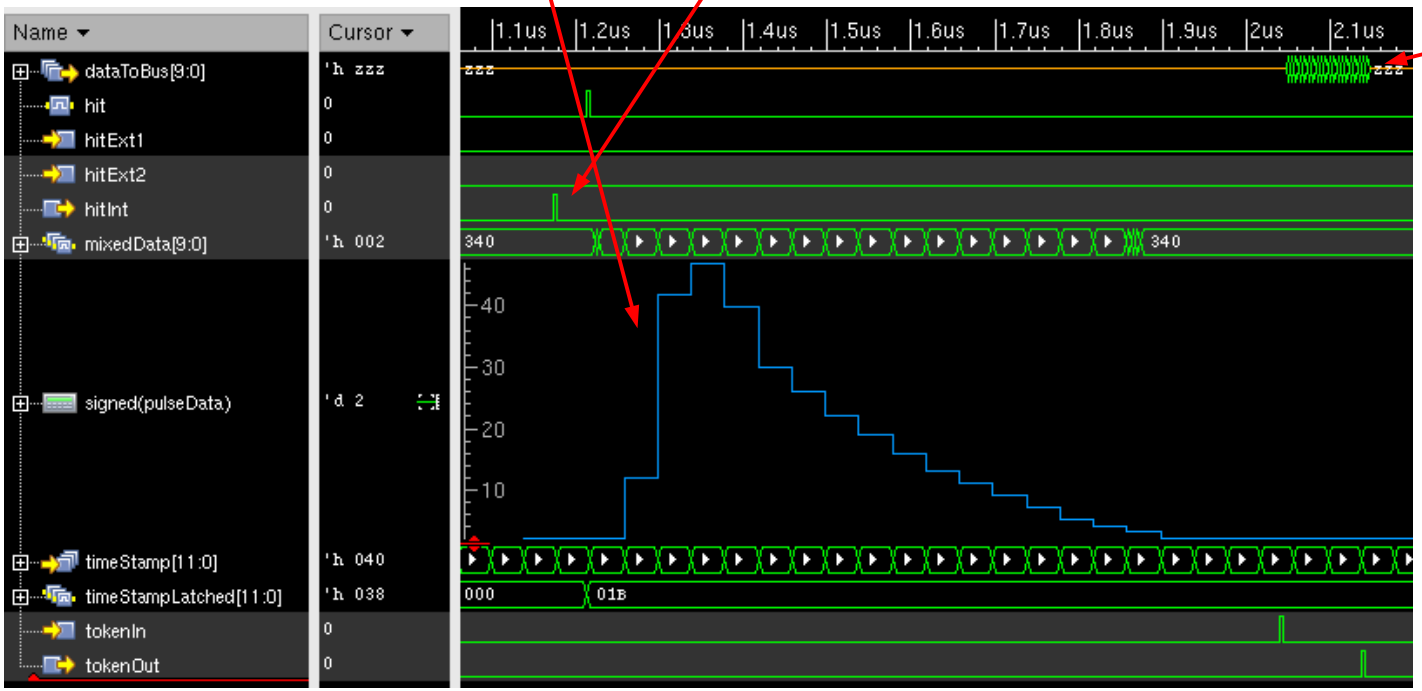
- RED: IIR filter input pulse with very long ion tail
- BLUE: IIR output after ion tail cancellation (preliminary results)
  - strong overcompensation, but probably due to quantization (compare to Mathematica results)
  - adjustment of filter factors should lead to better results

Digital Hit Detector and Package Builder



Example 1: Internal Hit

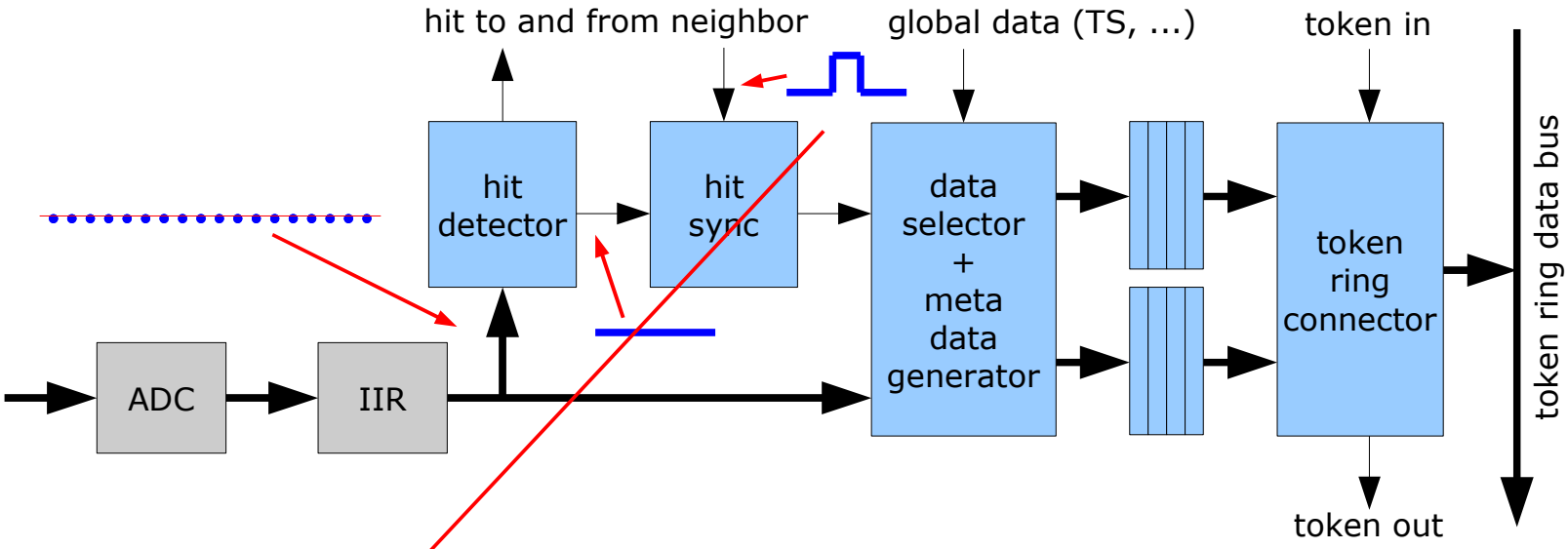


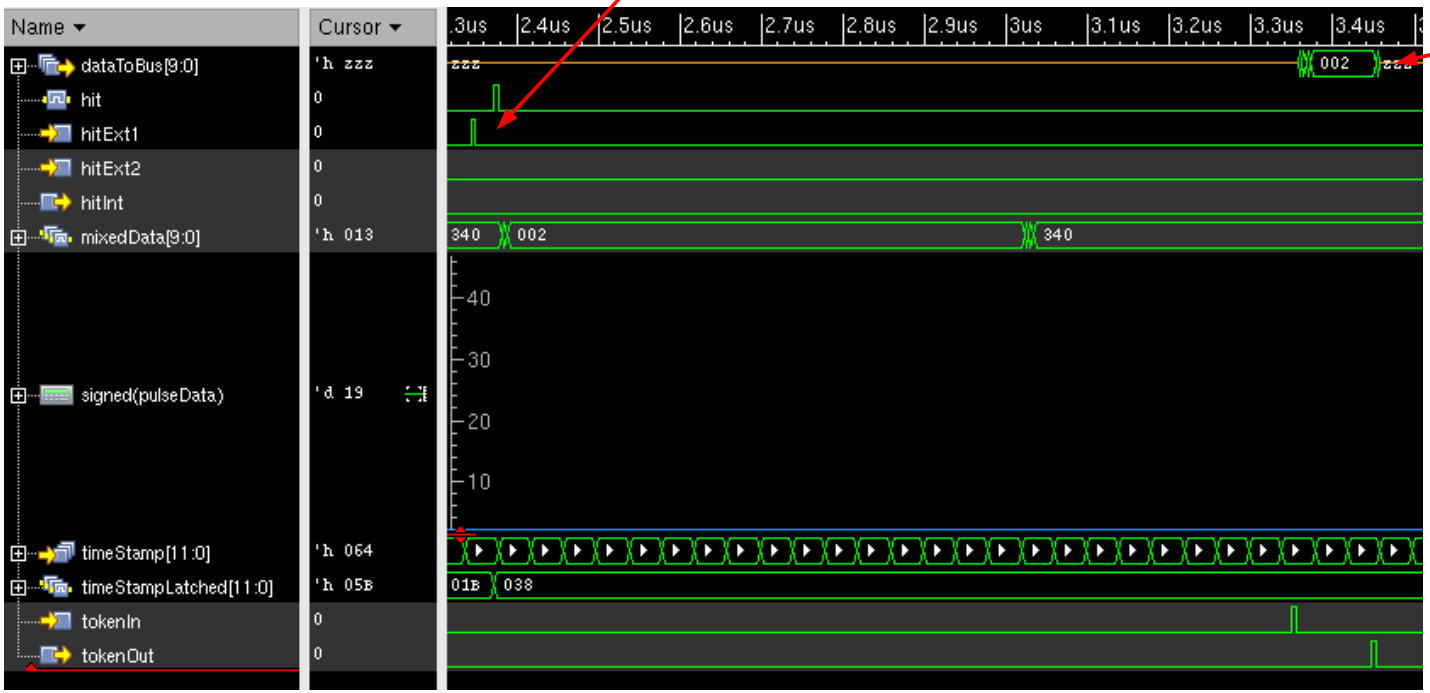


Token bus output package:

SOF: 16 data packages sent
TS1: 000000 (part 1)
TS2: 011011 (part 2)
DATA: 12
DATA: 42
DATA: 47
DATA: 40
DATA: 30
DATA: 26
[...]
DATA: 5
DATA: 4
DATA: 3
EOF: internal hit

Example 2: External Hit

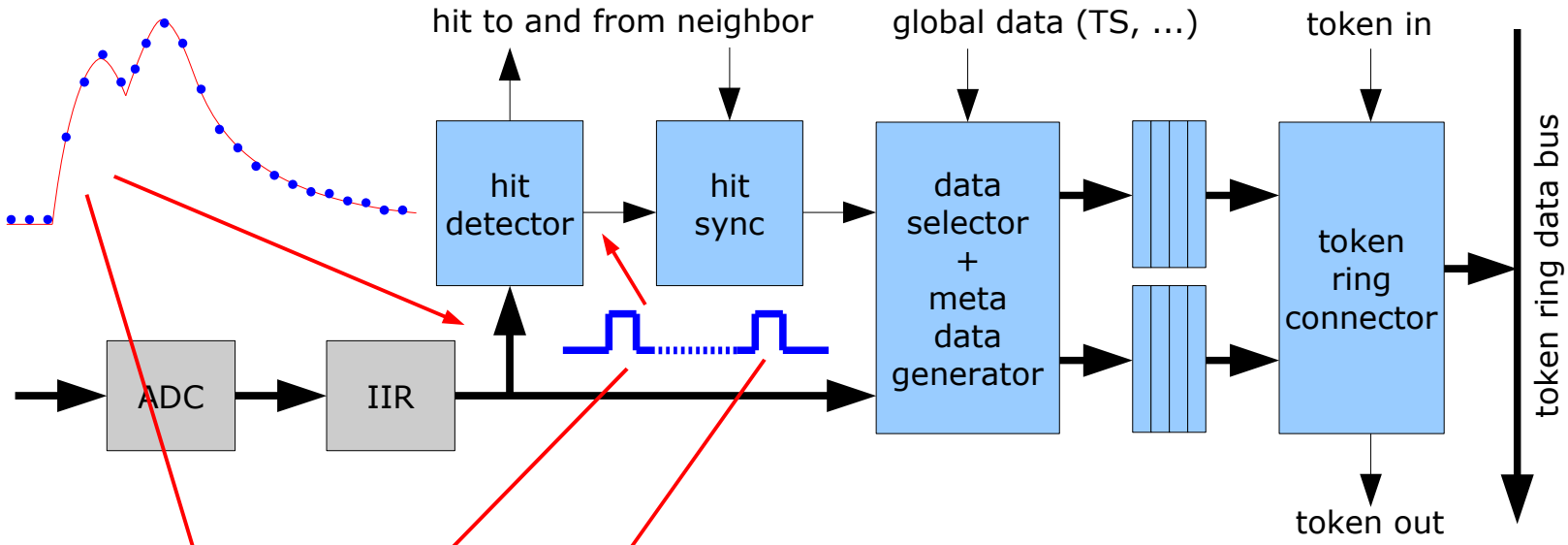


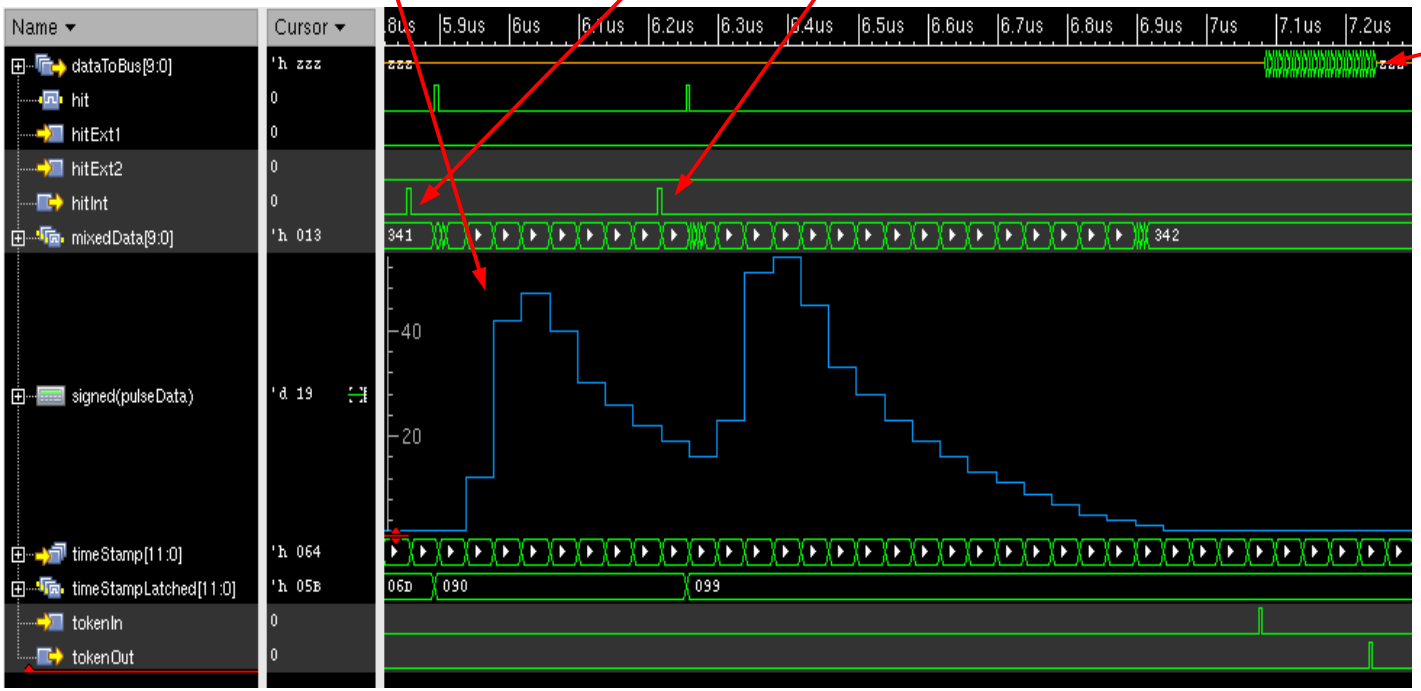


Token bus output package:

SOF: 16 data packages sent
TS1: 000000 (part 1)
TS2: 111000 (part 2)
DATA: 2
DATA: 2
DATA: 2
DATA: 2
DATA: 2
[...]
DATA: 2
DATA: 2
DATA: 2
DATA: 2
EOF: external hit

Example 3: Internal Double Hit





Token bus output package:

SOF: 25 data packages sent
TS1: 000010 (part 1)
TS2: 010000 (part 2)
DATA: 12
DATA: 42
[...]
DATA: 16 **"double hit marker"**
HTP: internal hit
TS1: 000010 (part 1)
TS2: 011001 (part 2)
DATA: 23
DATA: 51
[...]
DATA: 3
EOF: internal hit

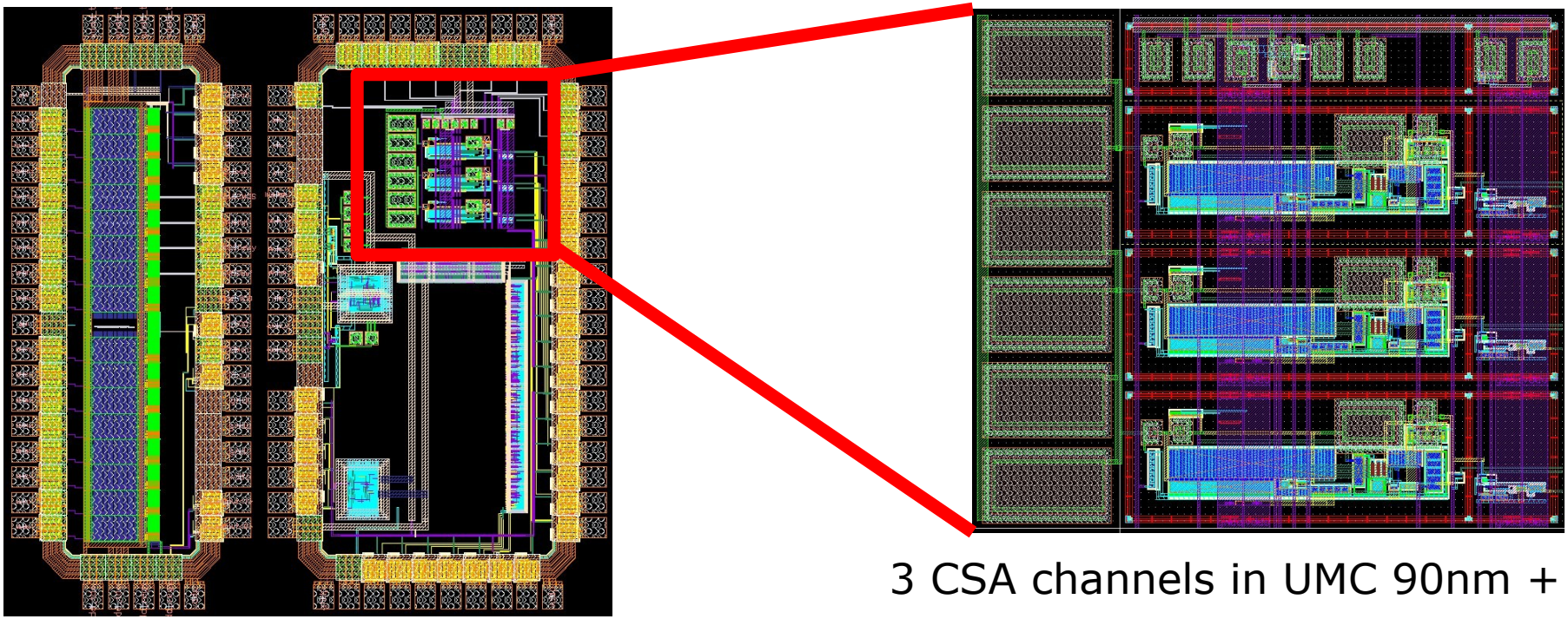
5. Excursion to UMC 90nm

CSA Submission in UMC 90nm

Motivation

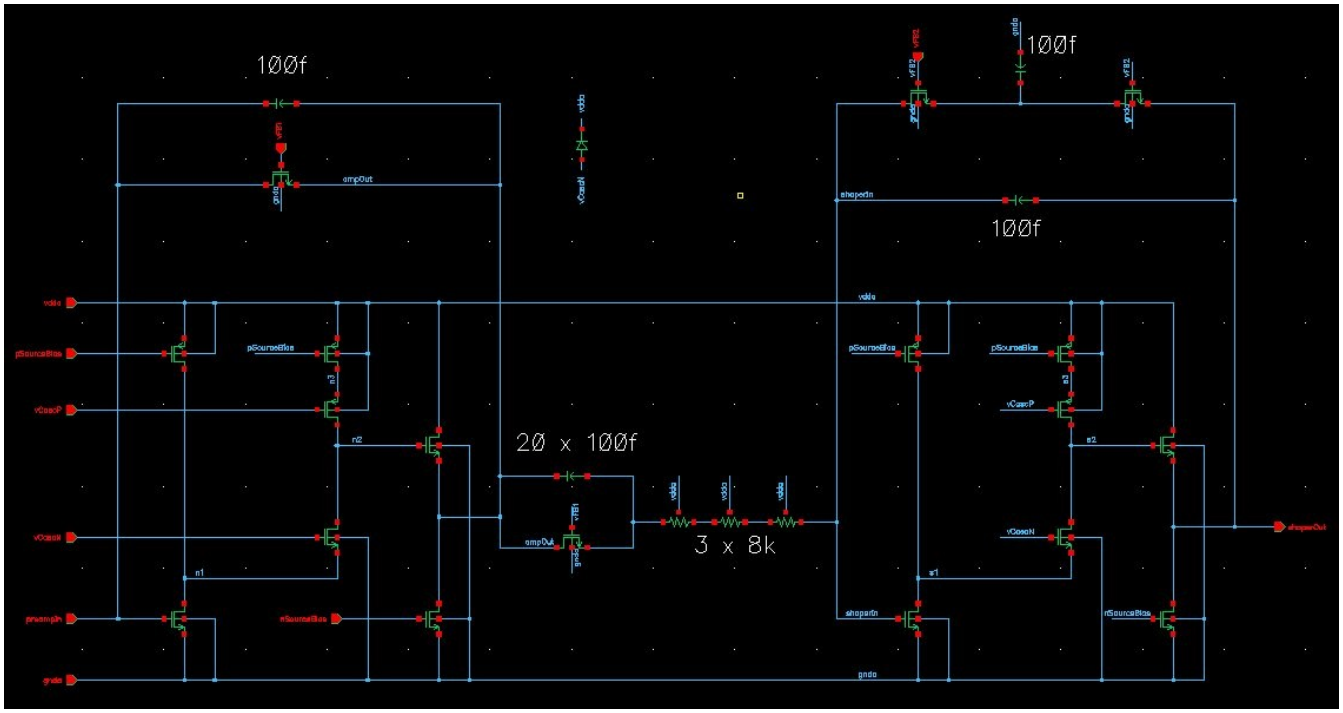
- UMC 90nm technology available via Europractice
- Still a lot of free space on our first 90nm multi-design test-chip (VCO, SRAM, CMOS-counter, …)
- Large deviation between measured and simulated noise in 180nm
- General discussion in analog design: 180nm vs. 90nm

=> Submission of a simple CSA design (preamp, shaper, discriminator) on March 22, 2010



3 CSA channels in UMC 90nm + Bias

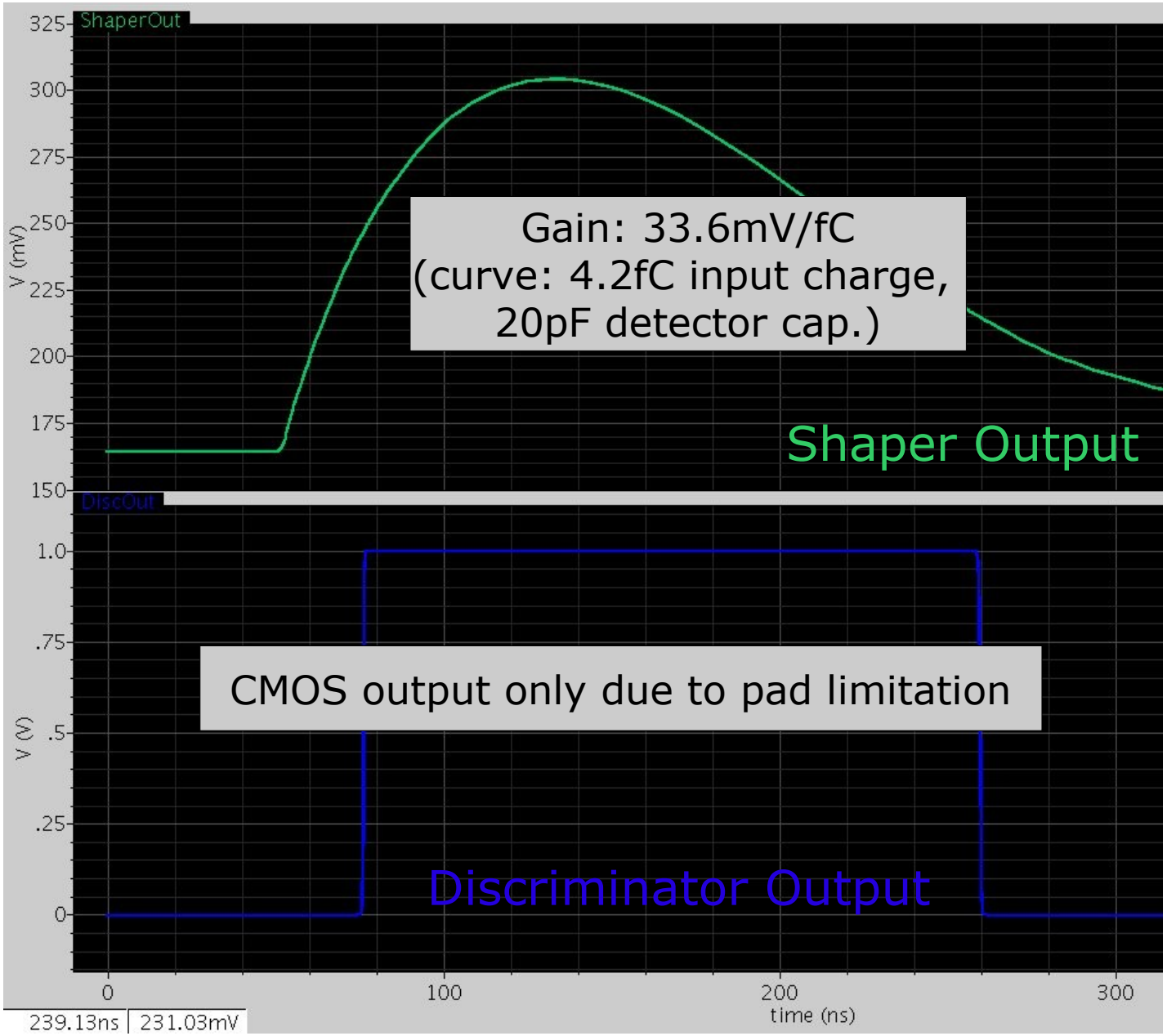
90nm CSA Characteristics



Characteristics from simulation

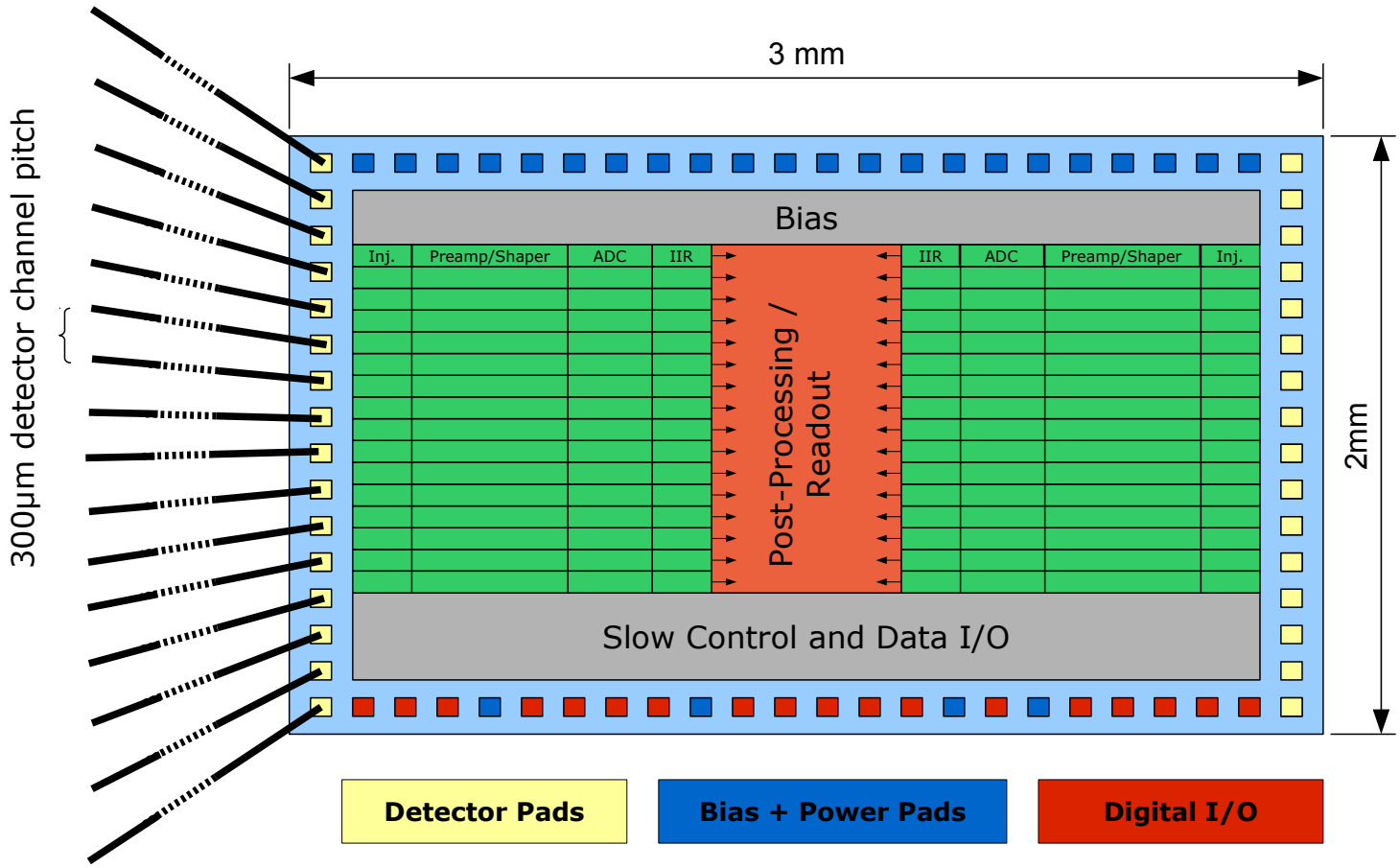
- 3 channels with on-die detector capacitors (0pF, 12.6pF, 25.2pF)
- NMOS input, O'Connor feedback, 2nd order shaper
- Peaking-Time: 83ns, Rise-Time: 47ns
- Power consumption: 2.3mW (VDD 1.0V)
- Noise: 377e @ 20pF
- Note: no optimization, minimum on-chip bias circuitry, 5 days of work for the whole design

90nm CSA Shaper Output Pulse



6. Future Plans and Summary

Floor Plan Proposal



- 3 x 2 mm² estimated die size
- 32 channels, 40-80µm pitch, (mostly) symmetric layout, low(er) IR-drops
- Detector connection-pads on two sides (chips will probably be attached to back of detector-module, this relaxes routing/spacing)

Summary

Status of analog chip design:

- Measurement results so far promising
- Further tests still have to be done (find optimal settings, test ESD pads, connect CSAs to ADCs, ...)

Status of digital channel back-end design:

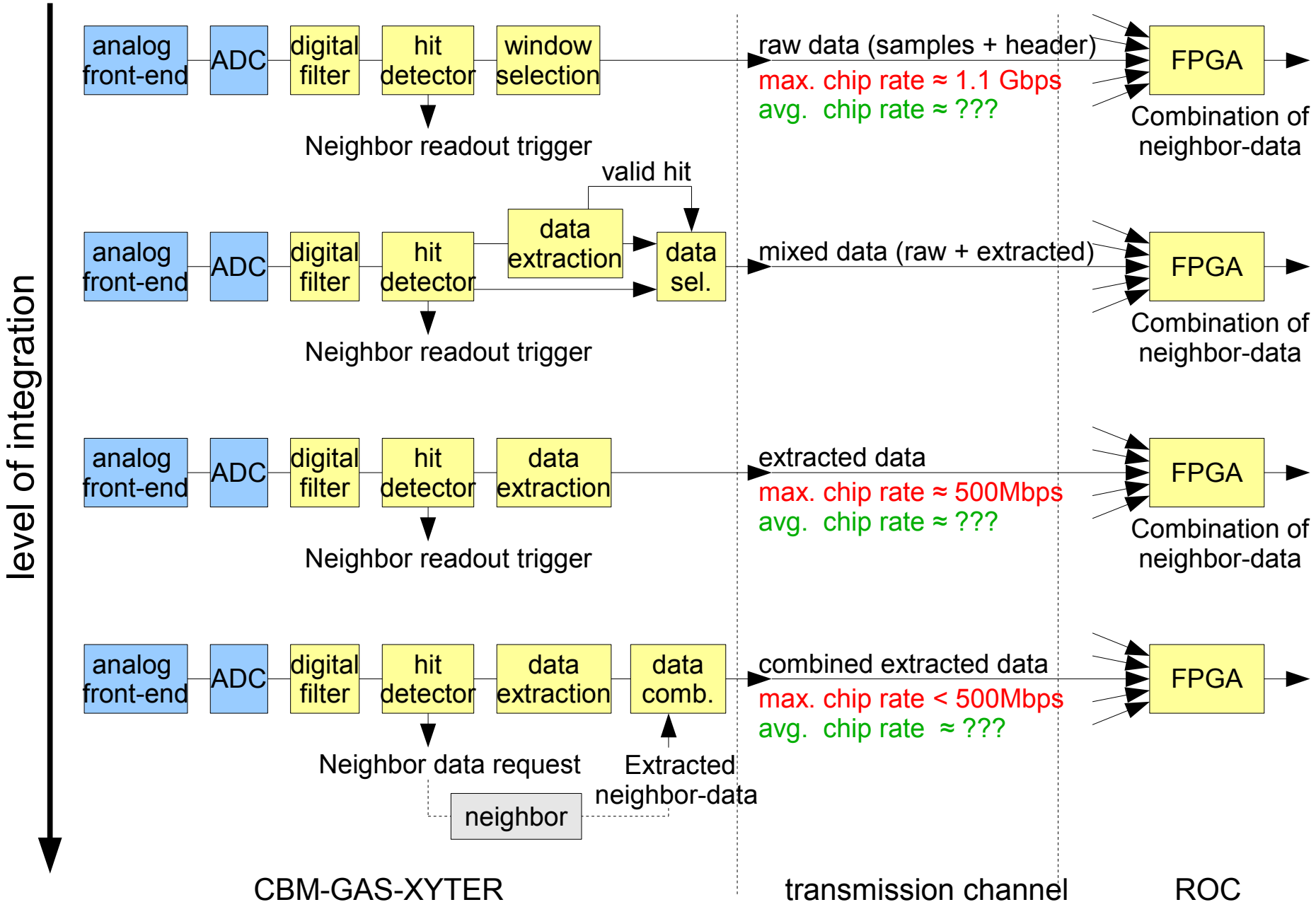
- First design proposal of digital back-end completed
- Good simulation results, ongoing development of larger verification environment
- Large construction site: IIR filter (good topic for a diploma thesis)

Next Steps:

- Complete chip measurement
- Connect chip to some gas-chamber (e.g. from Frankfurt)
- Start tests of digital channel back-end on some FPGA board
- Maybe submit a completely digital test-ASIC
- Do first steps towards the CBM-GAS-XYTER design (layout concept, ...)
- Find a better name for CBM-GAS-XYTER

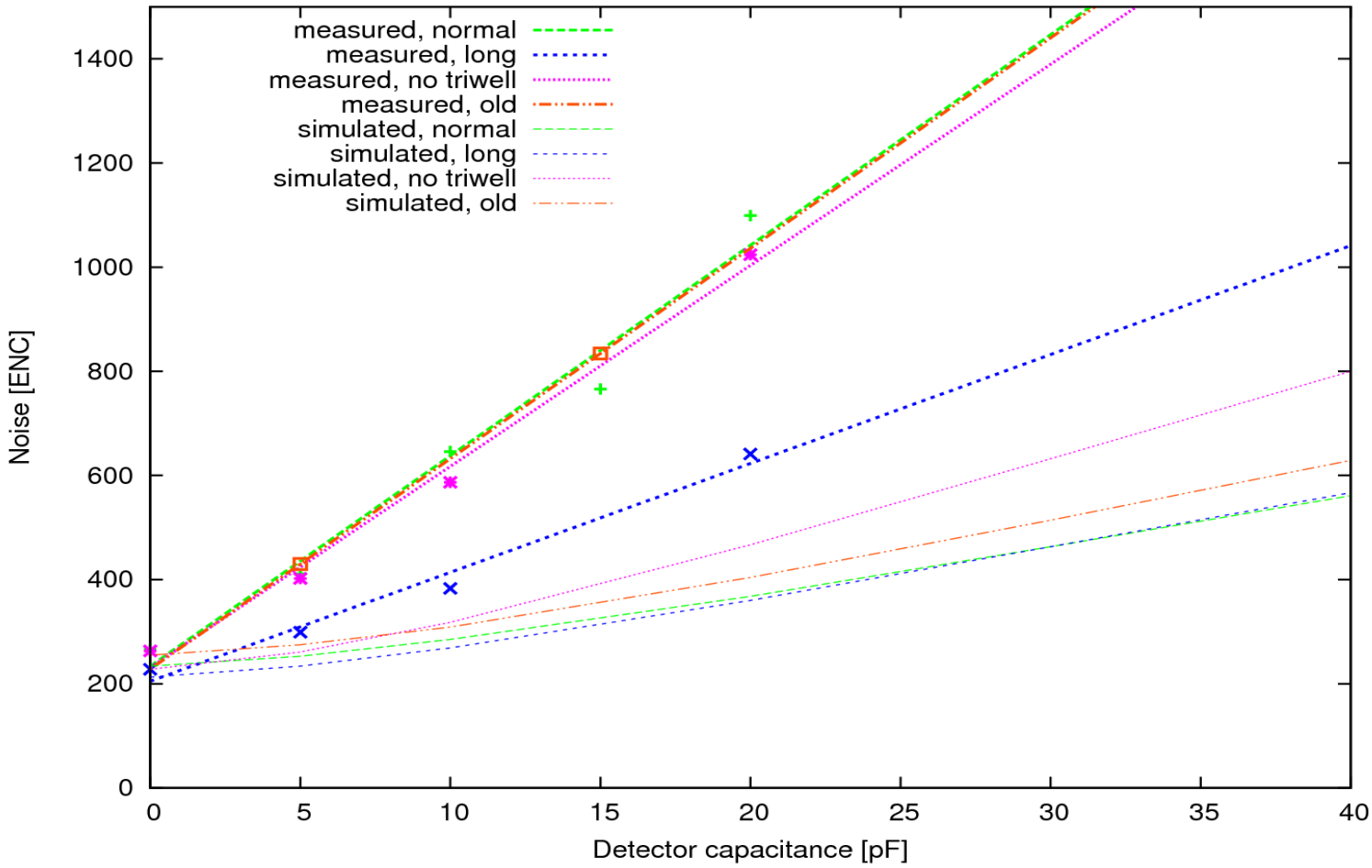
Thank you!

Raw Data vs. Extracted Data: System Options



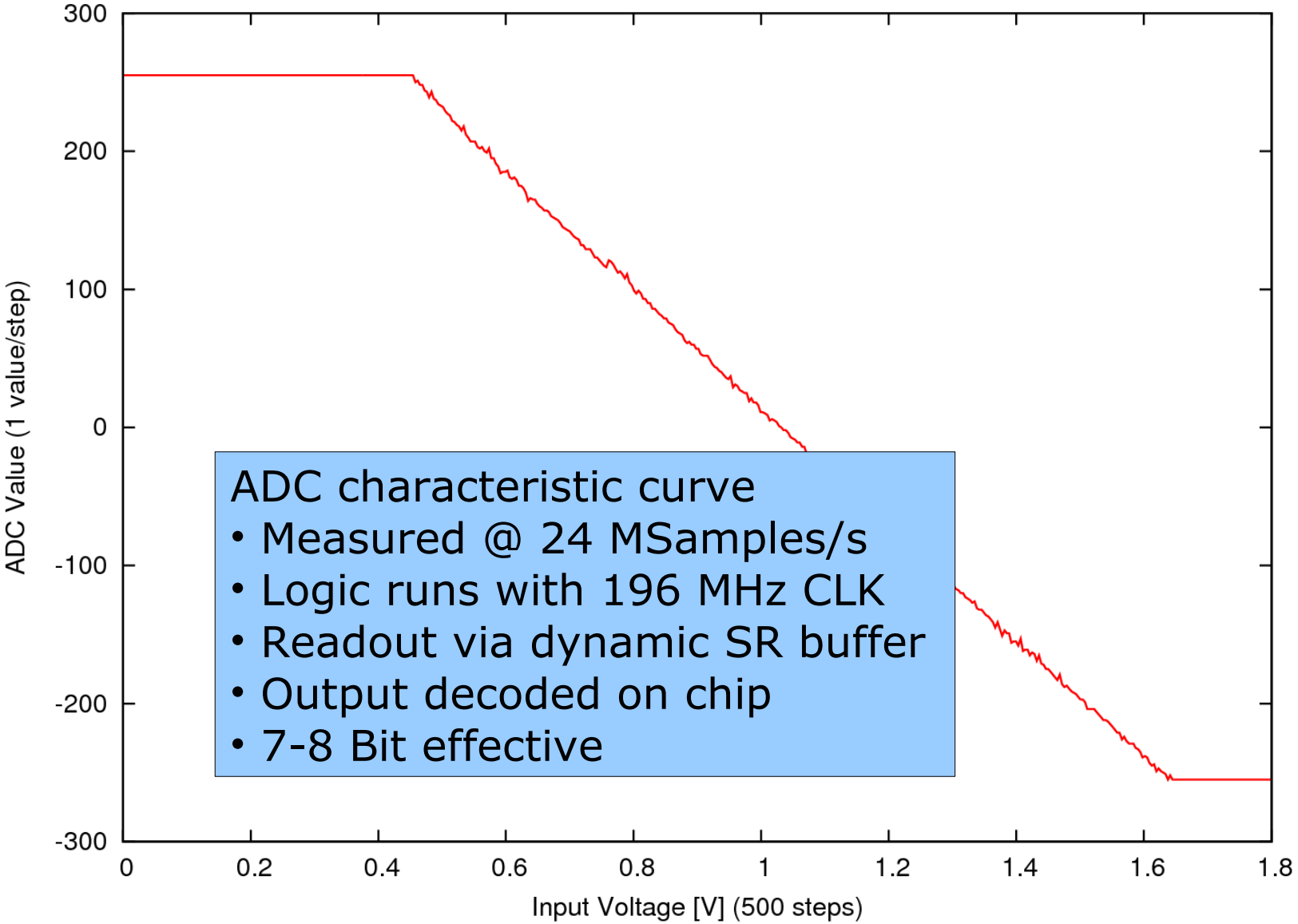
Chip: Preamp/Shaper Results

- Noise was measured with s-curve scans using the discriminator
- Injection capacitor calibrated via test circuit
- 4 different preamplifier types: old, normal, no triwell, long



- Results:
  - Noise values of normal (triwell NMOS input, minimal length) and no triwell (NMOS without triwell, minimal length) channel show no significant difference compared to the old channel => values still much worse than simulated
  - Noise slope of long (triwell NMOS input, 320 nm length) channel about two-times smaller => **about 800 e ENC @ 30 pF** achievable, still worse than in simulation

Chip: ADC Results



ADC characteristic curve
- Measured @ 24 MSamples/s
- Logic runs with 196 MHz CLK
- Readout via dynamic SR buffer
- Output decoded on chip
- 7-8 Bit effective