UNIVERSITÄT HEIDELBERG

# SPADIC v0.3 and v1.0

**S**elf-triggered **P**ulse **A**mplification and **D**igitization as**IC**


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FEE/DAQ Meeting @ FIAS (Frankfurt)

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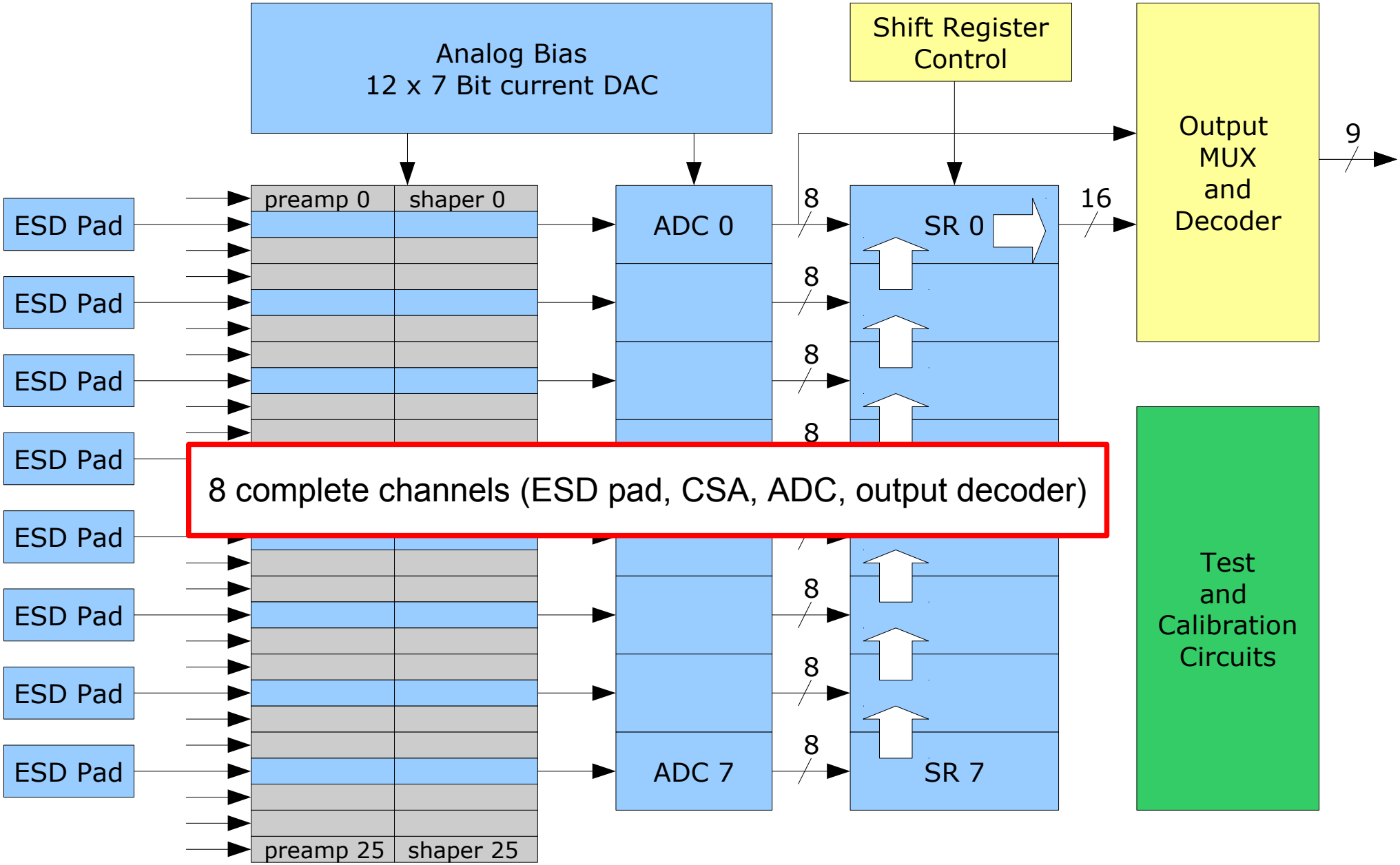
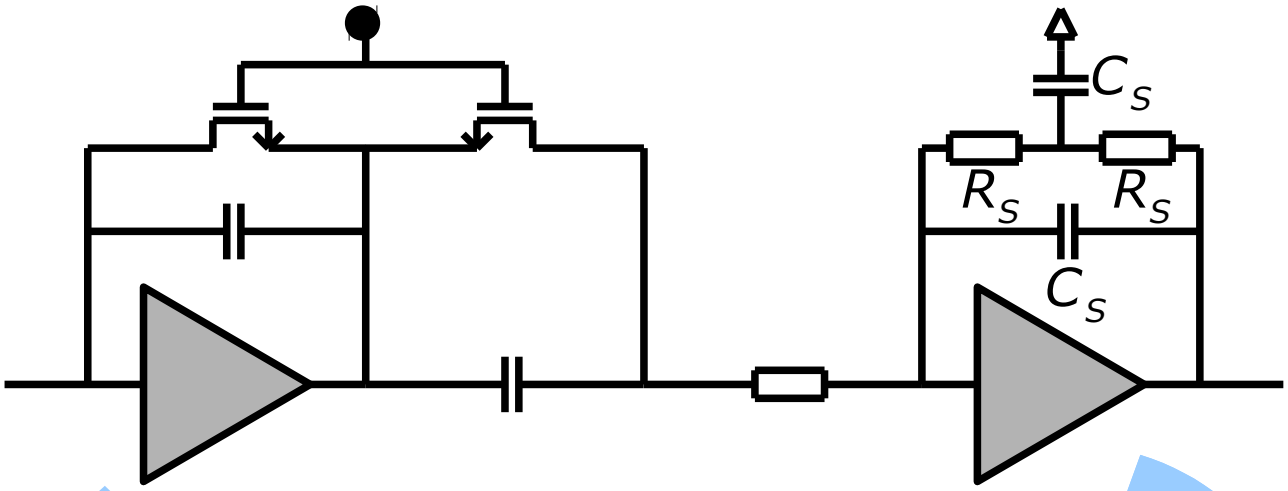
# 1. Latest Chip Architecture (v0.3)

# Block Diagram of Current ASIC



# Reminder: Preamplifier/Shaper Circuit



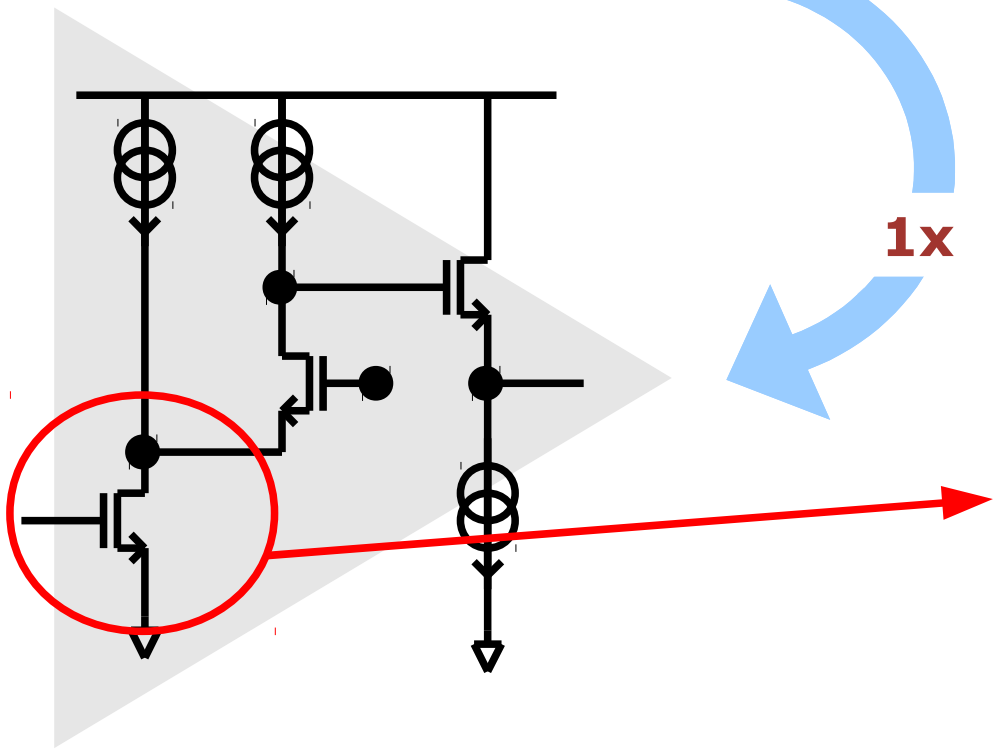

$$H(s) \approx \frac{A_{DC}}{(1+sR_sC_s)^2}$$

- O'Connor FB
- 2nd order shaper
- Shaping time: 82 ns
- Unified amplifier cell
- N-MOS input
- ≈ 3.6 mW/channel

**11x**

(also channels with less instances for test purpose on chip)

**1x**

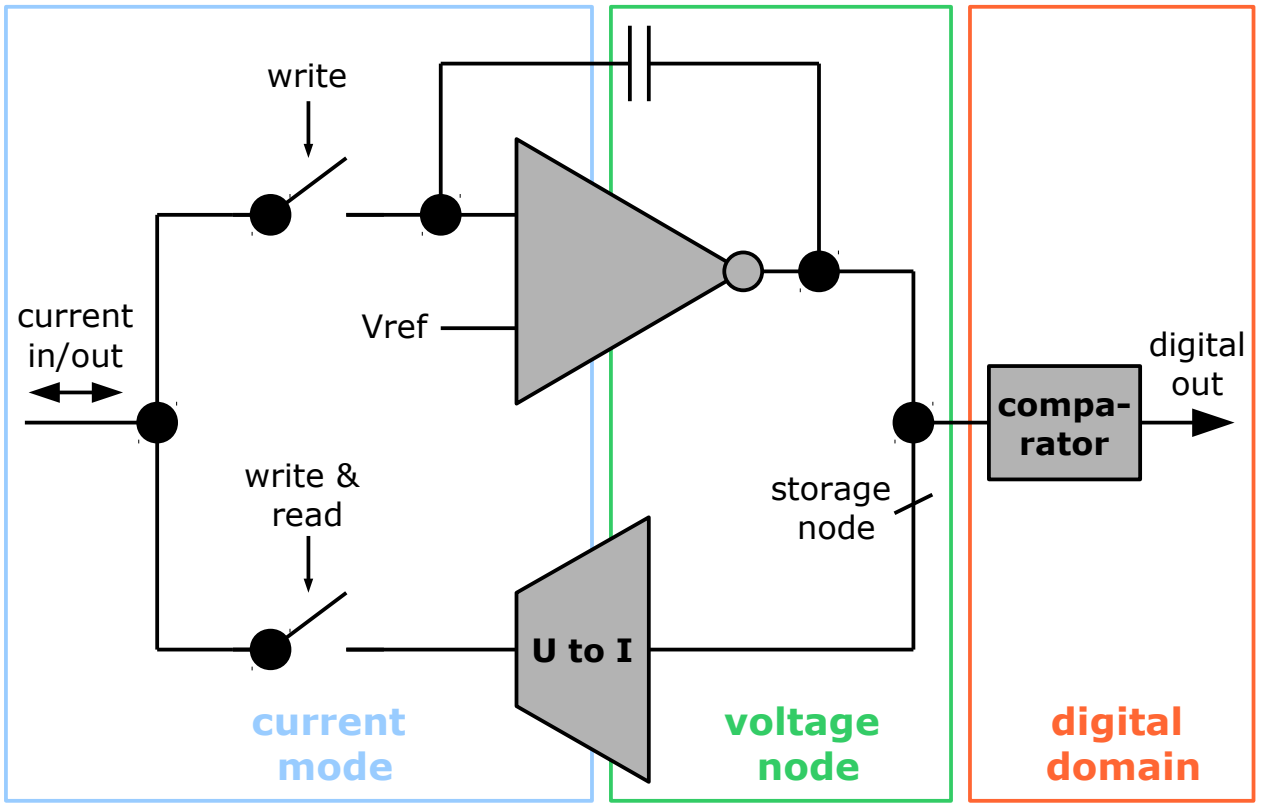


New:

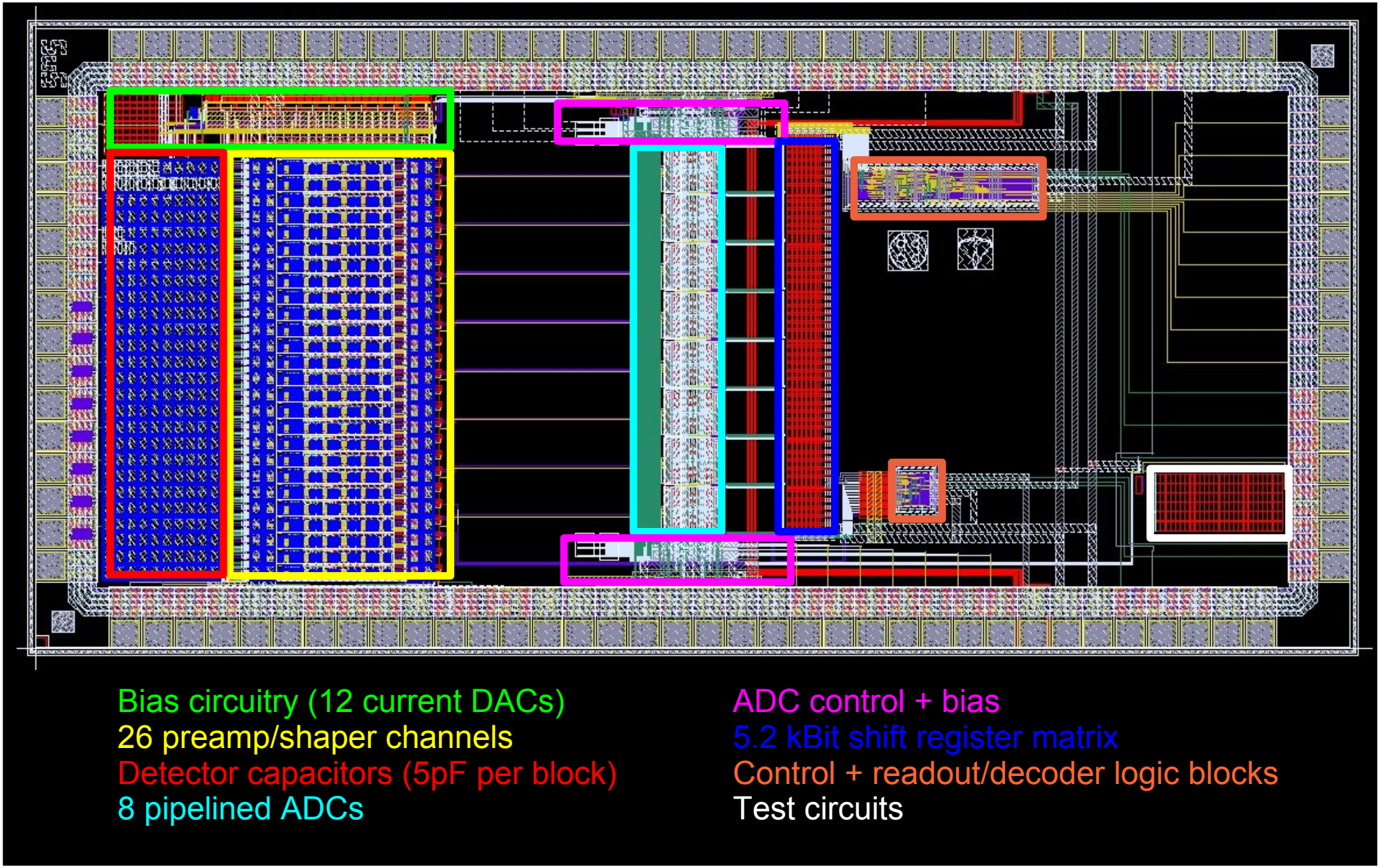
- Scaled lengths of input NMOS (180, 250, 320, 390, 460nm)
- Re-Layout of input NMOS: The (long) gate-fingers have been cut into smaller pieces to decrease gate resistance

# Reminder: Algorithmic ADC Design

- 8 (scaled) pipeline stages, therefore 9 Bit design, **7.5 Bits effective** so far
- Algorithmic working principle ("1.5 redundant Bits" / conversion step)
- **25 MSamples/s, layout only 130x120 µm², power consumption 4.5 mW**
- Core unit: Novel current storage cell:



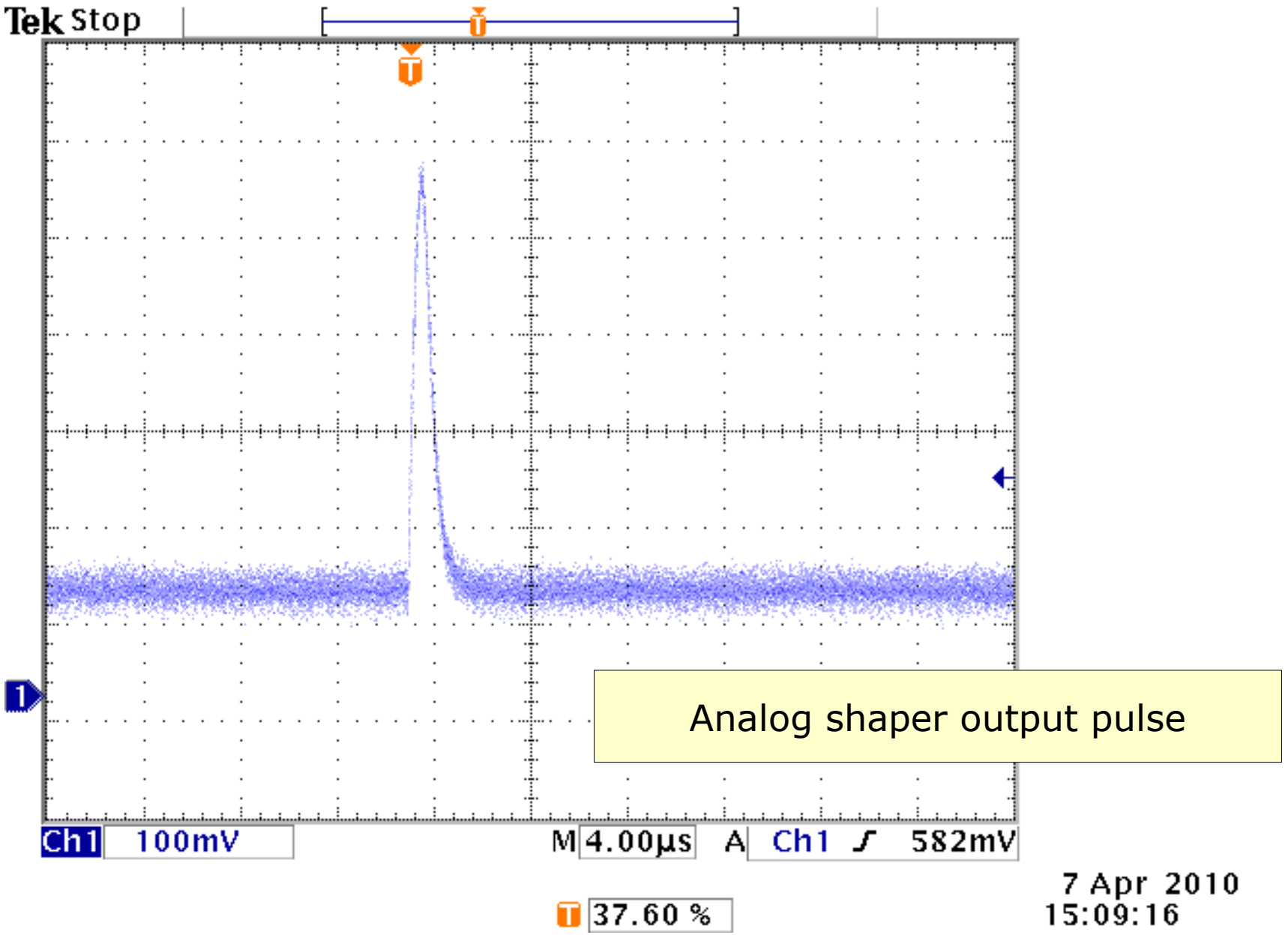
# Current Test-Chip: Layout



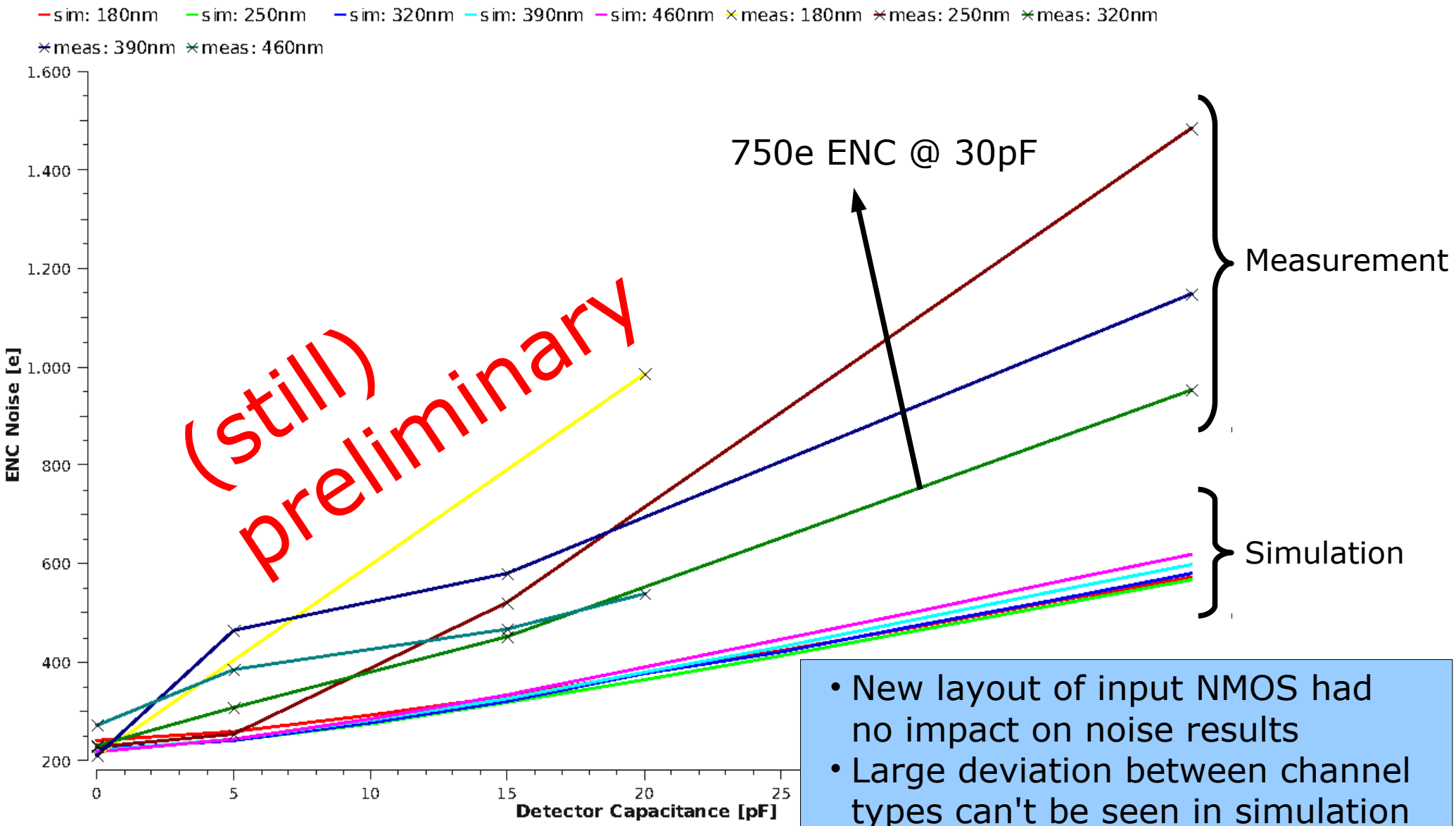
Bias circuitry (12 current DACs)
26 preamp/shaper channels
Detector capacitors (5pF per block)
8 pipelined ADCs

ADC control + bias
5.2 kBit shift register matrix
Control + readout/decoder logic blocks
Test circuits

# Typical Analog Shaper Pulse

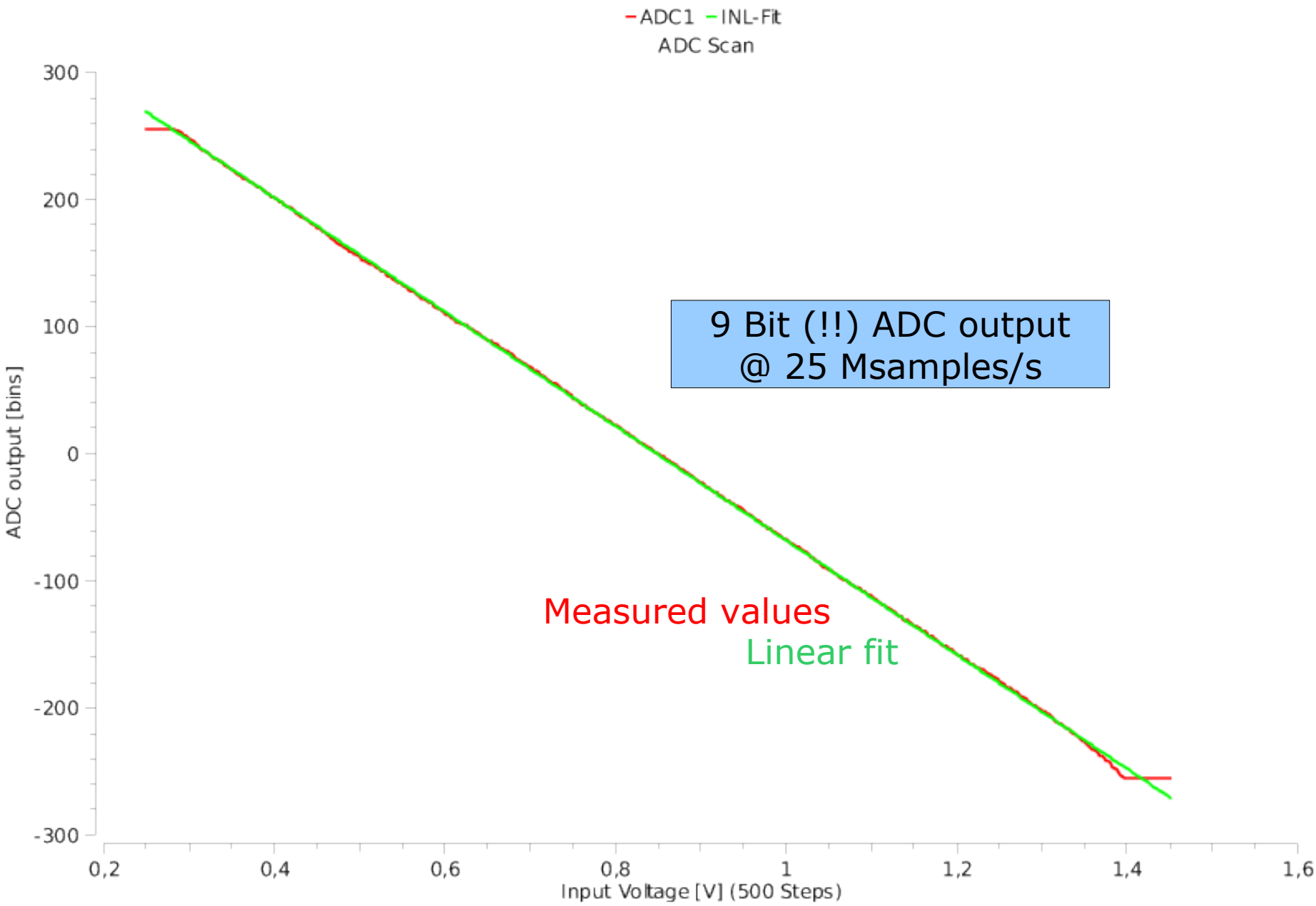


# Preamp/Shaper Noise

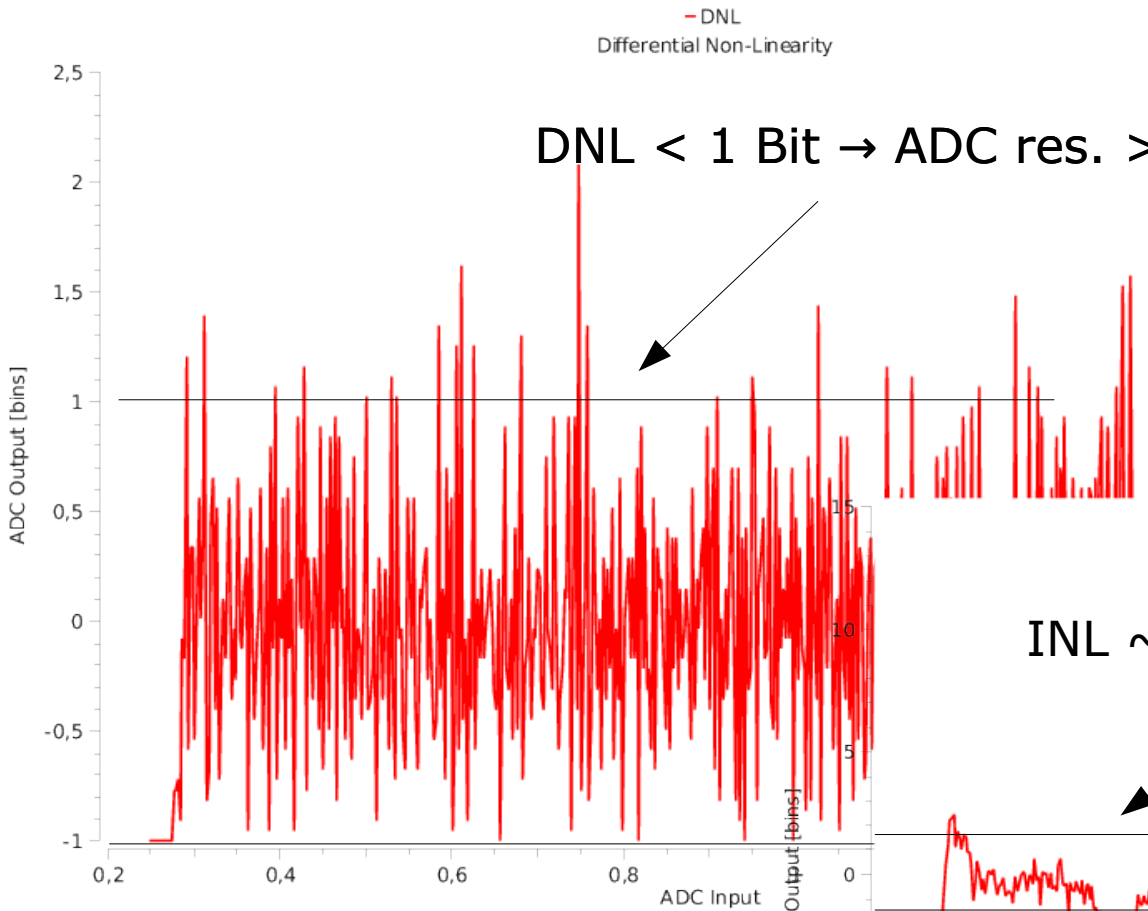



- New layout of input NMOS had no impact on noise results
- Large deviation between channel types can't be seen in simulation
- 320nm is the best choice

# Characteristic ADC Curve

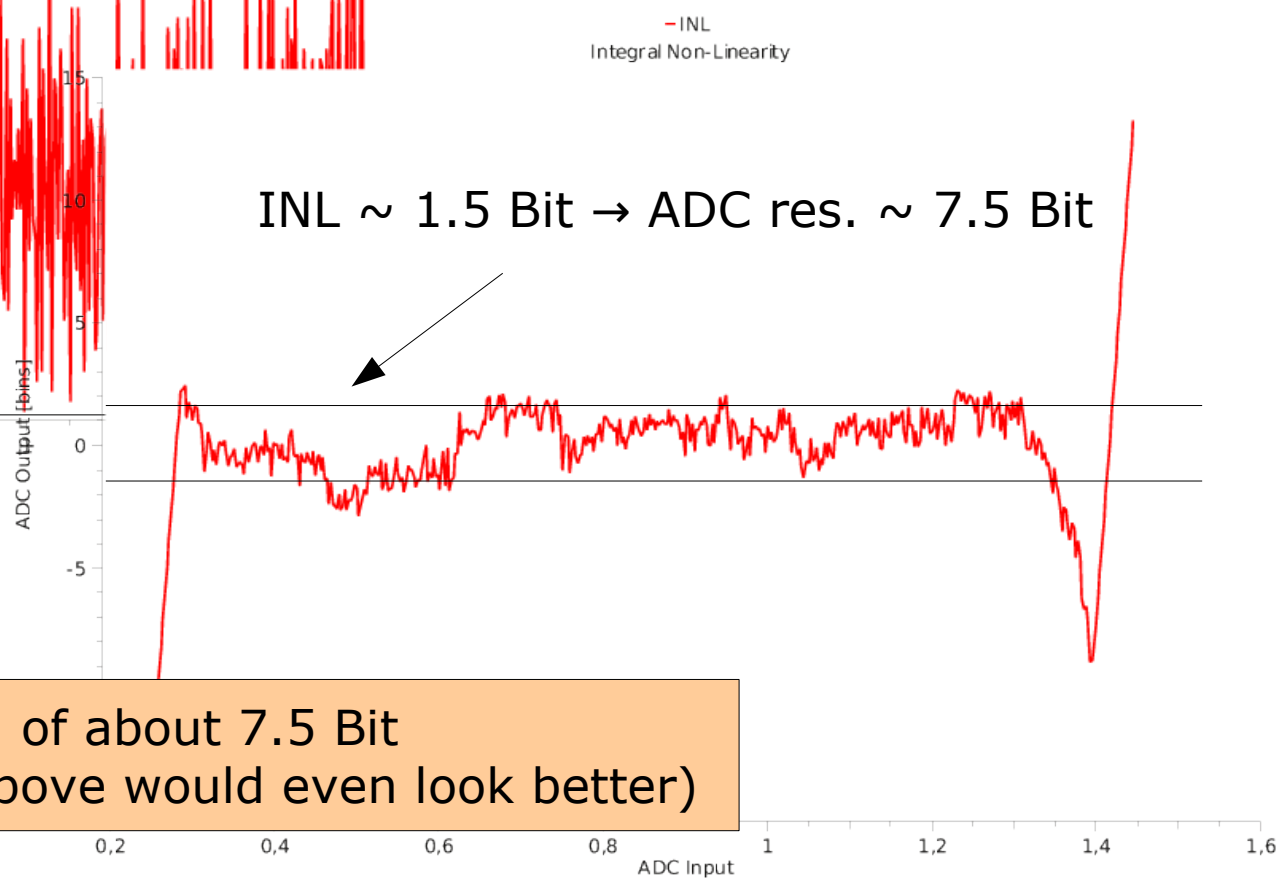


# ADC's DNL and INL




DNL < 1 Bit → ADC res. > 8 Bit

@ 25 Msamples/s
(40 ns sample period)

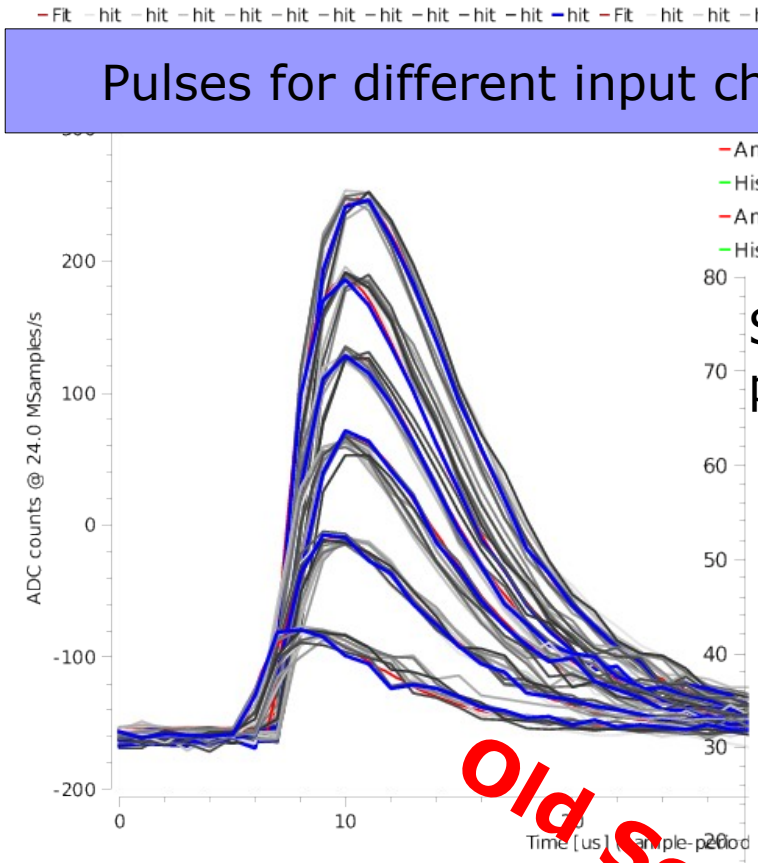



INL ~ 1.5 Bit → ADC res. ~ 7.5 Bit

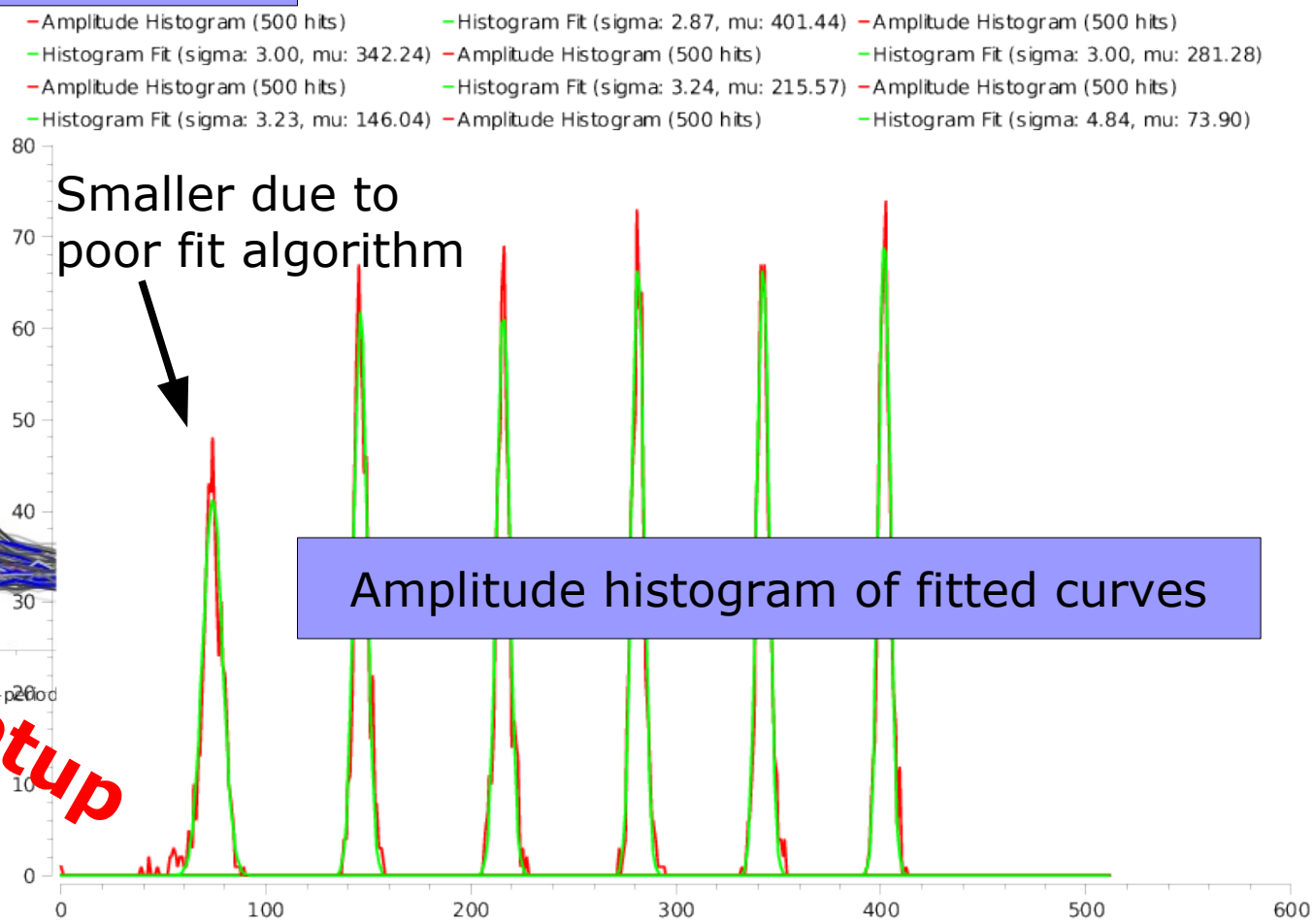
Current ADC resolution of about 7.5 Bit
(In sigma the values above would even look better)

# First (yet noisy) digitized pulses

Pulses for different input charges



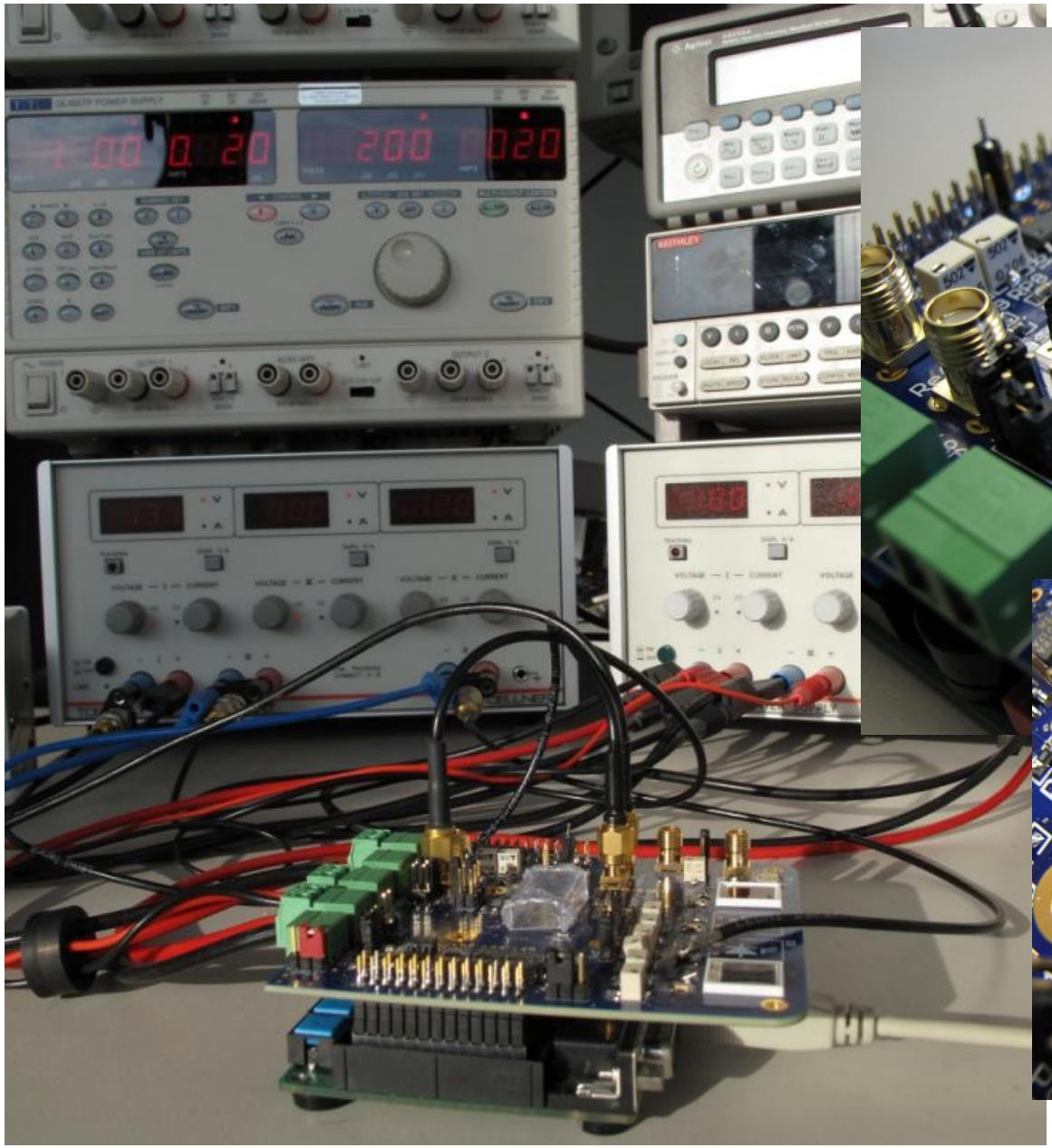

Smaller due to poor fit algorithm

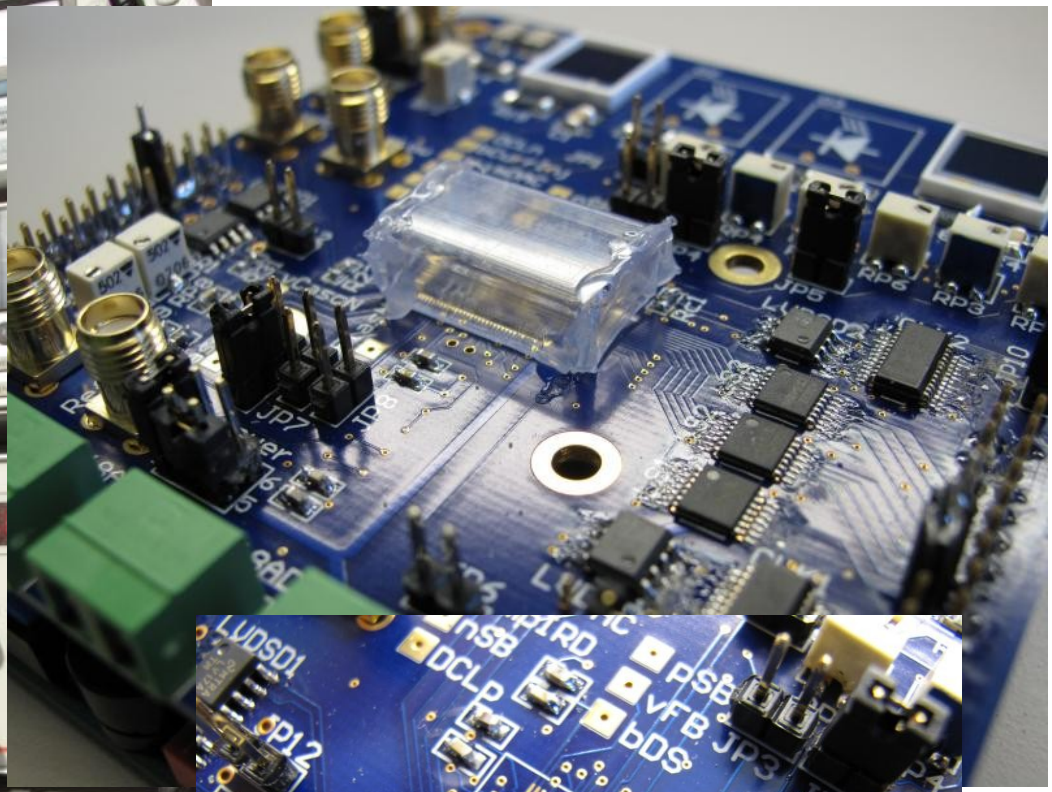


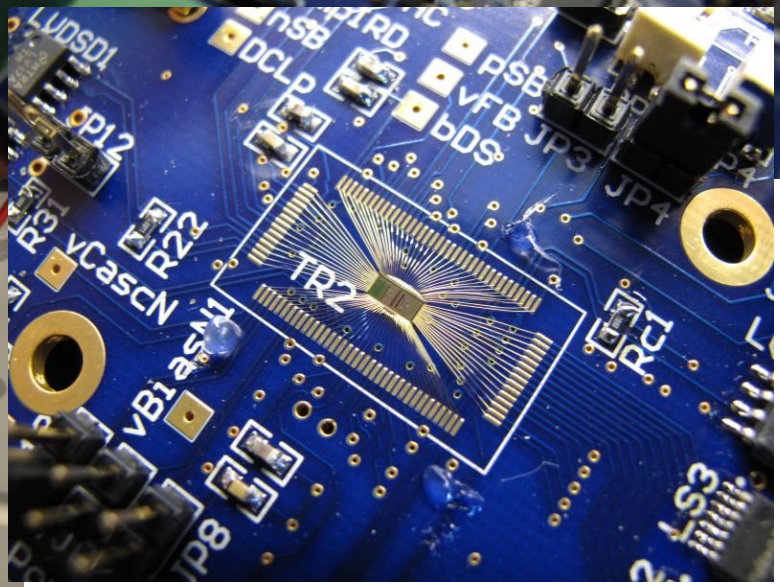

Amplitude histogram of fitted curves

**Pulses with new setup look even much smoother (see next slides), but no measurement available yet :-(**

# (Old) Pre-Testbeam Setup





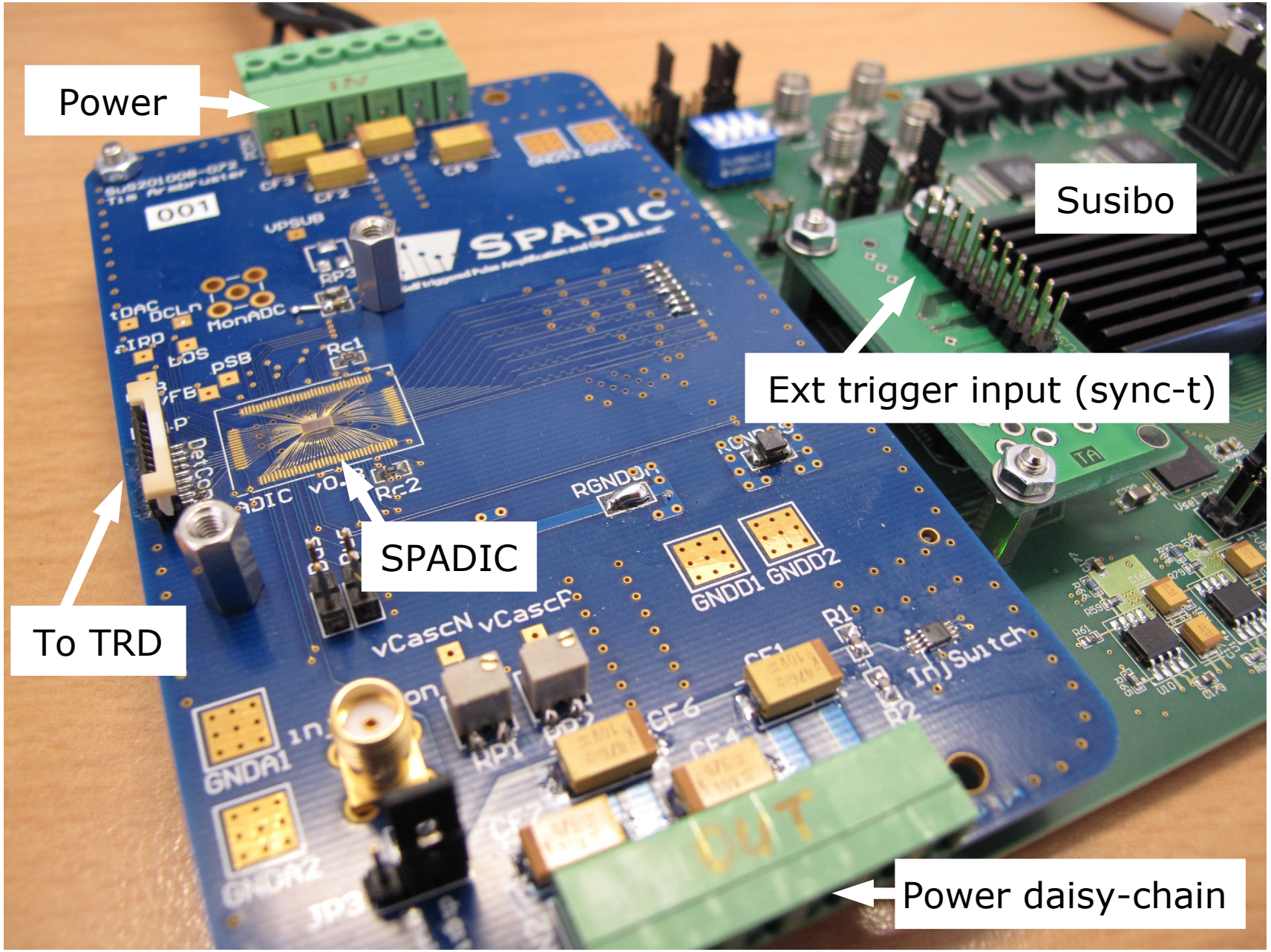
# 2. Testbeam Setup

# Testbeam Setup Overview

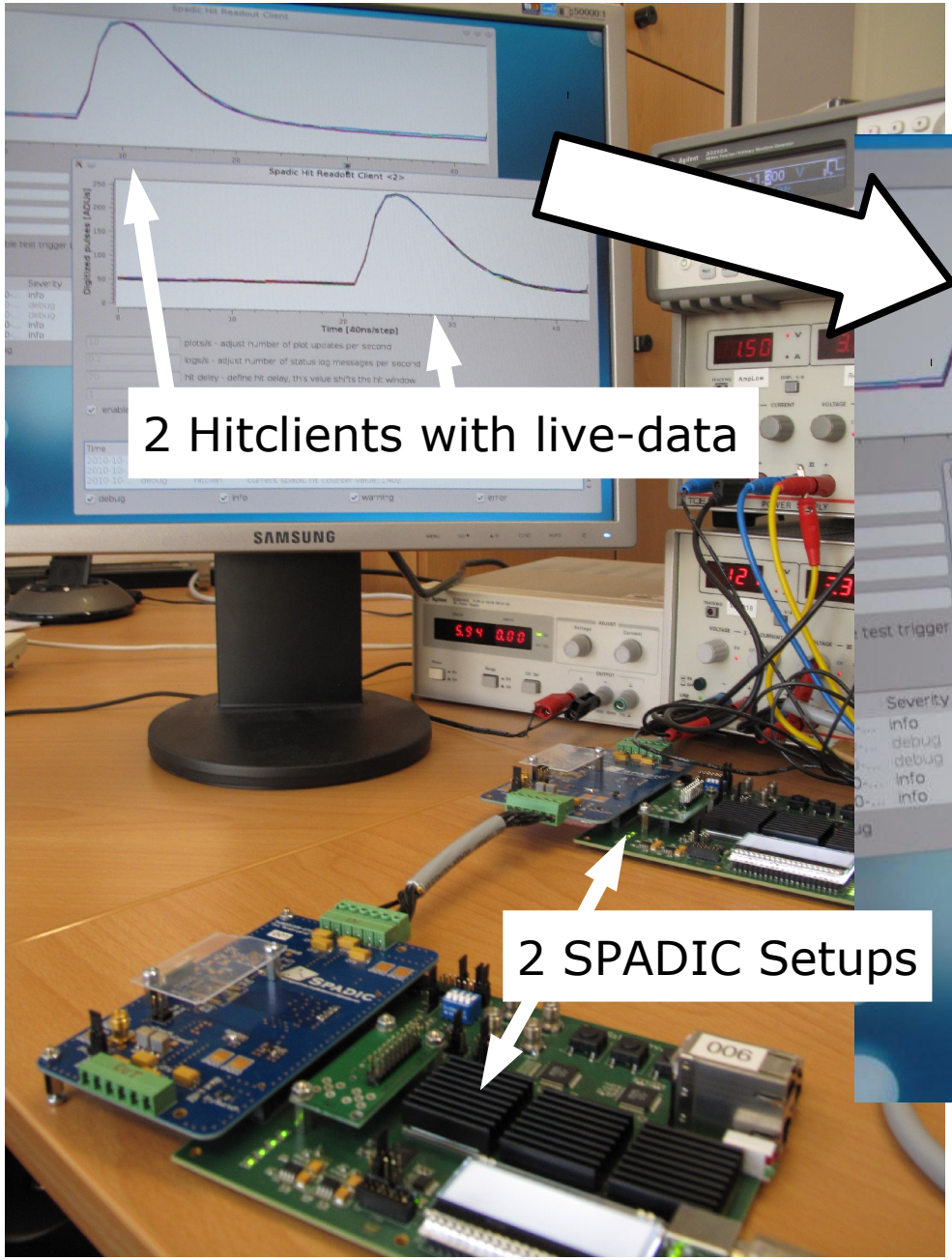
- "Old" chip (Spadic v0.3) but …
  - New front-end PCB
    - Low-noise layout, several smaller improvements
    - Harwin ZIF connector compatible (same connector type as in ALICE TRD)
  - New FPGA readout controller (Susibo)
    - Virtex 5, 2MB SRAM, FTDI (USB 2.0), EEPROM(s), ...
  - New firmware
    - High readout rate of up to 8k events/s (368 Byte/event)
    - Package based protocol
    - New Features like local time-stamp, external event-id extraction (sync-t), …
  - New Software-Library
    - Provides abstract functions like (dis-)connect(), readNextPackage(), status(), …
    - Necessary for integration in DABC framework
  - New stand-alone readout client (hitclient)
- Beamtime target: 8 completely running Setups (8 channels each)
  - Last-minute point landing, also the Susibo was "just in time"
  - A lot of problems with assembly and bonding

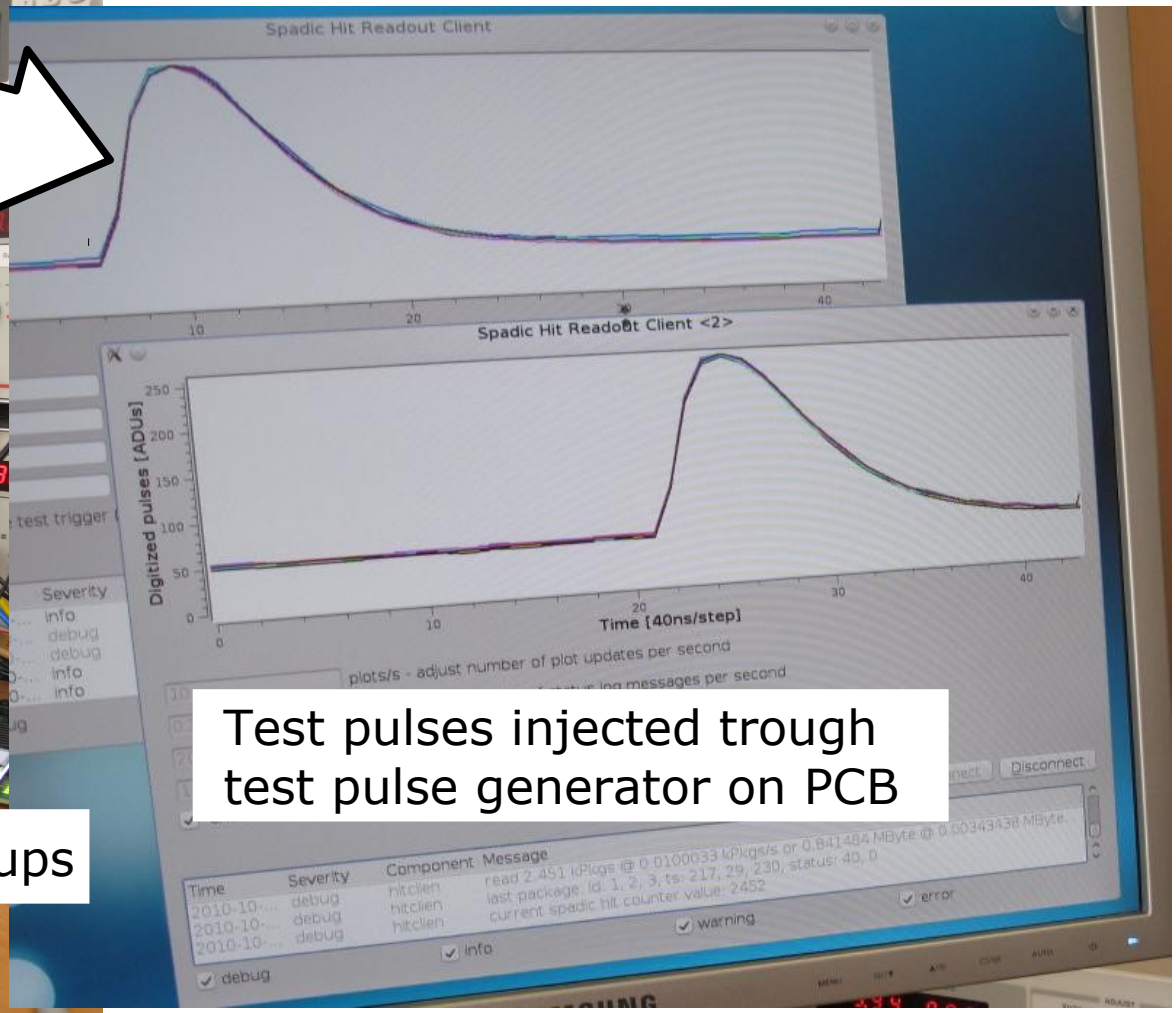
**=> Finally 8 setups worked (most of the beam-time only 6 were run in parallel)**

# SPADIC plugged on Susibo

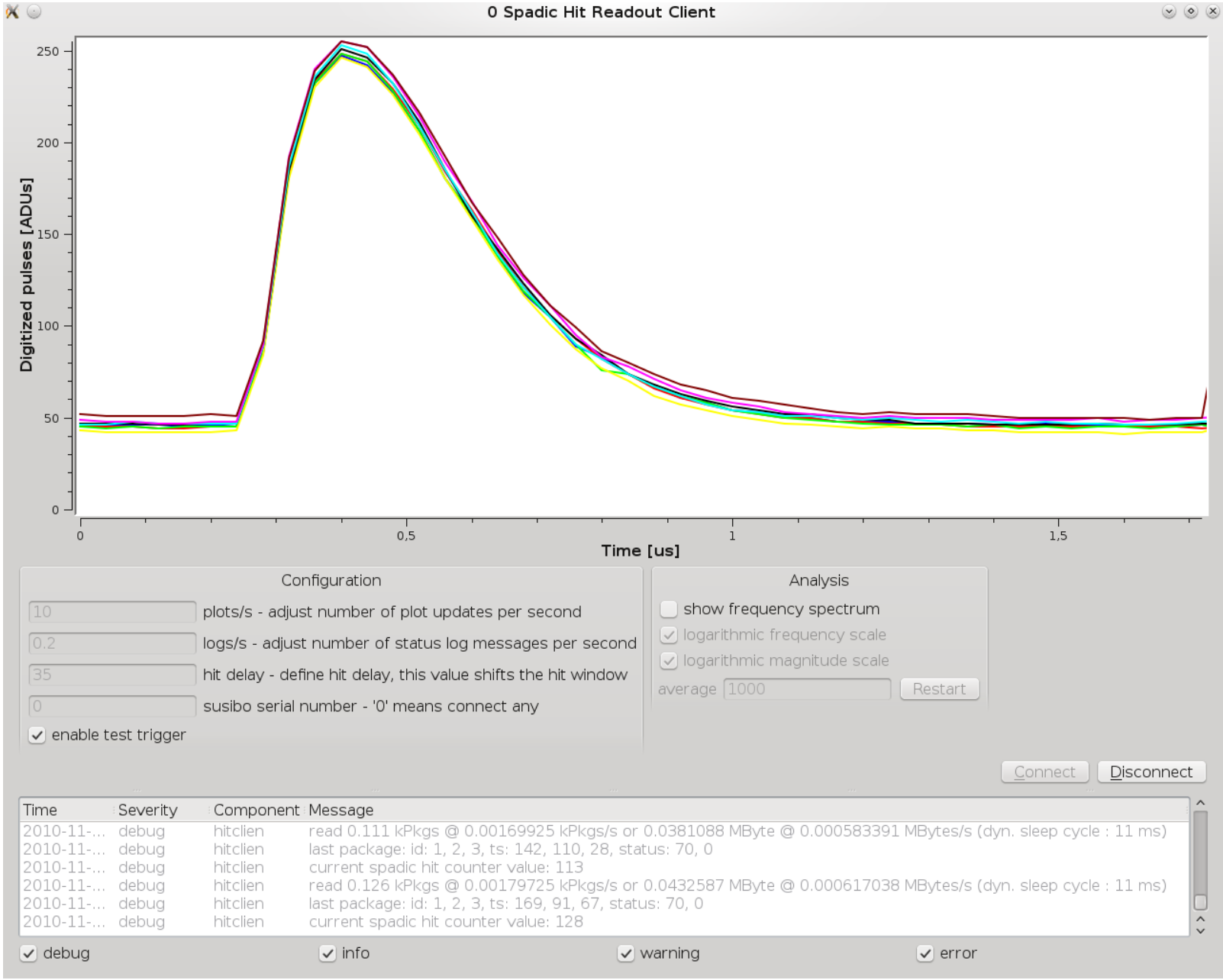


# Setup in Lab


2 Hitclients with live-data
2 SPADIC Setups
SAMSUNG


Spadic Hit Readout Client
Spadic Hit Readout Client <2>
Digitized pulses [ADUs]
Time [40ns/step]
plots/s - adjust number of plot updates per second
Test pulses injected trough
test pulse generator on PCB
Severity
info
debug
Time
Component
Message
Disconnect
warning
error

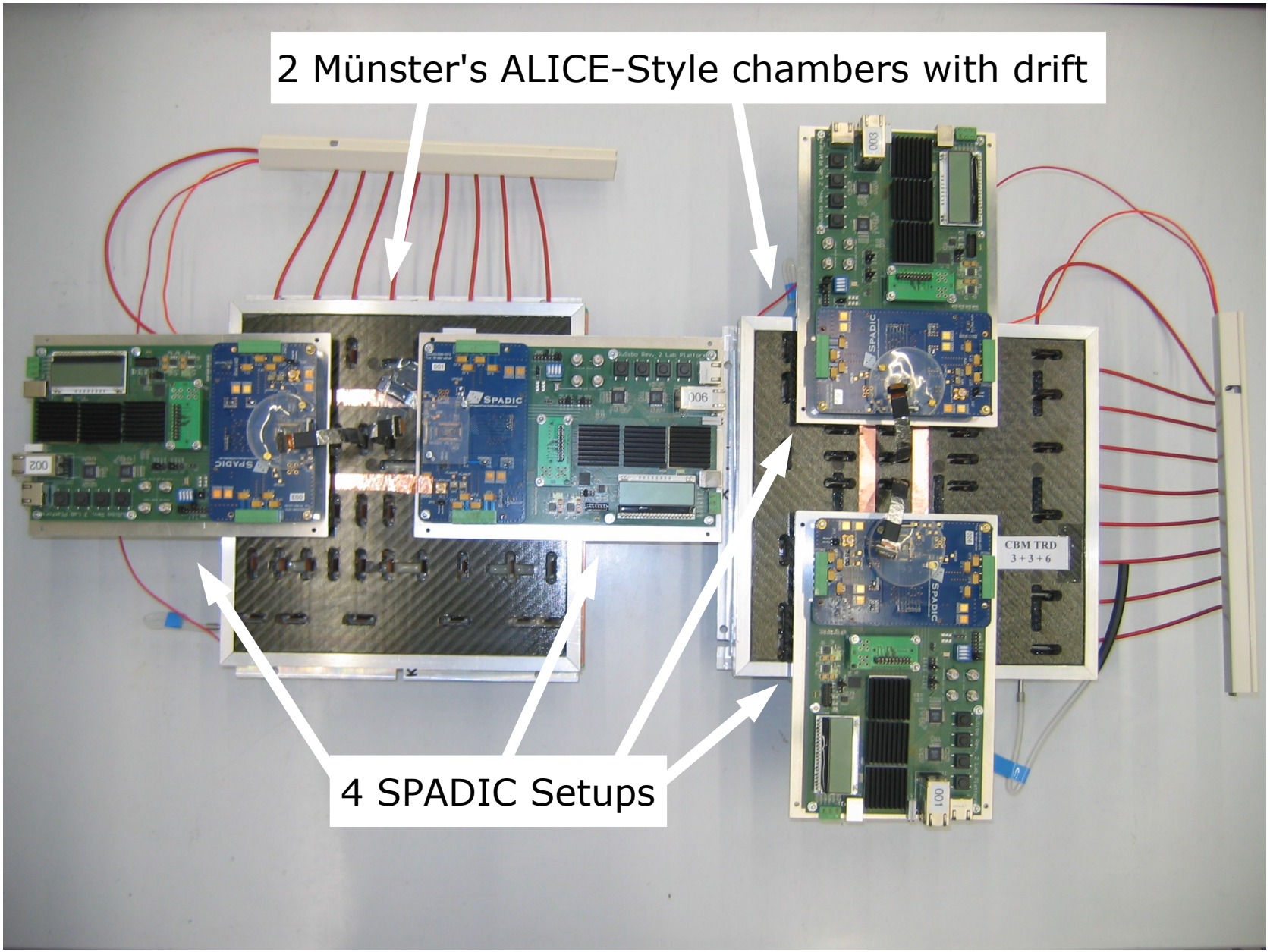
# Hitclient Screenshot



# Frankfurt's TRD-SPADIC Setup

Sorry, problem with my digi-cam :-(

# Münster's TRD-SPADIC Setup



# Setup in the Experimental Hall

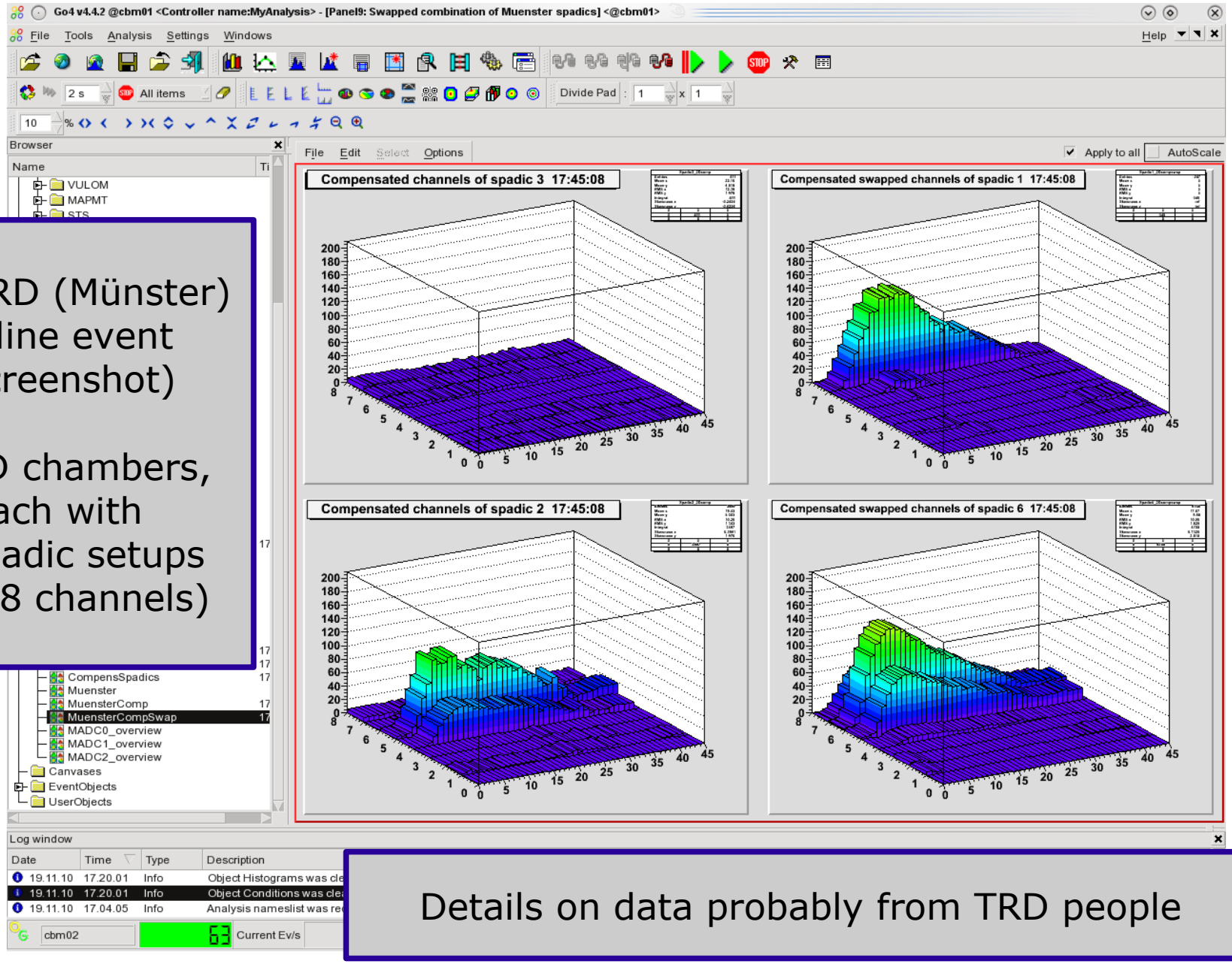
Sorry, problem with my digi-cam :-(

# 3. First Testbeam Results

# Results from an electronic's point of view

- Bad :-(
  - Many problems with pickup (external noise) – a lot of effort was necessary to reduce the different kinds of oscillation to a tolerable minimum
  - **Even after "optimization" some boards still showed strong oscillations**
  - (Due to known reasons) the chip's configuration was very unstable – a lot of re-configurations/restarts were necessary
  - Strange baseline-shift (DC-level) of shaper outputs if detectors were connected AND the ADCs were running (yet there was no time to investigate this)
- Good :-)
  - 8 Spadic/Susibo setups finished just in time
  - Successful integration of Spadic software library into DABC (thanks to Sergey and Jörn)
  - External triggering-scheme worked well
  - Finally 6 working Spadic setups in parallel (4 x Münster, 2x Frankfurt)
  - **A lot of nice hits could be recorded** (but also some ugly)

# Go4 Spadic online event



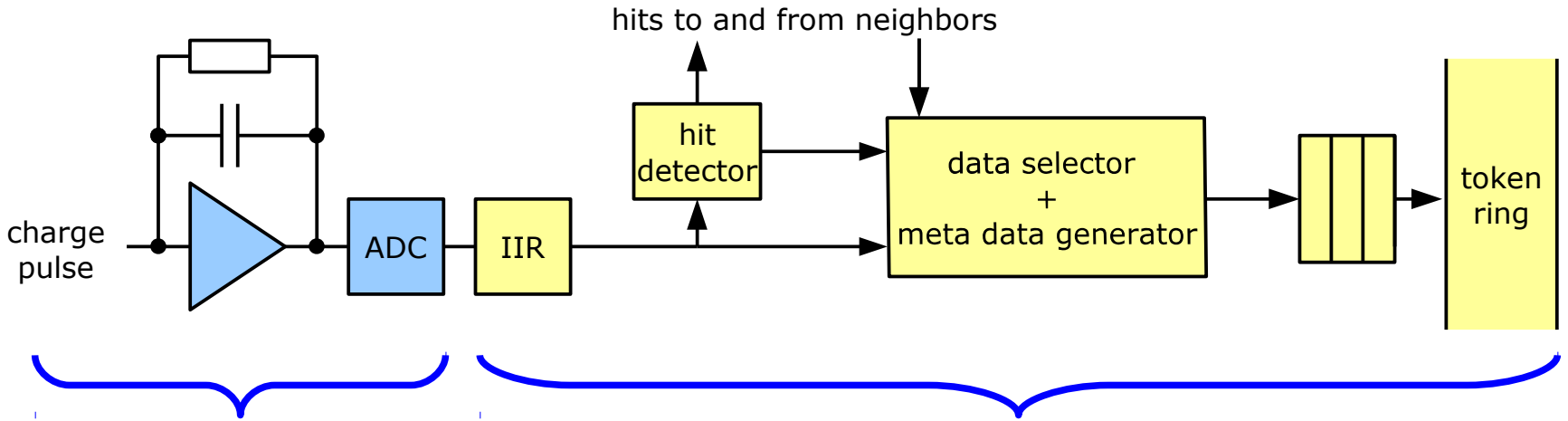

Go4 TRD (Münster) online event (screenshot)

2 TRD chambers, each with 2 Spadic setups (2 x 8 channels)

Details on data probably from TRD people

# 4. Towards SPADIC v1.0

# Status of Development



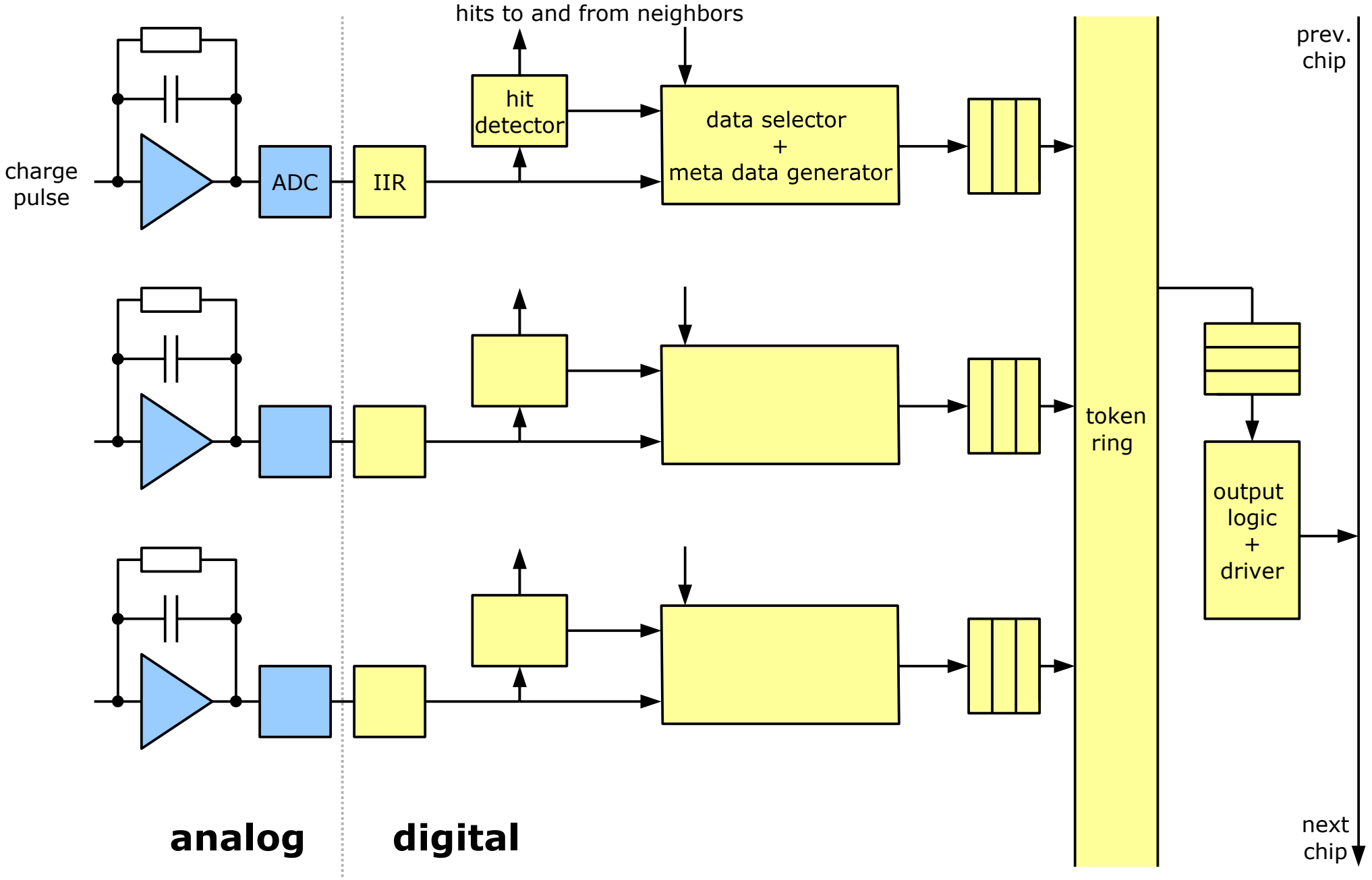

**Analog Parts: Preamp, Shaper and ADC**

- Several test-ASICs successfully designed and tested
- Working 8 channel readout setup (for testbeam as well as for chamber tests)
- Overall design concept mostly settled down
- A lot of parameters must be fixed soon

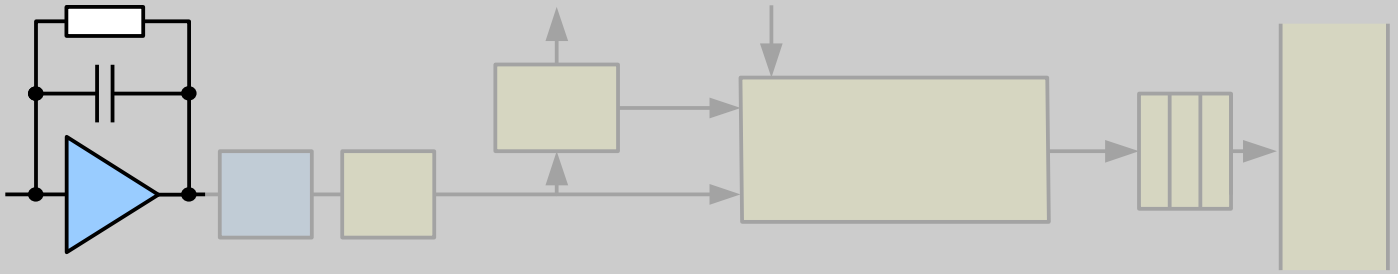
**Digital Parts: IIR filter, hit detector, feature extraction (?), package generator, neighbor logic, token ring, interface protocol (Frank Lemke), ...**

- First design proposal of data flow and control concept finished
- 1st Verilog iteration of most blocks available and simulated
- Michael Krieger, diploma student, working on IIR filter (ion-tail cancellation, ...)
- But: Still a lot of work to do …

# Conceptual Data Flow Diagram



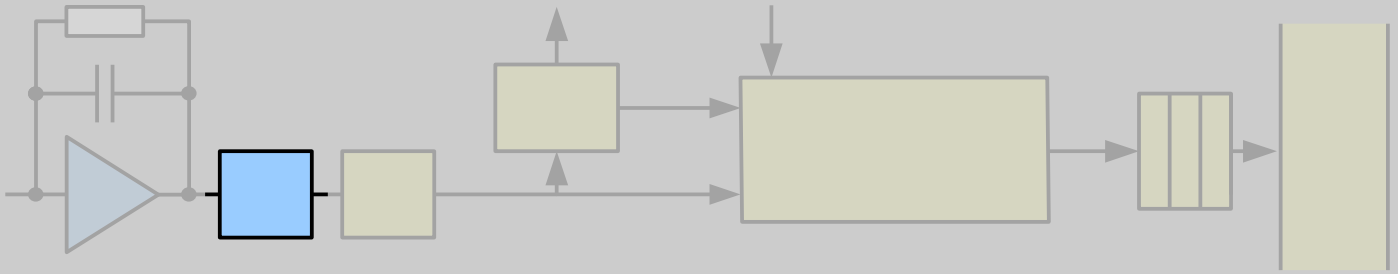
# Spadic 1.0: Preamplifier / Shaper



- Charge sensitive preamplifier (CSA)
  - Single ended, N-MOS input
  - Input protection
  - Switchable polarity
  - Switchable # amplifier cells
- Shaper
  - 2nd order, PZ-cancellation, 82 ns
  - Switchable shaping-time
  - Increased order
- Both
  - 750e ENC @ 30 pF, 3.8 mW
  - Switchable gain

Already Available
Planned feature
Possible feature

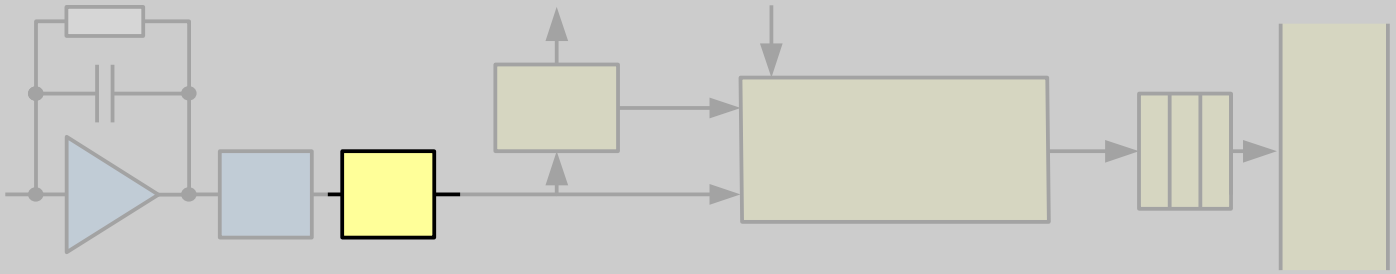
# Spadic 1.0: ADC



- Pipeline ADC, continuously running
  - Current-mode algorithmic ADC
  - 9 Bit design, 7.5 Bit effective
  - Up to 25 Msamples/s
  - 4.5 mW / rad-tolerant
  - Slightly better resolution (~ 8 Bit)
  - High resolution (> 8 Bit), possible but very expensive in terms of man-power, power consumption, chip area, …
  - Improved DC-Level / baseline adjustment mechanism

Already Available
Planned feature
Possible feature

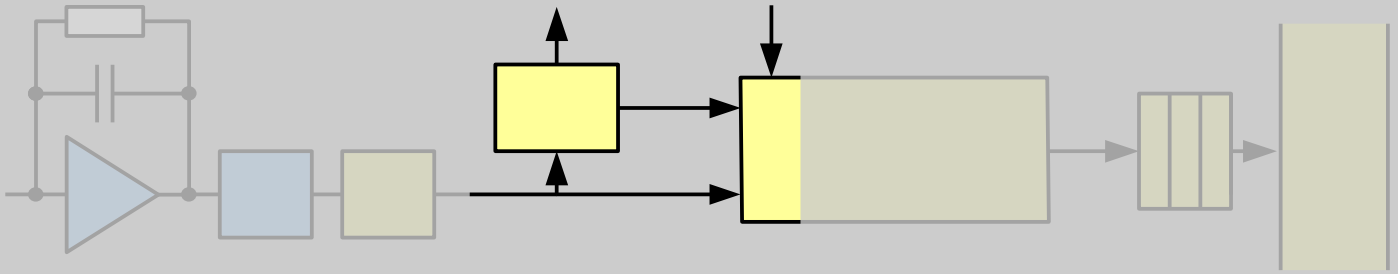
# Spadic 1.0: Infinite Impulse Response Filter (IIR)



- IIR Filter / data pre-processing
  - Michael Krieger's diploma thesis
  - Simulation framework developed
  - 10-14 Bit multiplier + adder
  - Ion-tail cancellation
  - Baseline correction
  - Higher order shaping
  - (Simple) additional ideas ???

Already Available
Planned feature
Possible feature

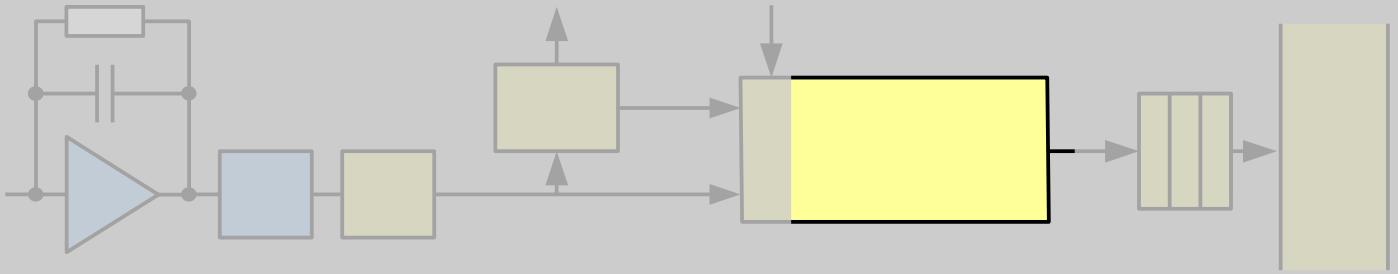
# Spadic 1.0: Hit Detector and Neighbor Trigger



- Digital hit detector
  - Digital hit extraction logic
  - Different hit extraction schemes (threshold, double threshold, pulse length, …)
  - 1th order Verilog, simulation works
- Neighbor readout logic
  - Automatic readout of neighbor channels
  - Trigger signal across chip edges
  - 1th order Verilog, simulation works

Already Available
Planned feature
Possible feature

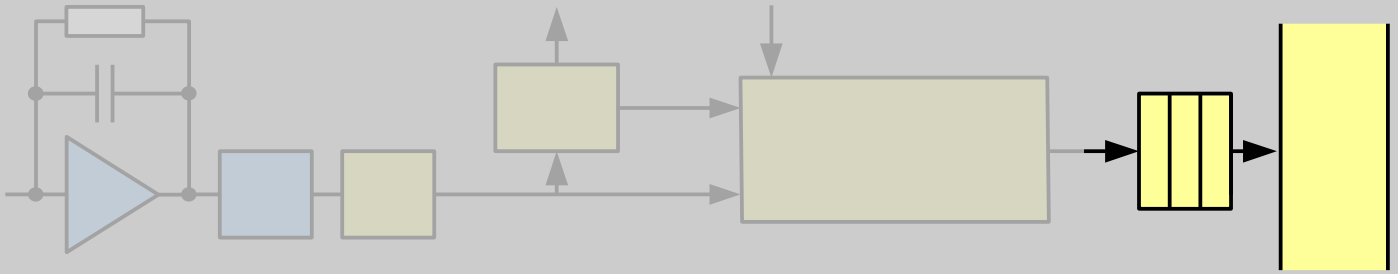
# Spadic 1.0: Meta Data Generator and Package Builder



- Meta Data Generator
  - Local and external time-stamp extraction
  - Hit type extraction (internal, neighbor, …)
  - Channel #, Chip ID, …
  - 1th order Verilog, simulation works
- Package builder
  - Generation of hit package including meta and hit data
  - 1th order Verilog, simulation works

Already Available
Planned feature
Possible feature

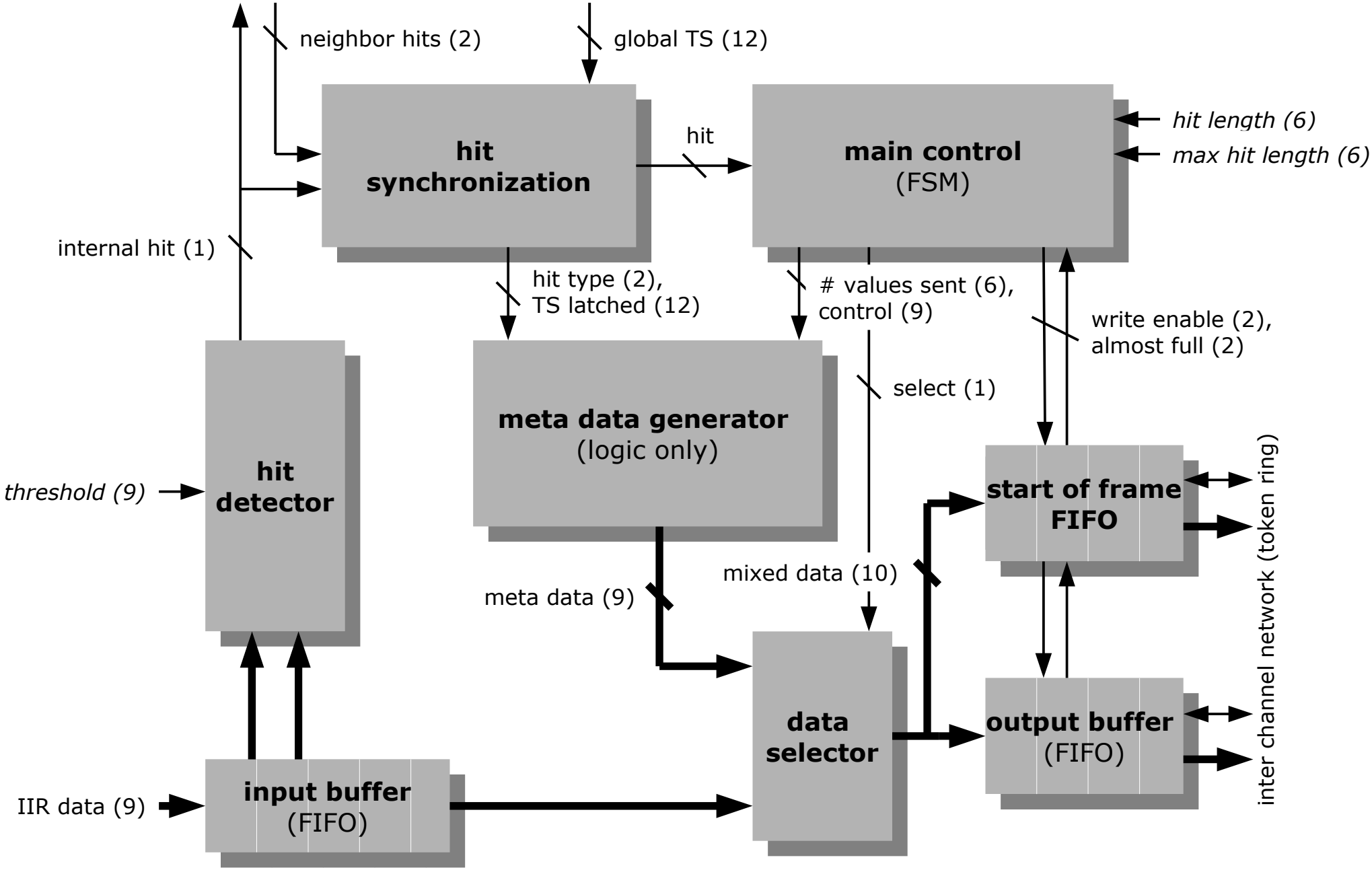
# Spadic 1.0: Output Interface



- Output Interface
  - FIFO package buffer
    - Need access to some UMC 018 SRAM generator
  - Token ring inter-channel network
  - Sophisticated deterministic latency output protocol (Frank Lemke)
  - CBM DAQ compatible !!!
  - Serializer
  - Output driver

Already Available
Planned feature
Possible feature

# Digital Hit Detector and Package Builder

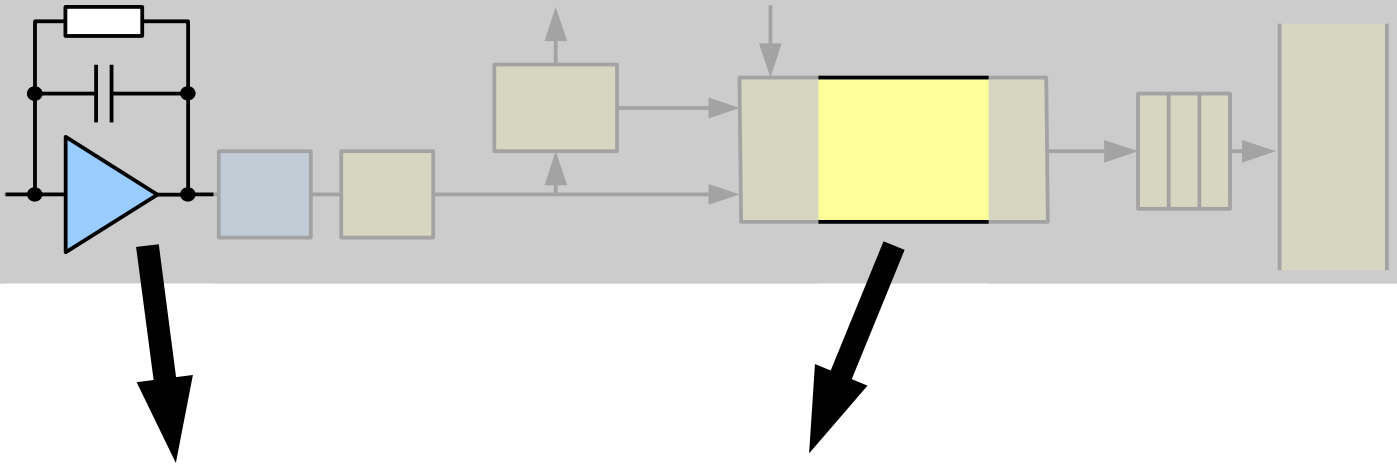


# Chip Concept


Planned feature
Possible feature

- Features on chip-level
  - 32 channels / chip (maybe 64)
  - Several test mechanisms (test injection, analog signal access, …)
  - On-chip bias circuitry (current DACs + diodes)
  - A lot of global and local configuration registers
  - Maskable channels
  - Power consumption / channel: analog ~ 10mW, digital ??? → power limit?
  - Data: LVDS inputs / outputs only
  - Additional channel as global reference to eliminate systematic disturbances (e.g. pick-up)

# If Spadic also goes for RICH people ...



- Necessary adjustments of Spadic 1.0 concept for RICH (Ring Imaging Cherenkov)
  - Much smaller input gain (max. 1.6 pC / hit) → switchable preamp/shaper gain
  - Negative input charge → bidirectional input stage
  - Very good time resolution ~ 2ns → sophisticated feature extraction on-chip or offline
    - Is this time resolution achievable (40 ns sampling period)?
  - Energy feature extraction → on-chip (preferred) or offline (?)
  - Opt: more than 32 channels (>= 64)
- **List not too long, but I'm already busy** → additional man-power on the horizon?

# (Updated) Data-Rate Calculation

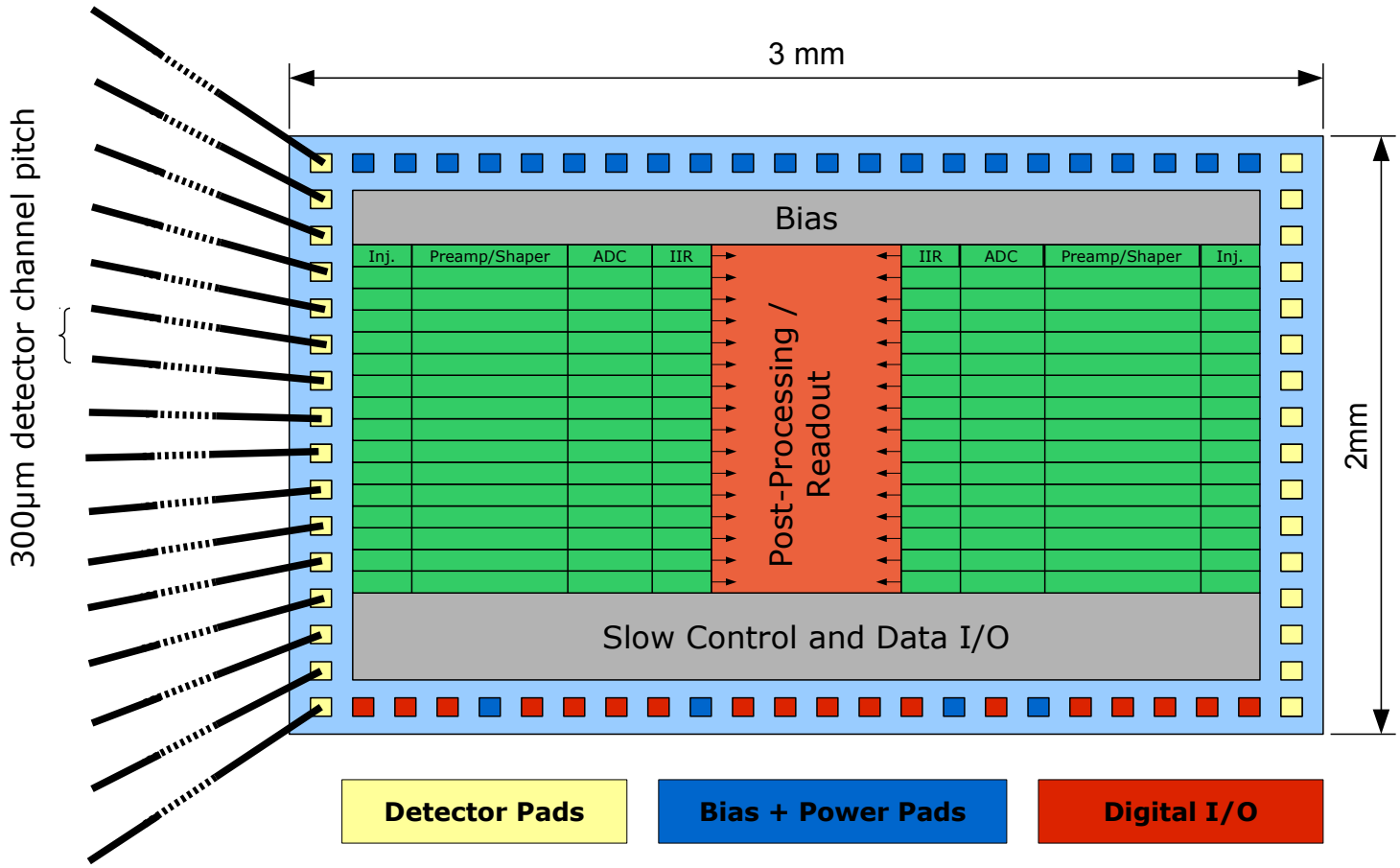
Some estimated numbers:

- 32 channels / chip
- 250 kHz maximum event rate / channel (one hit every 4 µs)
- 8 Bit ADC resolution
- 10 samples / event <= we need to further investigate here
- 12 Bit time-stamp / event (epoch length 164 µs @ 25MSamples/s ADC speed)
- 5 Bit channel ID

$$R_{chip} = \underbrace{\frac{250\,k\,events}{channel \cdot s} \cdot 32\,channels}_{hit\,rate\,chip} \cdot \left( \underbrace{\frac{8\,bit}{sample} \cdot \frac{10\,samples}{event}}_{hit\,data} + \underbrace{\frac{17\,bit}{event}}_{time-stamp+ID} \right) = \frac{776\,Mbit}{s}$$

- => Conservative estimation: about 12 Bytes / (hit + channel)!
- => Planned output protocol from computer architecture group (Ulrich Brüning and Frank Lemke) foresees two links per chip with 500 Mbit/s each
- Note: Epoch counter + forward error correction overhead not considered here!

# Floor Plan Proposal




- 3 x 2 mm² estimated die size
- 32 channels, 80µm pitch, (mostly) symmetric layout for low(er) IR-drops
- Detector connection-pads on two sides (chips will probably be attached to back of detector-module, this relaxes routing/spacing)

# 5. Future of the Test-Beam-Setup

# Spadic User Community

- (Potential) users of the "Spadic Test-Beam" setup
  - **IKF, Frankfurt** – currently making first steps (2 boards)
  - **Uni Münster** – currently making first steps (2 boards)
  - **JINR Dubna** – showed interest in using the setup for their chambers
  - **RICH, GSI** – readout of the photomultipliers with Spadic just as a proof of principle and to get familiar with the setup (usage of course not as a working horse)
- Other planned "Spadic Test-Beam" setup activities
  - Readout of some strip diodes from Johann (GSI) as a proof of principle and to measure some spectra
  - GSI would like to gather bonding-experience with some Spadic chips

=> To a certain limit, **I would like to improve the current setup** and …

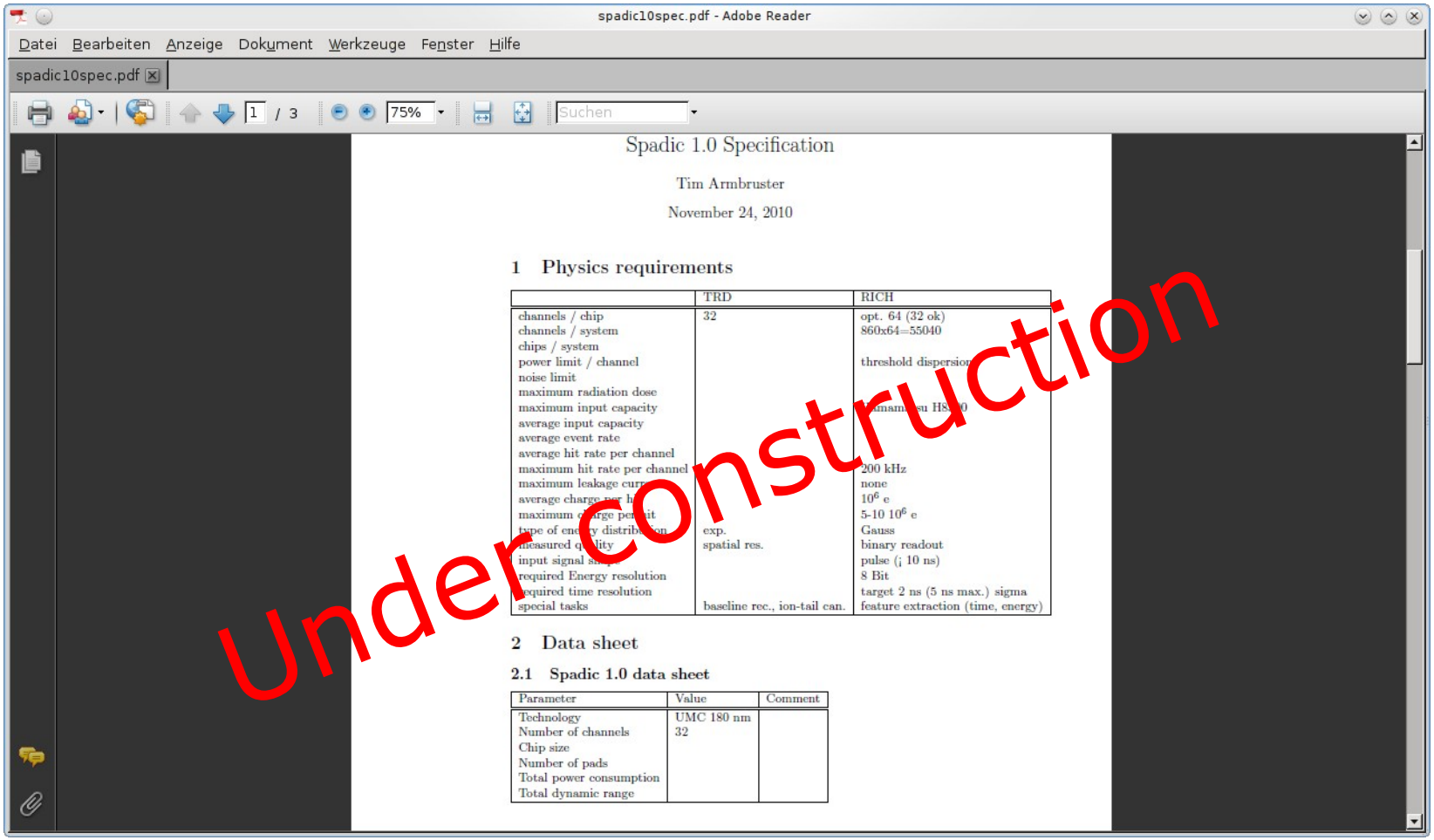
  - … add some additional features (e.g. include a sync-t trigger generator)
  - … stabilize the readout
  - … re-iterate the front-end PCB (remove some little bugs, optimize the detector connectivity, consider some external advice, add footprint for strip diode, …)

**But all this strongly depends on available man-power and willingness to cooperate!**

# 6. Next steps and timetable

# Next Step: Iterate over Specification

- I've started a Spadic 1.0 specification file
- Everybody concerned should help interating it
- We need to fix all basic numbers before the chip development starts



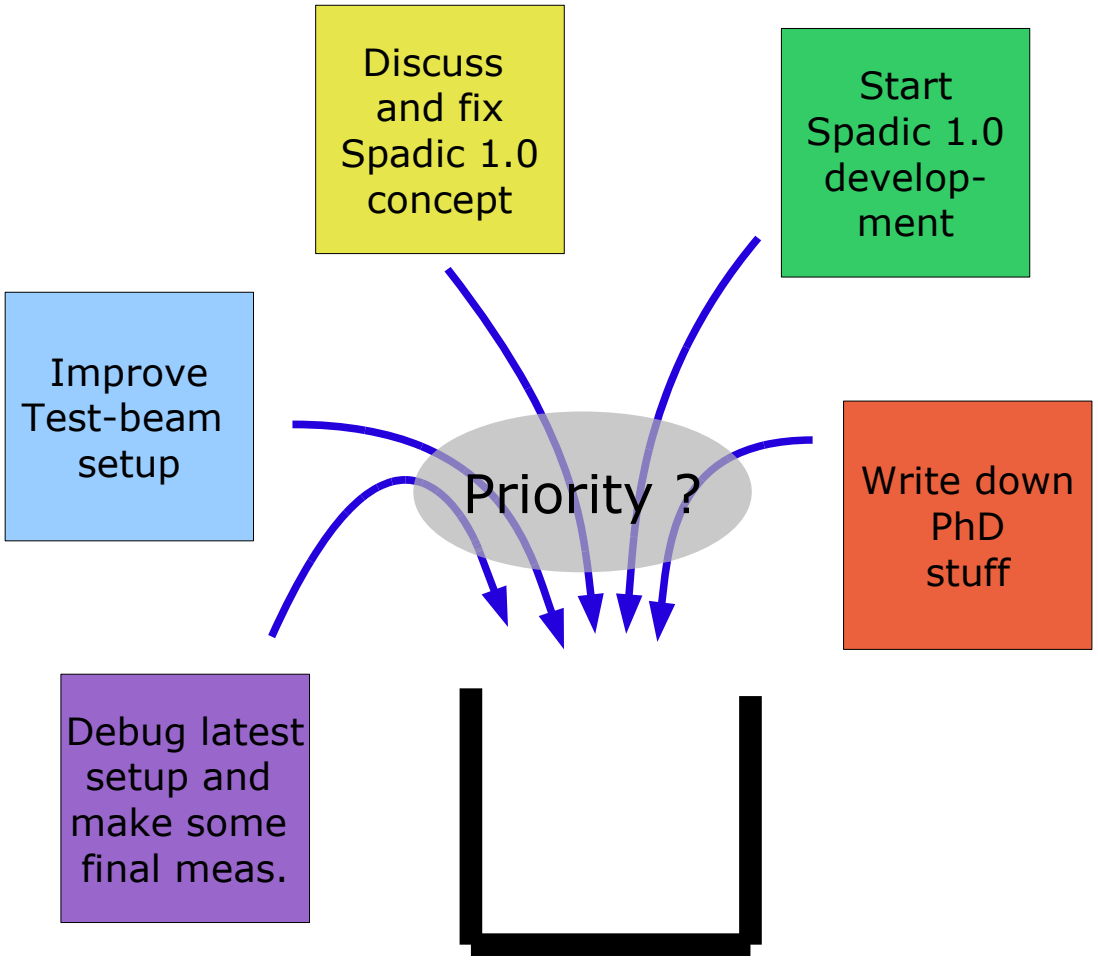
# Next Step: Debug and improve Testbeam-Setup

- We still need to understand …
  - … the strange baseline shift …
  - … the high sensitivity to pick-up noise (PCB, chip or detector problem?) …

- We probably should gather some more experience by …
  - … reading out some silicon strip detector …
  - … (maybe) reading out the RICH photodiodes …
  - … further improving the setup (see need to understand) …

… **before** we finish the Spadic 1.0 development.

# Timetable




- A lot of different tasks
- I need to decide when to start writing down my PhD (plan was to start at beginning of 2011)
- A **very** optimistic estimation for the submission of Spadic 1.0 is middle of 2011
- A priority list, working packages and a time-table must soon be defined
- **The focus should go as soon as possible to the Spadic 1.0 development!**

# 5. Summary and Outlook

# Summary and Outlook

**Status of the latest setup:**

- 8 working Spadic v0.3 / Susibo setups
- Successful integration in CBM test-beam environment
- Promising results in lab and from test-beam but also open problems
- A lot of interest in using the current setup from different groups

**Status of Spadic 1.0 design concept**

- Complete design concept available
- Analog part (except for some improvements) conceptually completed
- Most digital building blocks still in a very early design phase
- Many features still need to be discussed
- Design kick-off as early as possible in 2011

**Next Steps:**

- Improve latest setup and gather more experience with chambers and silicon
- Discuss and fix specification
- **Focus on Spadic 1.0 development**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