UNIVERSITÄT
HEIDELBERG

First SPADIC beamtime @ CERN

TRD readout with the new Susibo/Spadic testbeam setup

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SuS Meeting @ Mannheim

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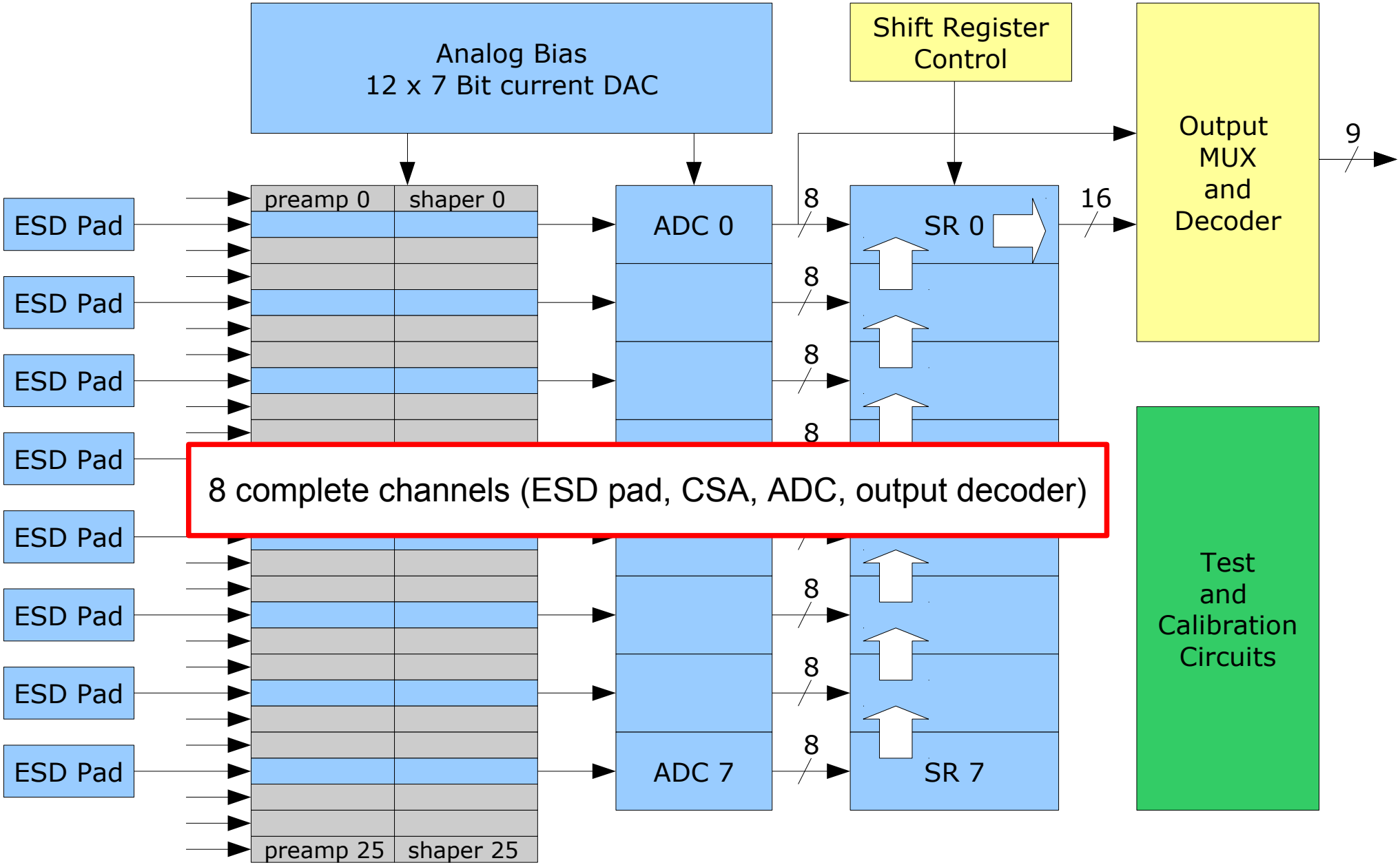
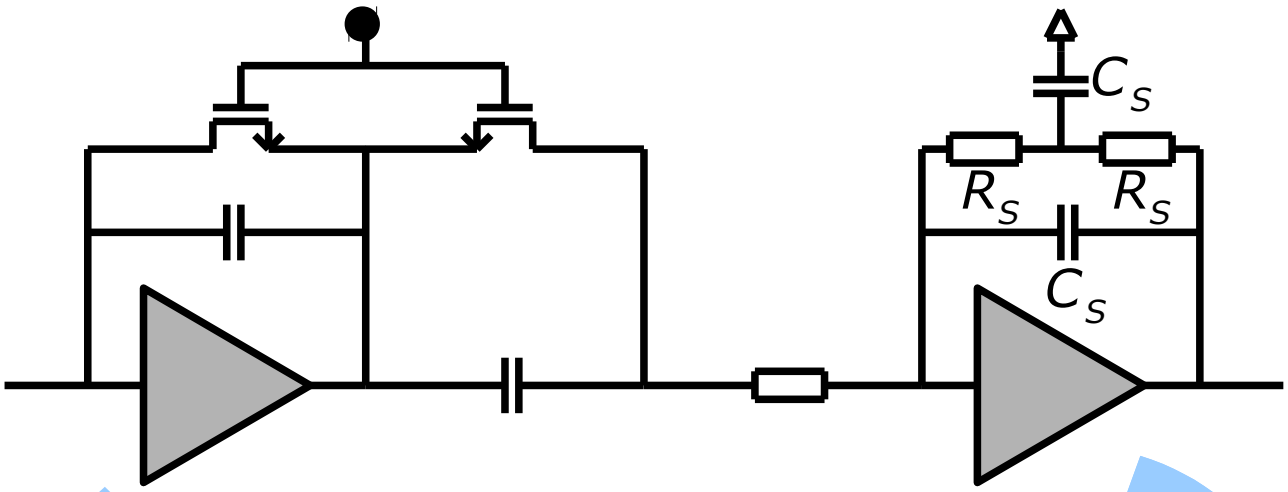
1. Spadic / Susibo Testbeam Setup

Block Diagram of Current ASIC



Reminder: Preamplifier/Shaper Circuit



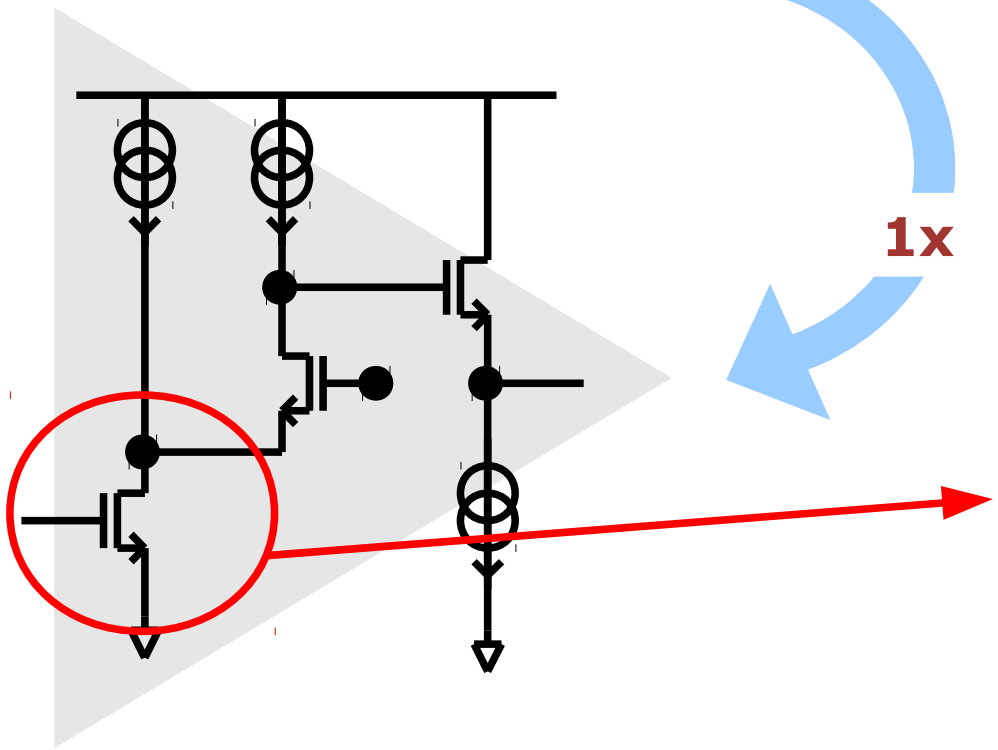
$$H(s) \approx \frac{A_{DC}}{(1+sR_sC_s)^2}$$

- O'Connor FB
- 2nd order shaper
- Shaping time: 82 ns
- Unified amplifier cell
- N-MOS input
- ≈ 3.6 mW/channel

11x

1x

(also channels with less instances for test purpose on chip)

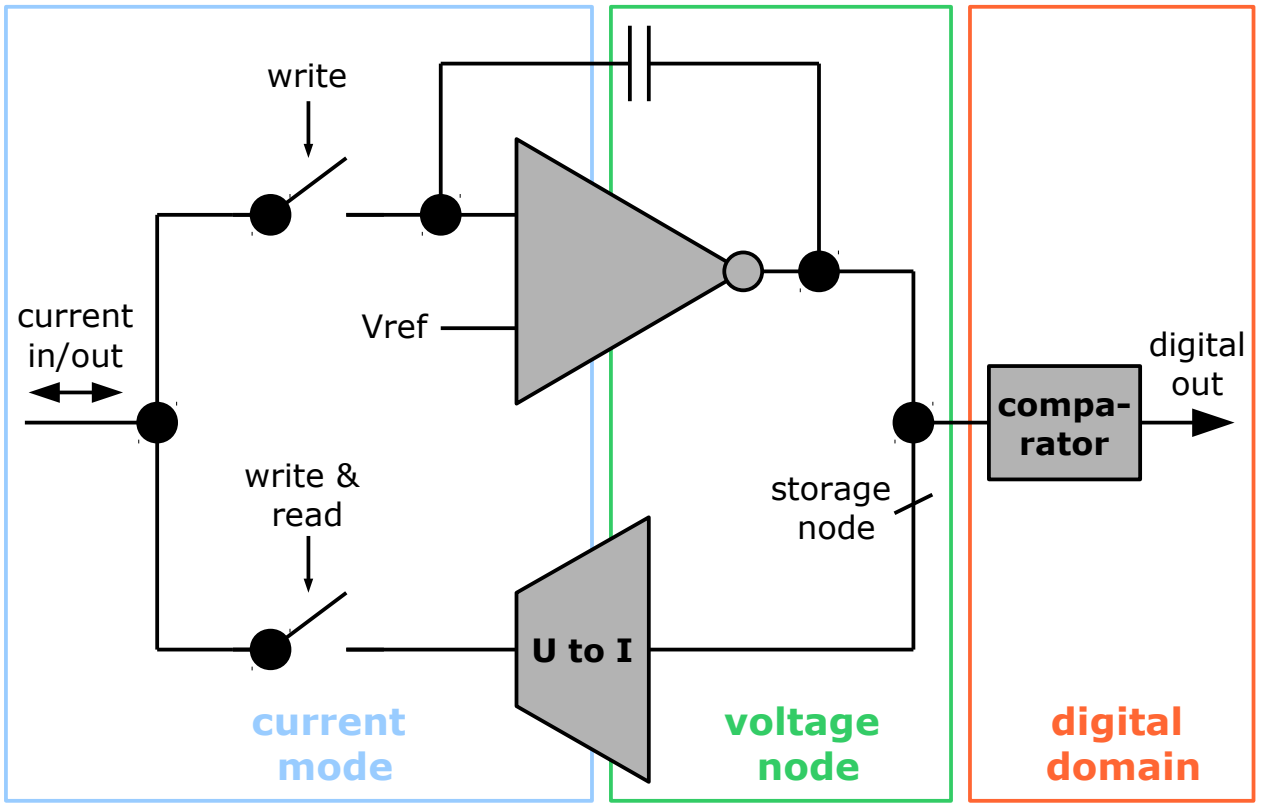


New:

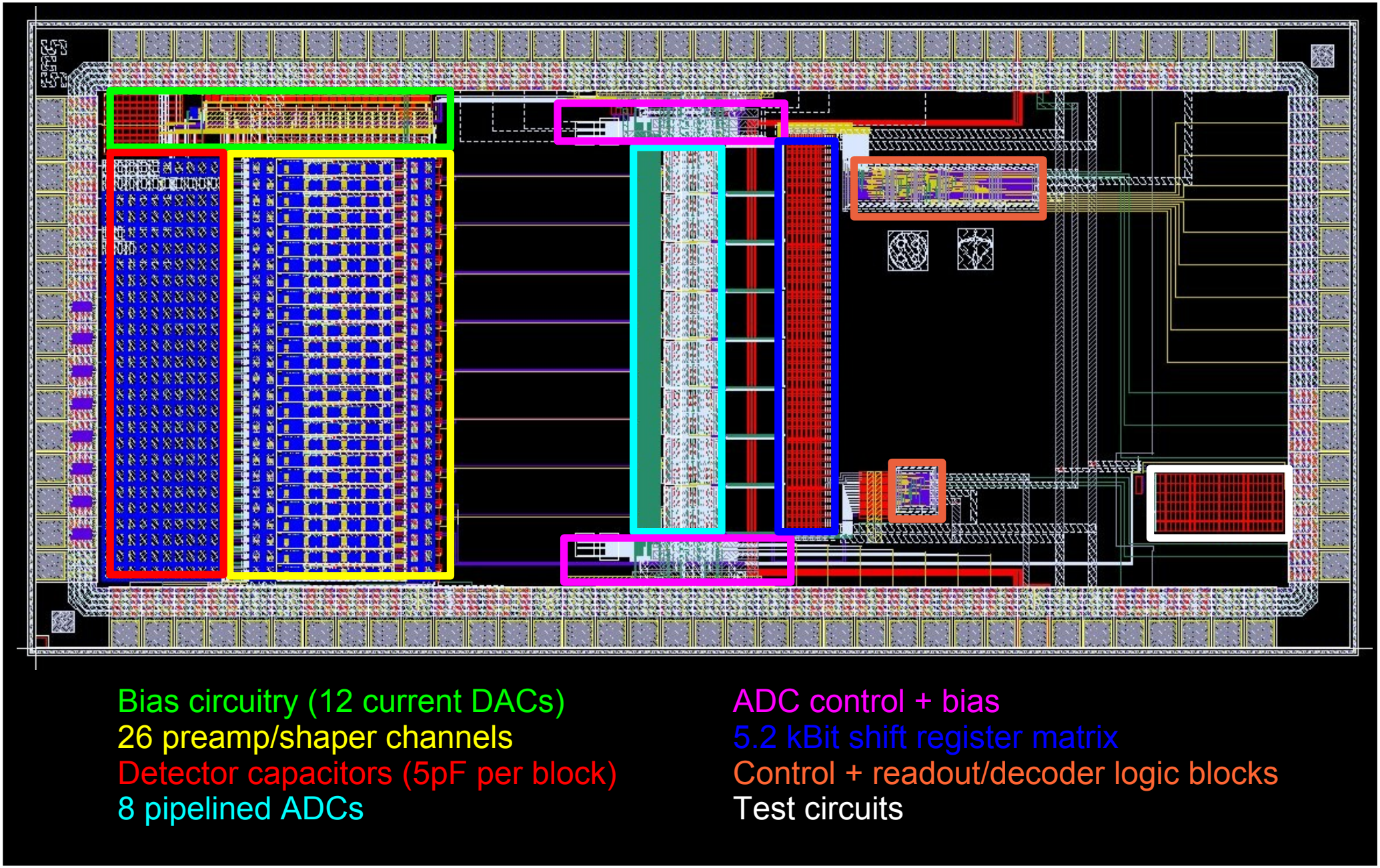
- Scaled lengths of input NMOS (180, 250, 320, 390, 460nm)
- Re-Layout of input NMOS: The (long) gate-fingers have been cut into smaller pieces to decrease gate resistance

Reminder: Algorithmic ADC Design

- 8 (scaled) pipeline stages, therefore 9 Bit design, **7.5 Bits effective** so far
- Algorithmic working principle ("1.5 redundant Bits" / conversion step)
- **25 MSamples/s, layout only 130x120 µm², power consumption 4.5 mW**
- Core unit: Novel current storage cell:



Current Test-Chip: Layout



Bias circuitry (12 current DACs)
26 preamp/shaper channels
Detector capacitors (5pF per block)
8 pipelined ADCs

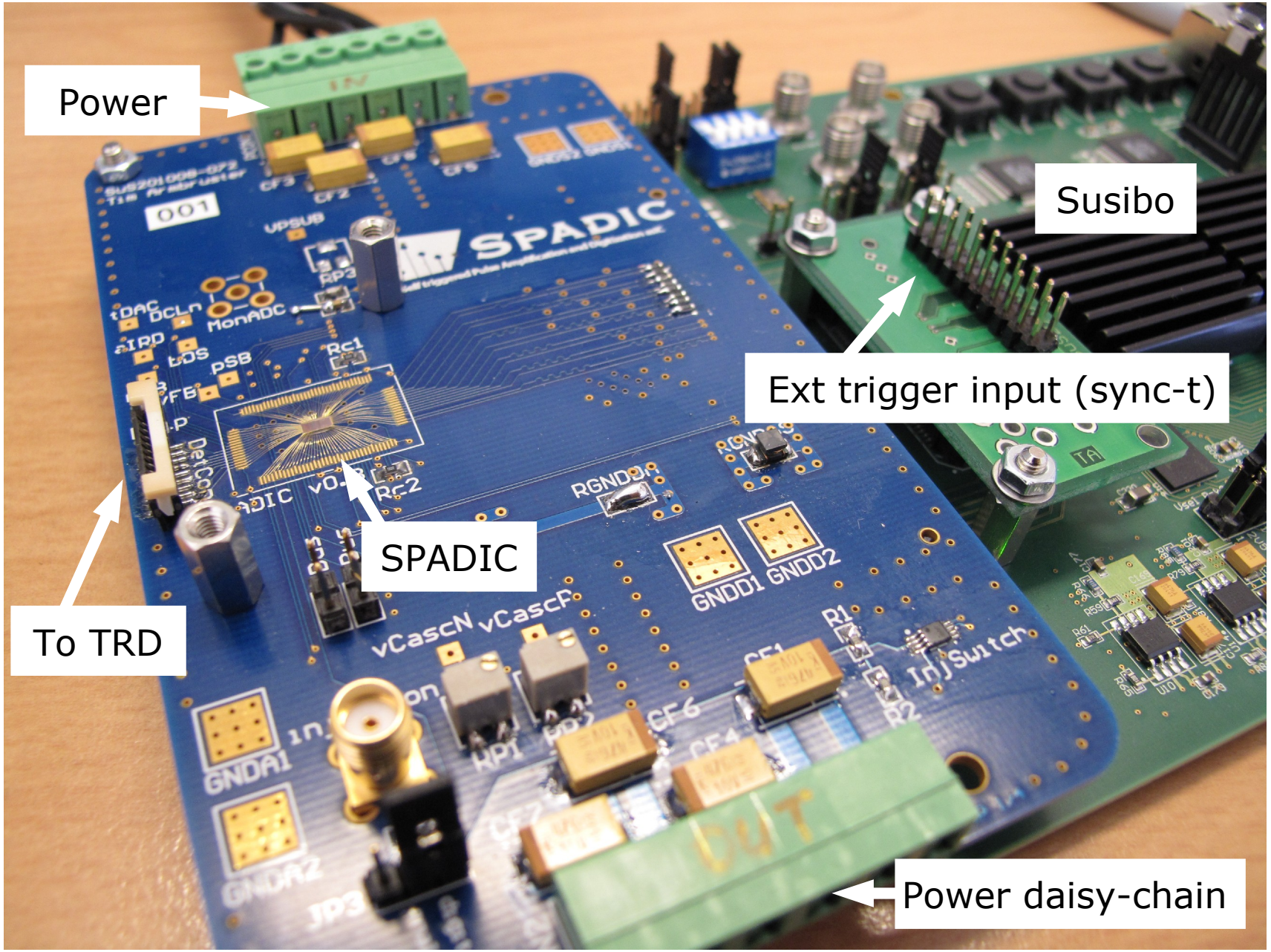
ADC control + bias
5.2 kBit shift register matrix
Control + readout/decoder logic blocks
Test circuits

(Old) Pre-Testbeam Setup

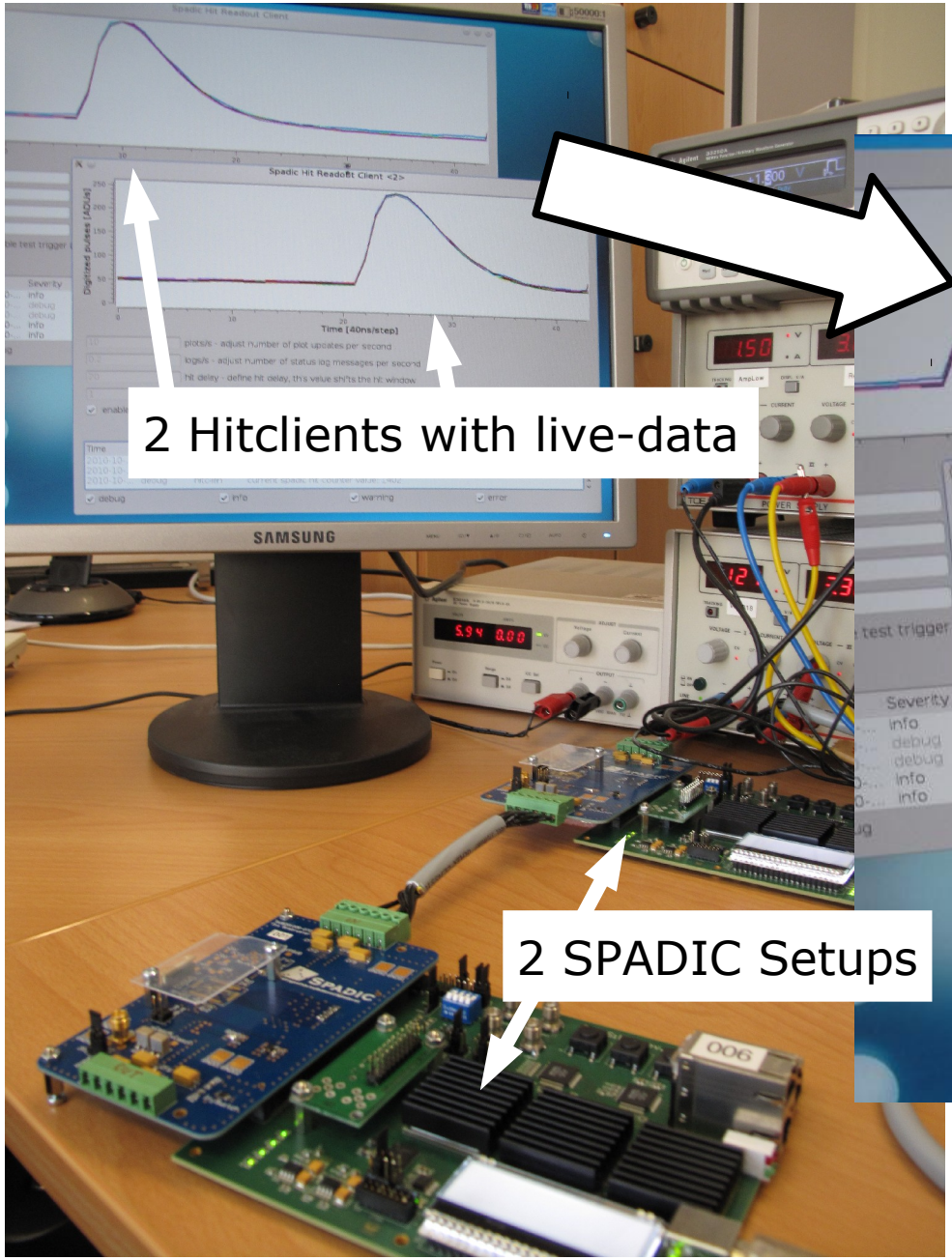
Testbeam Setup Overview

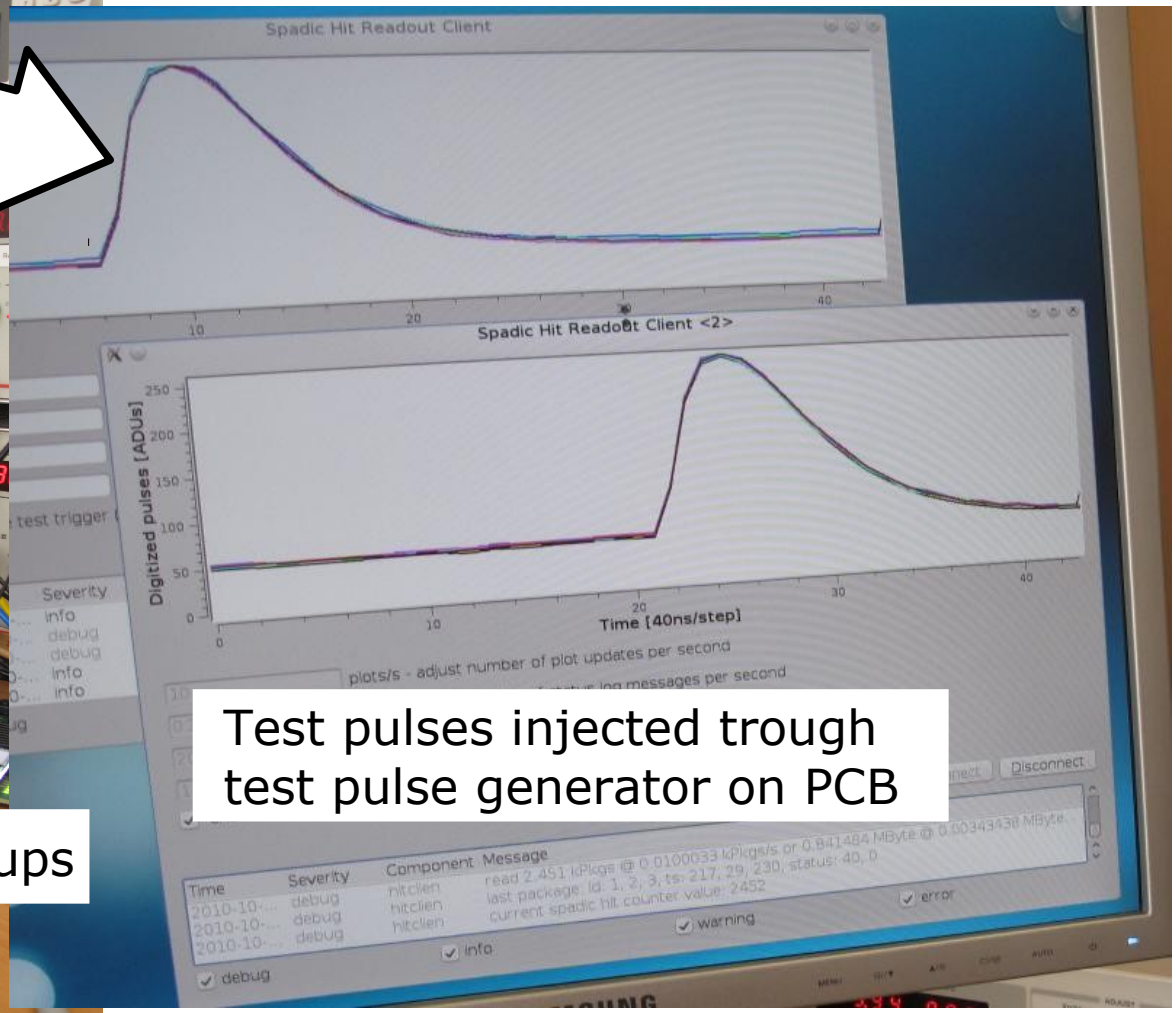
- "Old" chip (Spadic v0.3) but …
  - New front-end PCB
    - Low-noise layout, several smaller improvements
    - Harwin ZIF connector compatible (same connector type as in ALICE TRD)
  - New FPGA readout controller (Susibo)
    - Virtex 5, 2MB SRAM, FTDI (USB 2.0), EEPROM(s), ...
  - New firmware
    - High readout rate of up to 8k events/s (368 Byte/event)
    - Package based protocol
    - New Features like local time-stamp, external event-id extraction (sync-t), …
  - New Software-Library
    - Provides abstract functions like (dis-)connect(), readNextPackage(), status(), …
    - Necessary for integration in DABC framework
  - New stand-alone readout client (hitclient)
- Beamtime target: 8 completely running Setups (8 channels each)

SPADIC plugged on Susibo



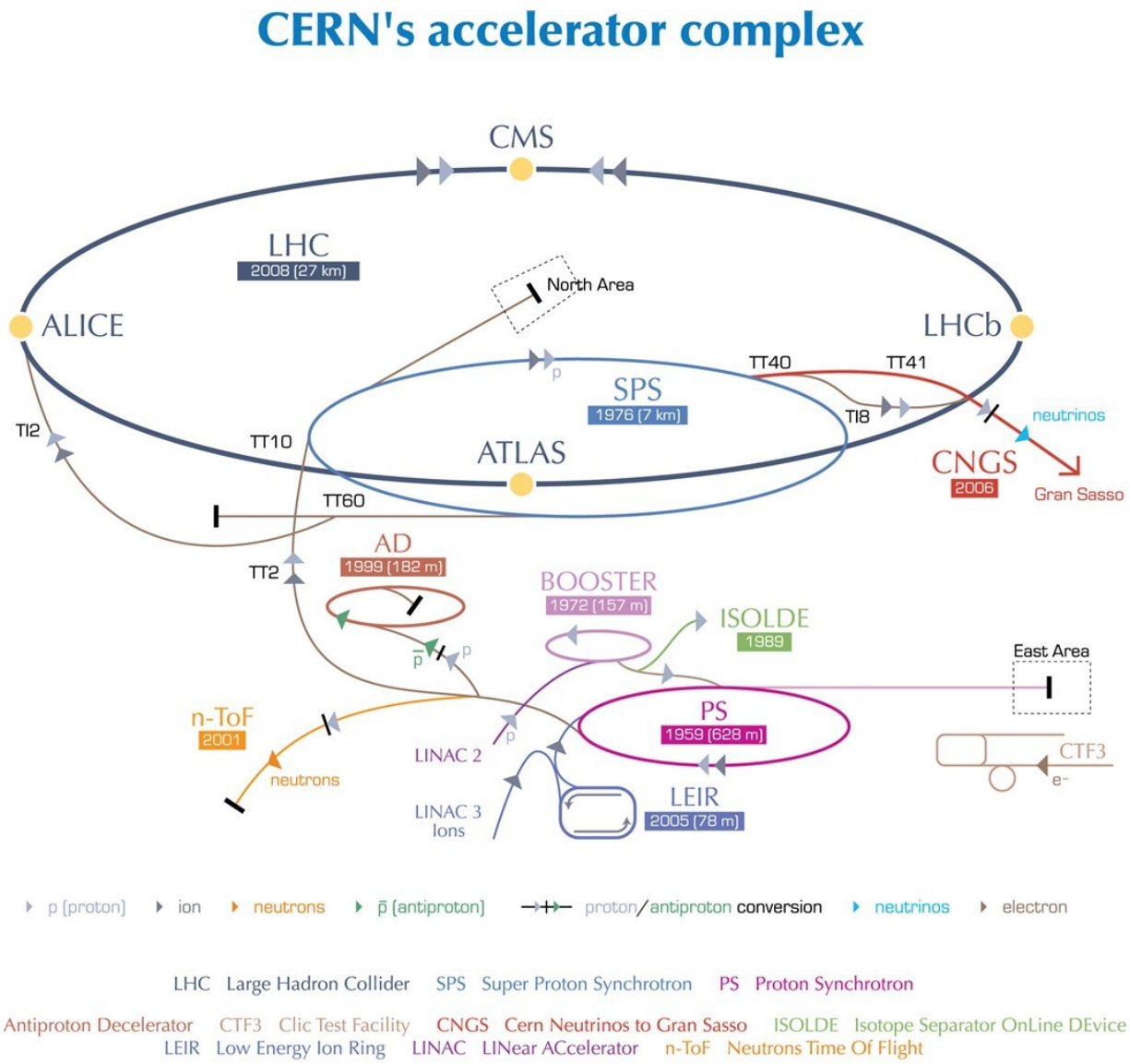
Setup in Lab


2 Hitclients with live-data
2 SPADIC Setups


Spadic Hit Readout Client
Spadic Hit Readout Client <2>
Digitized pulses [ADUs]
Time [40ns/step]
plots/s - adjust number of plot updates per second
Test pulses injected trough
test pulse generator on PCB

2. Beamtime @ CERN

CERN's Accelerators



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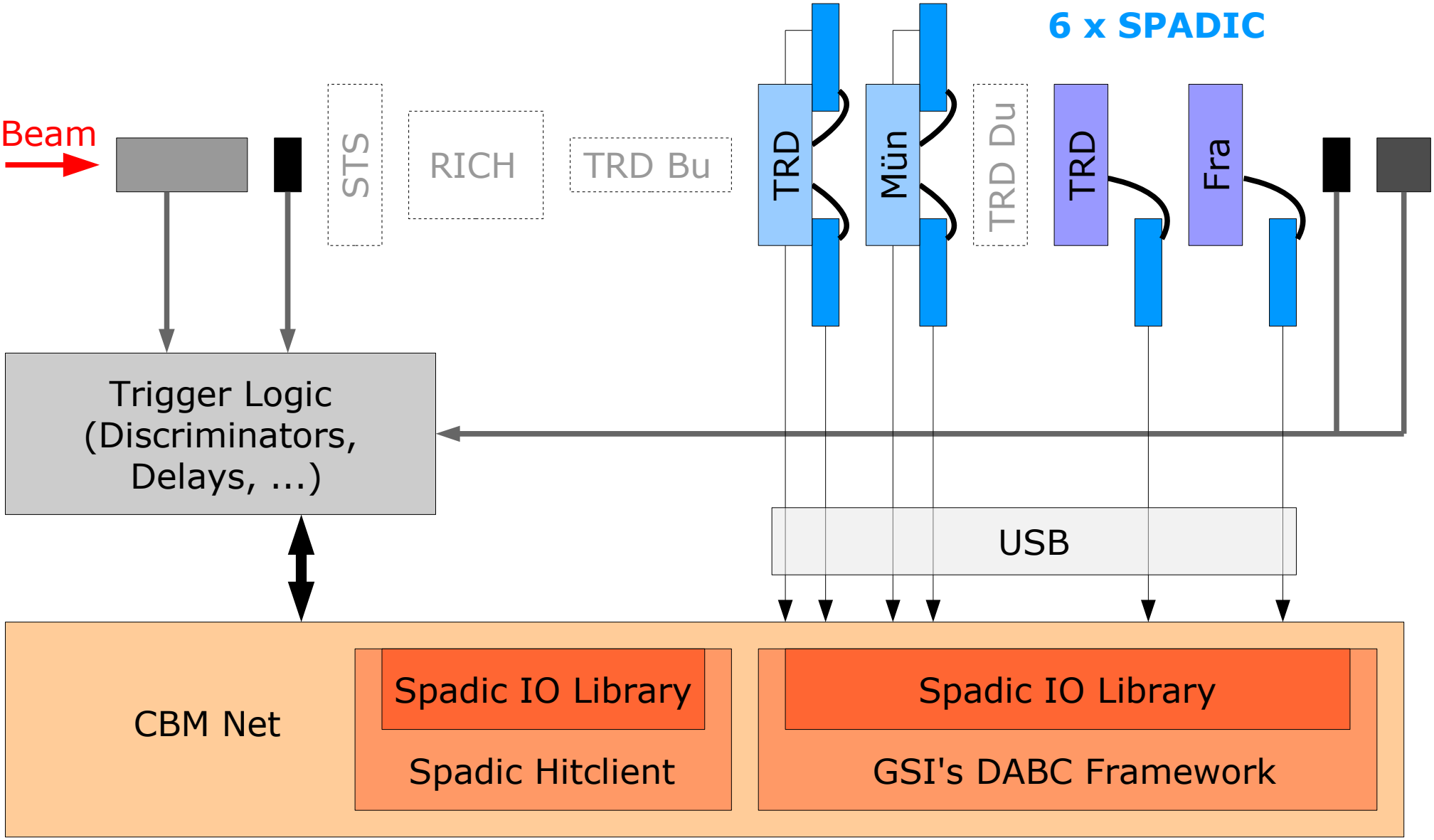
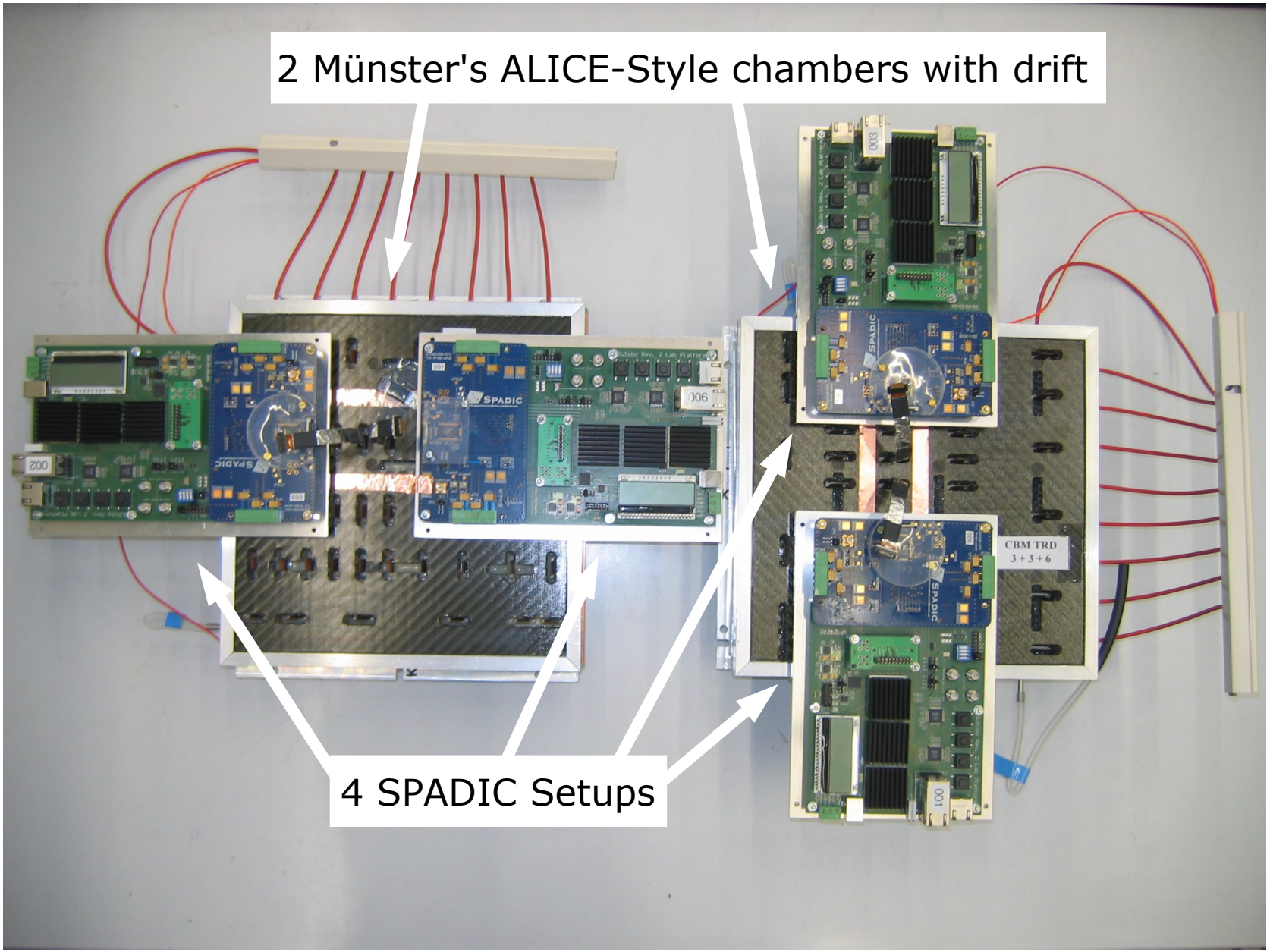
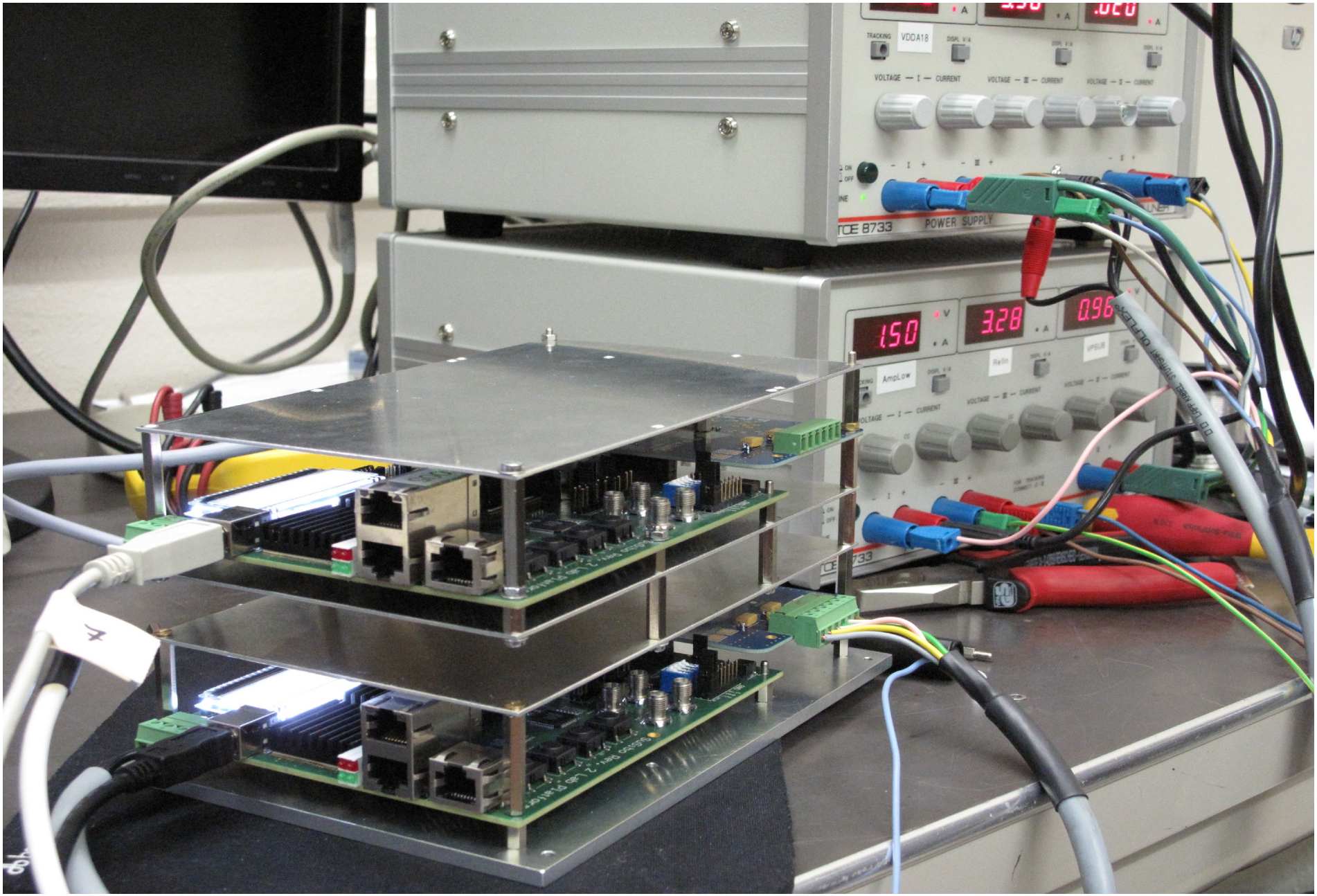
Overview Testbeam Setup



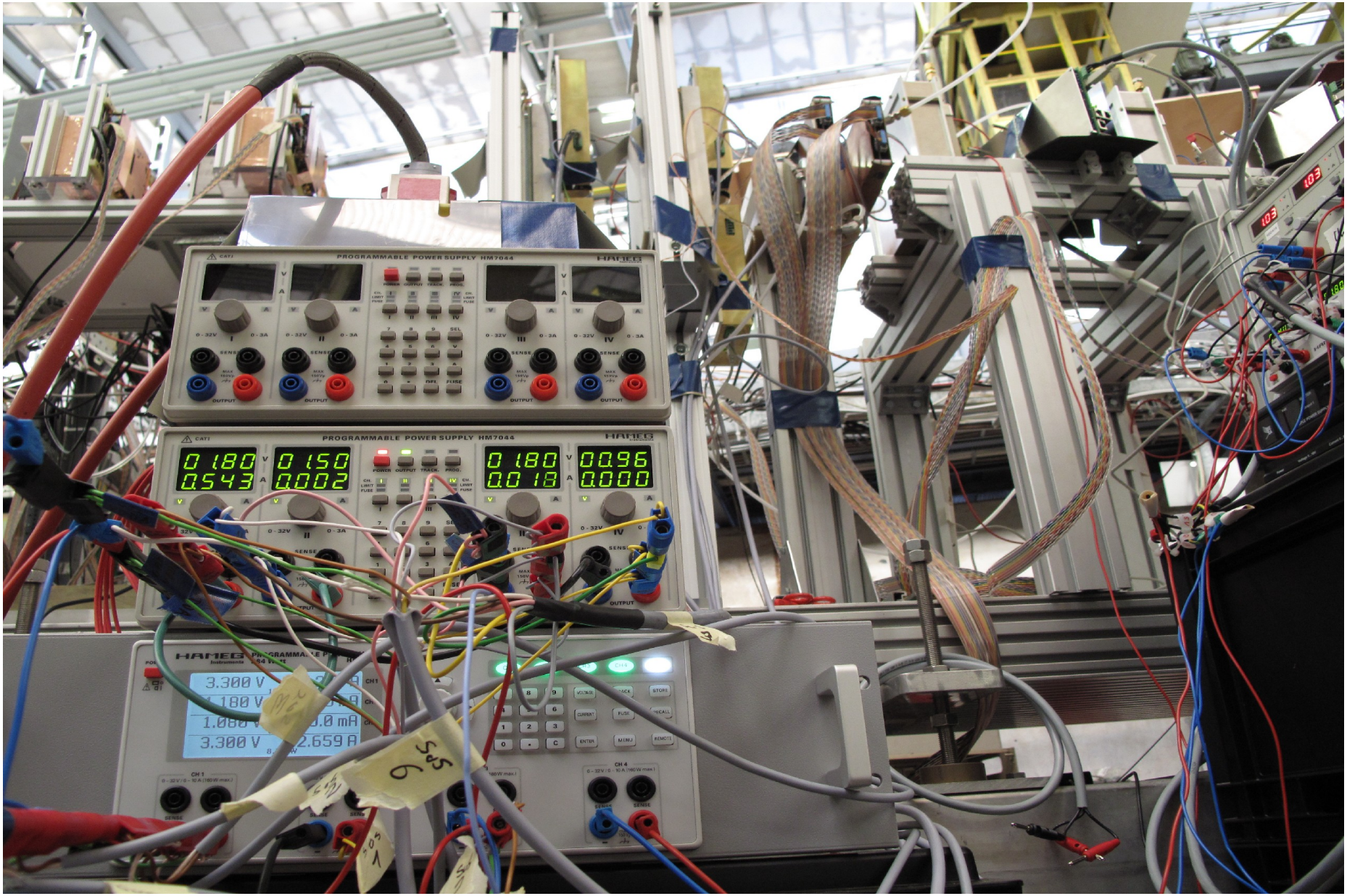
Münster's TRD-SPADIC Setup



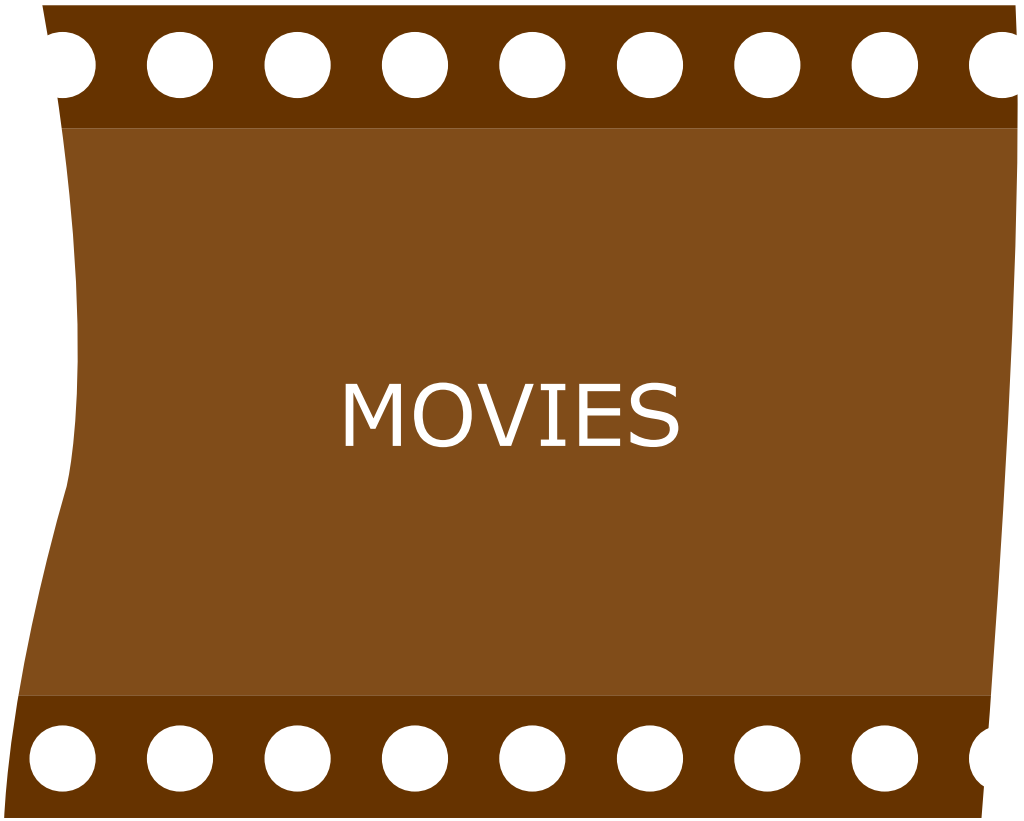
Frankfurt's TRD-SPADIC Setup



Beam Setup


PROGRAMMABLE POWER SUPPLY HM7044
HAMEG
PROGRAMMABLE POWER SUPPLY HM7044
HAMEG
0.180
0.543
0.150
0.002
0.180
0.018
0.096
0.000
HAMEG
3.300 V
180 V
1.080 V
0.0 mA
3.300 V
2.659 A

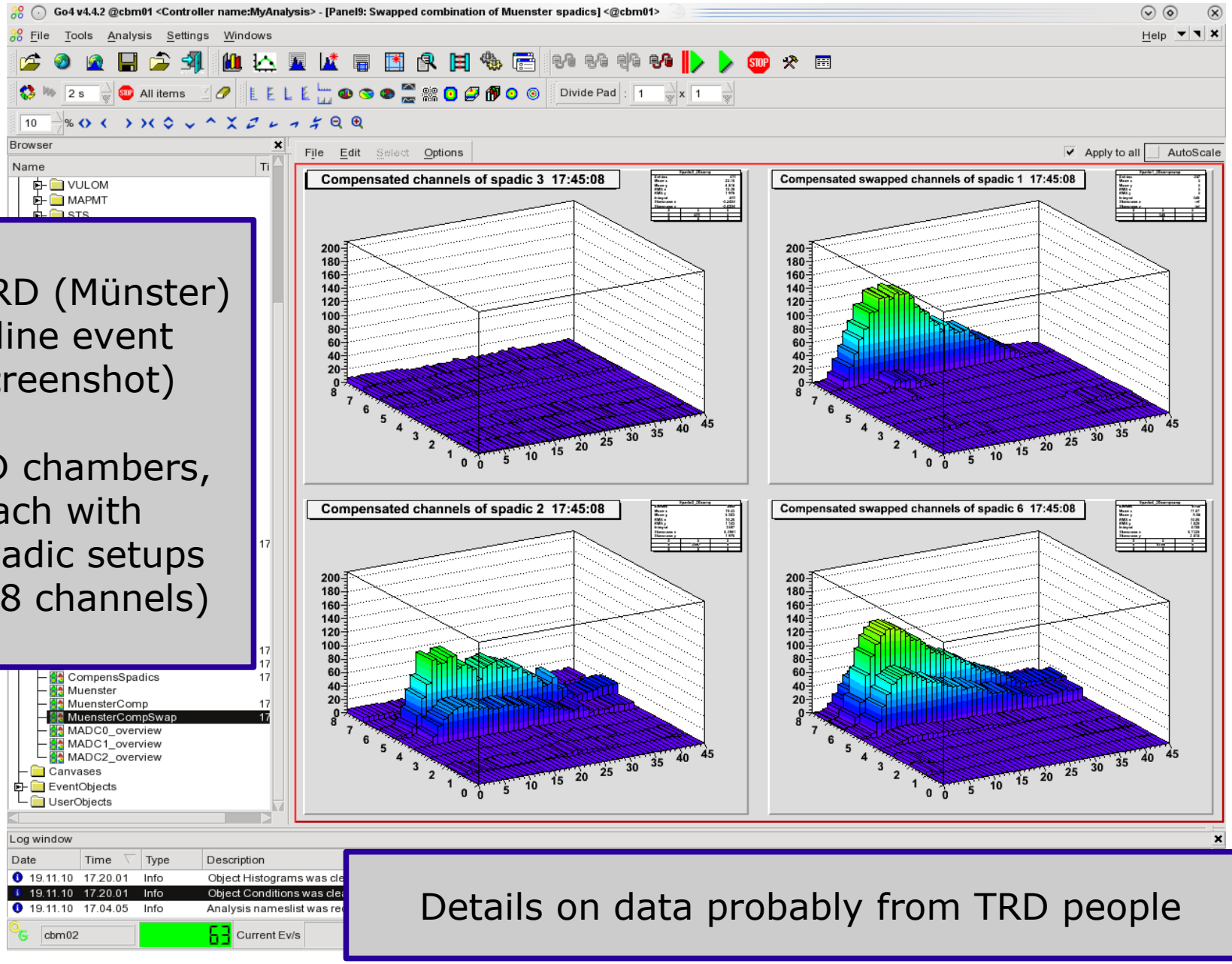
Beam Setup



Go4 Spadic online event

Go4 TRD (Münster) online event (screenshot)

2 TRD chambers, each with 2 Spadic setups (2 x 8 channels)



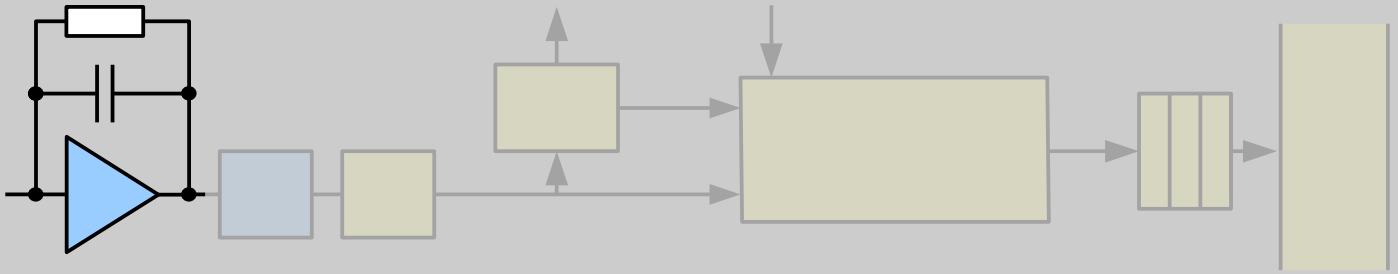
Details on data probably from TRD people

Results from an electronic's point of view

- Bad :-(
  - Many problems with pickup (external noise) – a lot of effort was necessary to reduce the different kinds of oscillation to a tolerable minimum
  - **Even after "optimization" some boards still showed strong oscillations**
  - (Due to known reasons) the chip's configuration was very unstable – a lot of re-configurations/restarts were necessary
  - Strange baseline-shift (DC-level) of shaper outputs if detectors were connected AND the ADCs were running (yet there was no time to investigate this)
- Good :-)
  - 8 Spadic/Susibo setups finished just in time
  - Successful integration of Spadic software library into DABC (thanks to Sergey and Jörn)
  - External triggering-scheme worked well
  - Finally 6 working Spadic setups in parallel (4 x Münster, 2x Frankfurt)
  - **A lot of nice hits could be recorded** (but also some ugly)

3. Towards SPADIC 1.0

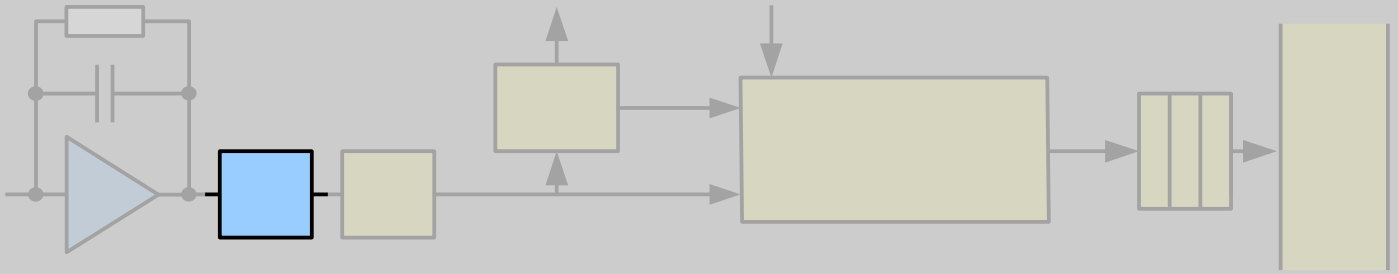
Spadic 1.0: Preamplifier / Shaper



- Charge sensitive preamplifier (CSA)
  - Single ended, N-MOS input
  - Input protection
  - Switchable polarity
  - Switchable # amplifier cells
- Shaper
  - 2nd order, PZ-cancellation, 82 ns
  - Switchable shaping-time
  - Increased order
- Both
  - 750e ENC @ 30 pF, 3.8 mW
  - Switchable gain

Already Available
Planned feature
Possible feature

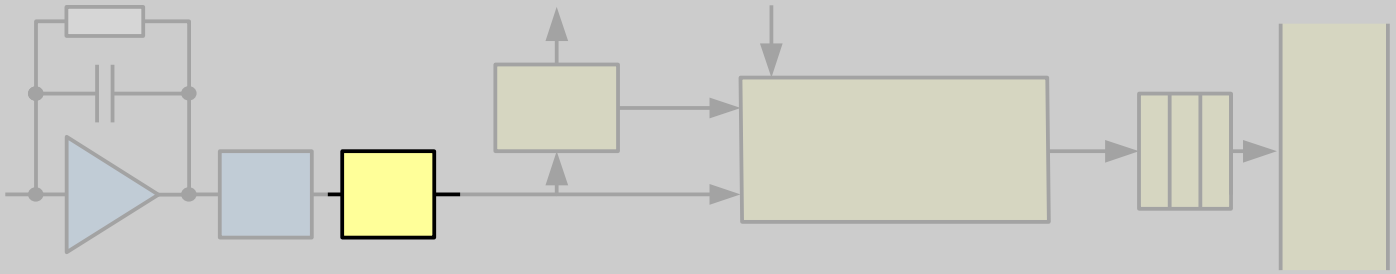
Spadic 1.0: ADC



- Pipeline ADC, continuously running
  - Current-mode algorithmic ADC
  - 9 Bit design, 7.5 Bit effective
  - Up to 25 Msamples/s
  - 4.5 mW / rad-tolerant
  - Slightly better resolution (~ 8 Bit)
  - High resolution (> 8 Bit), possible but very expensive in terms of man-power, power consumption, chip area, …
  - Improved DC-Level / baseline adjustment mechanism

Already Available
Planned feature
Possible feature

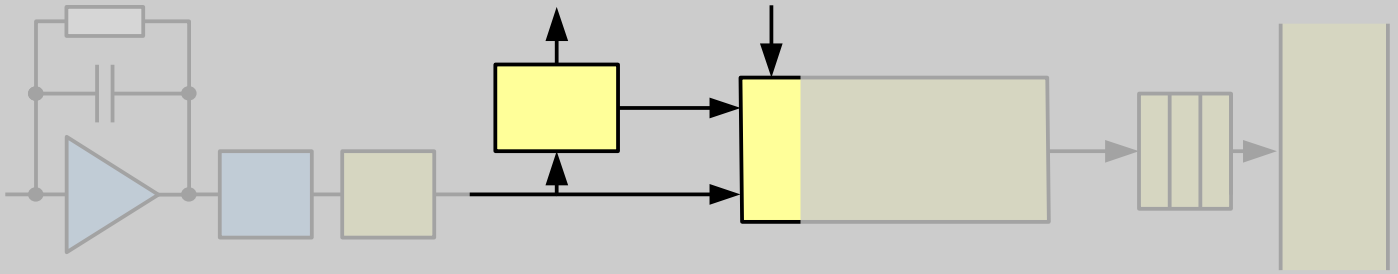
Spadic 1.0: Infinite Impulse Response Filter (IIR)



- IIR Filter / data pre-processing
  - Michael Krieger's diploma thesis
  - Simulation framework developed
  - 10-14 Bit multiplier + adder
  - Ion-tail cancellation
  - Baseline correction
  - Higher order shaping
  - (Simple) additional ideas ???

Already Available
Planned feature
Possible feature

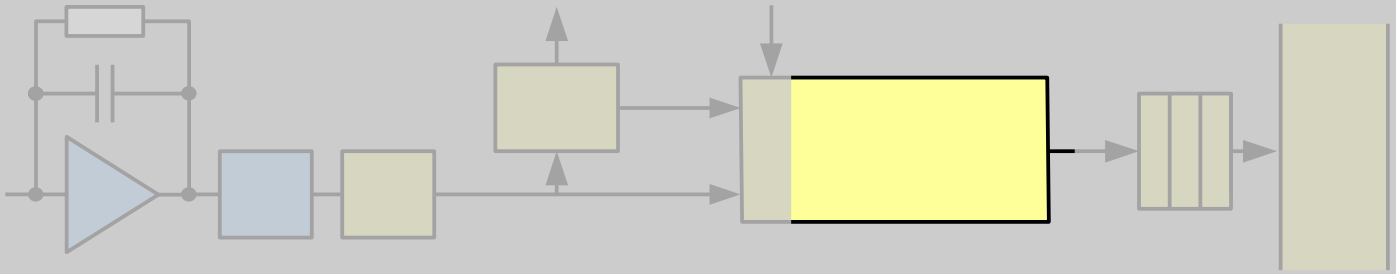
Spadic 1.0: Hit Detector and Neighbor Trigger



- Digital hit detector
  - Digital hit extraction logic
  - Different hit extraction schemes (threshold, double threshold, pulse length, …)
  - 1th order Verilog, simulation works
- Neighbor readout logic
  - Automatic readout of neighbor channels
  - Trigger signal across chip edges
  - 1th order Verilog, simulation works

Already Available
Planned feature
Possible feature

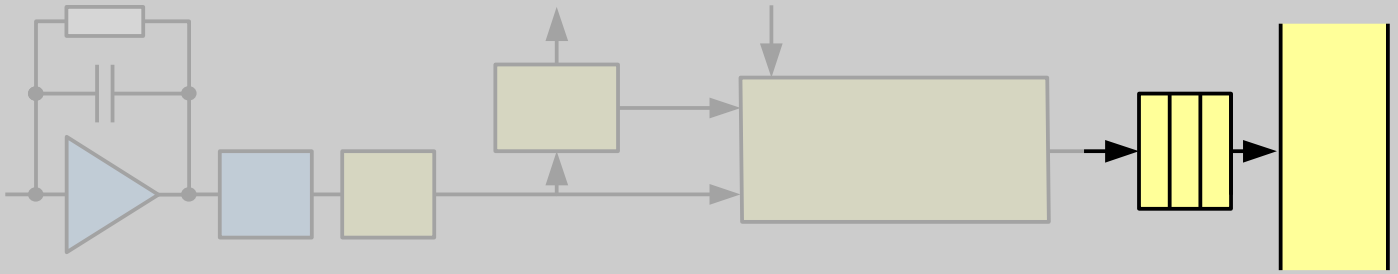
Spadic 1.0: Meta Data Generator and Package Builder



- Meta Data Generator
  - Local and external time-stamp extraction
  - Hit type extraction (internal, neighbor, …)
  - Channel #, Chip ID, …
  - 1th order Verilog, simulation works
- Package builder
  - Generation of hit package including meta and hit data
  - 1th order Verilog, simulation works

Already Available
Planned feature
Possible feature

Spadic 1.0: Output Interface



- Output Interface
  - FIFO package buffer
    - Need access to some UMC 018 SRAM generator
  - Token ring inter-channel network
  - Sophisticated deterministic latency output protocol (Frank Lemke)
  - CBM DAQ compatible !!!
  - Serializer
  - Output driver

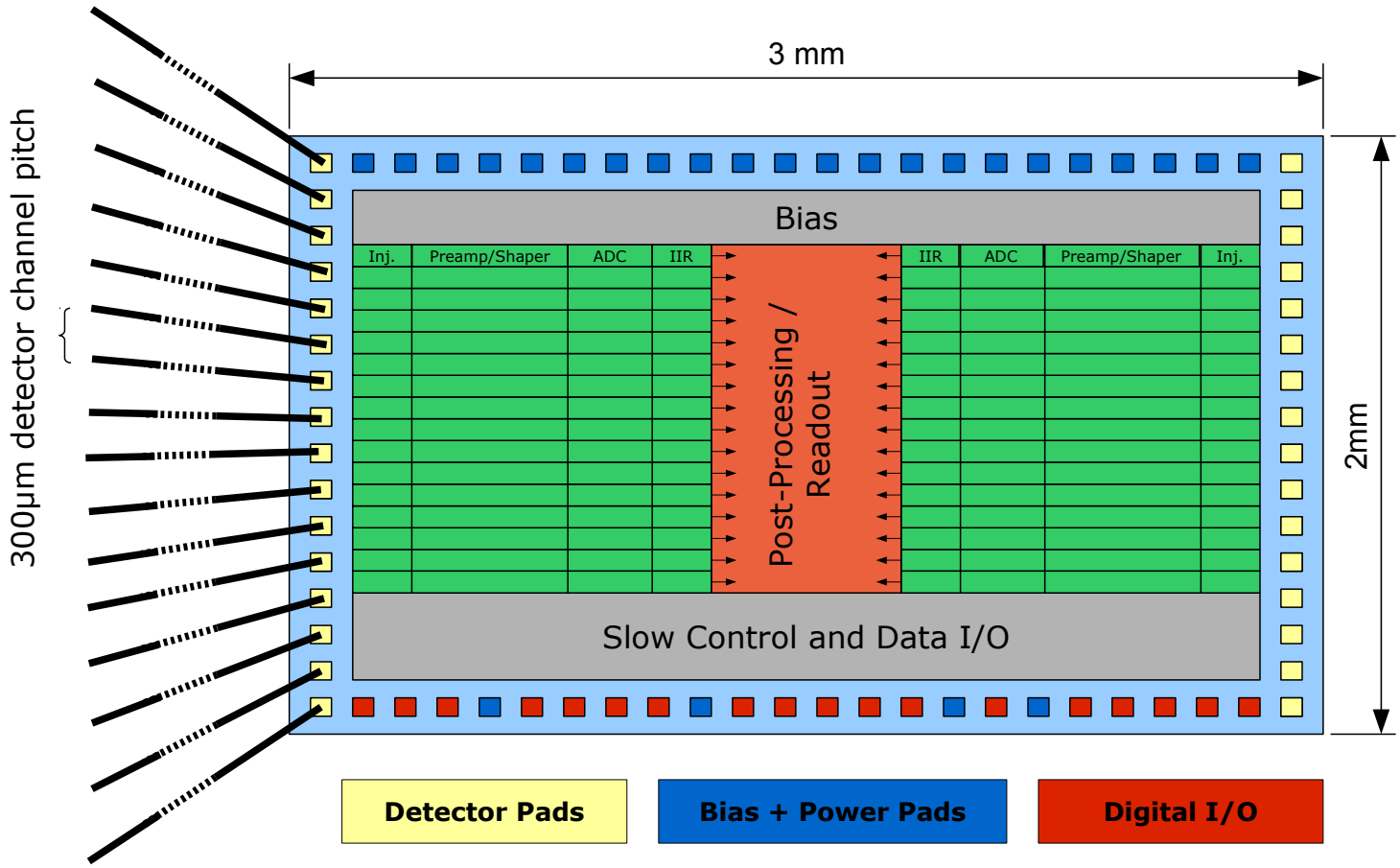
Already Available
Planned feature
Possible feature

Chip Concept

Planned feature
Possible feature

- Features on chip-level
  - 32 channels / chip (maybe 64)
  - Several test mechanisms (test injection, analog signal access, …)
  - On-chip bias circuitry (current DACs + diodes)
  - A lot of global and local configuration registers
  - Maskable channels
  - Power consumption / channel: analog ~ 10mW, digital ??? → power limit?
  - Data: LVDS inputs / outputs only
  - Additional channel as global reference to eliminate systematic disturbances (e.g. pick-up)

Floor Plan Proposal



- 3 x 2 mm² estimated die size
- 32 channels, 80µm pitch, (mostly) symmetric layout for low(er) IR-drops
- Detector connection-pads on two sides (chips will probably be attached to back of detector-module, this relaxes routing/spacing)

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