



# SPADIC: Front-End ASIC for CBM TRD

... and its potential use for MUCH



Tim Armbruster

tim.armbruster@ziti.uni-heidelberg.de

Muon Detector Workshop @ GSI

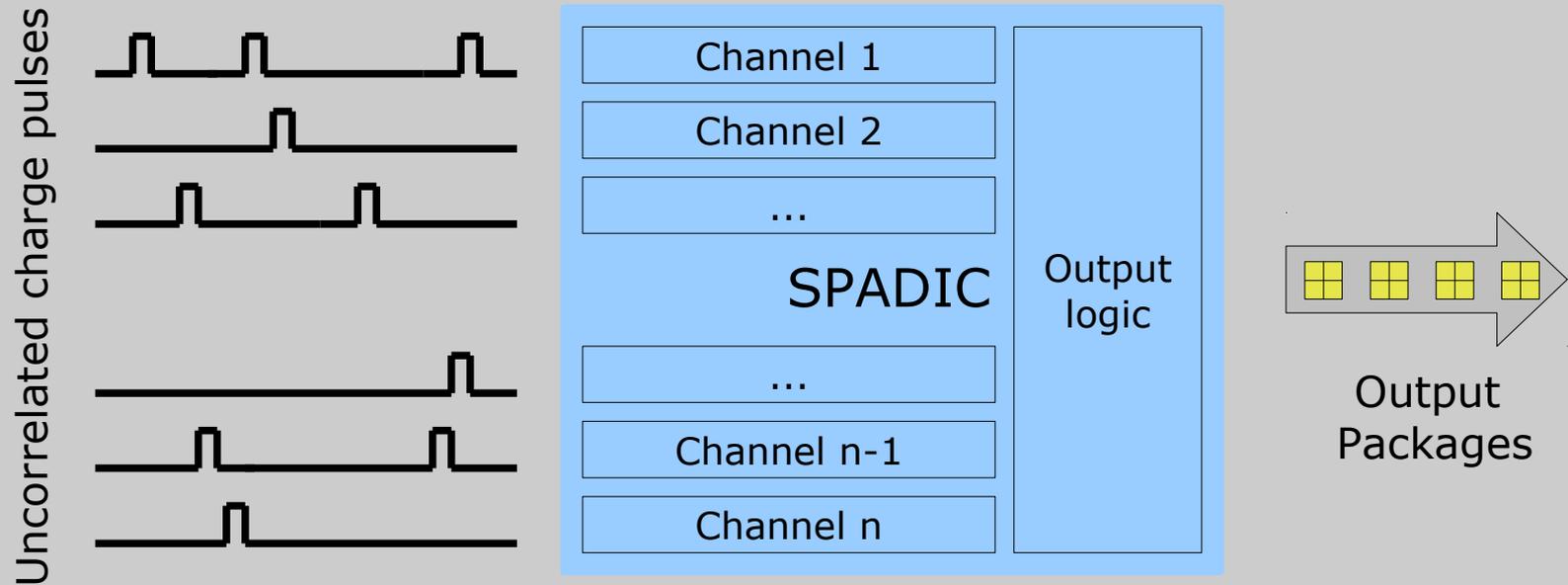
January 2011

Visit <http://spadic.uni-hd.de>

# 1. (Planned) Final SPADIC Architecture

# Introduction to SPADIC

## SPADIC: **S**elf-triggered **P**ulse **A**mplification and **D**igitization as**IC**



### Abstract Data Flow Concept

Charge Pulse Amplification and Shaping →  
Continuous Digitization →  
Continuous Filtering →  
Digital Hit Detection →  
Package building  
(pulse snap-shots plus meta-data) →  
Fast serial output interface

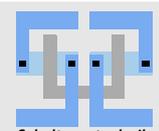
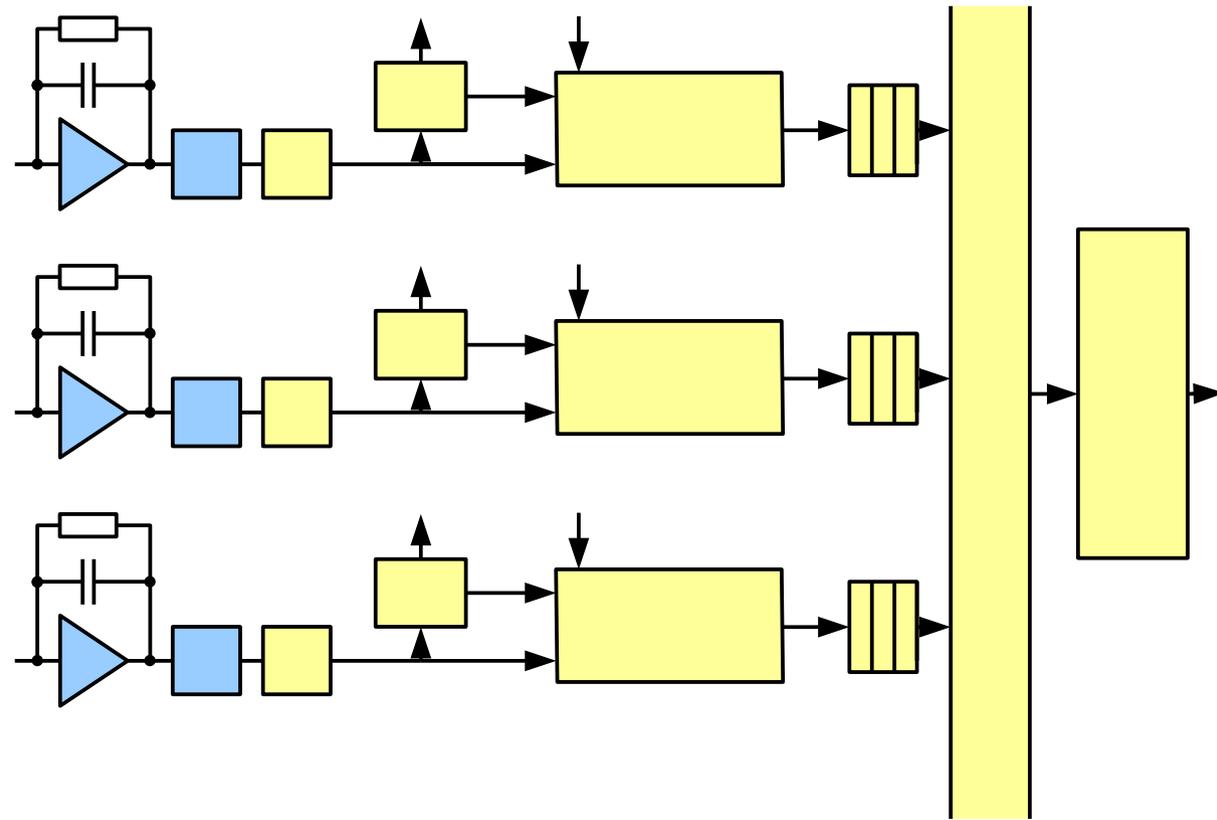
### SPADIC applications

- TRD
- Maybe RICH
- MUCH ?
- ...

# Planned SPADIC Architecture and Building Blocks

- 32 channels ASIC in UMC 180 nm
- Basic channel structure
  - Input protection
  - Preamplifier / Shaper ( $\sim 90$  ns shaping time, positive pulses)
  - ADC ( $\sim 8$  Bit)
  - IIR Filter (ion-tail cancellation, baseline correction, ...)
  - Digital trigger logic (self-triggered scheme)
  - Package builder (payload, timestamp, channel #, ...)
- Global parts after the channels
  - Inter-channel network (token ring)
  - DAQ compatible protocol encoder (computer architecture group, HD)
  - Serializer, driver (two 500 Mbit/s links per chip)

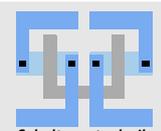
( New parts / Already realized parts )



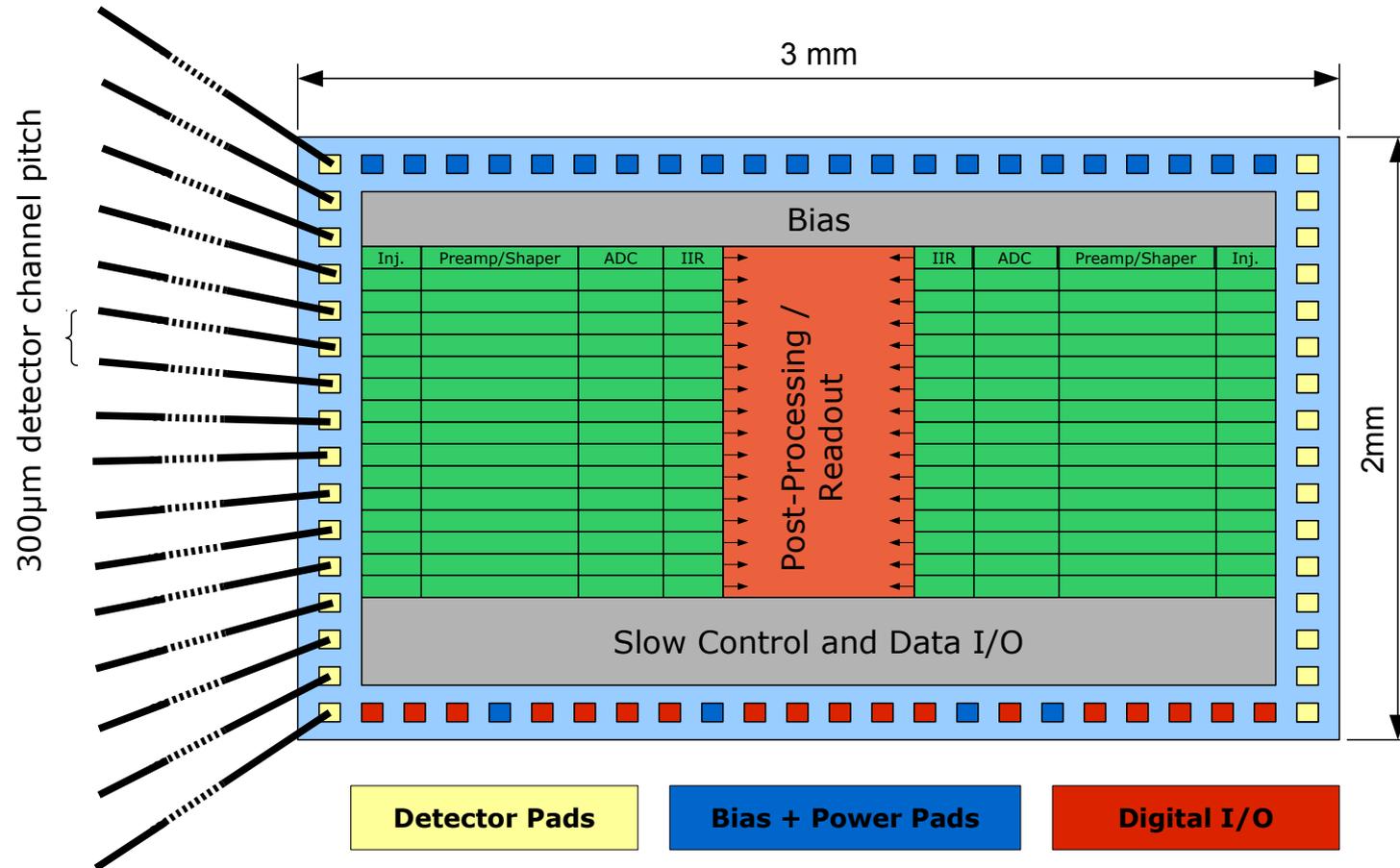
# Additional Features

## (Possible) Additional Features

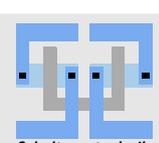
- Preamplifier/Shaper
  - Switchable tradeoff between preamplifier noise and power consumption
  - Input mode for large negative input pulses (up to  $10^6$  electrons, RICH)
  - Switchable gain (2-4 steps)
  - Switchable shaping time (2-4 steps)
- Digital
  - Different hit detection modes (e.g. single-/dual-threshold)
  - Neighbor readout (channels will be able to trigger the readout of neighbor channels)
  - Pulse data selection mask (select only certain values of a digitized pulse)



# Floor Plan Proposal

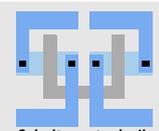
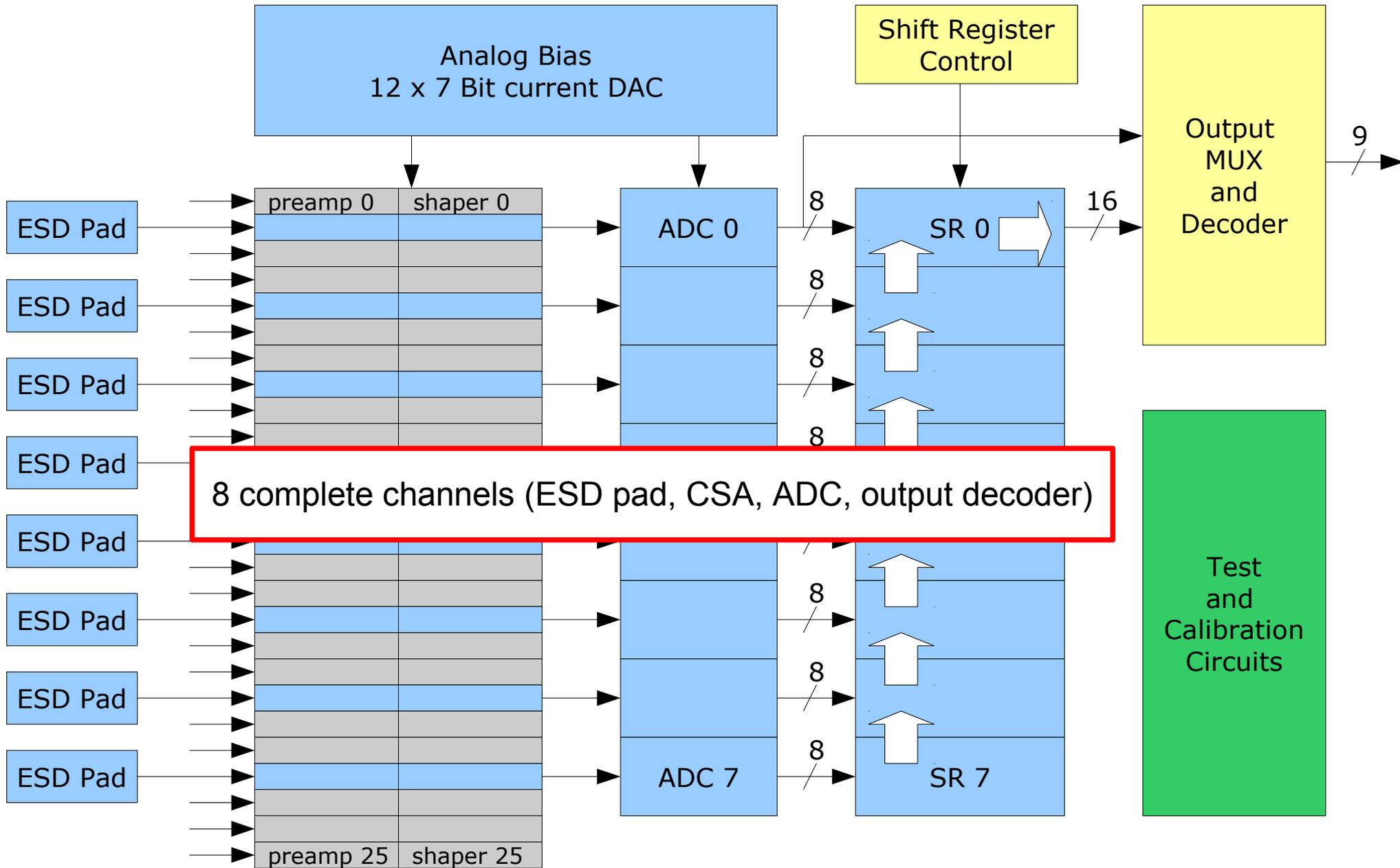


- 3 x 2 mm<sup>2</sup> estimated die size
- 32 channels, 80 μm pitch
- Option in discussion: Detector connections on two sides (relaxes routing/spacing)

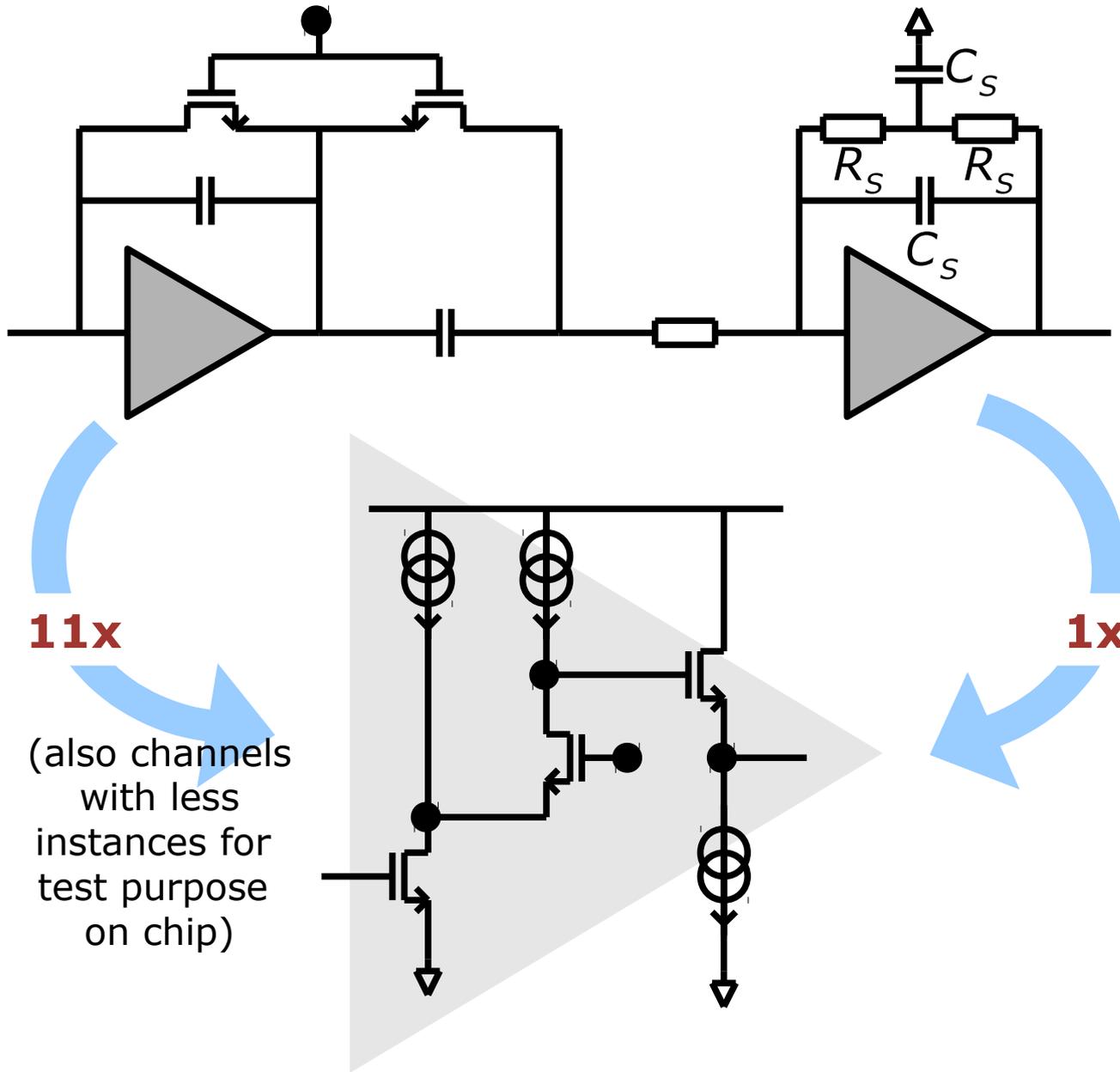


## 2. Status of the Latest SPADIC Version

# Block Diagram of Latest SPADIC v0.3



# Front-End Amplifier: Preamplifier/Shaper Circuit



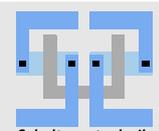
$$H(s) \approx \frac{A_{DC}}{(1 + sR_S C_S)^2}$$

**11x**

(also channels with less instances for test purpose on chip)

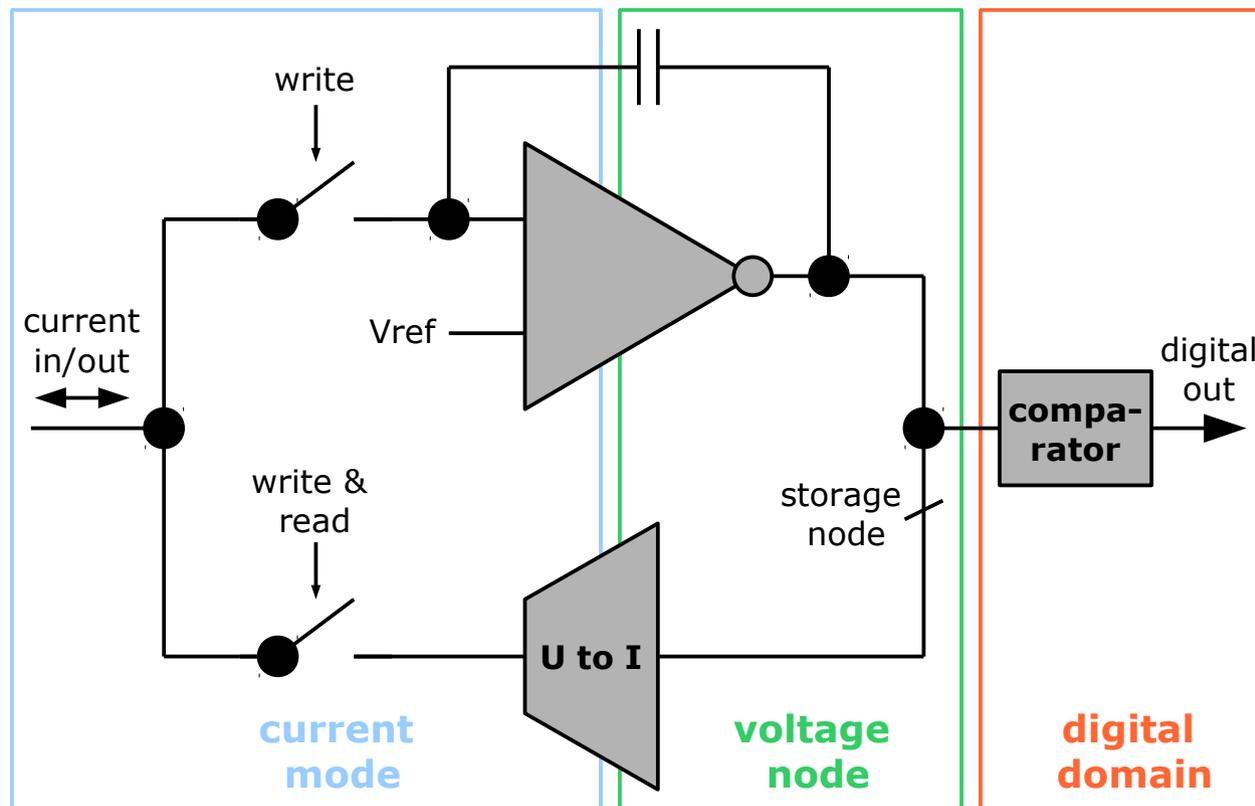
**1x**

- O'Connor FB
- 2<sup>nd</sup> order shaper
- Shaping time: 82 ns
- Unified amplifier cell
- N-MOS input
- $\approx 3.6$  mW/channel

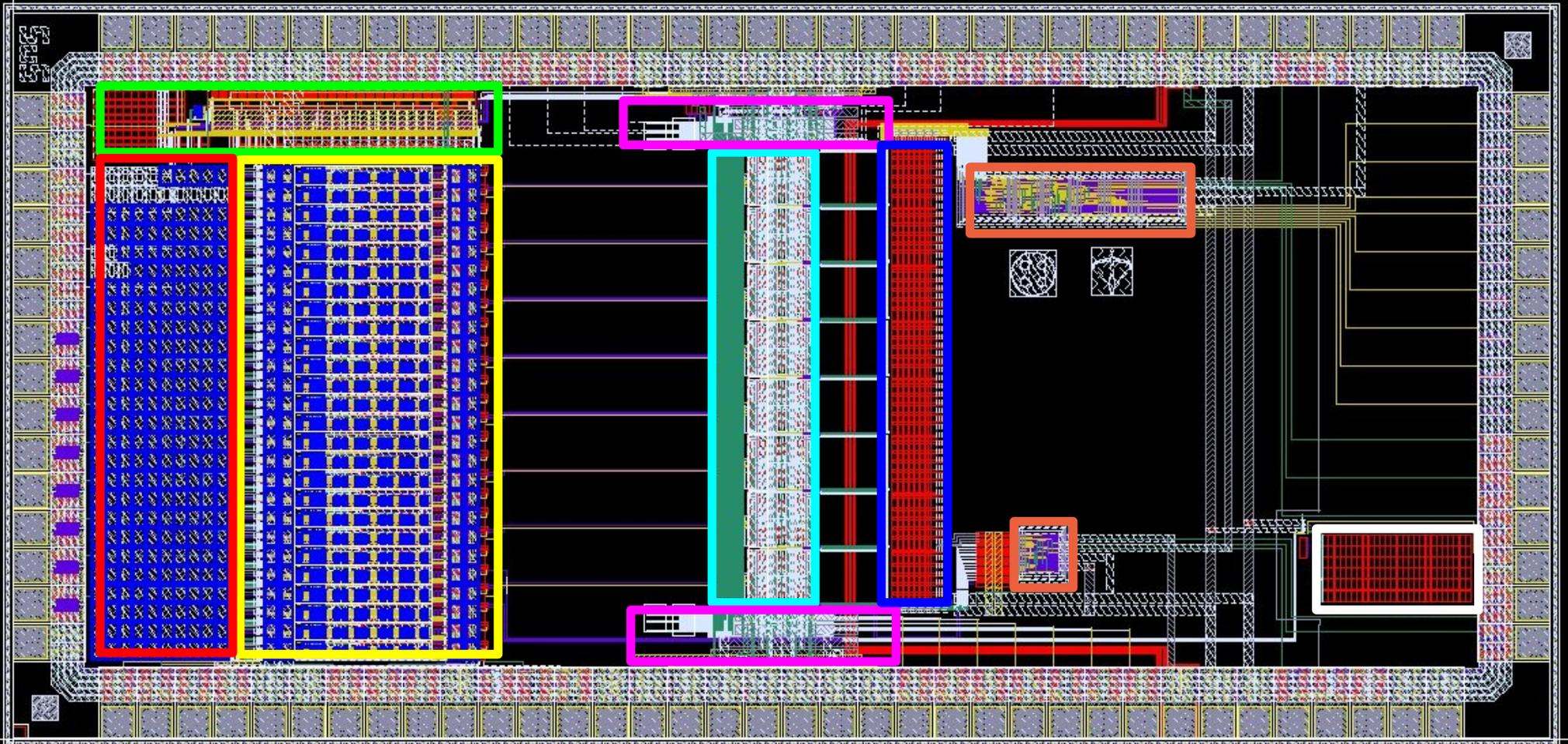


# Algorithmic ADC Design

- 8 (scaled) pipeline stages, therefore 9 Bit design, **7.5 Bits effective** so far
- Algorithmic working principle (“1.5 redundant Bits” / conversion step)
- **25 MSamples/s, layout only 130x120  $\mu\text{m}^2$ , power consumption 4.5 mW**
- Core unit: Novel current storage cell:



# Latest SPADIC: Layout



Bias circuitry (12 current DACs)

26 preamp/shaper channels

Detector capacitors (5pF per block)

8 pipelined ADCs

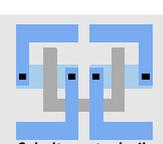
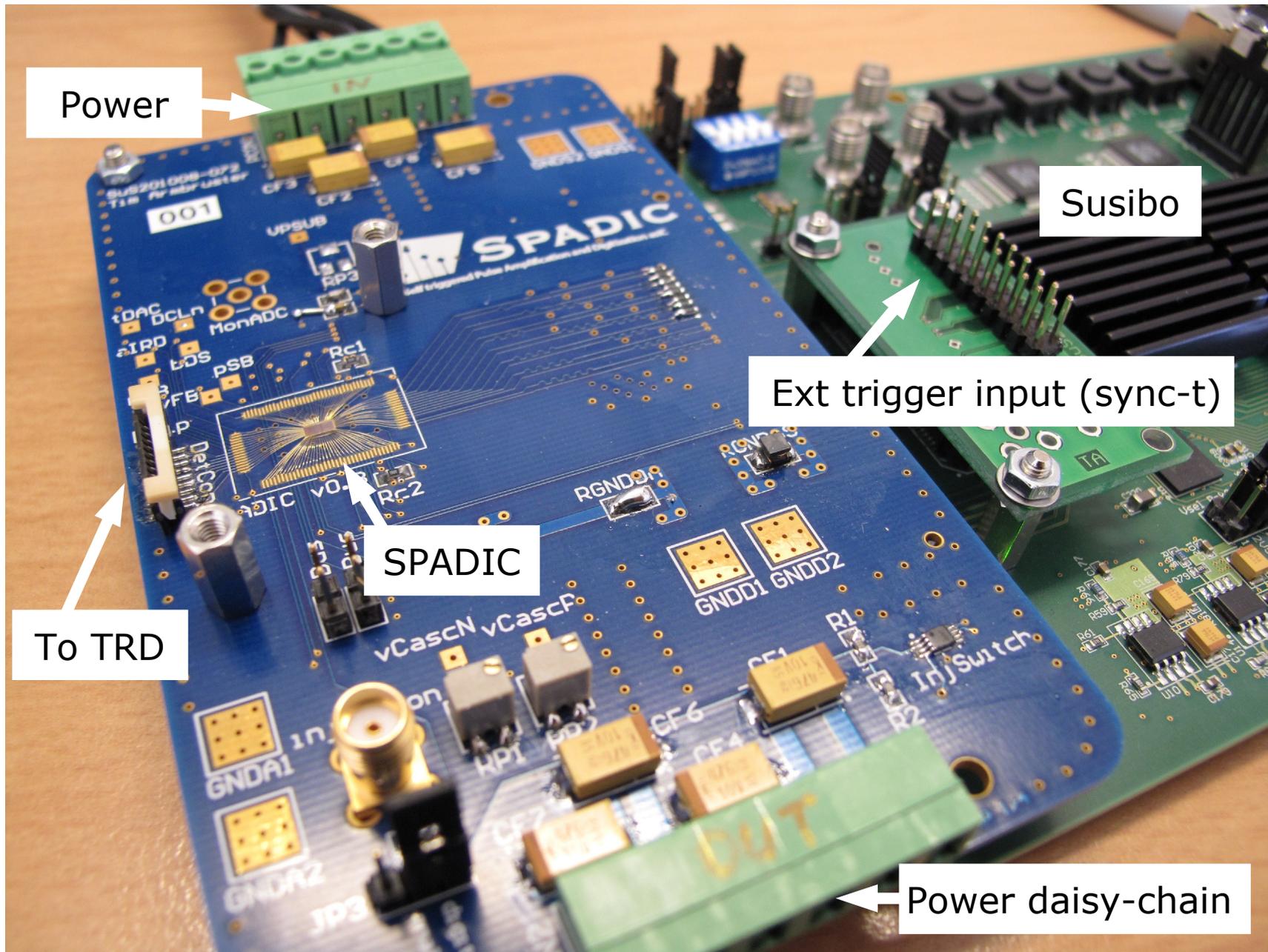
ADC control + bias

5.2 kBit shift register matrix

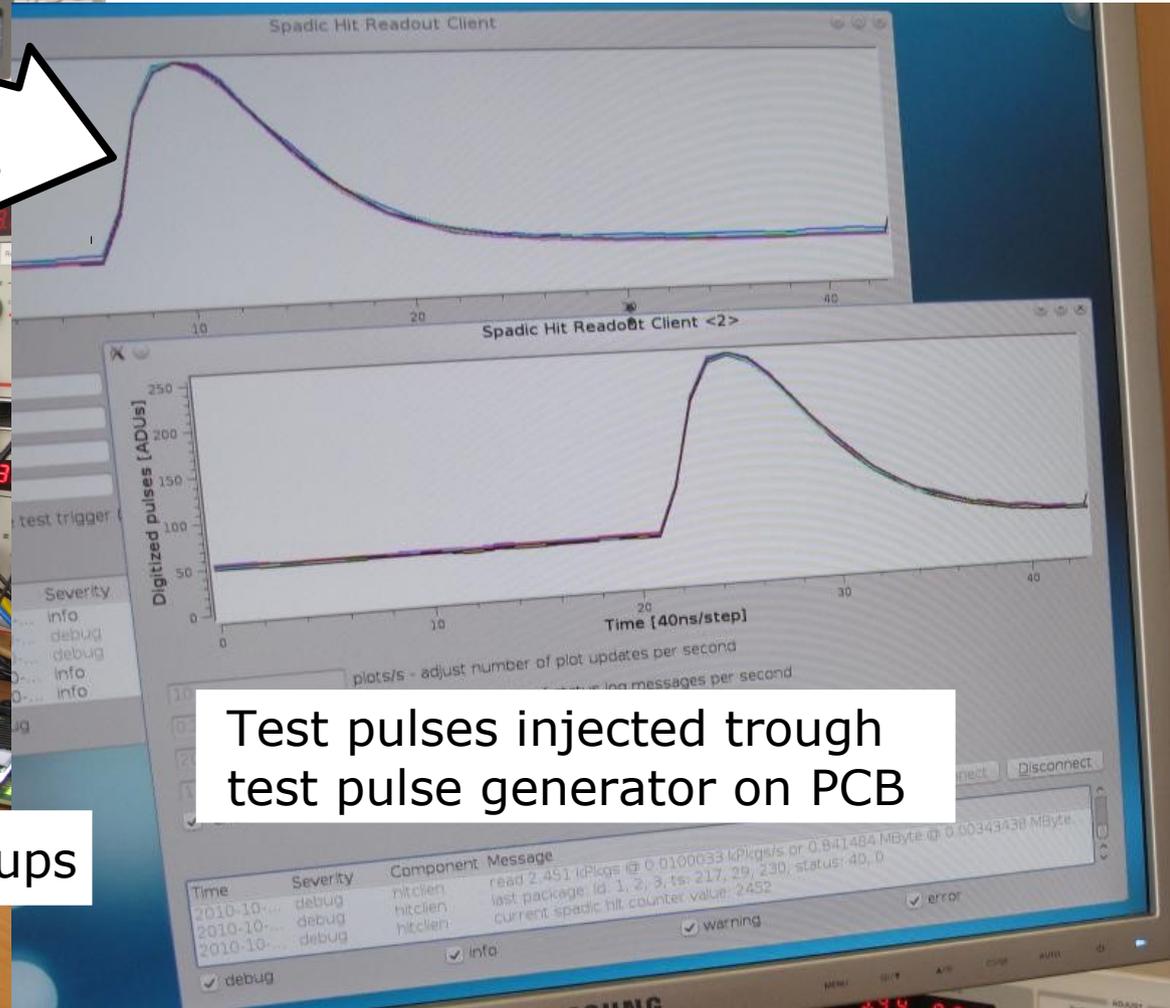
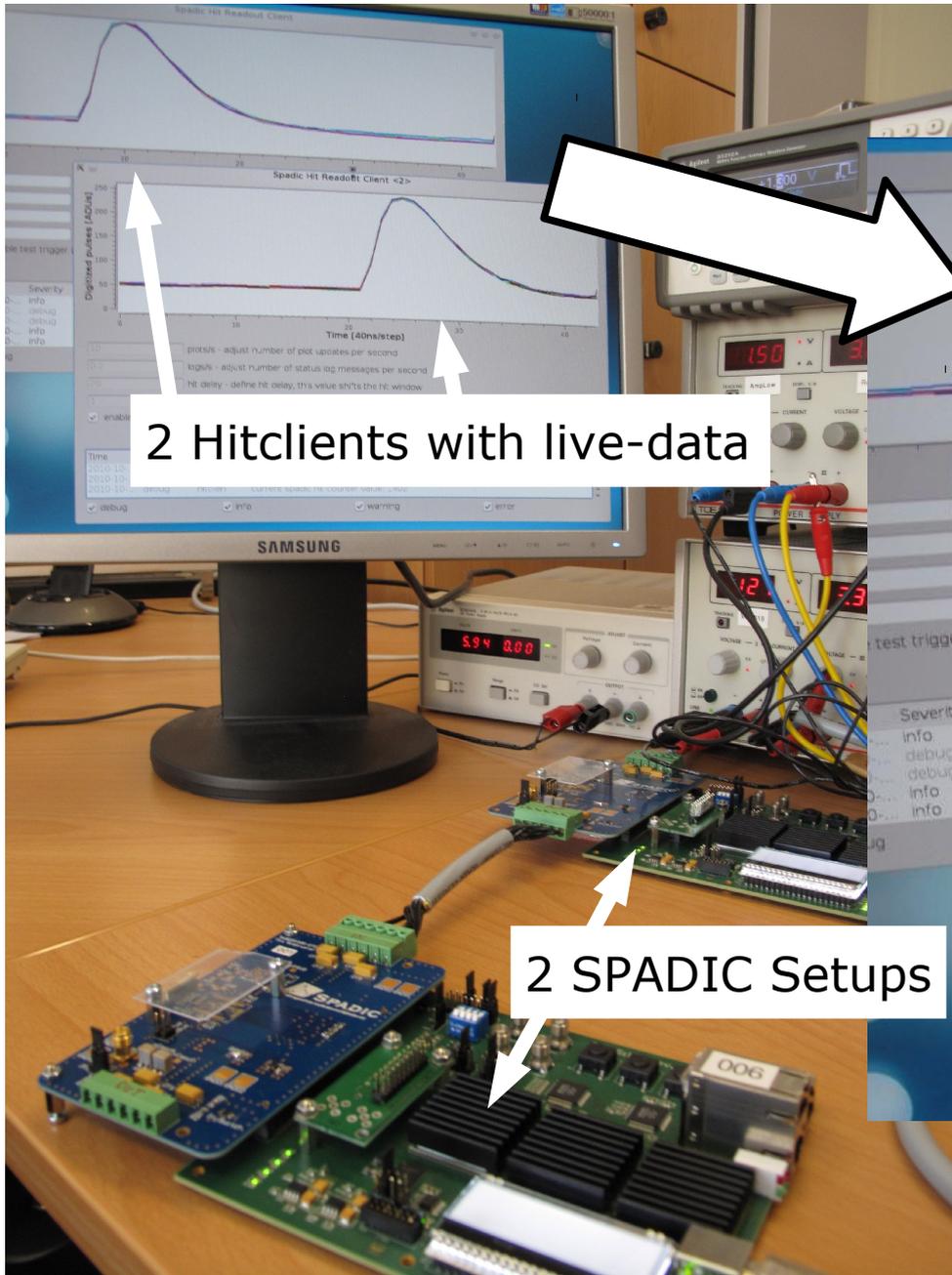
Control + readout/decoder logic blocks

Test circuits

# Test-Setup: SPADIC plugged on Susibo

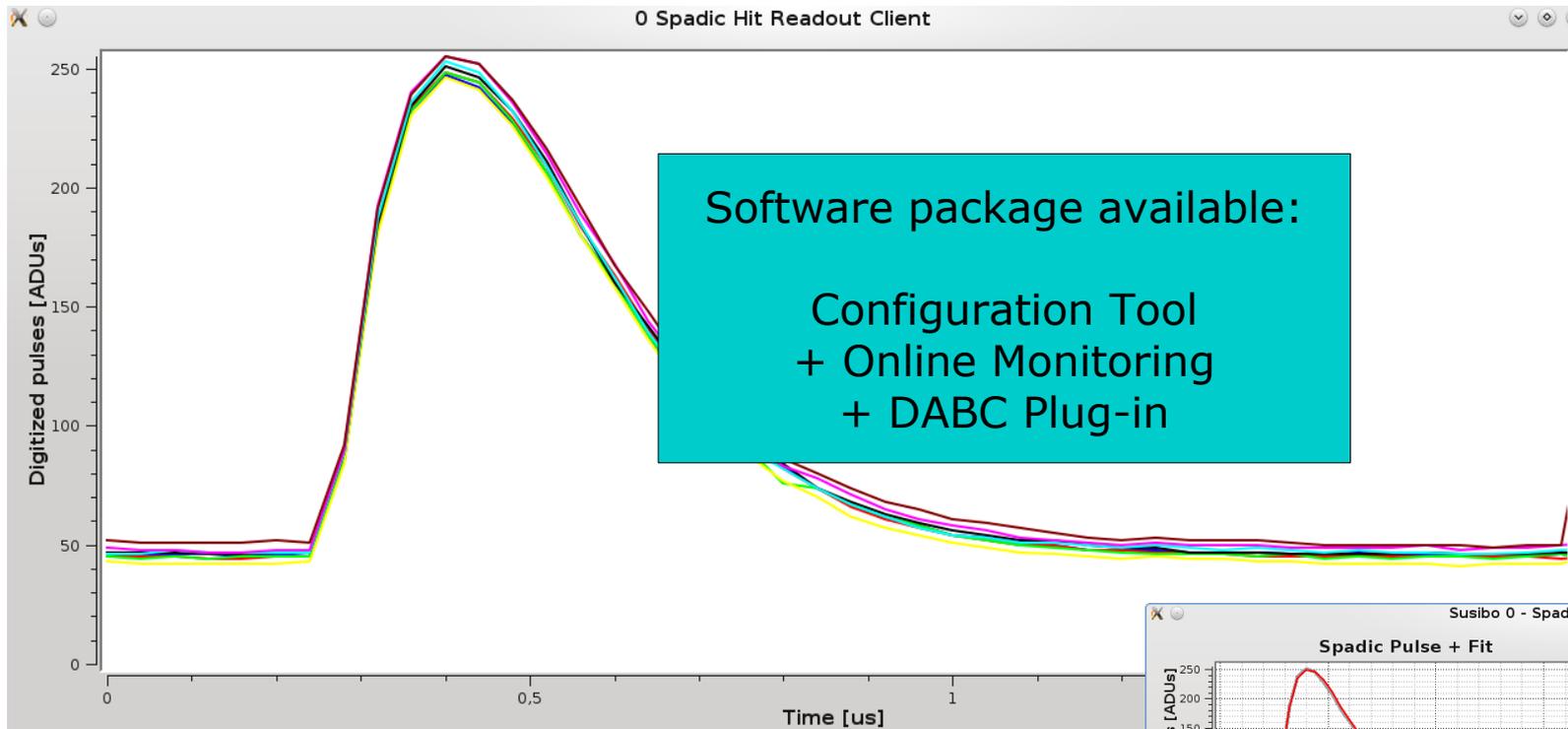


# Setup in Lab



2 Hitclients with live-data

# Hitclient Screenshot



Software package available:  
 Configuration Tool  
 + Online Monitoring  
 + DABC Plug-in

Configuration

10 plots/s - adjust number of plot updates per second

0.2 logs/s - adjust number of status log messages per second

35 hit delay - define hit delay, this value shifts the hit window

0 susibo serial number - '0' means connect any

enable test trigger

Analysis

show frequency spectrum

logarithmic frequency scale

logarithmic magnitude scale

average 1000

Time	Severity	Component	Message
2010-11-...	debug	hitclien	read 0.111 kPkgs @ 0.00169925 kPkgs/s or 0.0381088 MByte @ 0.0005833
2010-11-...	debug	hitclien	last package: id: 1, 2, 3, ts: 142, 110, 28, status: 70, 0
2010-11-...	debug	hitclien	current spadic hit counter value: 113
2010-11-...	debug	hitclien	read 0.126 kPkgs @ 0.00179725 kPkgs/s or 0.0432587 MByte @ 0.0006170
2010-11-...	debug	hitclien	last package: id: 1, 2, 3, ts: 169, 91, 67, status: 70, 0
2010-11-...	debug	hitclien	current spadic hit counter value: 128

debug  info  warning

Susibo 0 - Spadic Hit Readout Client

Spadic Pulse + Fit

ADC values [ADUs]

Time [us]

Amplitude Histogram

Frequency [Norm.]

Amplitude [ADUs]

Configuration

10 plots/s

0.2 logs/s

35 hit delay

0 susibo serial

enable test trigger

Histogram

record histogram

show:  amplitude  hit time

1 channel number (0-7)

show only reference curve and fit

0.7 max frequency

Spectrum Analysis

show frequency spectrum

logarithmic frequency scale

logarithmic magnitude scale

floating average 1000

Reset

Reset

Reset

Reset

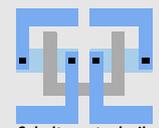
Reset

Reset

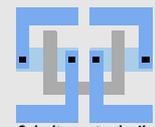
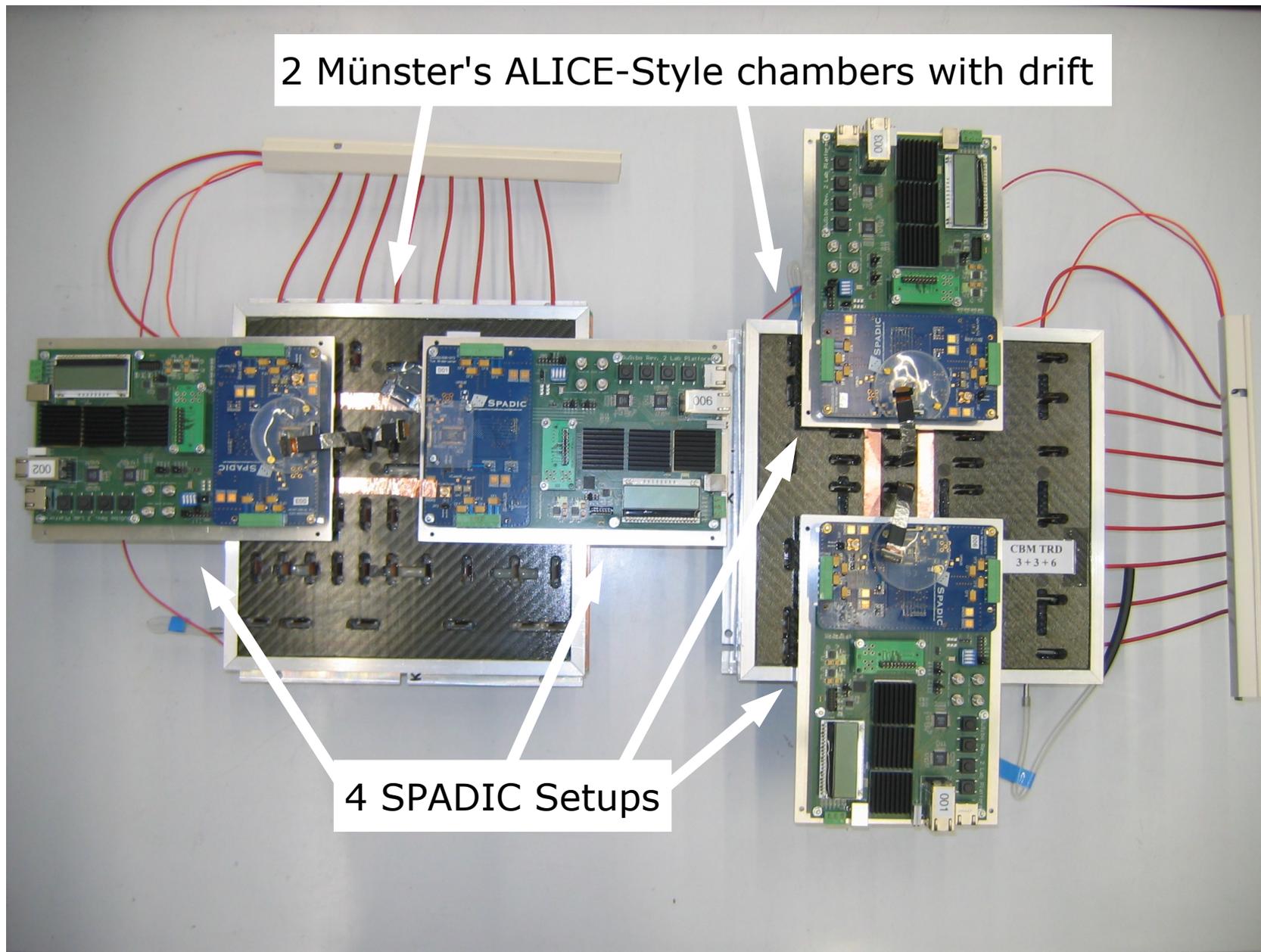
Time	Severity	Component	Message
2010-12-...	debug	hitclien	read 0.099 kPkgs @ 0.00988616 kPkgs/s or 0.033989 MByte @ 0.00339414 MByte...
2010-12-...	debug	hitclien	last package: id: 1, 2, 3, ts: 67, 16, 132, status: 70, 0
2010-12-...	debug	hitclien	current spadic hit counter value: 100
2010-12-...	info	spadic	spadic readout deactivated
2010-12-...	info	spadic	ftdi disconnected

debug  info  warning  error

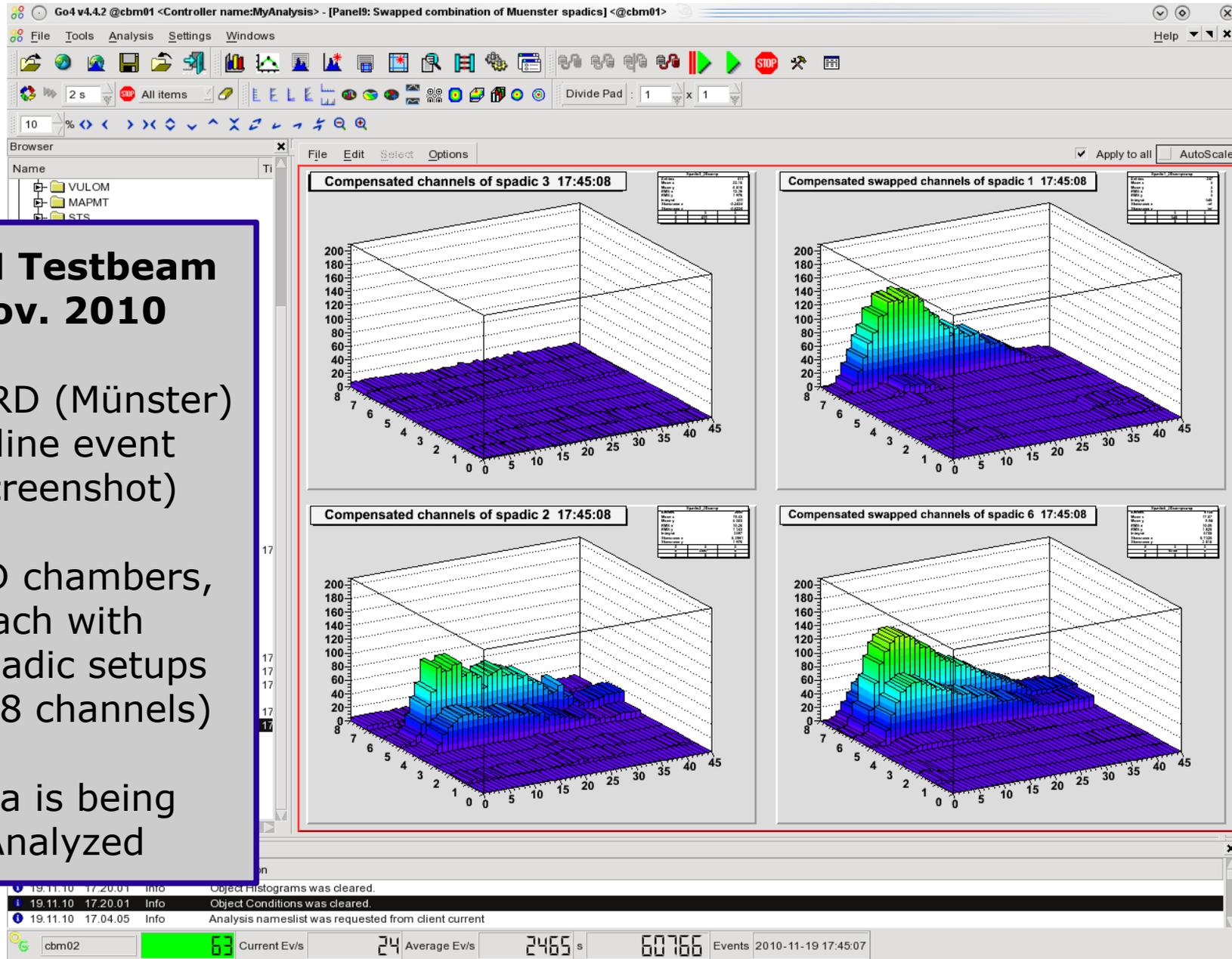
Screenshot of latest version  
 (12/2010)



# CERN Testbeam 2010: Münster's TRD-SPADIC Setup



# CERN Testbeam 2010: Go4 Spadic online event



**CERN Testbeam  
Nov. 2010**

Go4 TRD (Münster)  
online event  
(screenshot)

2 TRD chambers,  
each with  
2 Spadic setups  
(2 x 8 channels)

Data is being  
Analyzed

# 3. MUCH and Summary

# SPADIC Specification

- If MUCH is interested in joining the SPADIC development ...
  - ... we need to write down all MUCH requirements
  - ... we need to compare them to the TRD/RICH requirements
  - ... I'll probably need some helping hands
- A SPADIC specification is currently under construction
  - We should go through the physics requirements table and add a MUCH column

Spadic 1.0 Specification

Tim Armbruster  
November 24, 2010

## 1 Physics requirements

	TRD	RICH
channels / chip	32	opt. 64 (32 ok)
channels / system		64x64=55040
chips / system		
power limit / chip		threshold dispersion
noise limit		
maximum radiation dose		Hamamatsu RS-9
maximum input capacity		
average input capacity		
average event rate		
maximum hit rate per channel		10 kHz
maximum hit rate per channel		10 <sup>6</sup> e
maximum leakage current		5-10 10 <sup>6</sup> e
average charge per hit		Gauss
maximum charge per hit		binary readout
type of energy distribution		pulse (< 10 ns)
measured quantity		8 Bit
input signal shape		target 2 ns (5 ns max.) sigma
required Energy resolution		feature extraction (time, energy)
required time resolution		
special tasks	baseline rec., ion-tail can.	

## 2 Data sheet

### 2.1 Spadic 1.0 data sheet

Parameter	Value	Comment
Technology	UMC 180 nm	
Number of channels	32	
Chip size		
Number of pads		
Total power consumption		
Total dynamic range		

# Summary

- **Status of Latest Prototype (SPADIC v0.3)**

- 8 complete channels (plus 18 test channels)
- Positive input charges, about 0..40fC input range
- 2<sup>nd</sup> order shaping, 90 ns shaping time
- Noise: 800e @ 30 pF capacitive input load
- ADC with 7.5 Bit effective (INL) @ 25 Msamples/s
- Power per Channel/ADC: 3.8/4.5 mW
- Size: 1.5 x 3.2 mm<sup>2</sup>

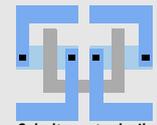
- **Status of Latest Setup**

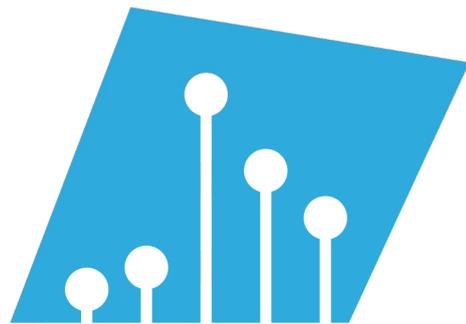
- 8 complete setups have been available @ CERN Testbeam Nov. 2010
- New PCB with low noise layout and reduced ground loops under construction, almost finished
- Ongoing software development

- **First full-blown SPADIC (v1.0)**

- Start of design phase: February 2011
- Planned Submission: summer/fall 2011
- First measurement results end of 2011 at the earliest

If there is any need for additional features (e.g. for MUCH) start discussion now and finish it soon!





# SPADIC

Self triggered Pulse Amplification and Digitization asIC

<http://spadic.uni-hd.de>