UNIVERSITÄT HEIDELBERG

SPADIC: Front-End ASIC for CBM TRD

... and its potential use for MUCH

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Muon Detector Workshop @ GSI

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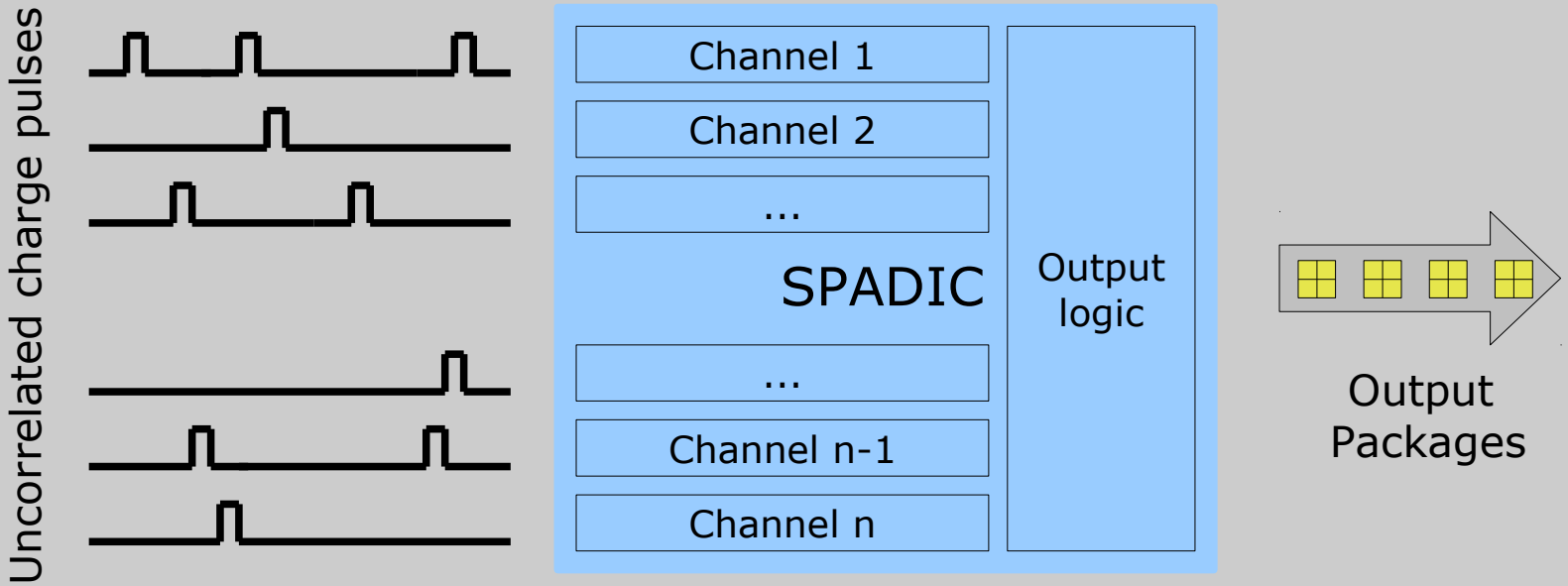
Visit http://spadic.uni-hd.de

1. (Planned) Final SPADIC Architecture

Introduction to SPADIC

SPADIC: **S**elf-triggered **P**ulse **A**mplification and **D**igitization as**IC**



Abstract Data Flow Concept

Charge Pulse Amplification and Shaping →
Continuous Digitization →
Continuous Filtering →
Digital Hit Detection →
Package building
(pulse snap-shots plus meta-data) →
Fast serial output interface

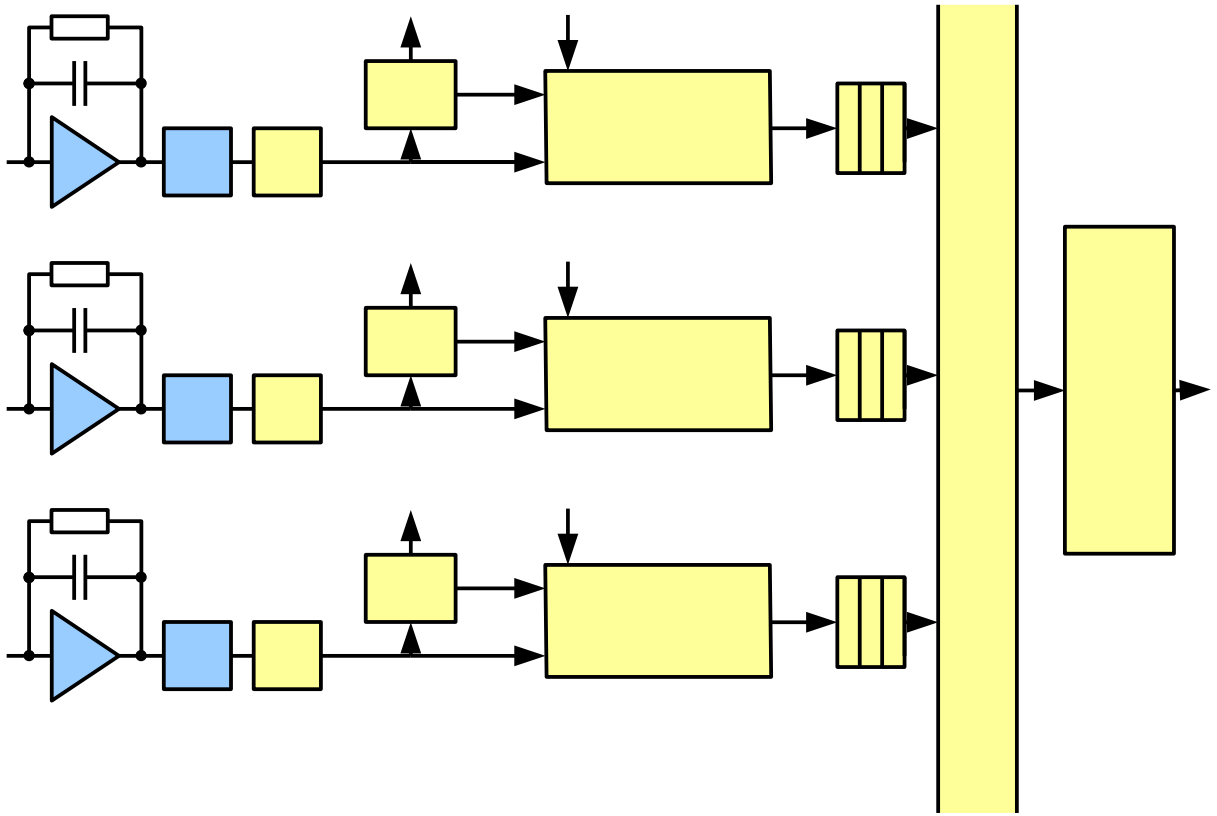
SPADIC applications

- TRD
- Maybe RICH
- MUCH ?
- ...

Planned SPADIC Architecture and Building Blocks

- 32 channels ASIC in UMC 180 nm
- Basic channel structure
  - Input protection
  - Preamplifier / Shaper (~ 90 ns shaping time, positive pulses)
  - ADC (~ 8 Bit)
  - IIR Filter (ion-tail cancellation, baseline correction, ...)
  - Digital trigger logic (self-triggered scheme)
  - Package builder (payload, time-stamp, channel #, …)
- Global parts after the channels
  - Inter-channel network (token ring)
  - DAQ compatible protocol encoder (computer architecture group, HD)
  - Serializer, driver (two 500 Mbit/s links per chip)

(New parts / Already realized parts)

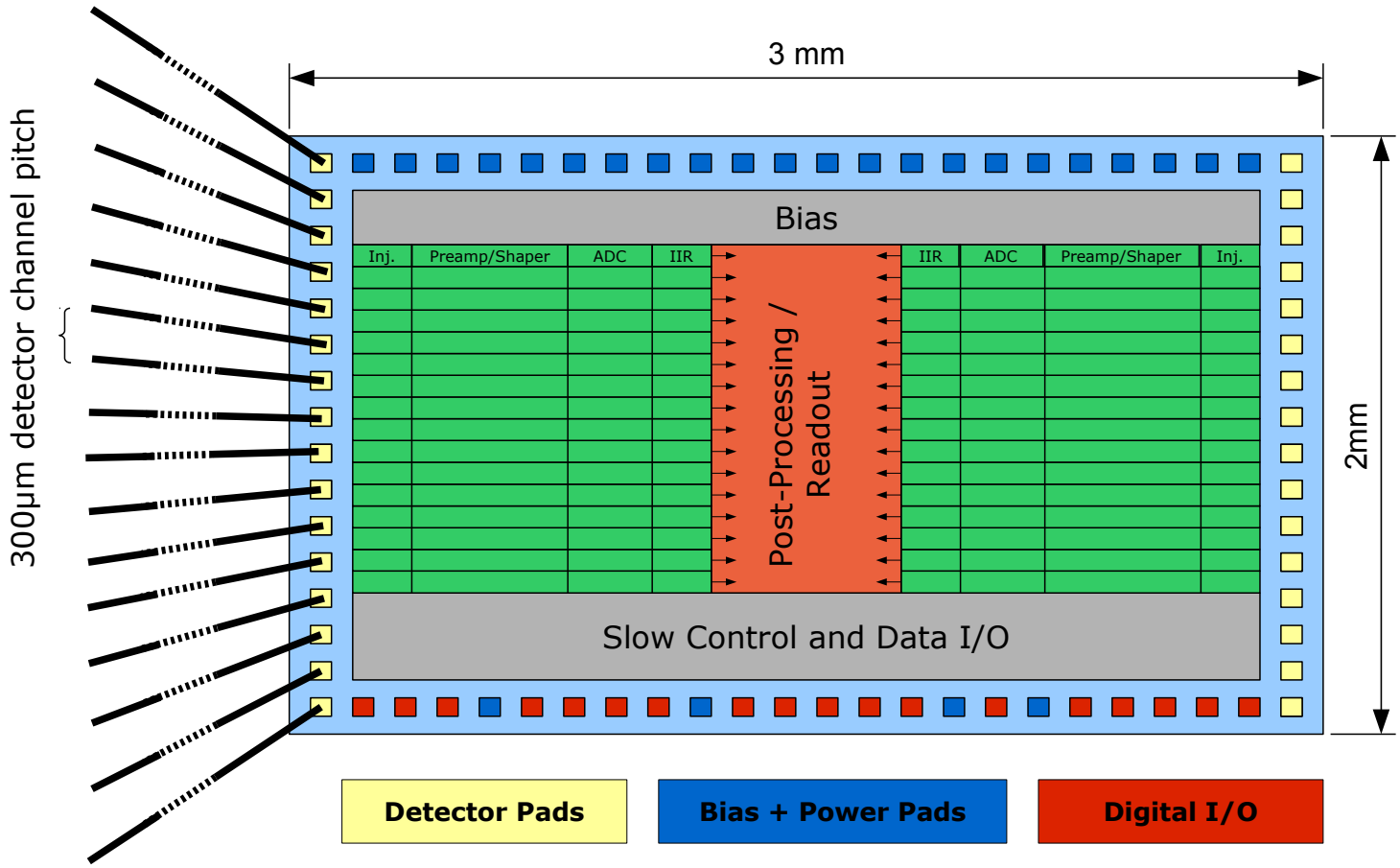


Additional Features

(Possible) Additional Features

- Preamplifier/Shaper
  - Switchable tradeoff between preamplifier noise and power consumption
  - Input mode for large negative input pulses (up to 10^6 electrons, RICH)
  - Switchable gain (2-4 steps)
  - Switchable shaping time (2-4 steps)
- Digital
  - Different hit detection modes (e.g. single-/dual-threshold)
  - Neighbor readout (channels will be able to trigger the readout of neigbor channels)
  - Pulse data selection mask (select only certain values of a digitized pulse)

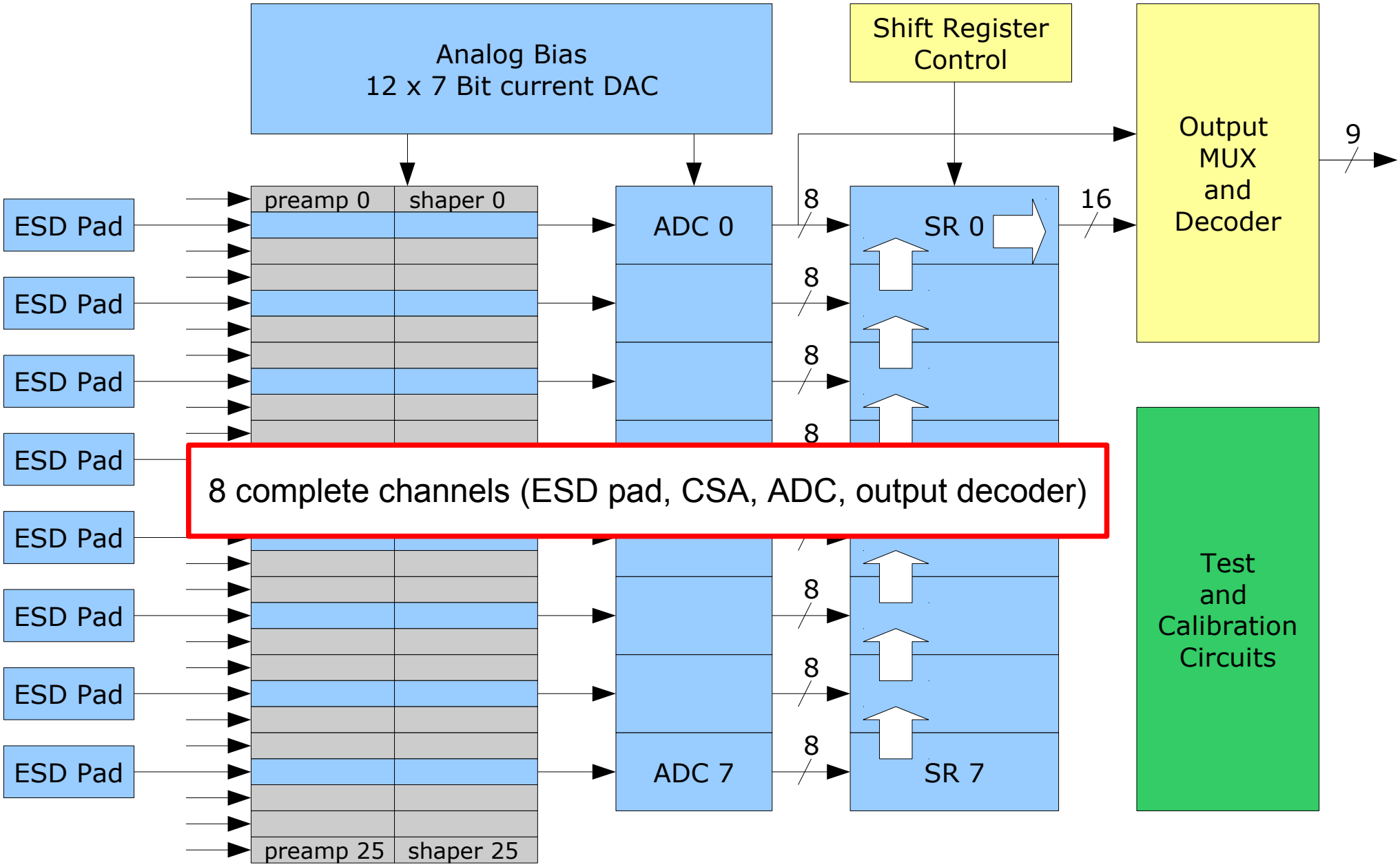
Floor Plan Proposal



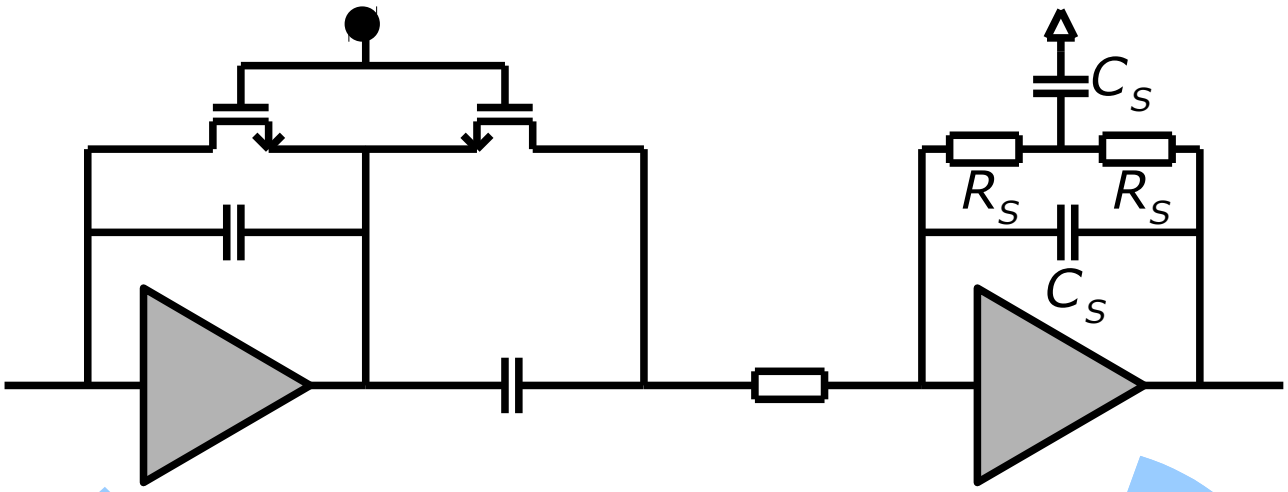
- 3 x 2 mm² estimated die size
- 32 channels, 80µm pitch
- Option in discussion: Detector connections on two sides (relaxes routing/spacing)

2. Status of the Latest SPADIC Version

Block Diagram of Latest SPADIC v0.3



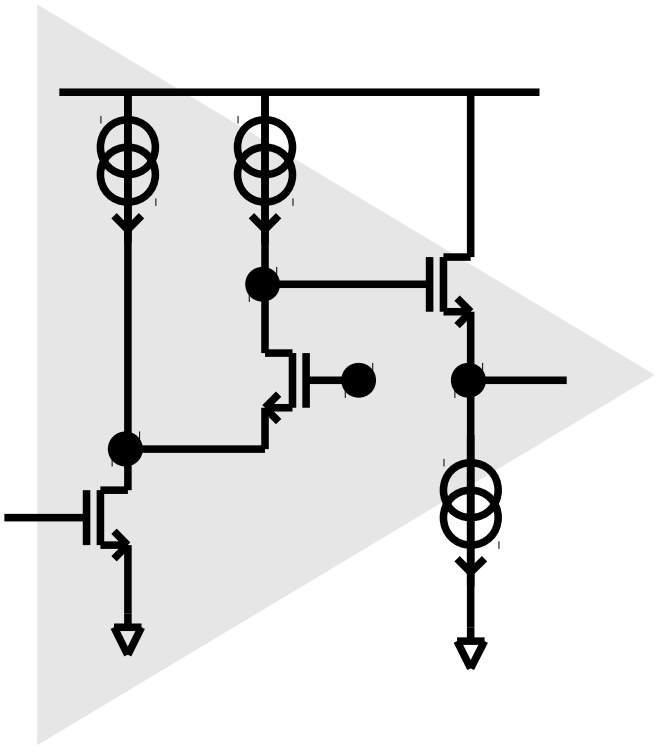
Front-End Amplifier: Preamplifier/Shaper Circuit



$$H(s) \approx \frac{A_{DC}}{(1+sR_SC_S)^2}$$

11x

(also channels with less instances for test purpose on chip)

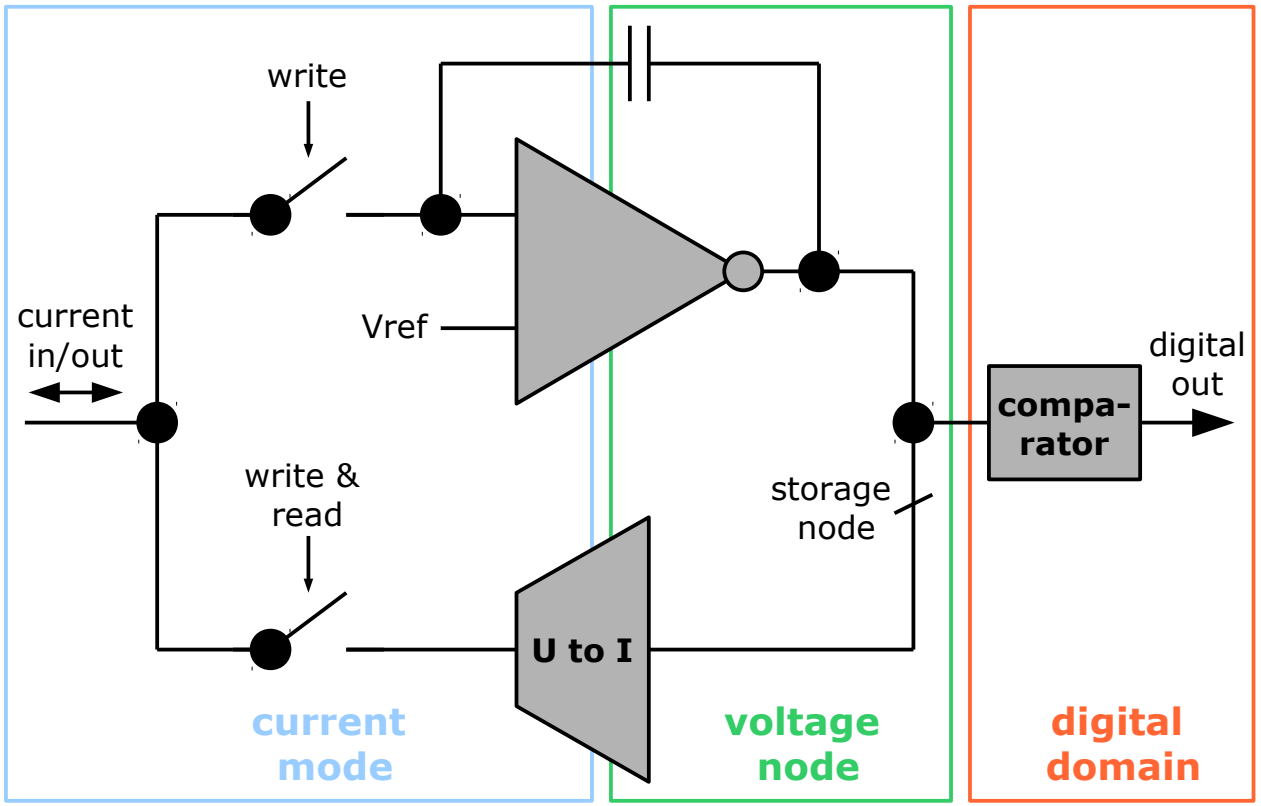


1x

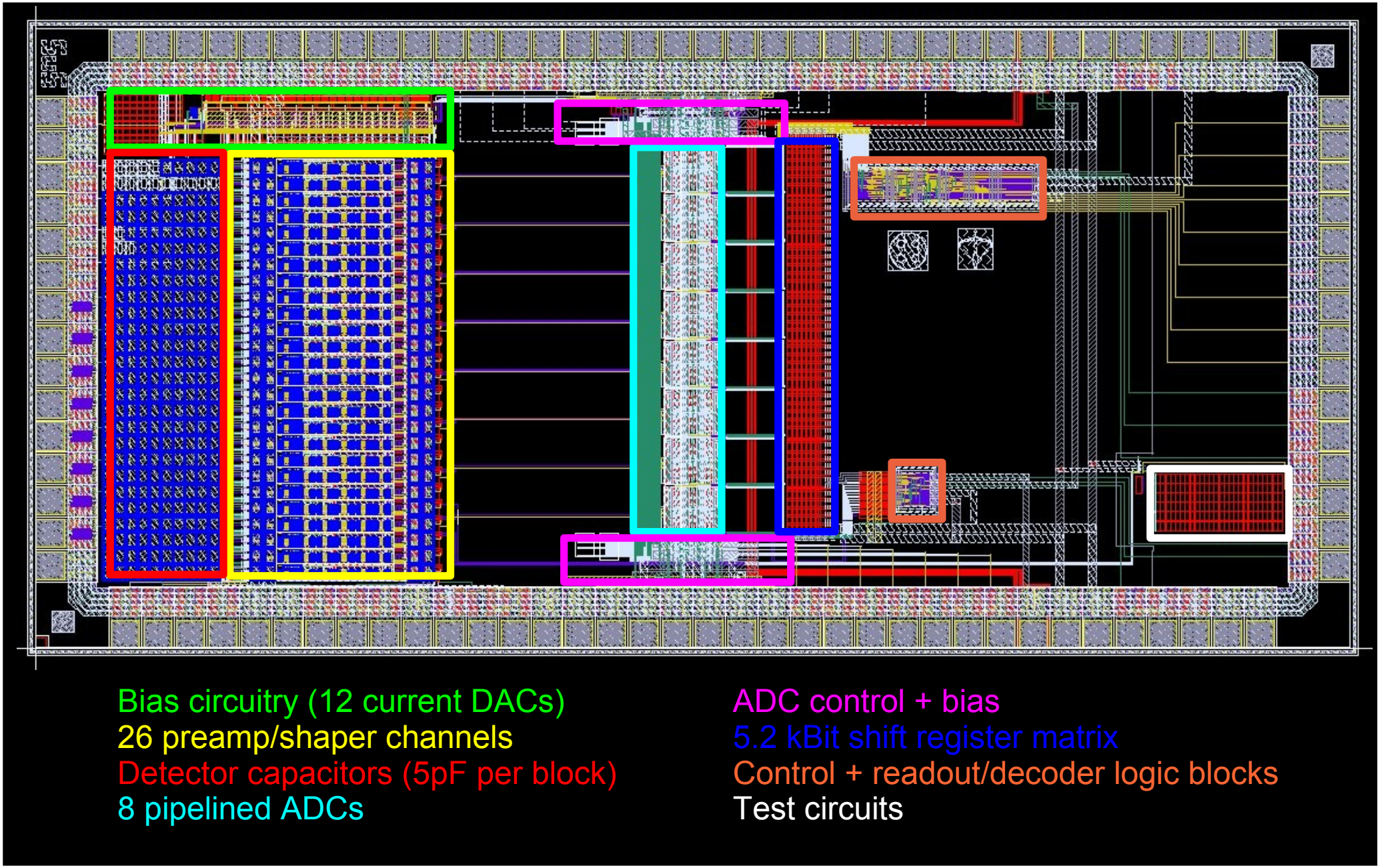
- O'Connor FB
- 2nd order shaper
- Shaping time: 82 ns
- Unified amplifier cell
- N-MOS input
- ≈ 3.6 mW/channel

Algorithmic ADC Design

- 8 (scaled) pipeline stages, therefore 9 Bit design, **7.5 Bits effective** so far
- Algorithmic working principle ("1.5 redundant Bits" / conversion step)
- **25 MSamples/s, layout only 130x120 µm², power consumption 4.5 mW**
- Core unit: Novel current storage cell:



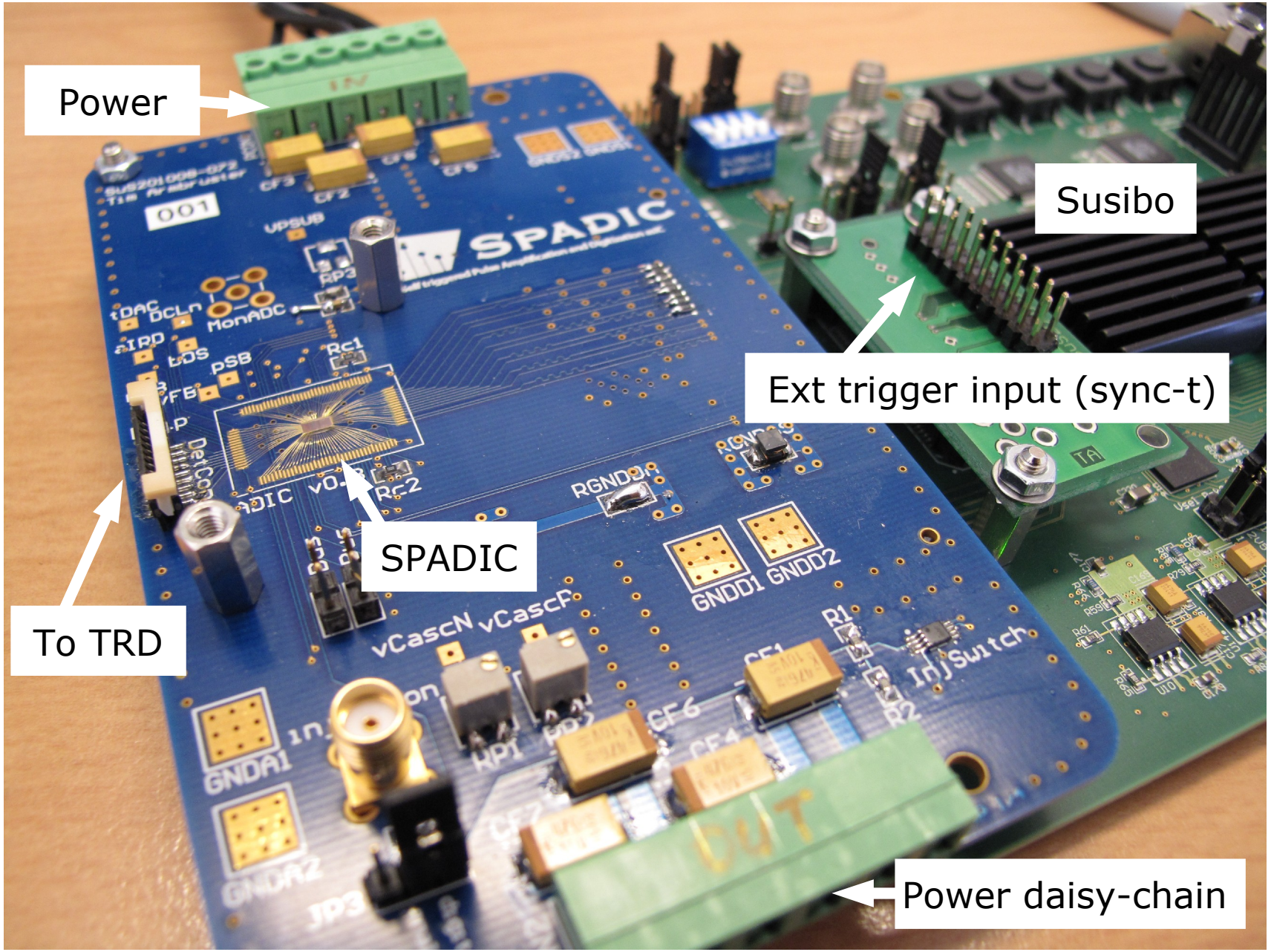
Latest SPADIC: Layout



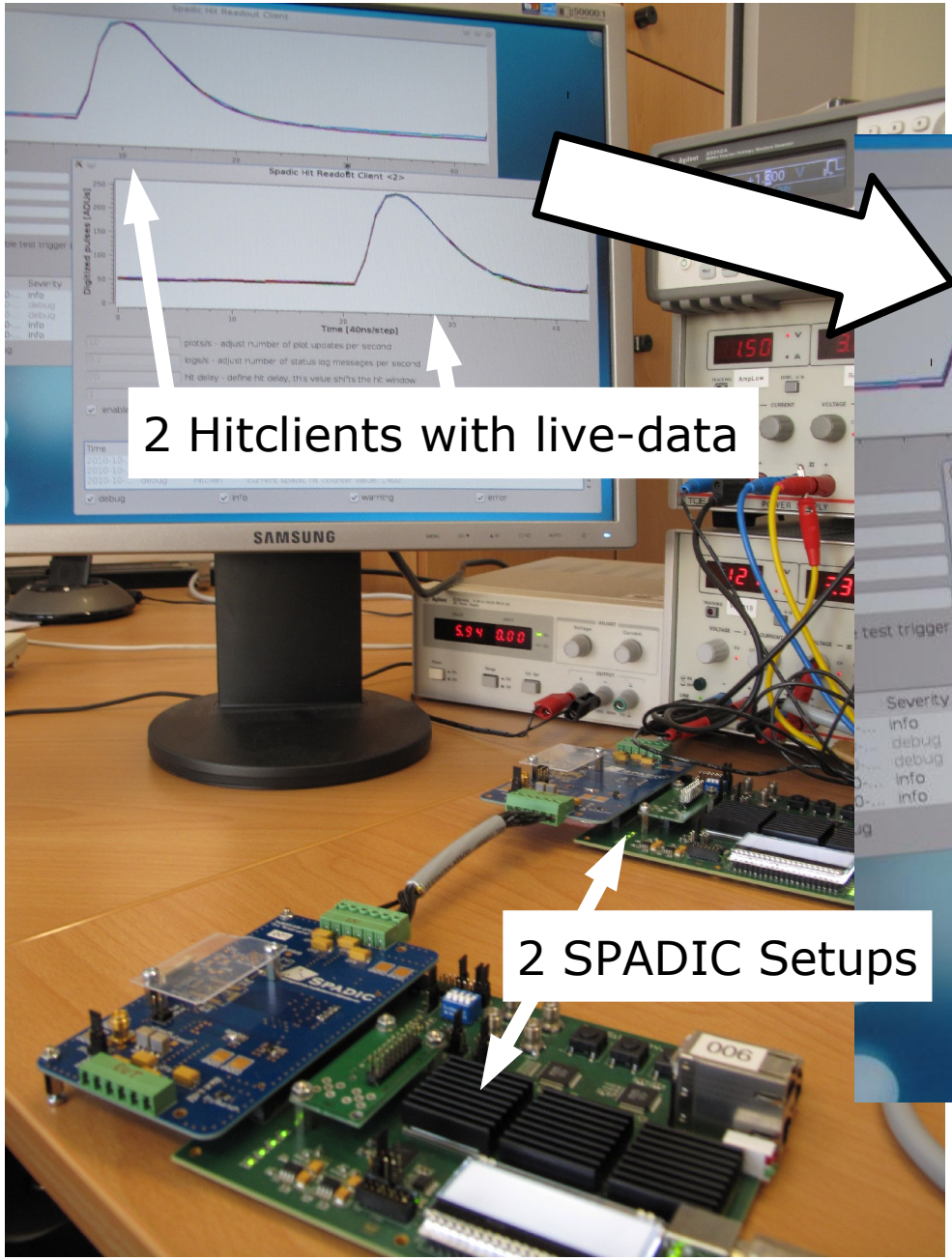
Bias circuitry (12 current DACs)
26 preamp/shaper channels
Detector capacitors (5pF per block)
8 pipelined ADCs

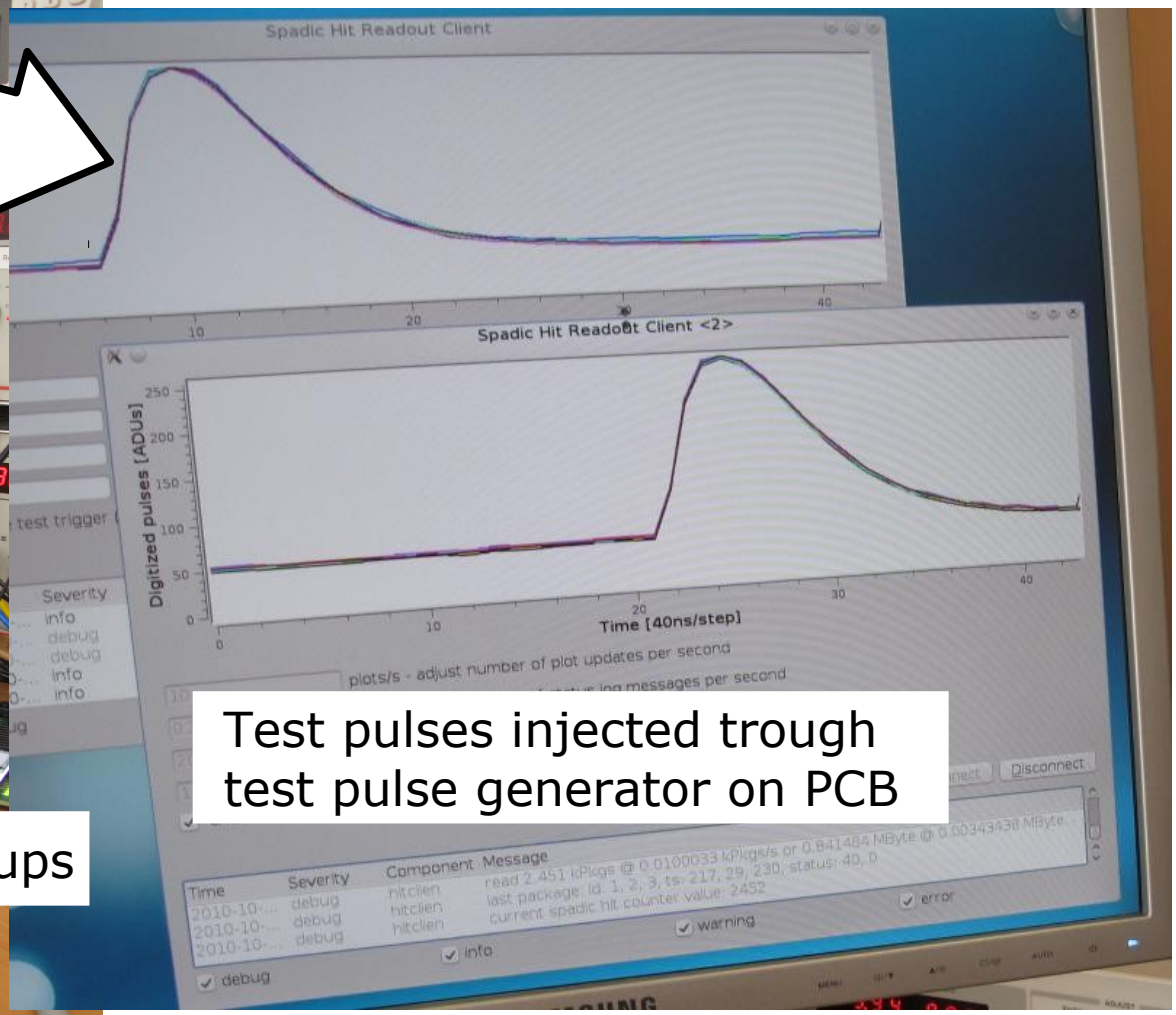
ADC control + bias
5.2 kBit shift register matrix
Control + readout/decoder logic blocks
Test circuits

Test-Setup: SPADIC plugged on Susibo

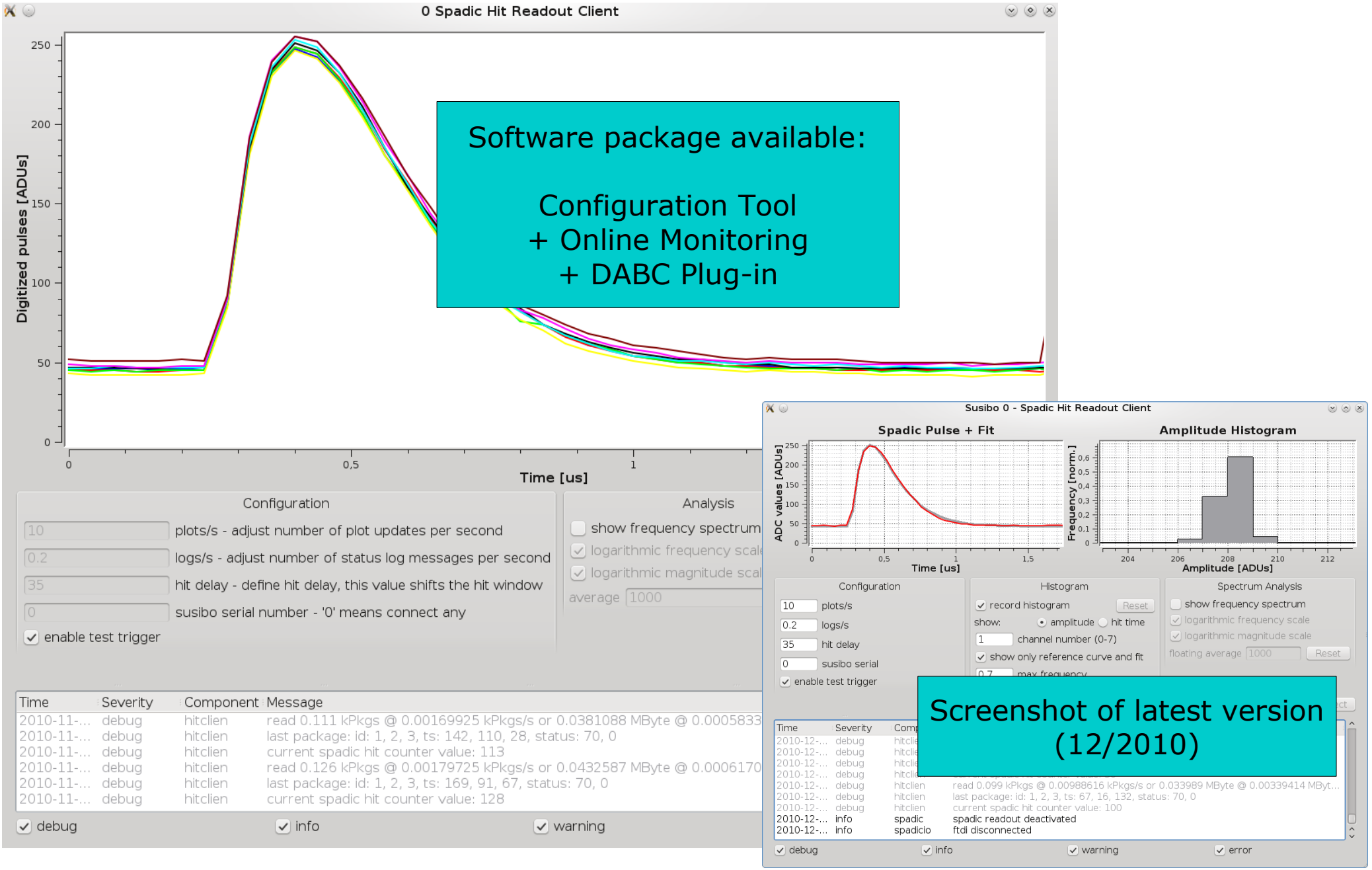


Setup in Lab

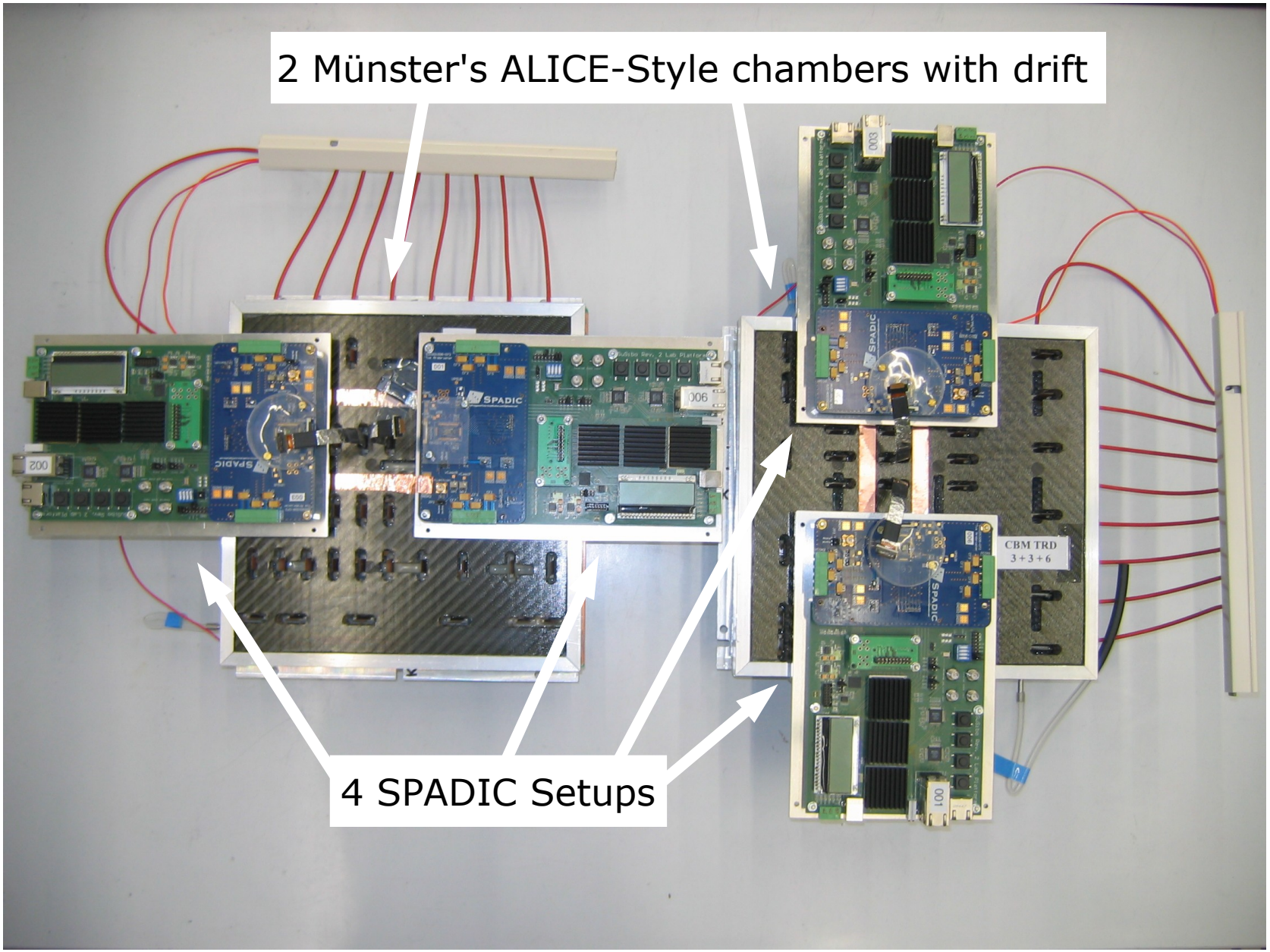

2 Hitclients with live-data
2 SPADIC Setups


Spadic Hit Readout Client
Spadic Hit Readout Client <2>
Digitized pulses [ADUs]
Time [40ns/step]
plots/s - adjust number of plot updates per second
Test pulses injected trough
test pulse generator on PCB

Hitclient Screenshot



CERN Testbeam 2010: Münster's TRD-SPADIC Setup



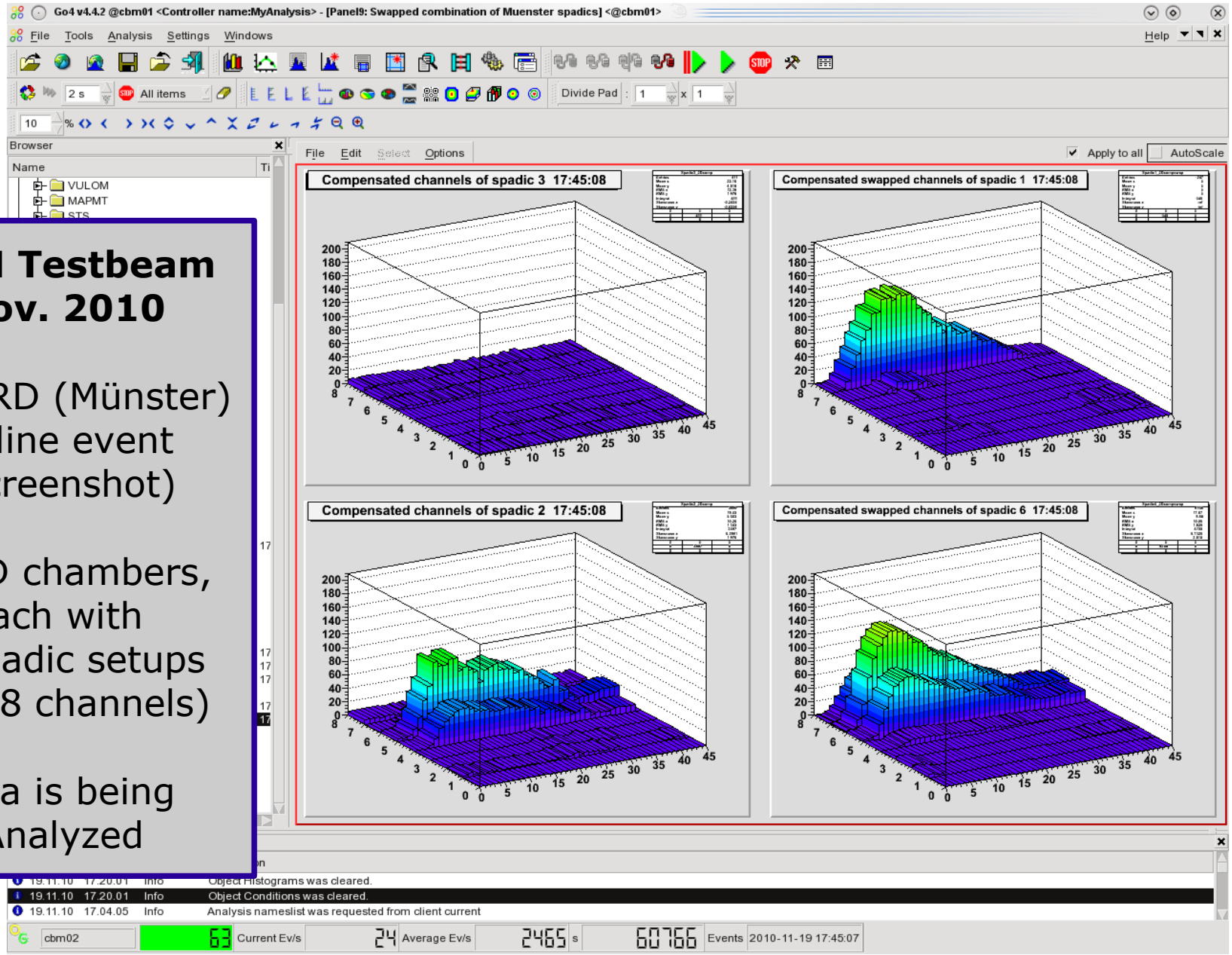
CERN Testbeam 2010: Go4 Spadic online event

CERN Testbeam Nov. 2010

Go4 TRD (Münster) online event (screenshot)

2 TRD chambers, each with 2 Spadic setups (2 x 8 channels)

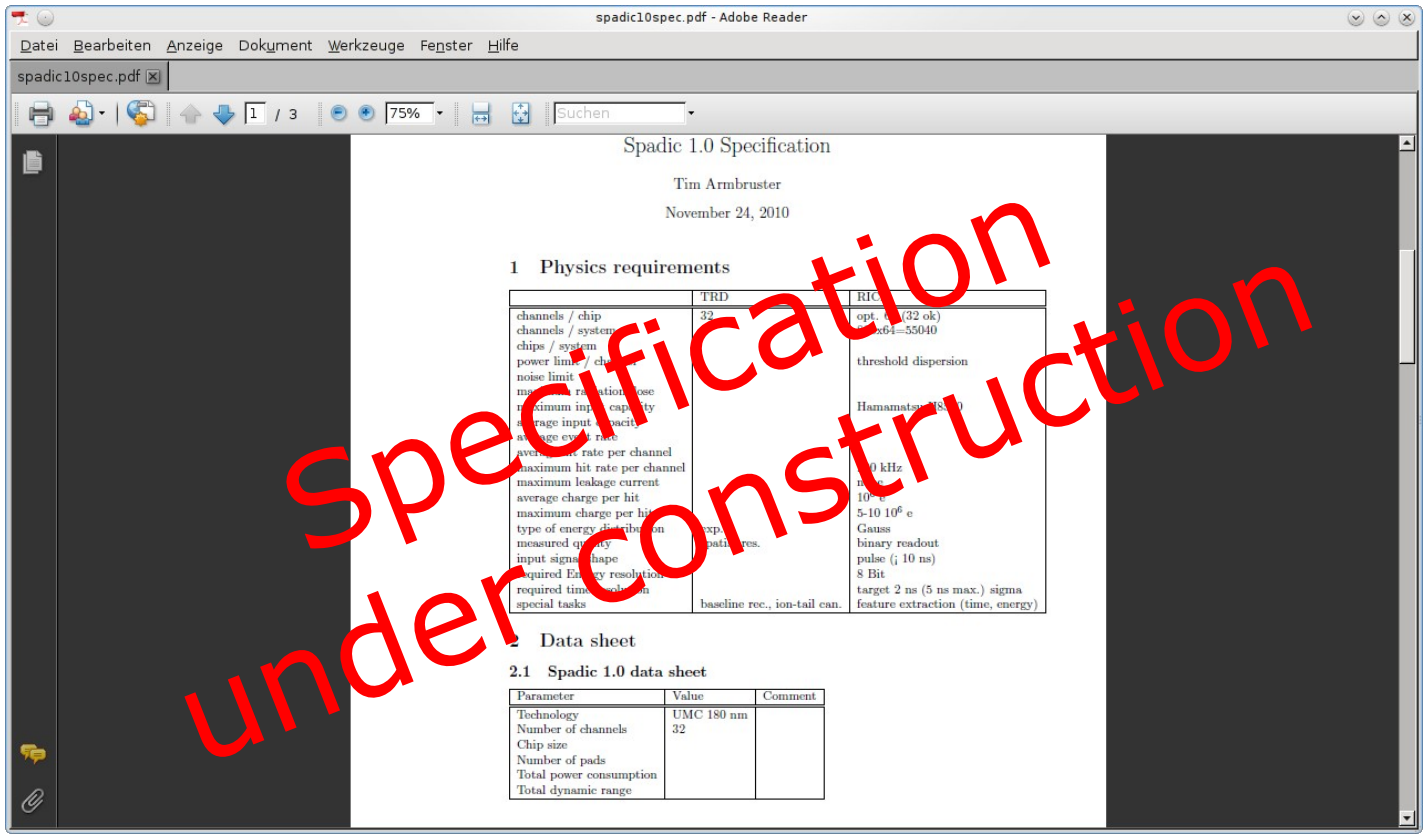
Data is being Analyzed



3. MUCH and Summary

SPADIC Specification

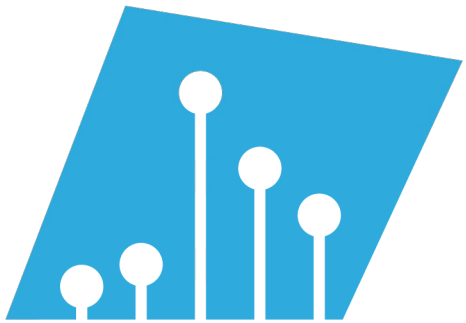
- If MUCH is interested in joining the SPADIC development …
  - … we need to write down all MUCH requirements
  - … we need to compare them to the TRD/RICH requirements
  - … I'll probably need some helping hands
- A SPADIC specification is currently under construction
  - We should go through the physics requirements table and add a MUCH column



Summary

- **Status of Latest Prototype (SPADIC v0.3)**
  - 8 complete channels (plus 18 test channels)
  - Positive input charges, about 0..40fC input range
  - 2^{nd} order shaping, 90 ns shaping time
  - Noise: 800e @ 30 pF capacitive input load
  - ADC with 7.5 Bit effective (INL) @ 25 Msamples/s
  - Power per Channel/ADC: 3.8/4.5 mW
  - Size: 1.5 x 3.2 mm²
- **Status of Latest Setup**
  - 8 complete setups have been available @ CERN Testbeam Nov. 2010
  - New PCB with low noise layout and reduced ground loops under construction, almost finished
  - Ongoing software development
- **First full-blown SPADIC (v1.0)**
  - Start of design phase: February 2011
  - Planned Submission: summer/fall 2011
  - First measurement results end of 2011 at the earliest

If there is any need for additional features (e.g. for MUCH) start discussion now and finish it soon!



SPADIC

Self triggered Pulse Amplification and Digitization asIC

http://spadic.uni-hd.de