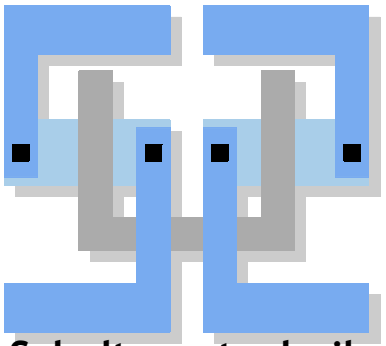
UNIVERSITÄT HEIDELBERG

SPADIC
Self triggered Pulse Amplification and Digitization asIC

Part 1: Results from SPADIC 0.3



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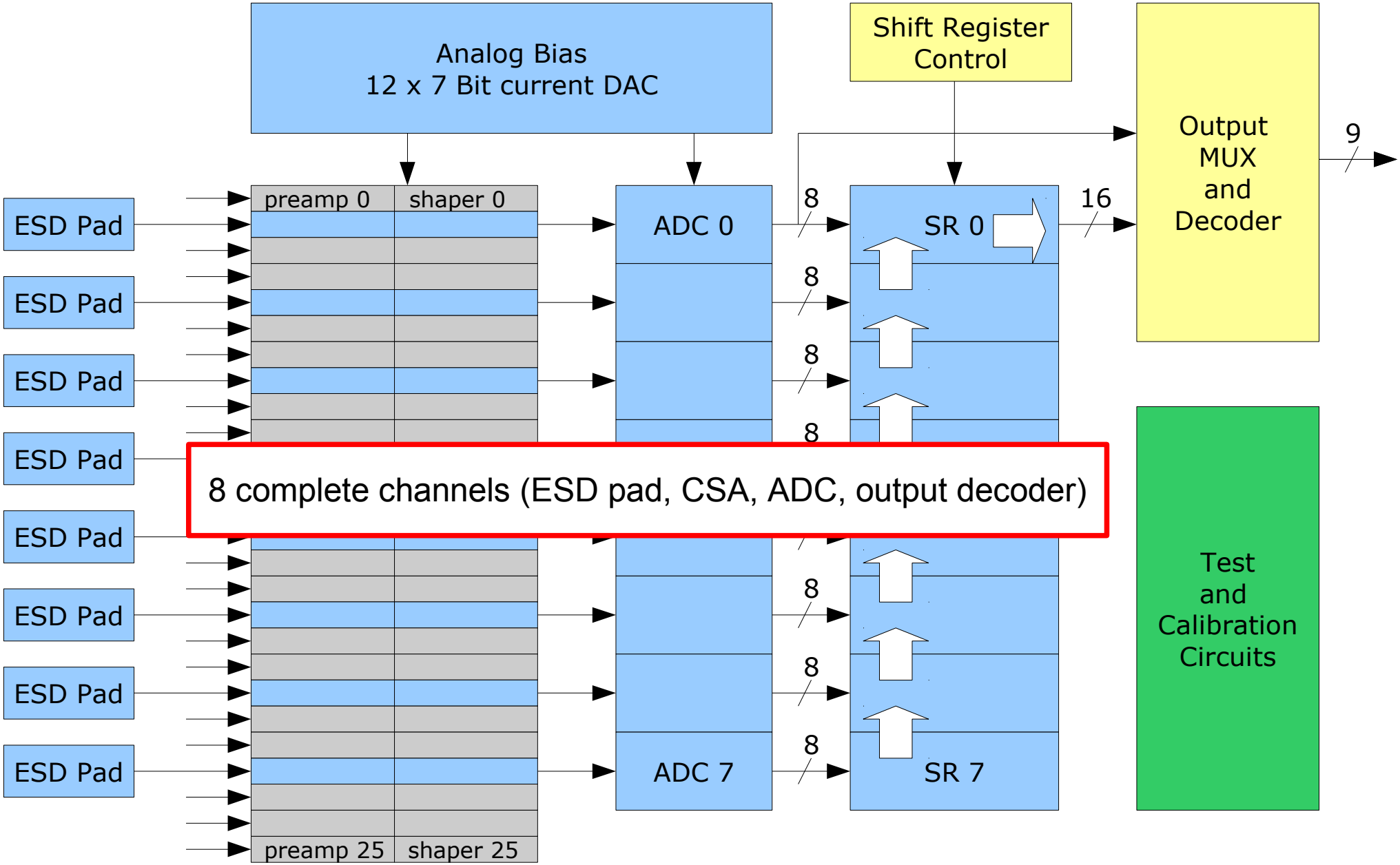
17th CBM CM, Dresden

April 2011

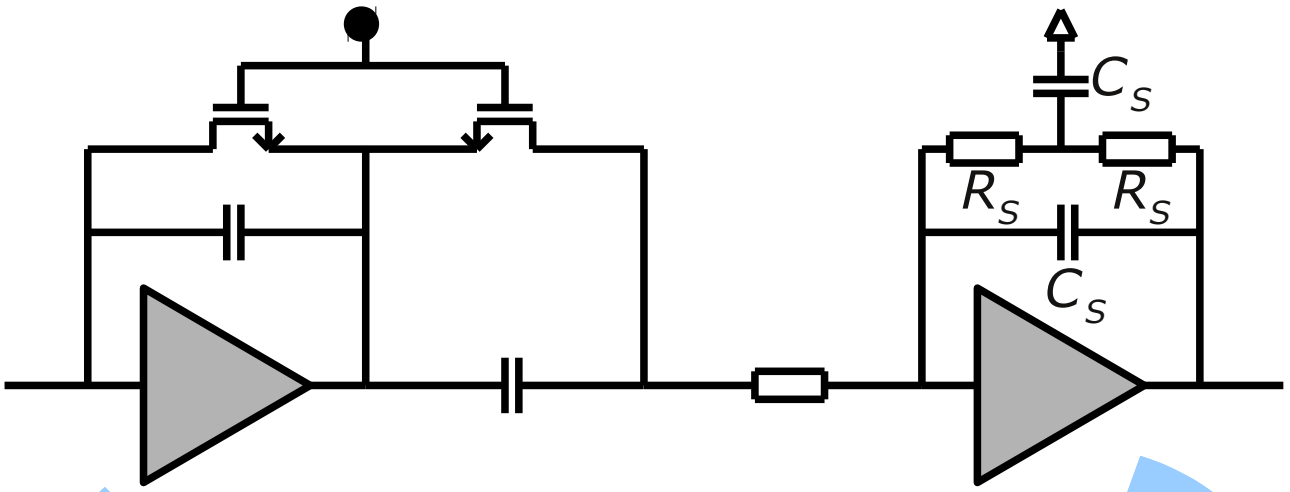
Visit http://www.spadic.uni-hd.de

1. Reminder: SPADIC 0.3 Architecture

Block Diagram of Latest SPADIC v0.3



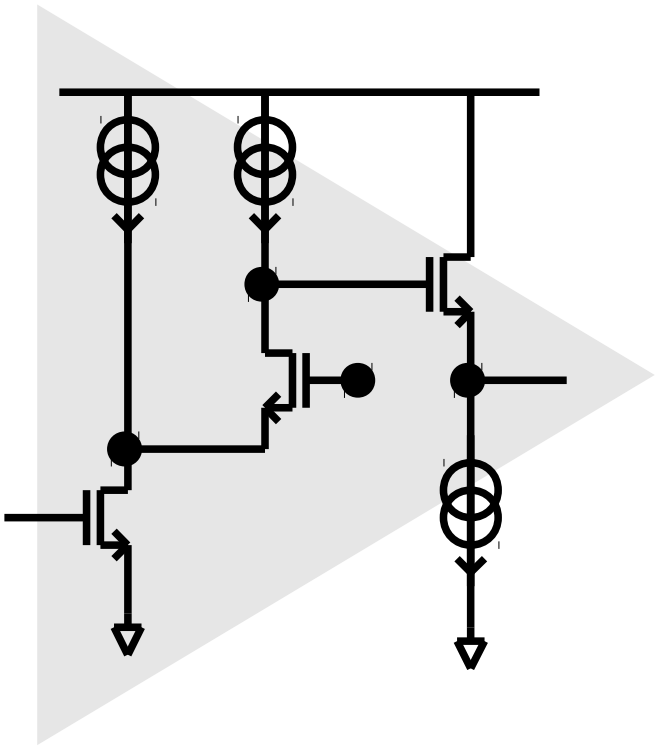
Front-End Amplifier: Preamplifier/Shaper Circuit



$$H(s) \approx \frac{A_{DC}}{(1+sR_SC_S)^2}$$

11x

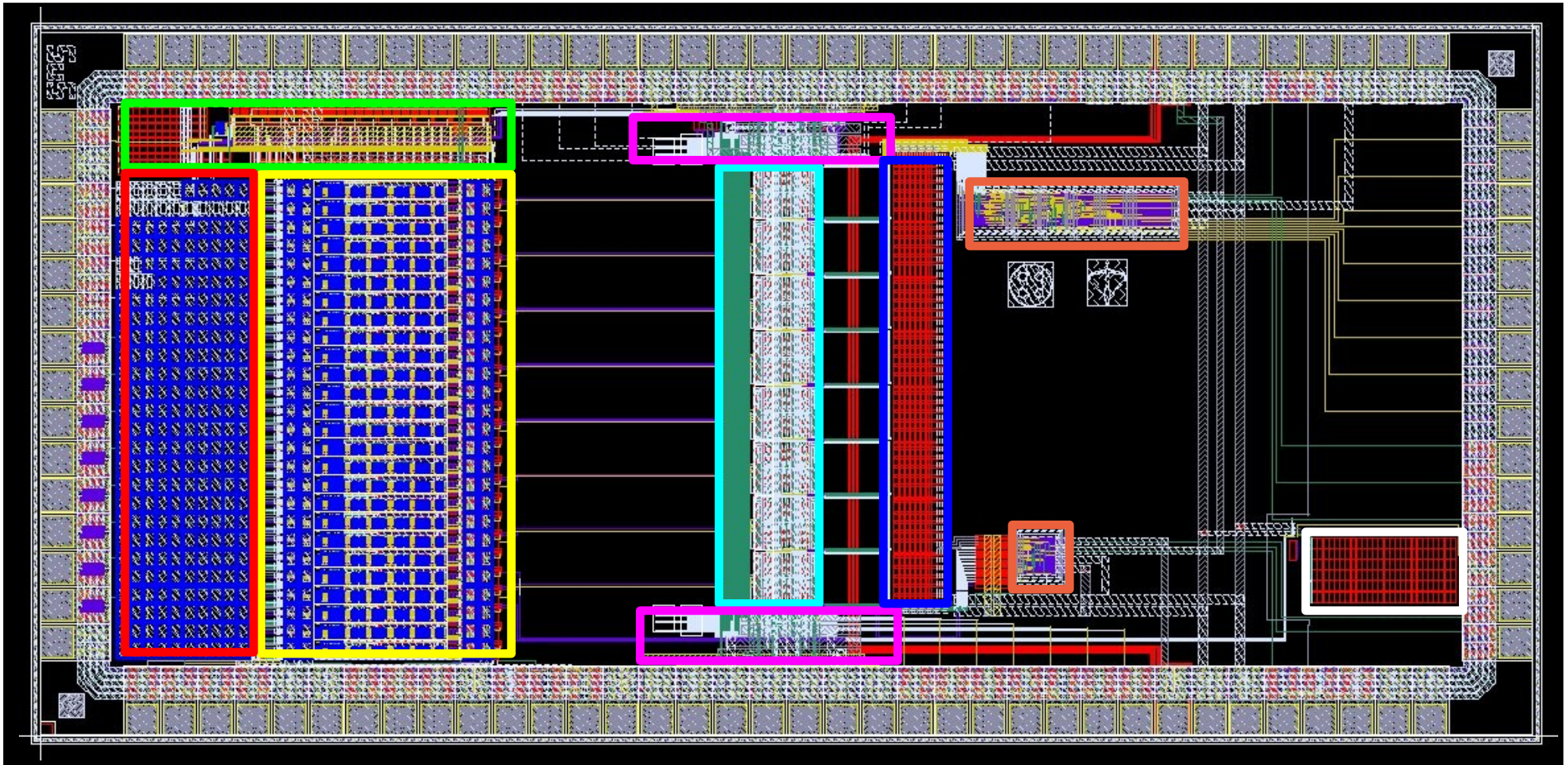
(also channels with less instances for test purpose on chip)



1x

- O'Connor FB
- 2nd order shaper
- Shaping time: 82 ns
- Unified amplifier cell
- N-MOS input
- ≈ 3.6 mW/channel

Latest SPADIC: Layout

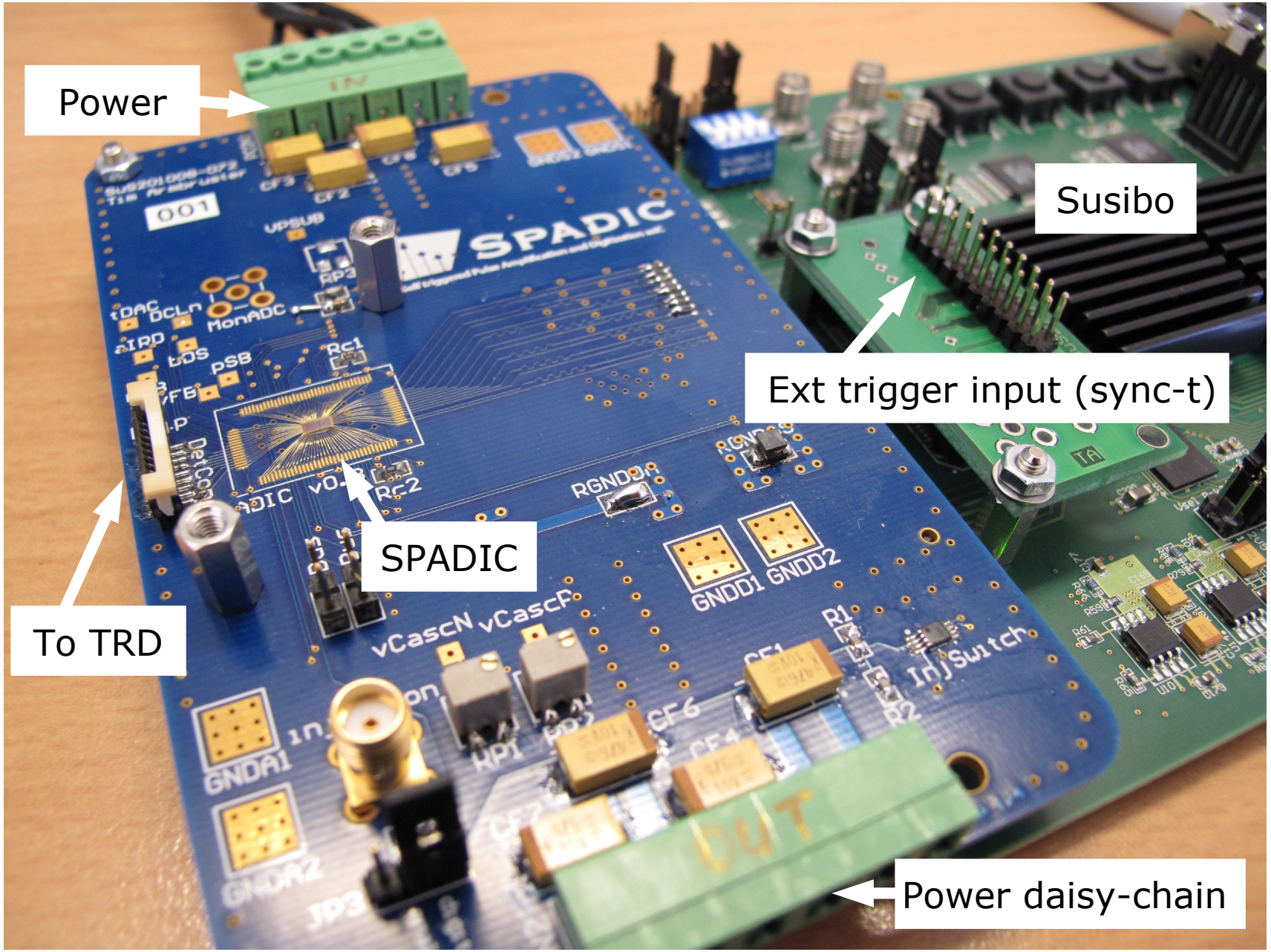


Bias circuitry (12 current DACs)
26 preamp/shaper channels
Detector capacitors (5pF per block)
8 pipelined ADCs

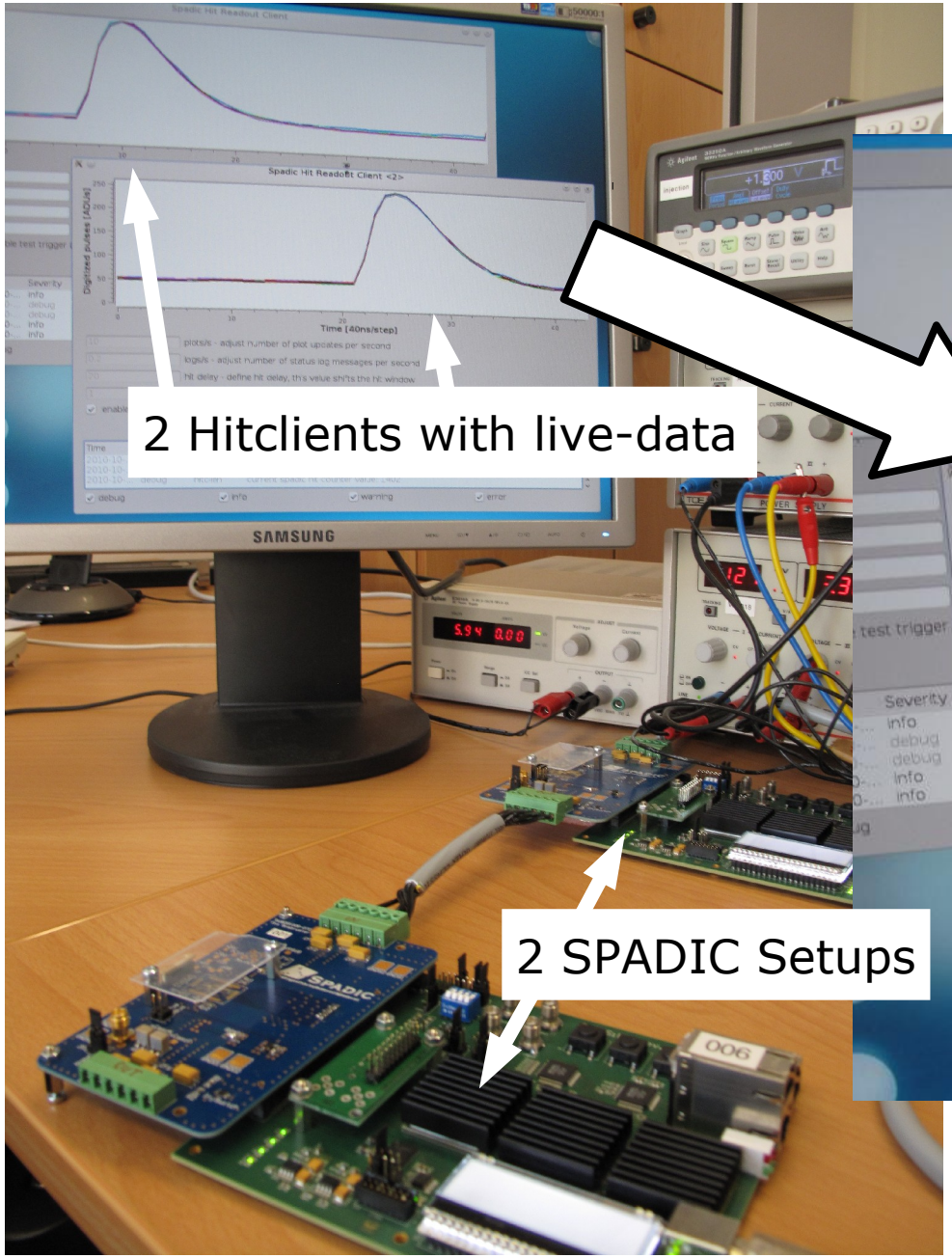
ADC control + bias
5.2 kBit shift register matrix
Control + readout/decoder logic blocks
Test circuits

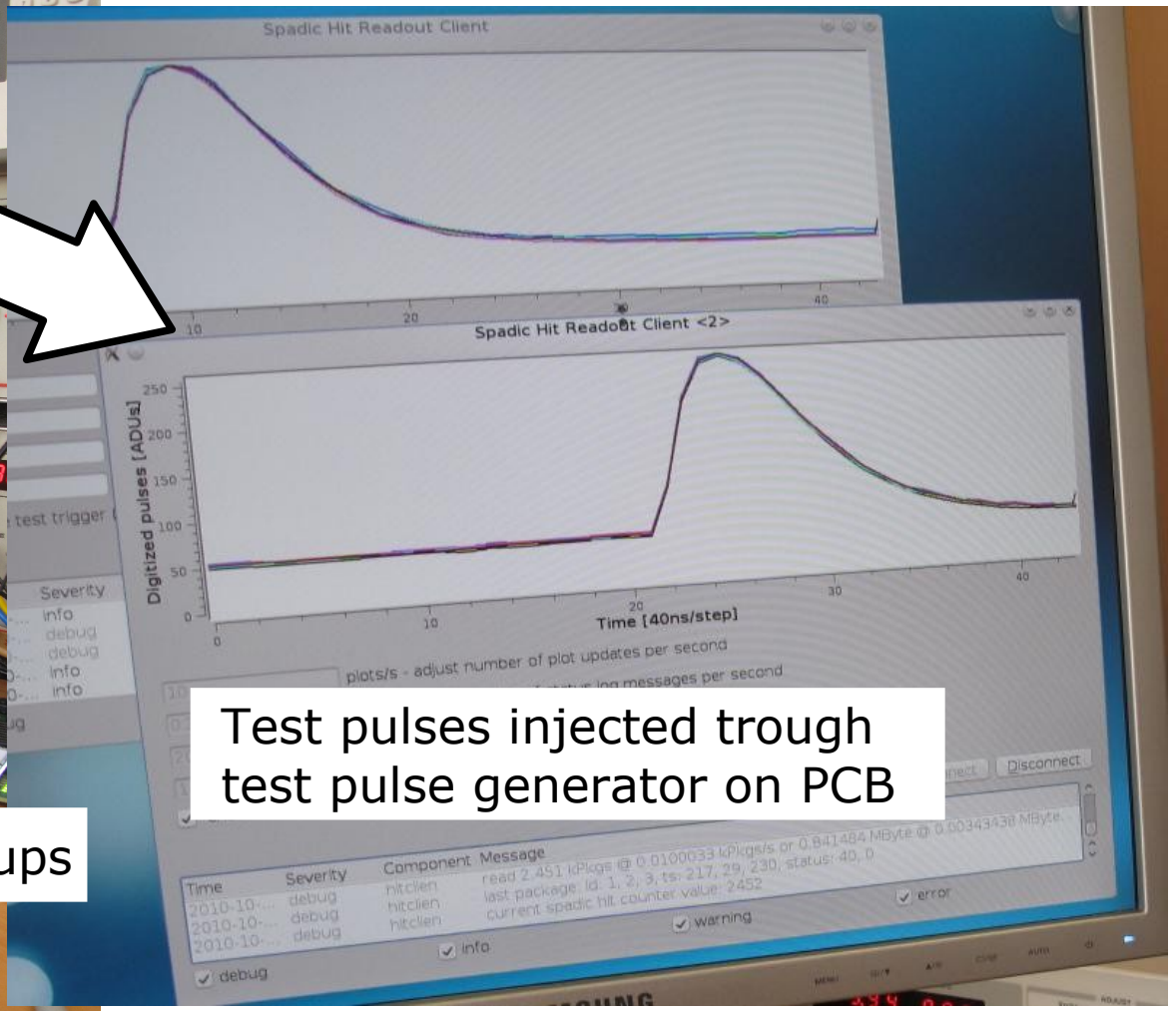
2. Reminder: CERN Testbeam 2010

Test-Setup: SPADIC plugged on Susibo

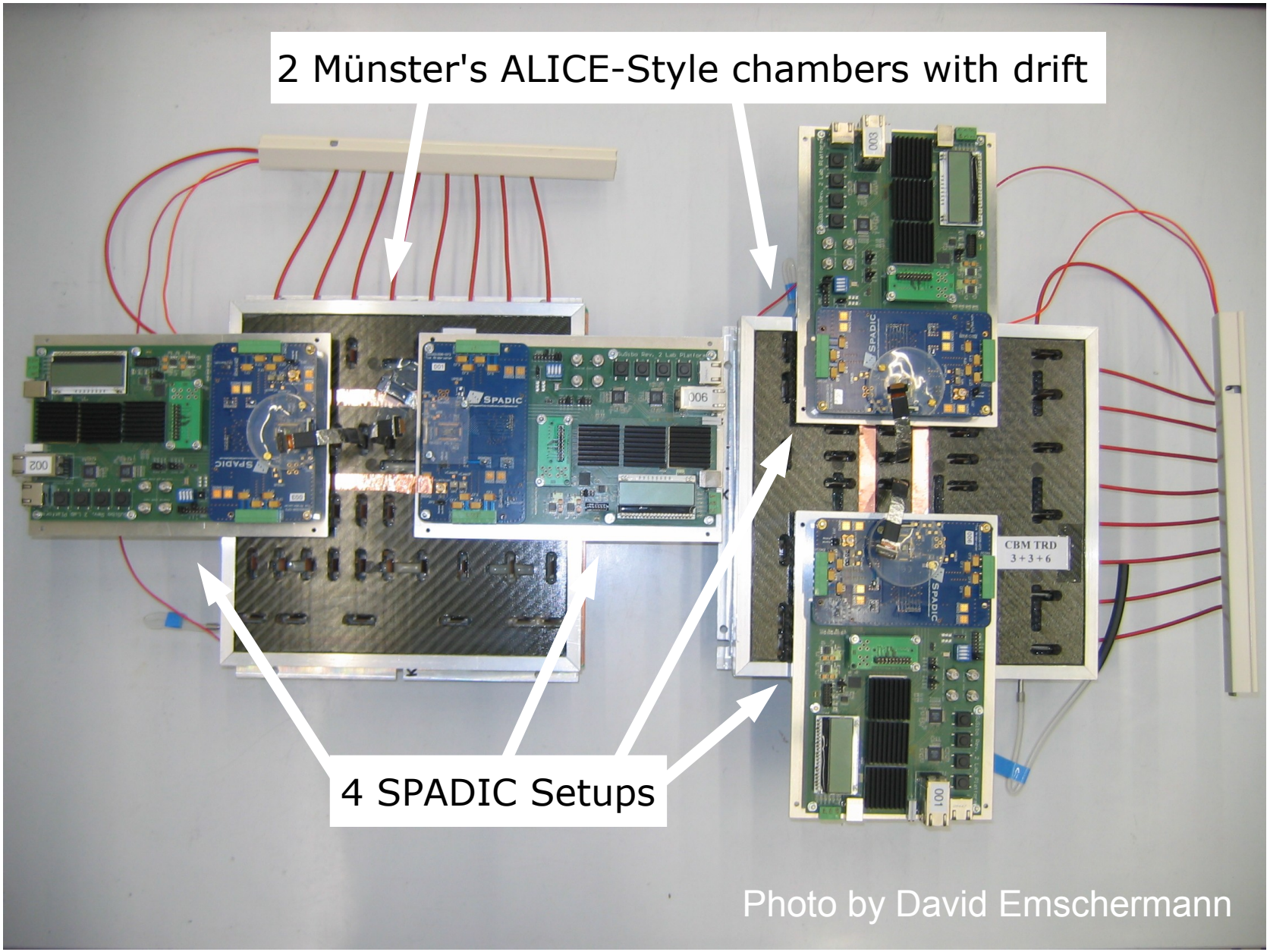


Setup in Lab

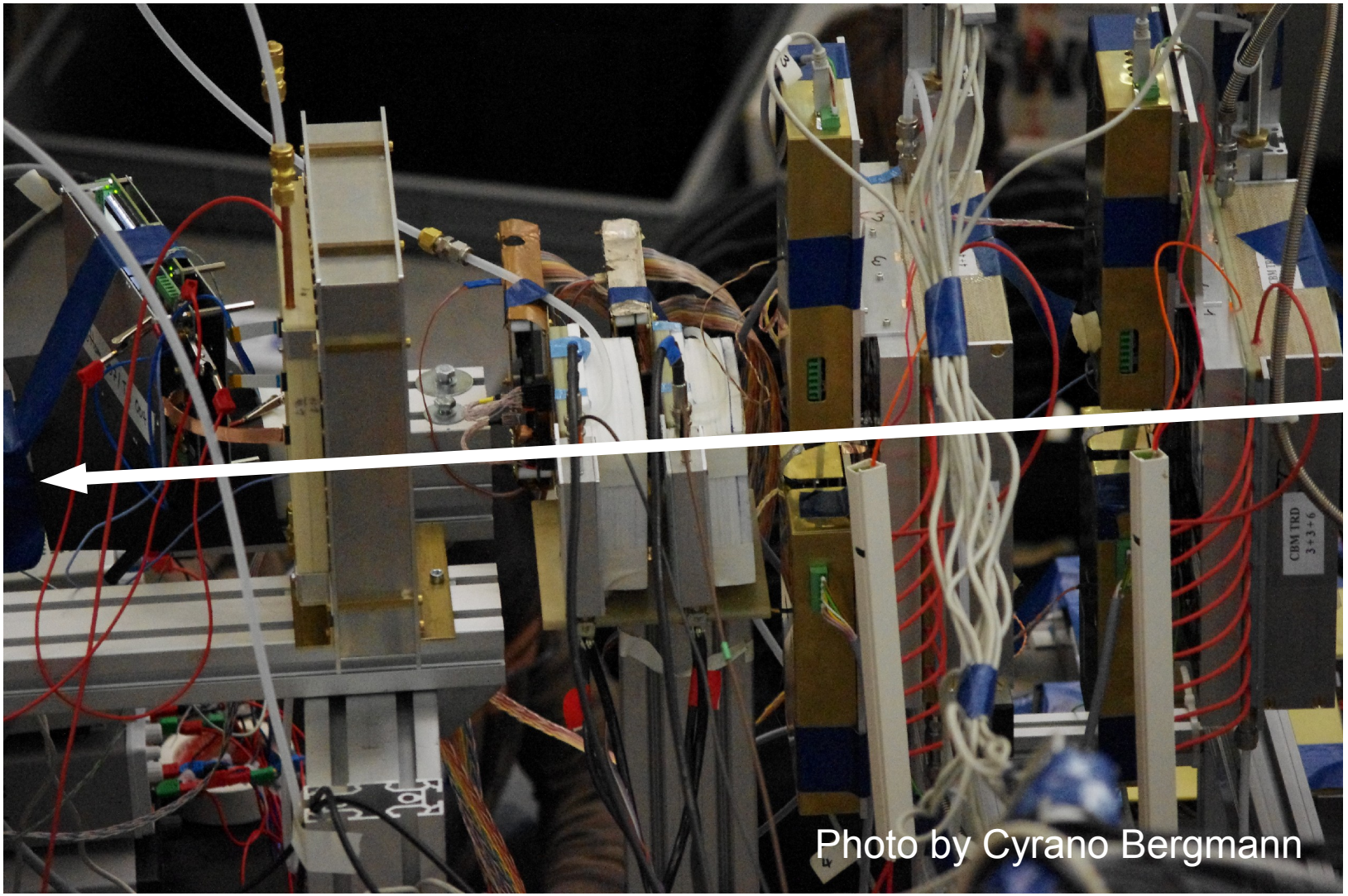

2 Hitclients with live-data
2 SPADIC Setups


Spadic Hit Readout Client
Spadic Hit Readout Client <2>
Digitized pulses [ADUs]
Time [40ns/step]
plots/s - adjust number of plot updates per second
Test pulses injected trough
test pulse generator on PCB

CERN Testbeam 2010: Münster's TRD-SPADIC Setup



CERN Testbeam 2010



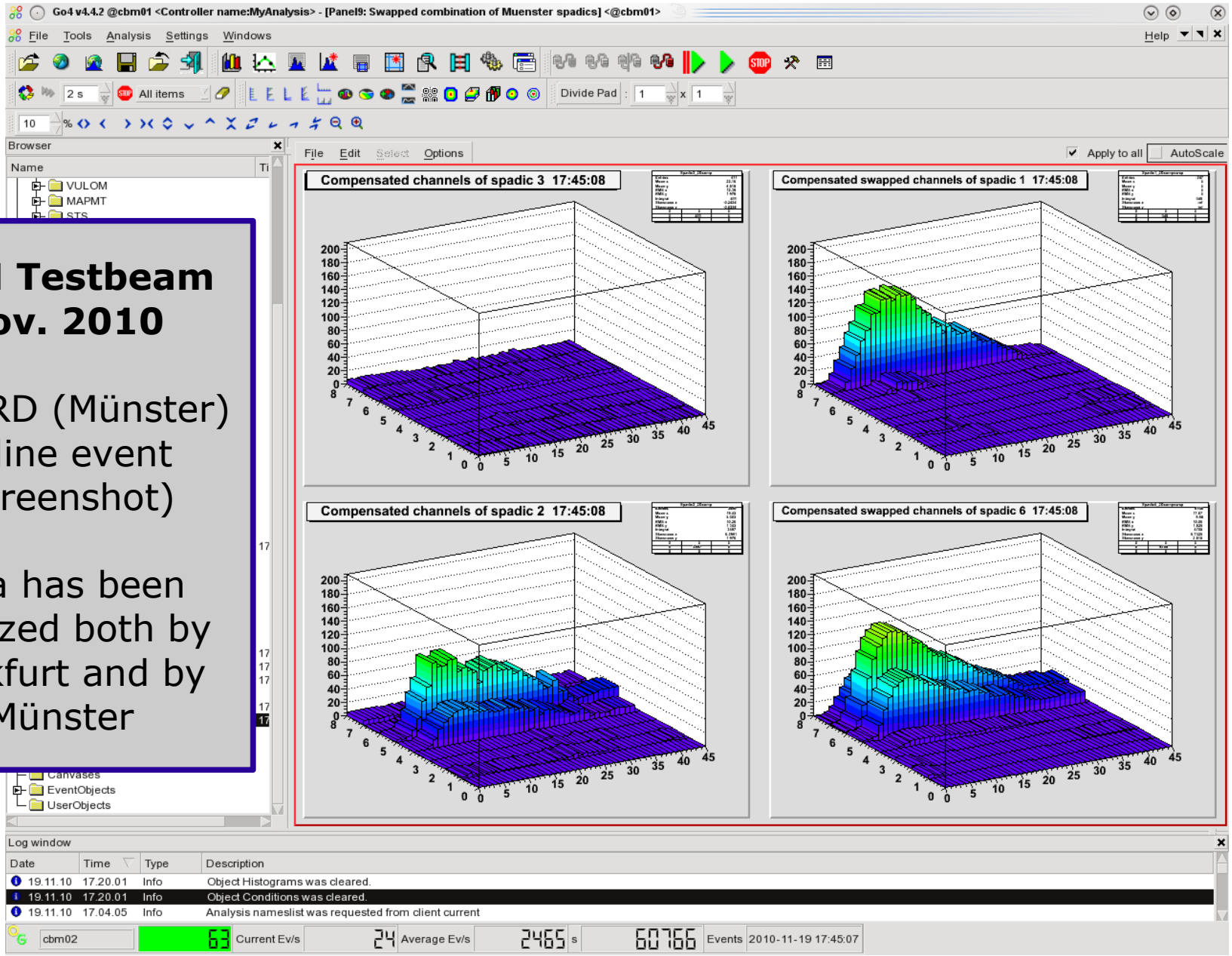
- 8 SPADIC readout setups were ready just in time
- 6 SPADIC setups were run in parallel

CERN Testbeam 2010: Go4 Spadic online event

CERN Testbeam Nov. 2010

Go4 TRD (Münster) online event (screenshot)

Data has been Analyzed both by Frankfurt and by Münster



3. Known Problems

Problem 1: Pick-up Noise

Problem

- Setup very sensitive to pick-up noise due to external disturbing sources. Stable as long as no detector is connected.

Possible Reason(s)

- Very long connection chain (8mm bonding-wire, 1cm wire on PCB, unshielded 9-pin connector, 10cm flex flat cable, unshielded 9-pin connector, 2cm wire on PCB)
- No consistent grounding scheme (both for PCB and chip)

Possible Solutions / Next Steps

- After a lot of trial and error, one can usually find a more or less stable setup
- Shielding: Seems to help!?
- Minimize length of connection chain (e.g. better PCB footprint)
- Develop more consistent grounding scheme (very important)
- Gather experience with the next SPADIC 0.3 PCB iteration

Problem 2: Baseline-Shift

Problem

- Baseline-shift (offset of pulses jumps) when some external load is connected. Shifts in both(!) directions (up/down) have been observed. Probably no impact on noise (but on dynamic range).

Possible Reason(s)

- Theoretically and from simulation: Some leakage current (several 10nA) can cause such a behavior. But for instance the TRD pads are well isolated. True reason hard to find – no good idea so far.

Possible Solutions / Next Steps

- Better grounding scheme (PCB and chip) might help here as well
- Isolation of analog input cells (leakage via protection circuitry?)
- Good ideas are very welcome!
- Check whether this problem still exists on the next SPADIC 0.3 PCB iteration (see later)

Problem 3: Too Strong Output Driver

Problem

- CMOS Output driver too strong. They cause power glitches which leads to different internal problems (e.g. loss of configuration).

Possible Reason(s)

- CMOS :-)

Possible Solutions / Next Steps

- Only LVDS on SPADIC 1.0
- Buffer on next SPADIC 0.3 readout board
- Latest SPADIC 0.3 readout board uses resistors to limit current (patch)

Problem 4: Broken Setups

Problem

- After some time, several SPADIC 0.3 Rev.2 boards stopped working. Symptoms: Much too much current flow, analog part still works (but noisy), digital part still works, but ADC seems to be death. Some users reported to have heard (!) discharges. No visible damage.

Possible Reason(s)

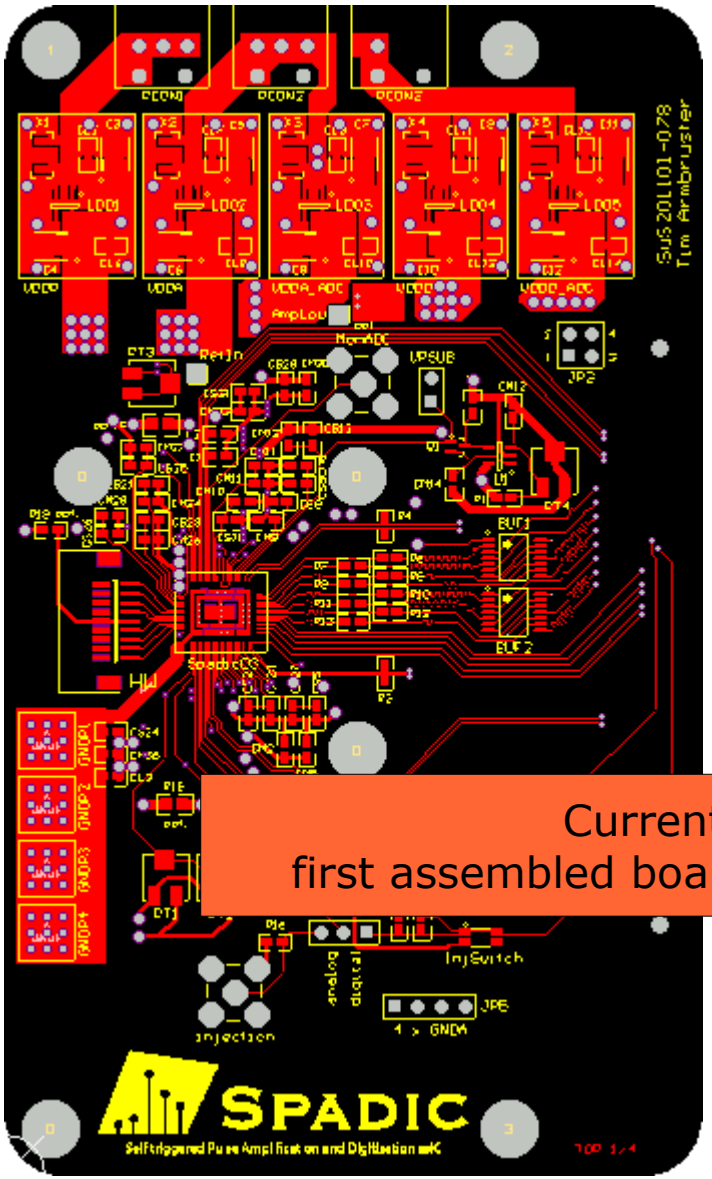
- Cross-current between power domains
- Electrostatic discharge
- ESD circuitry not sufficient
- Faulty operation

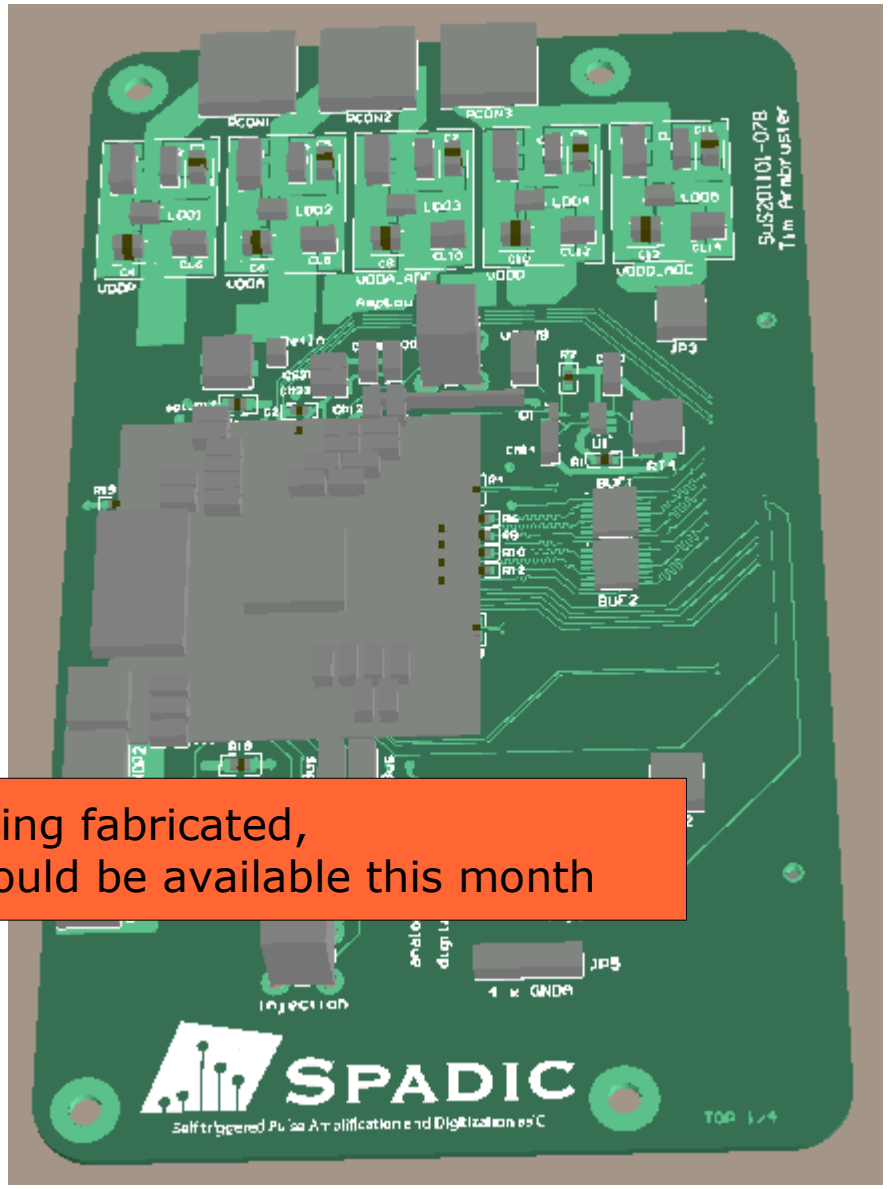
Possible Solutions / Next Steps

- Test: Better powering scheme on next SPADIC 0.3 readout board
- Use voltage regulators (less cables, less operational problems, more stable power signals)
- Try to use only power supplies with accurate current protection!

4. Improvements

New Setup: Improved PCB Layout, under construction



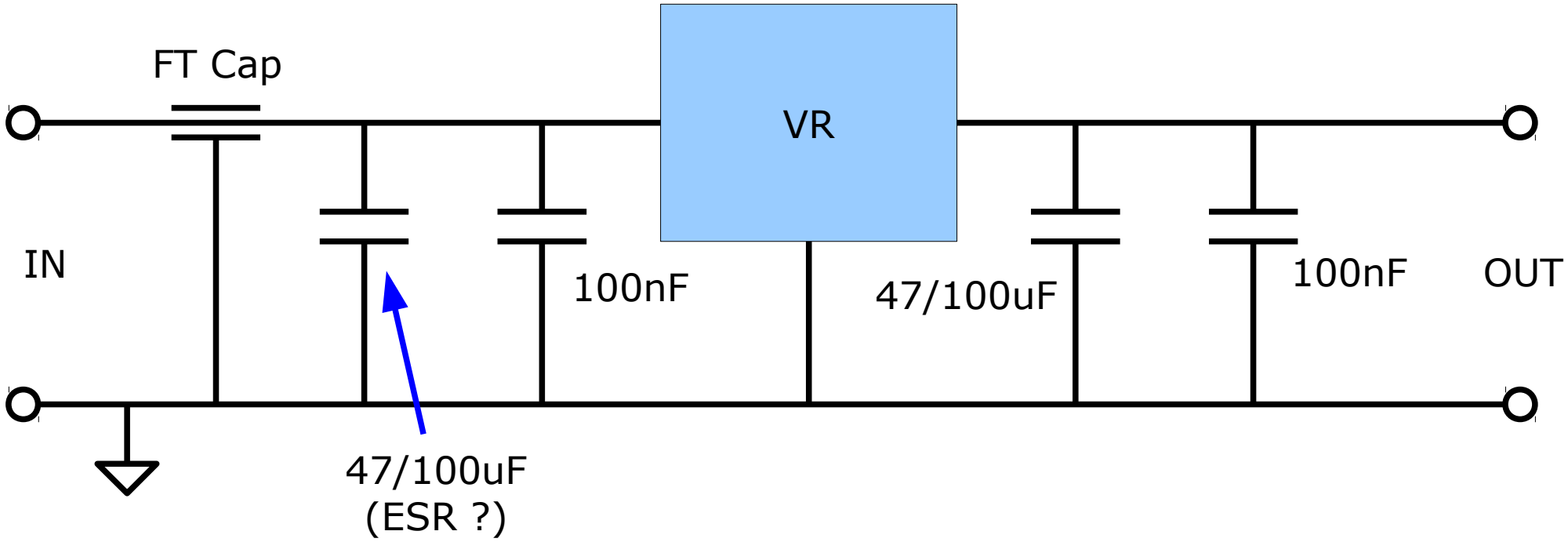


Currently being fabricated,
first assembled board should be available this month

SPADIC PCB Improvement #1: Voltage Regulators

Tip from Ivan Rusanov (GSI)

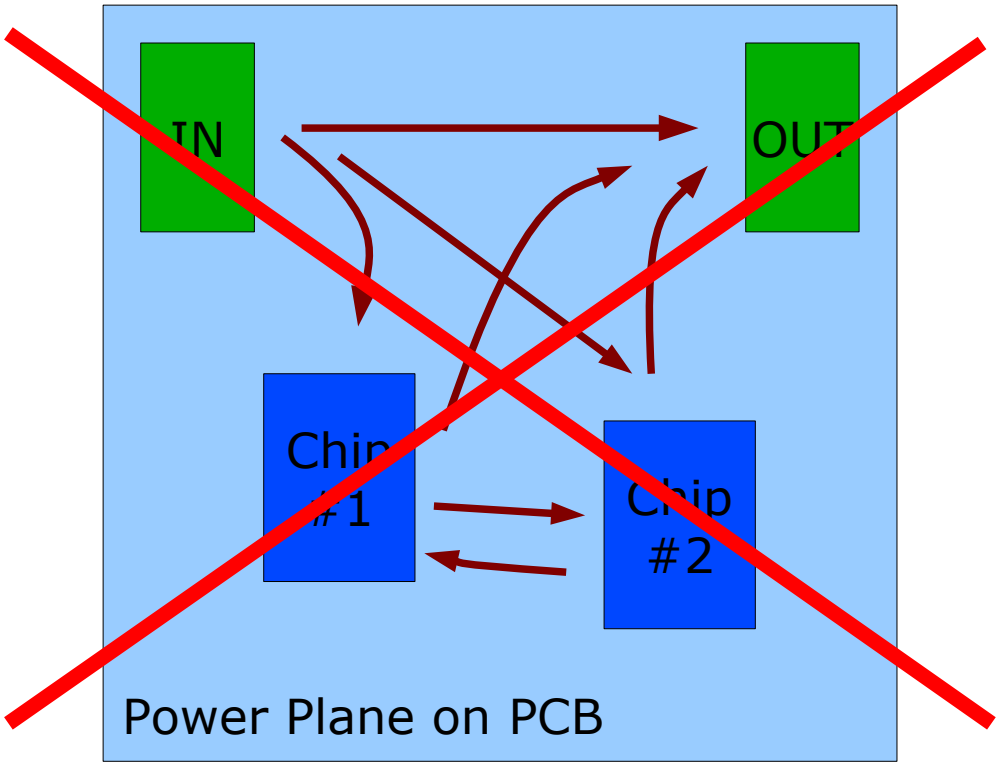
4 Power Domains: Preamp 1.8V, ADC analog 1.8V, ADC digital 1.8V, Digital 1.8V
3 Ground Domains: Pramp, ADC+Digital, Susibo
3 Bias-Voltages with current flow: AmpLow, RefIn, VPSUB

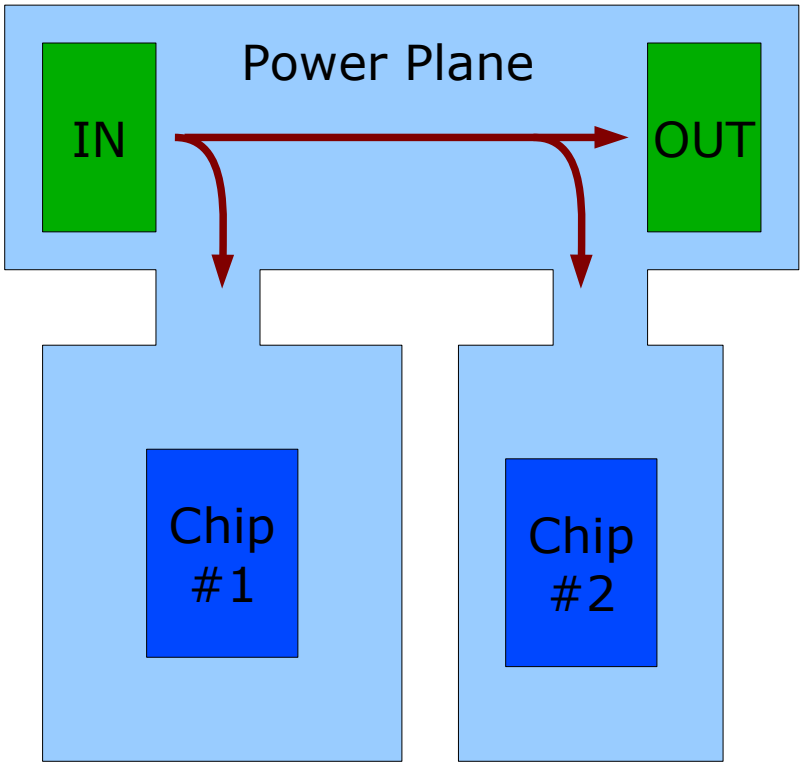


Use a voltage regulator for each power domain!
→ decrease voltage drop in power-daisy-chain

SPADIC PCB Improvement #2: Regulate Current Flows

Tip from Ivan Rusanov (GSI)

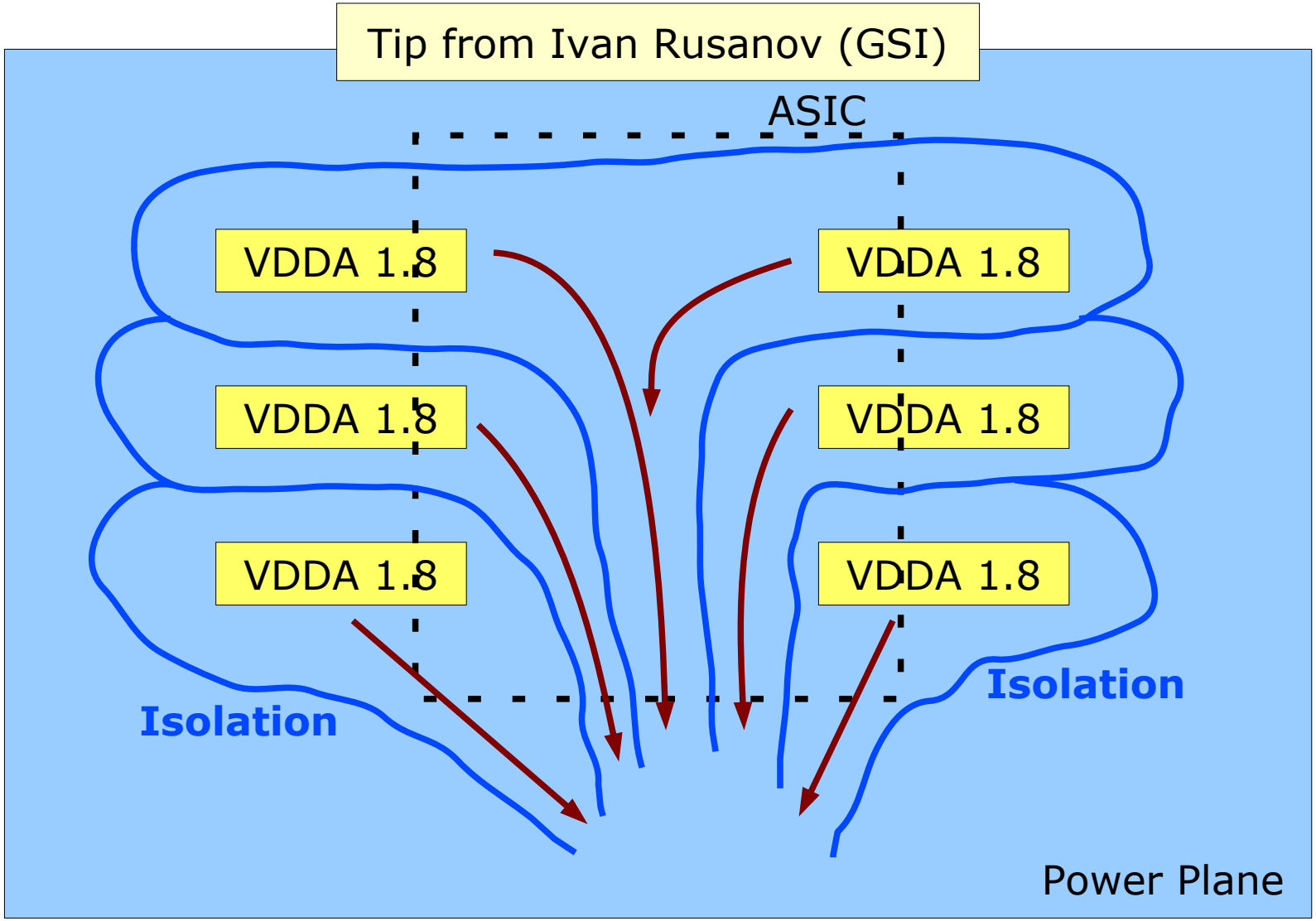




(Same scheme for current sink on a different layer)

Clearly regulate current flows
→ Remove possible sources for power/ground loops!

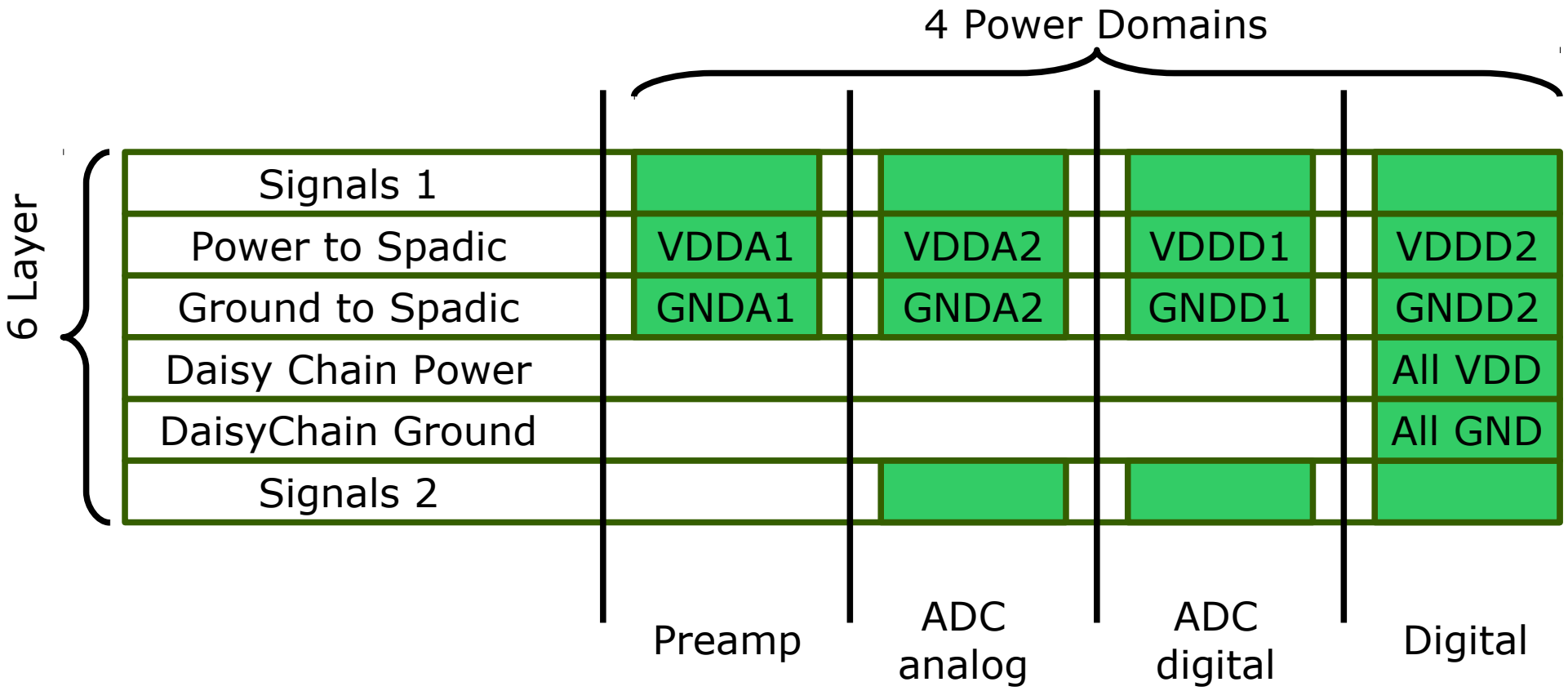
SPADIC PCB Improvement #3: Current Flows Next to Chip



Semi-isolate power pins of same domain to remove direct currents
→ Remove possible sources for power/ground loops!

SPADIC PCB Improvement #4: New Layer Stack

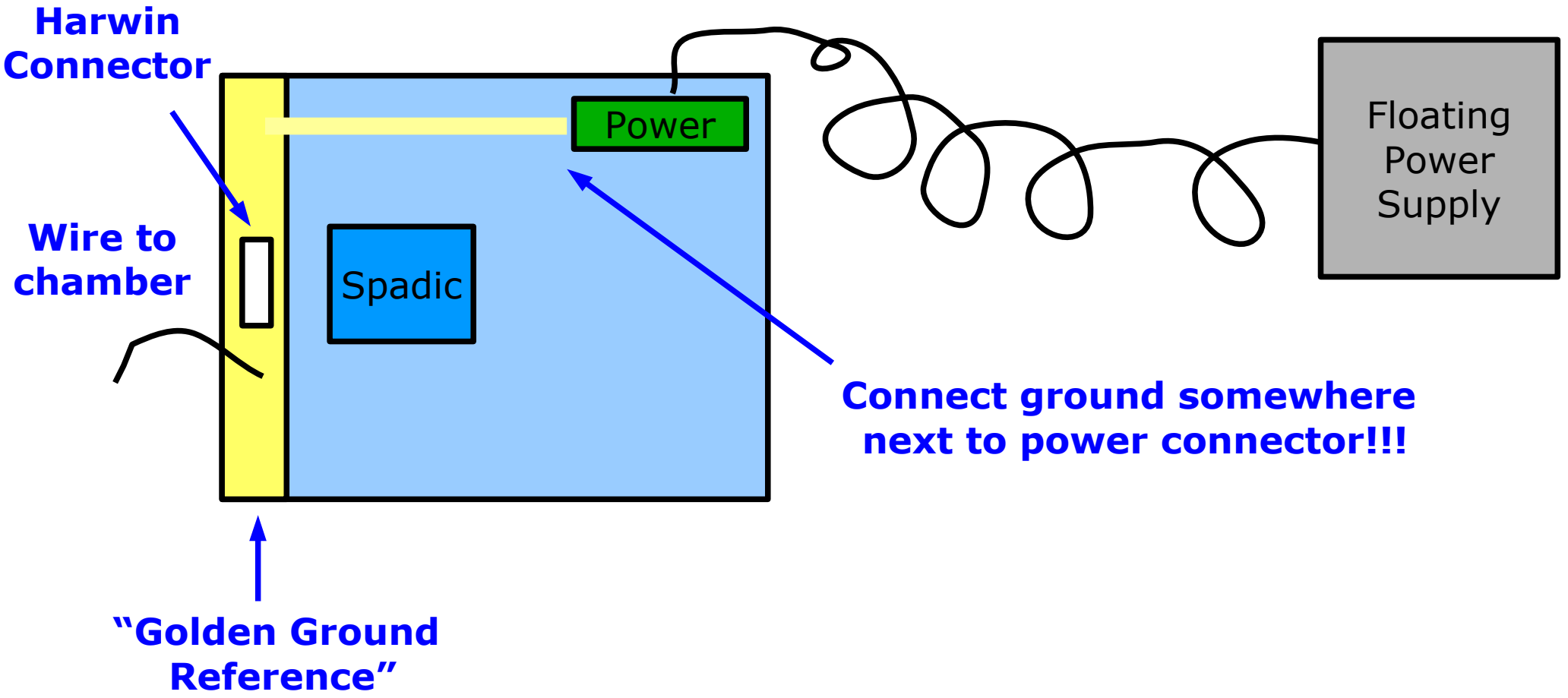
Tip from Ivan Rusanov (GSI)



Two additional layers for daisy chain powering
→ Clearer separation of power domains!

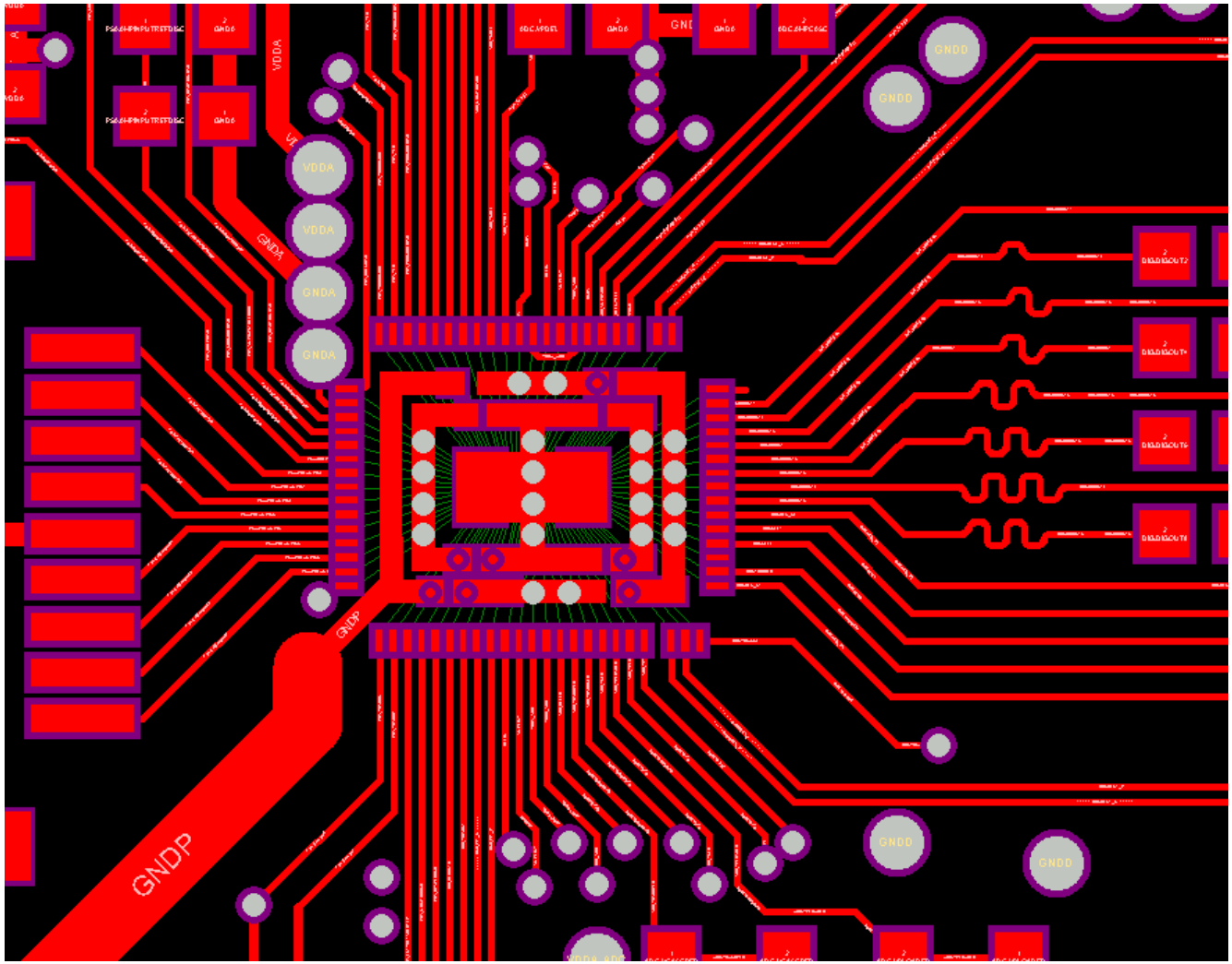
SPADIC PCB Improvement #5: Global Ground Reference

Tip from Ivan Rusanov (GSI)



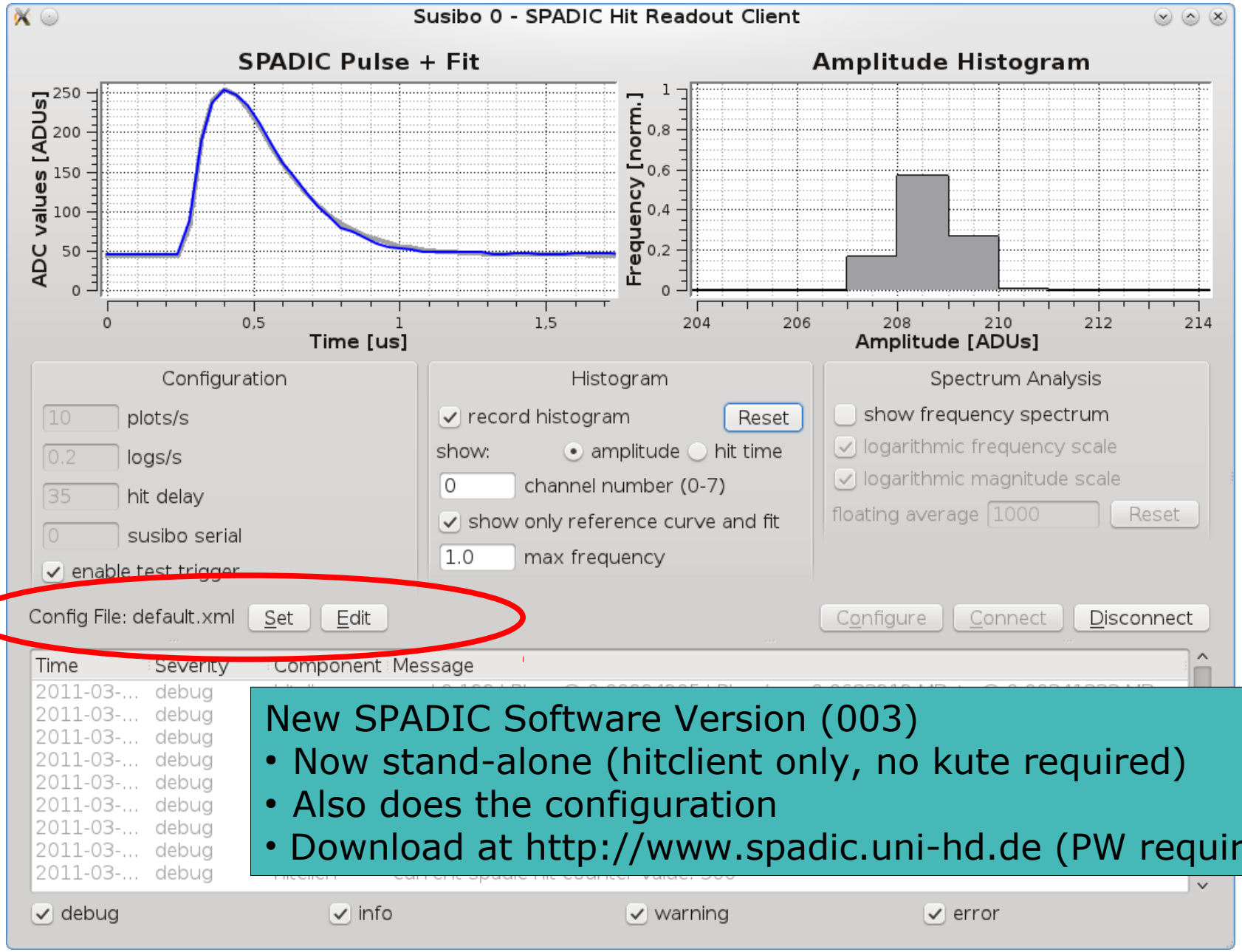
Geometrically set the analog power reference close to the SPADIC input
→ Well defined "Golden Ground"

SPADIC PCB Improvement #6: Better Footprint



Usage of power rings, well separated power domains, shorter bonding wires, much more relaxed bonding angles

Update! SPADIC Configuration, Control and Monitor Software



New SPADIC Software Version (003)

- Now stand-alone (hitclient only, no kute required)
- Also does the configuration
- Download at http://www.spadic.uni-hd.de (PW required)

5. Summary

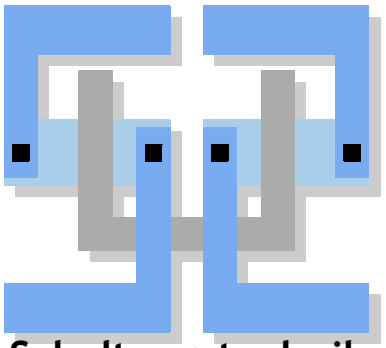
Summary

- **Parameters of SPADIC 0.3**
  - 8 complete channels (plus 18 test channels)
  - Positive input charges, about 0..32fC input range
  - 2^{nd} order shaping, 90 ns shaping time
  - Noise: 800e @ 30 pF capacitive input load
  - ADC with 8 Bit @ 25 Msamples/s
  - Power per Channel/ADC: 3.8/4.5 mW
  - Size: 1.5 x 3.2 mm²
- **Results from SPADIC 0.3**
  - At least 8 working devices (6 in parallel at CERN testbeam)
  - Complete chip works as well as the setup
  - Sophisticated readout library and software available
  - Nevertheless several problems (as shown)
  - There is a lot ideas for further improvements
  - New PCB addresses several of those improvements
  - New PCB setup will be used in the next TRD testbeam

UNIVERSITÄT HEIDELBERG

SPADIC
Self triggered Pulse Amplification and Digitization asIC

Part 2: Towards SPADIC 1.0



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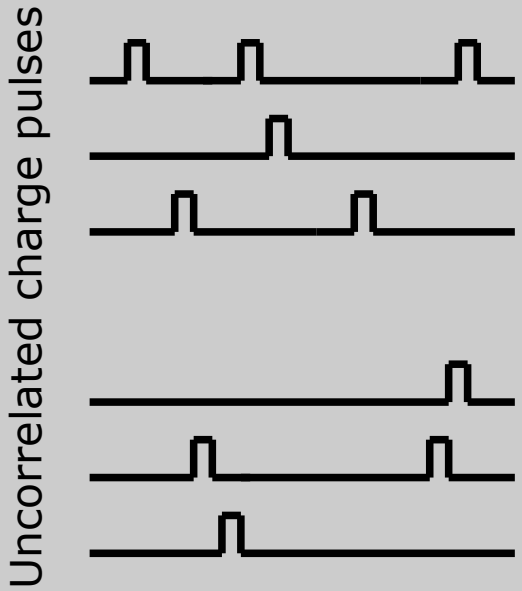
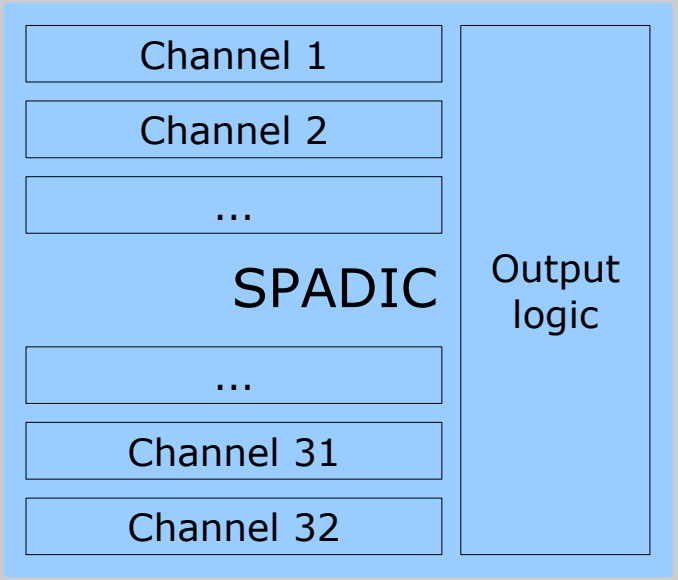
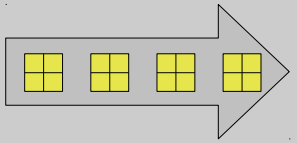
1. Introduction

Introduction to SPADIC 1.0

SPADIC: **S**elf-triggered **P**ulse **A**mplification and **D**igitization as**IC**







Output Packages @ 1Gbps (serial)

Abstract Data Flow Concept

Charge Pulse Amplification and Shaping →
Continuous Digitization →
Continuous Filtering →
Digital Hit Detection →
Package Building →
DAQ Protocol Encoding →
Fast Serial Output Interface

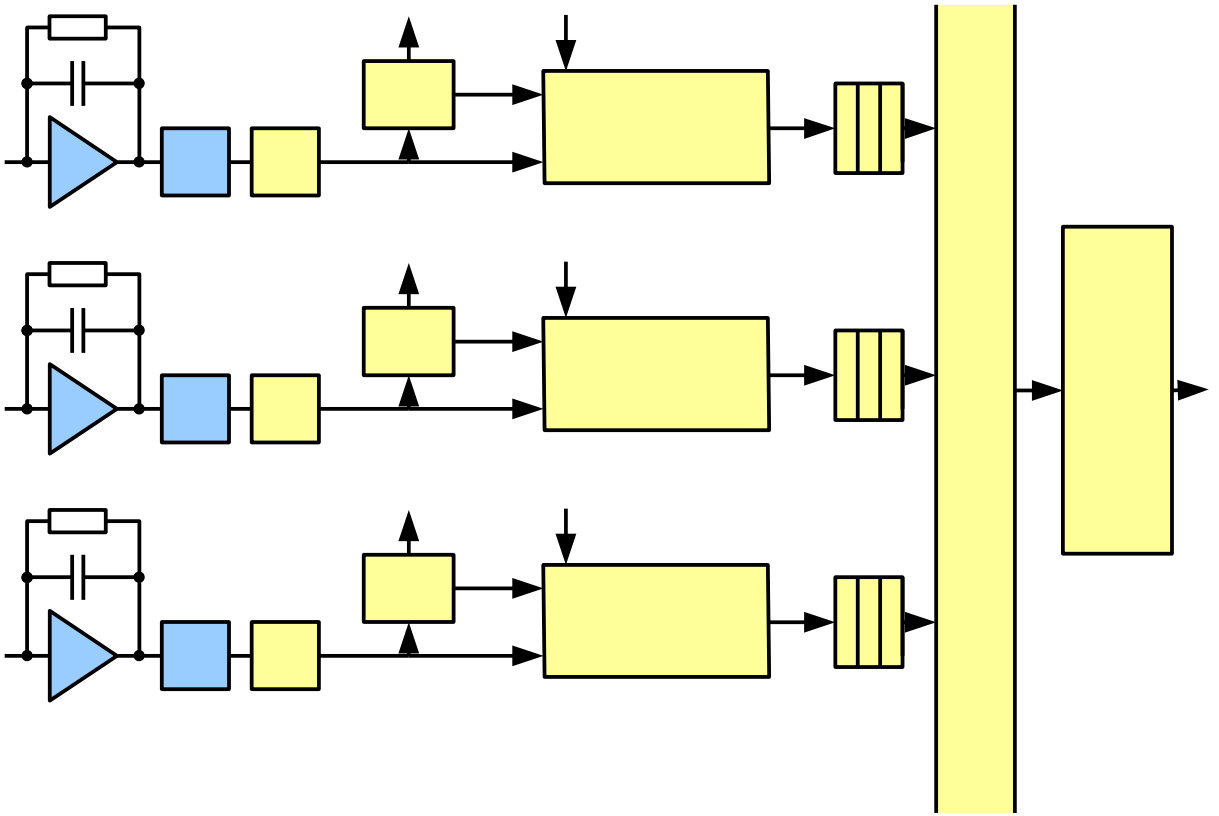
Possible SPADIC user

- **TRD**
- Maybe RICH
- MUCH ???
- ...

Planned SPADIC Architecture and Building Blocks

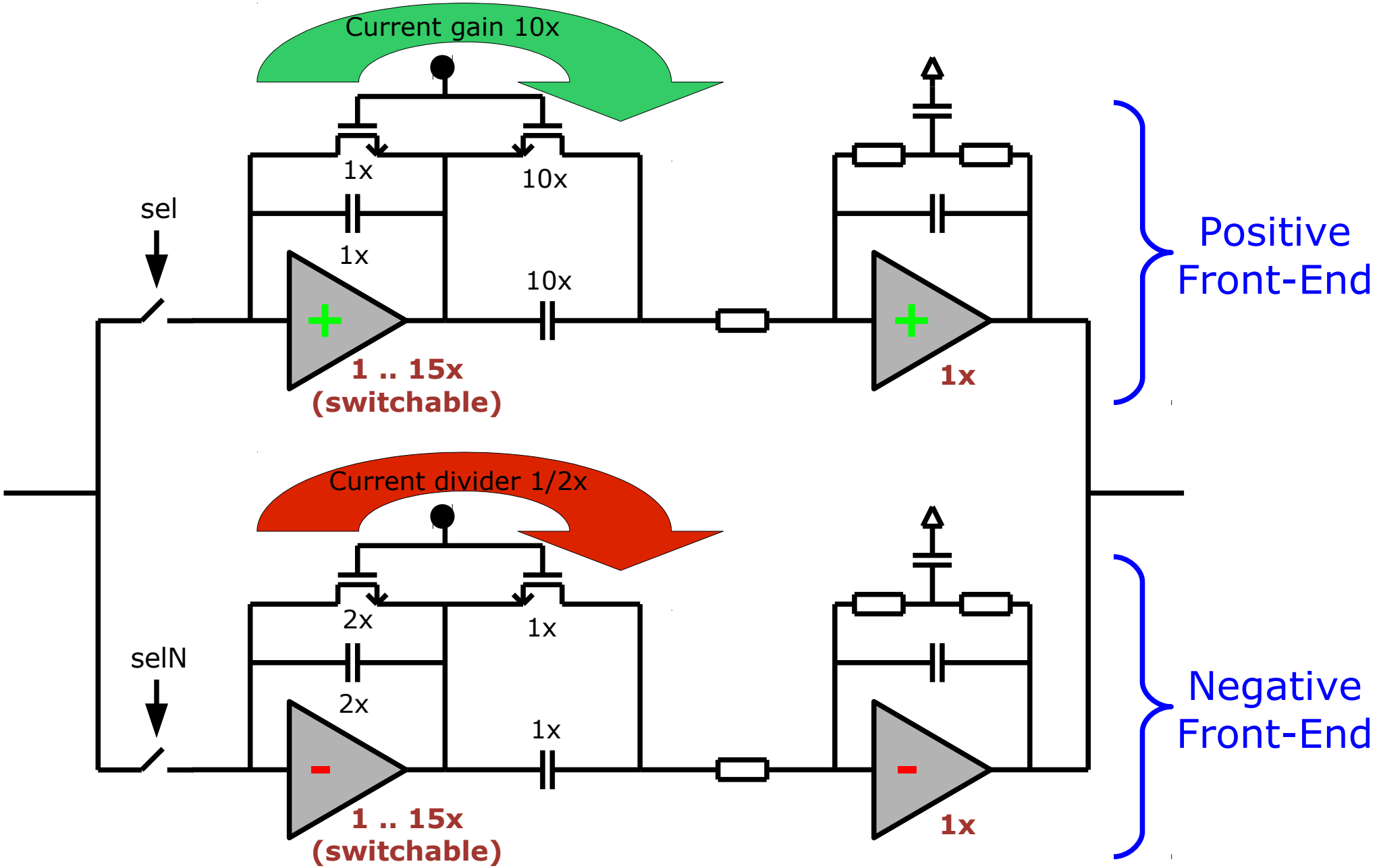
- 32 channels ASIC in UMC 180 nm
- Basic channel structure
  - Input protection
  - Preamplifier / Shaper (~ 90 ns shaping time, positive pulses)
  - ADC (~ 8 Bit)
  - IIR Filter (ion-tail cancellation, baseline correction, ...)
  - Digital trigger logic (self-triggered scheme)
  - Package builder (payload, time-stamp, channel #, …)
- Global parts after the channels
  - Inter-channel network (token ring)
  - DAQ compatible protocol encoder (computer architecture group, HD)
  - Serializer, driver (two 500 Mbit/s links per chip)

To be realized
Under construction
(Conceptually) completed

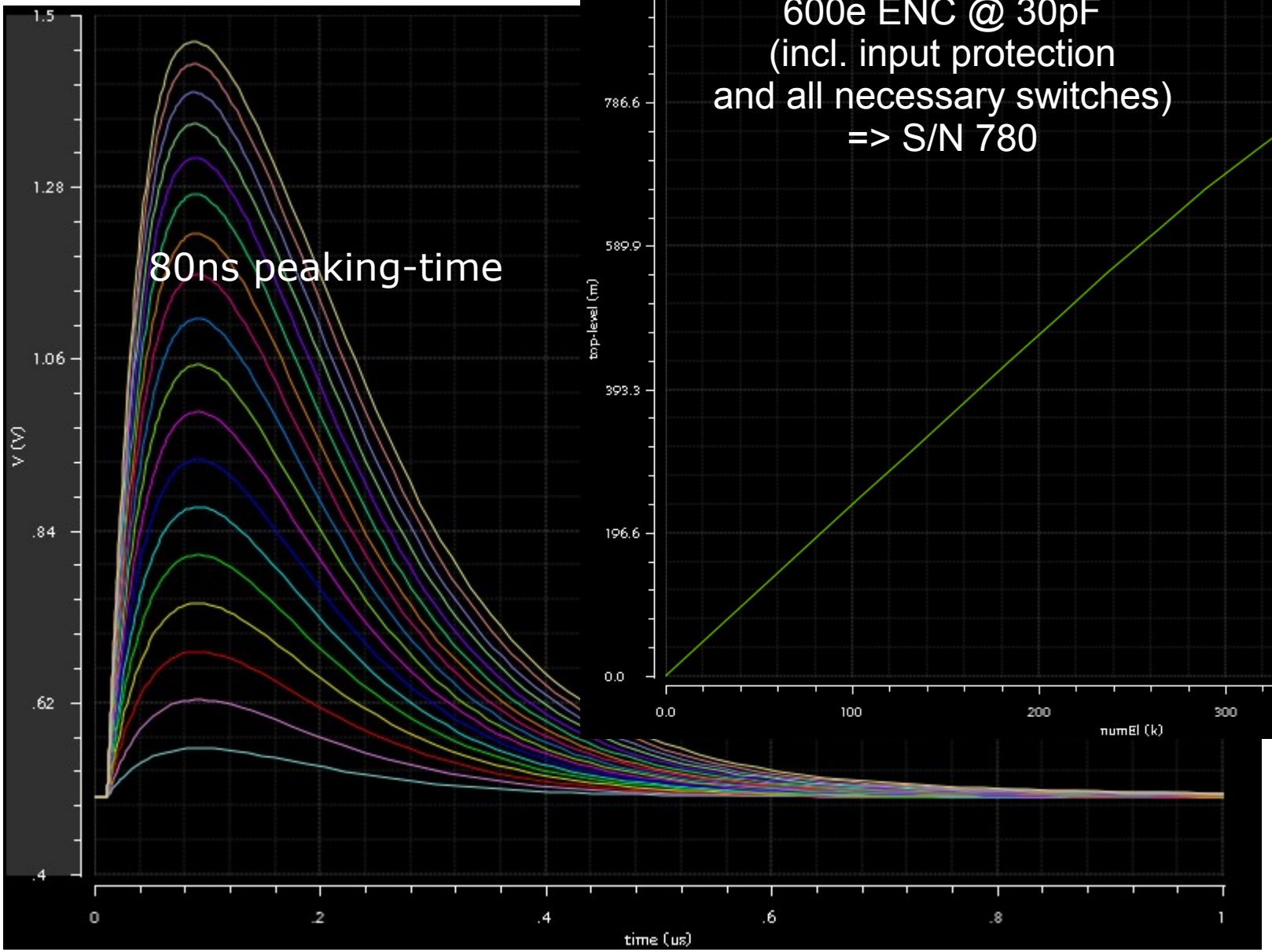


2. Analog Part

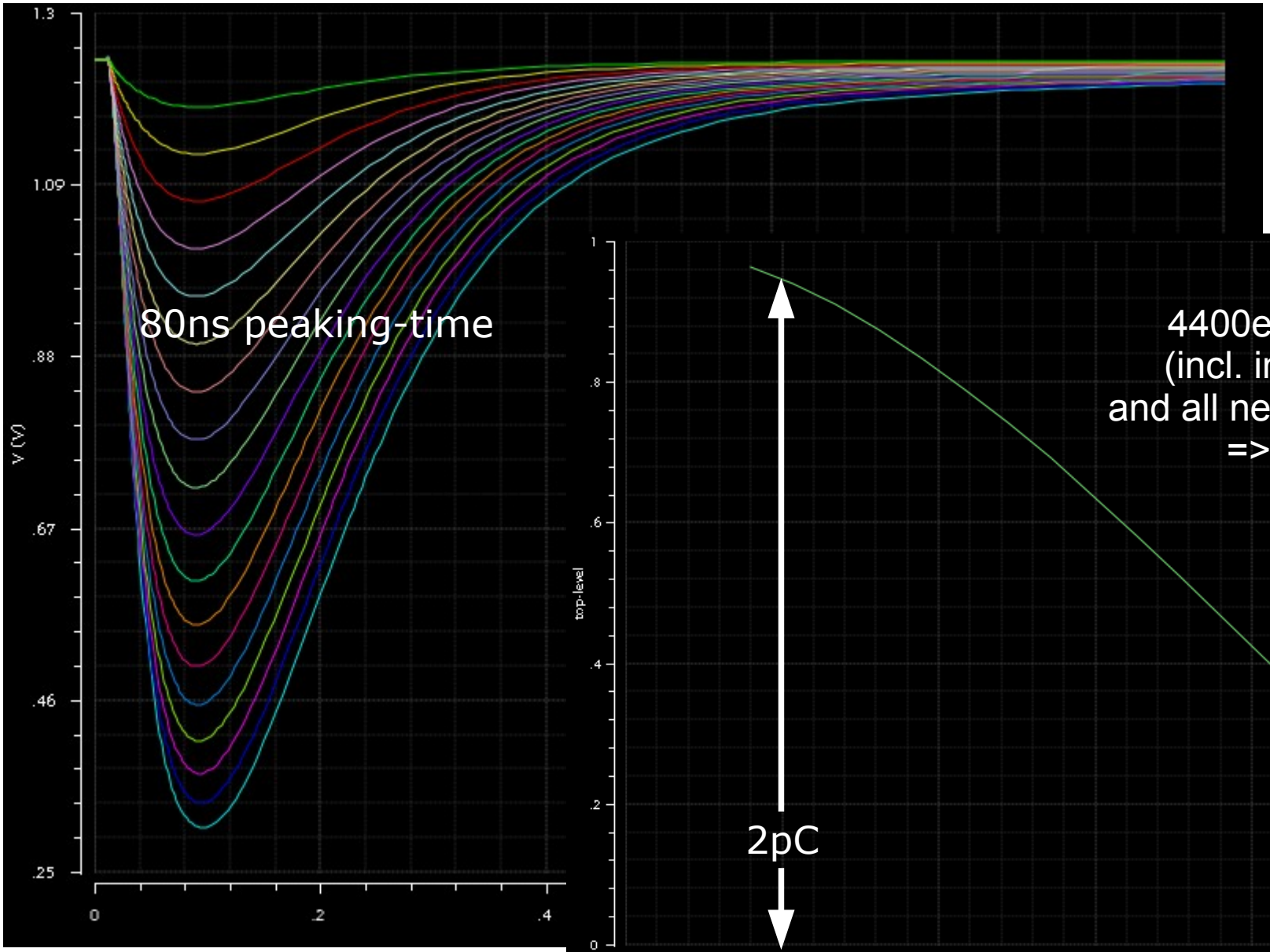
Positive Front-End Amplifier



Positive Front-End (high gain)

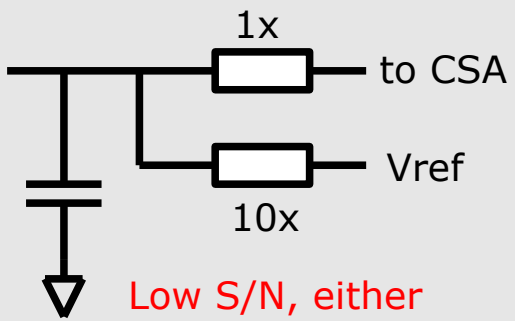


Negative Front-End (low gain)

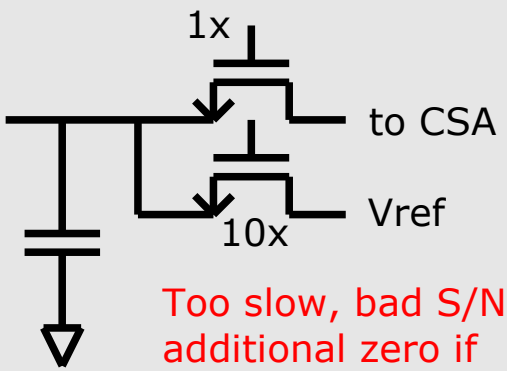


Low-Gain Ideas (and why they're not feasible)

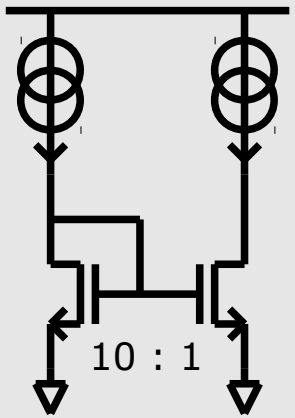
Nice to have: high gain front-end with optional charge dividers, but …
(e.g.: dynamic range TRD: 75fC, RICH: 2pC)



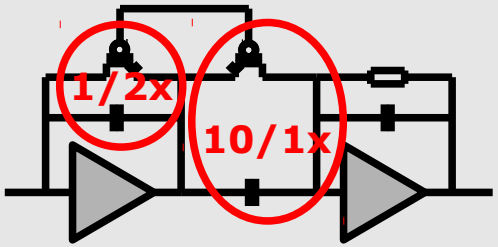
Low S/N, either time-constant too large or undershoot



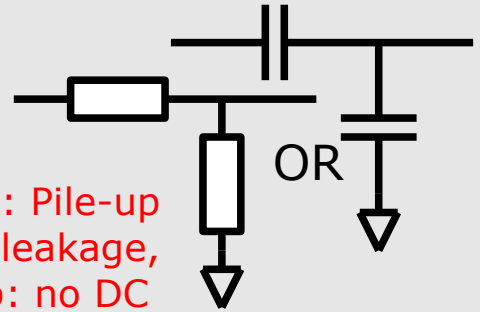
Too slow, bad S/N, additional zero if MOS too strong



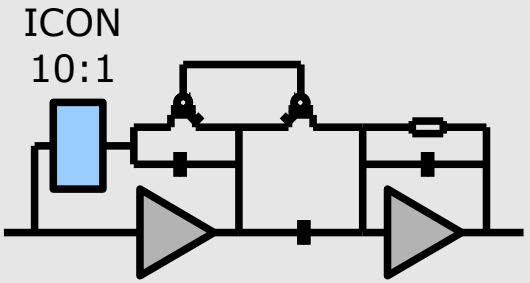
Proper biasing difficult, some kind of leakage compensation needed



Switchable: Due to several constraints very difficult, consumes much chip area



Res: Pile-up vs. leakage, Cap: no DC path, hides virtual ground

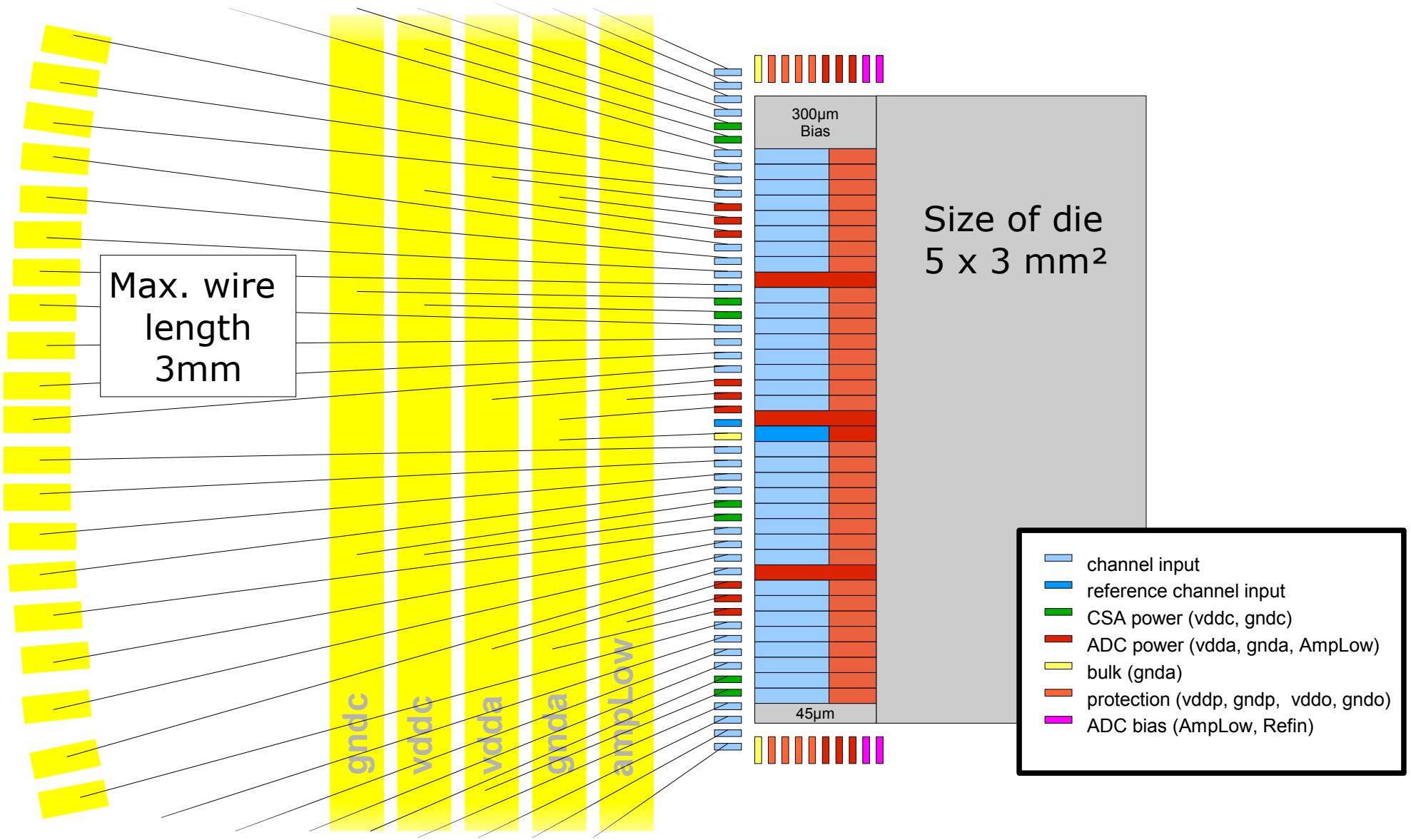


Virtual gain reduction: theoretically nice but design very difficult

… it's very difficult to divide the very fast pulses (< 10ns) properly!!!

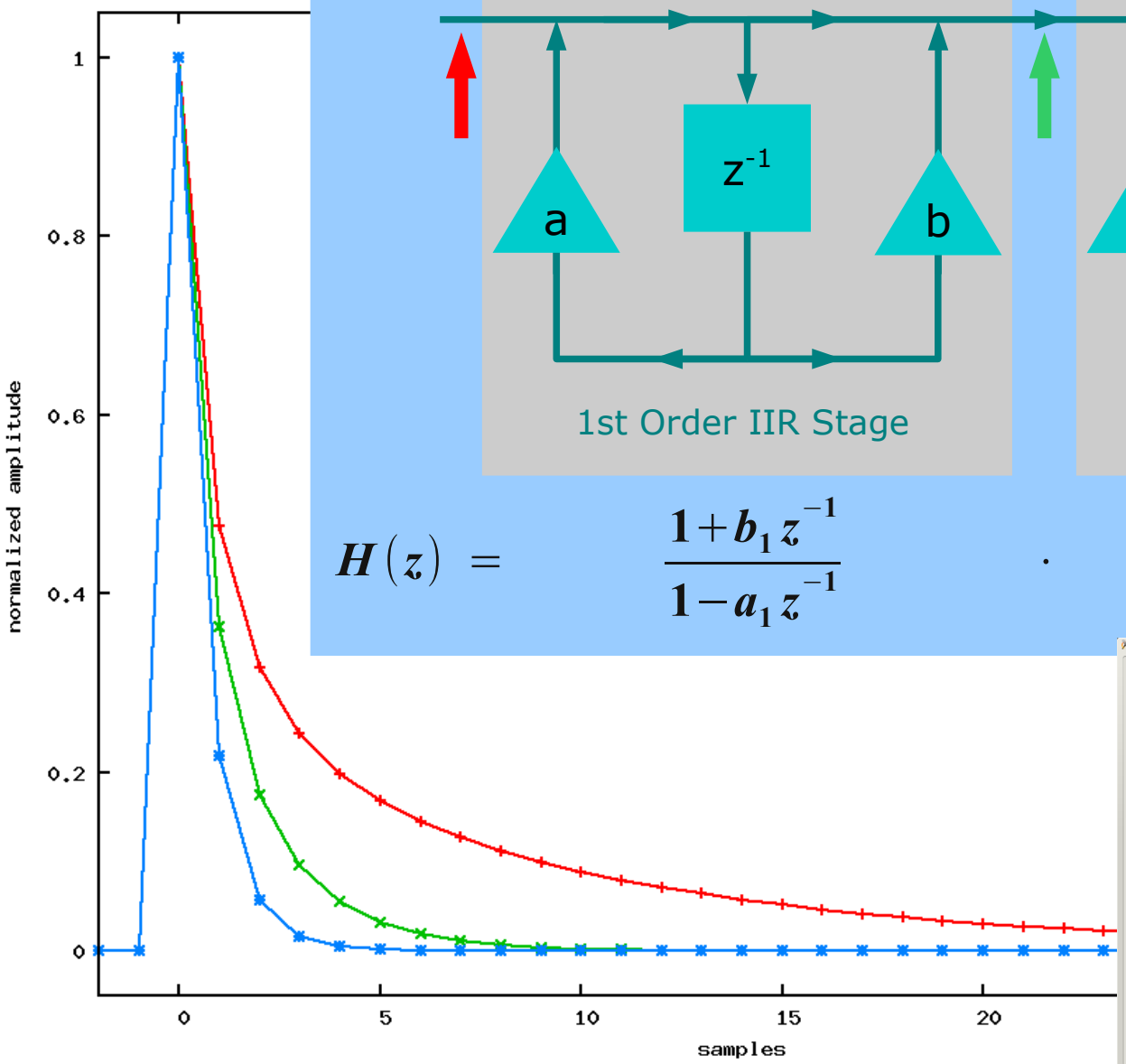
SPADIC 1.0 FE Pad Plan

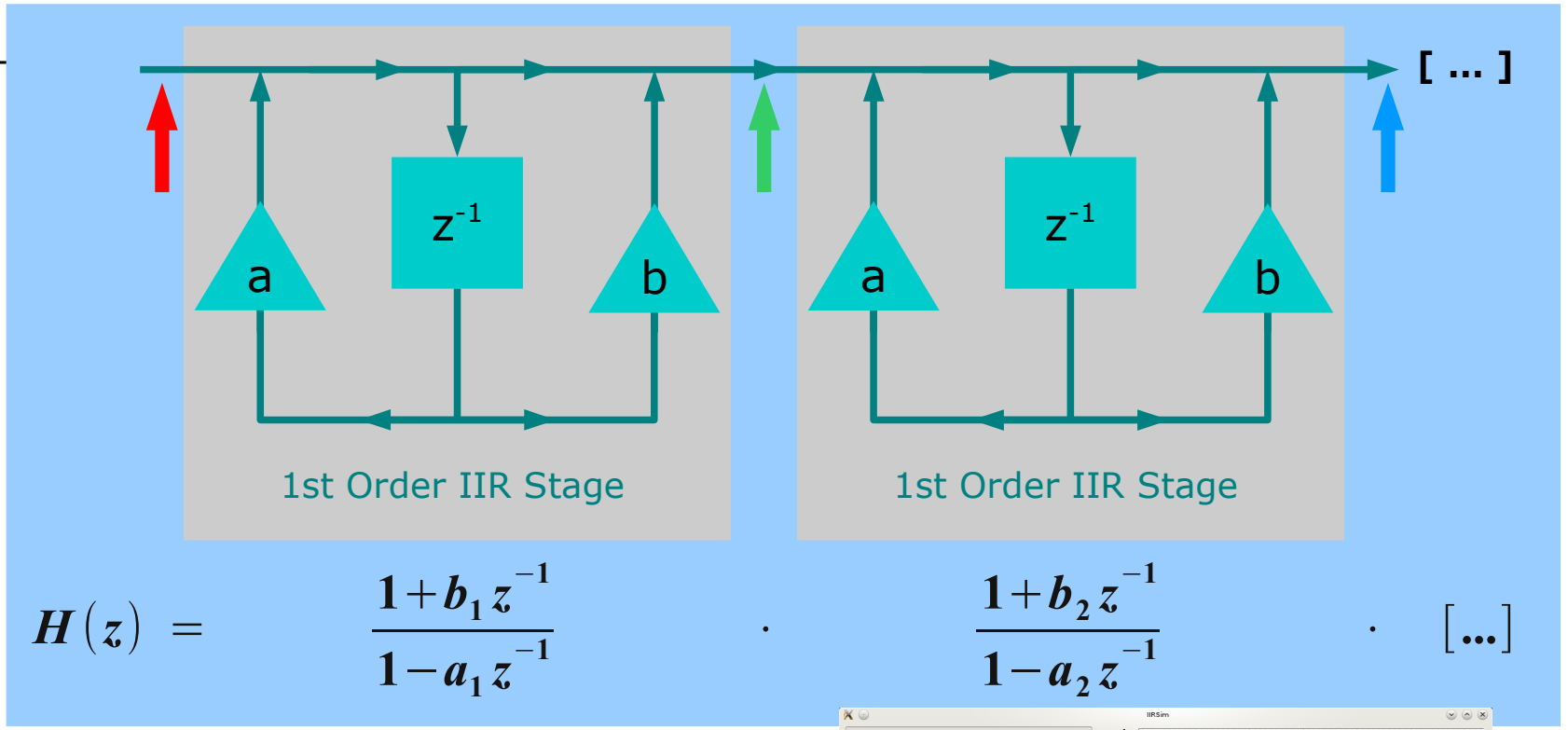
51 pads (95µm pitch), 120µm channel pitch
→ 32+1 channels, 9 x vdda/gnda/AmpLow (ADC), 8 x vddc/gndc (CSA), 1 x bulk (gnda)

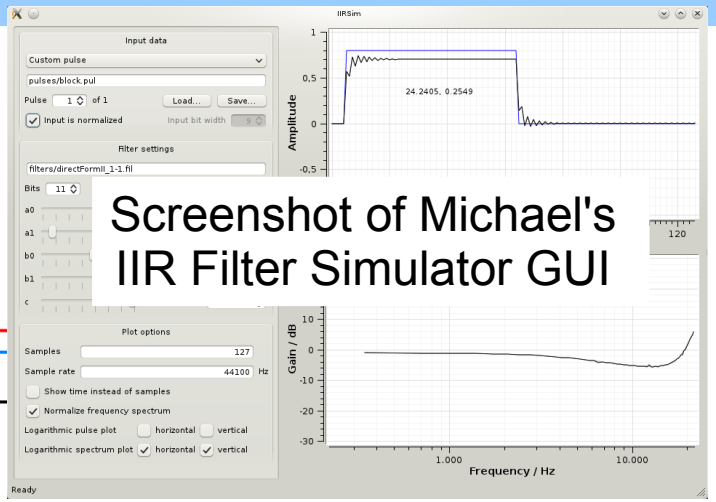


3. Digital Part

IIR Filter Concept (Ion-Tail Cancellation)

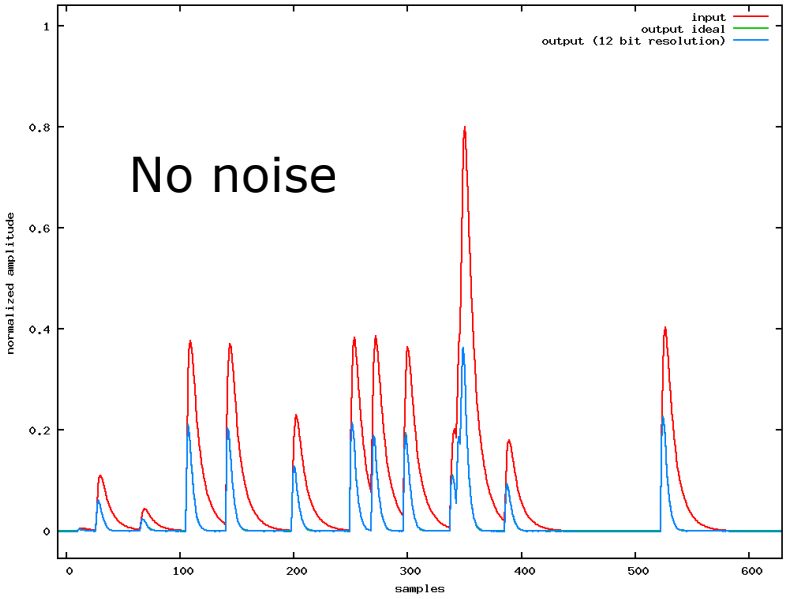


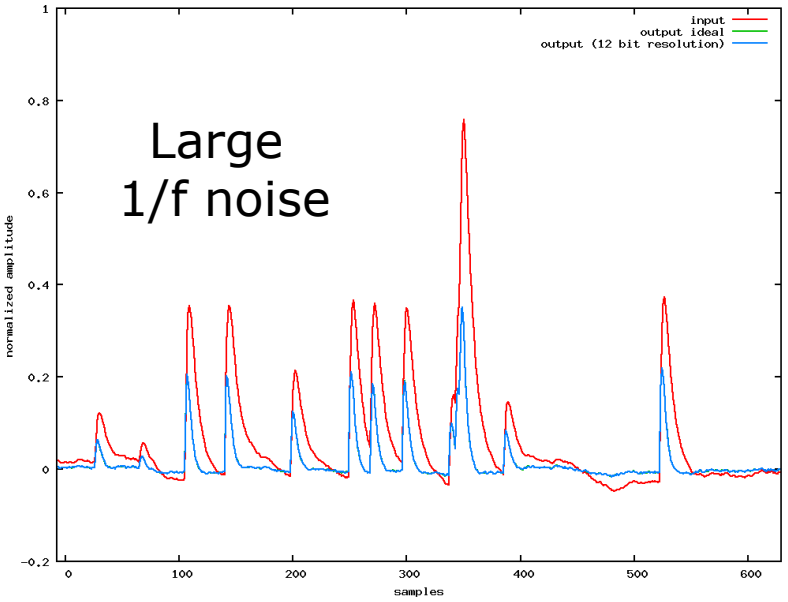


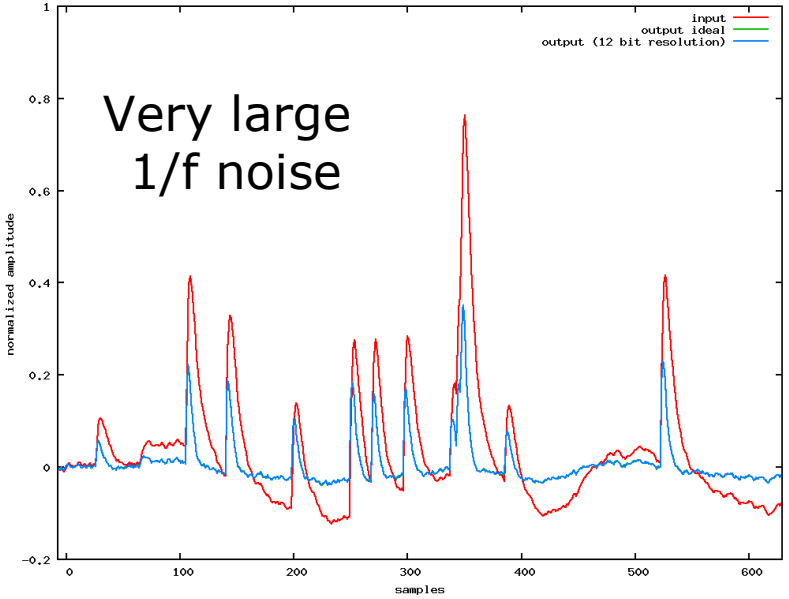


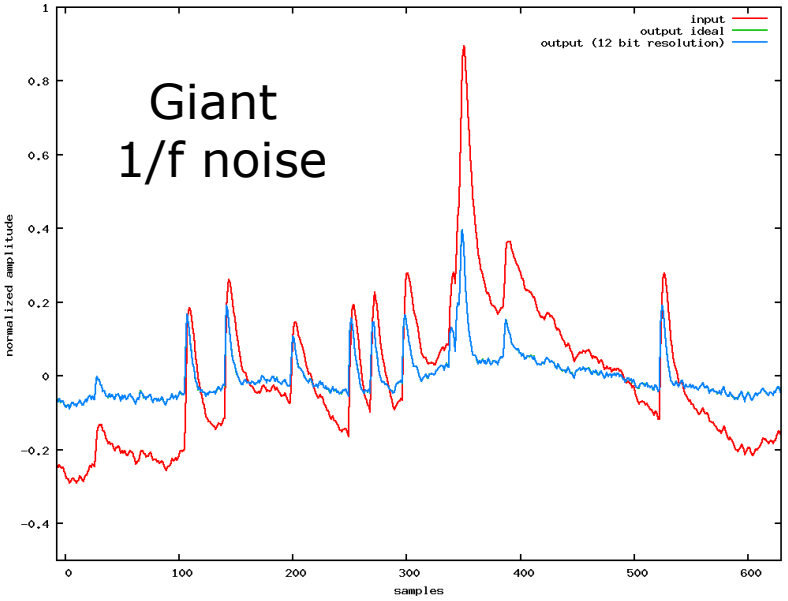
Results from Michael Krieger (Diploma Student)

Some Simulation Results









Results from Michael Krieger

Some IIR filter simulation results

red: Input signal with ion-tail

blue: IIR filter result (12 bit internal resolution)

green: Ideal IIR filter result (no difference to blue visible)

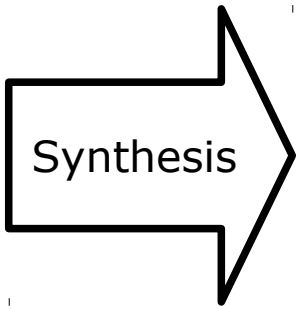
Multiplier

Simple (but probably best) approach:

```
Verilog:

input wire [11:0] A, B;
output wire [23:0] C;

assign C = A * B;
```



Without any optimization or constraints, mapped to our standard-cell library without HA or FA

Timing Report:

Critical path: 6.6 ns => 151 MHz

We need to perform two multiplications in 40 ns

=> *Already more than fast enough!*

Gate Report:

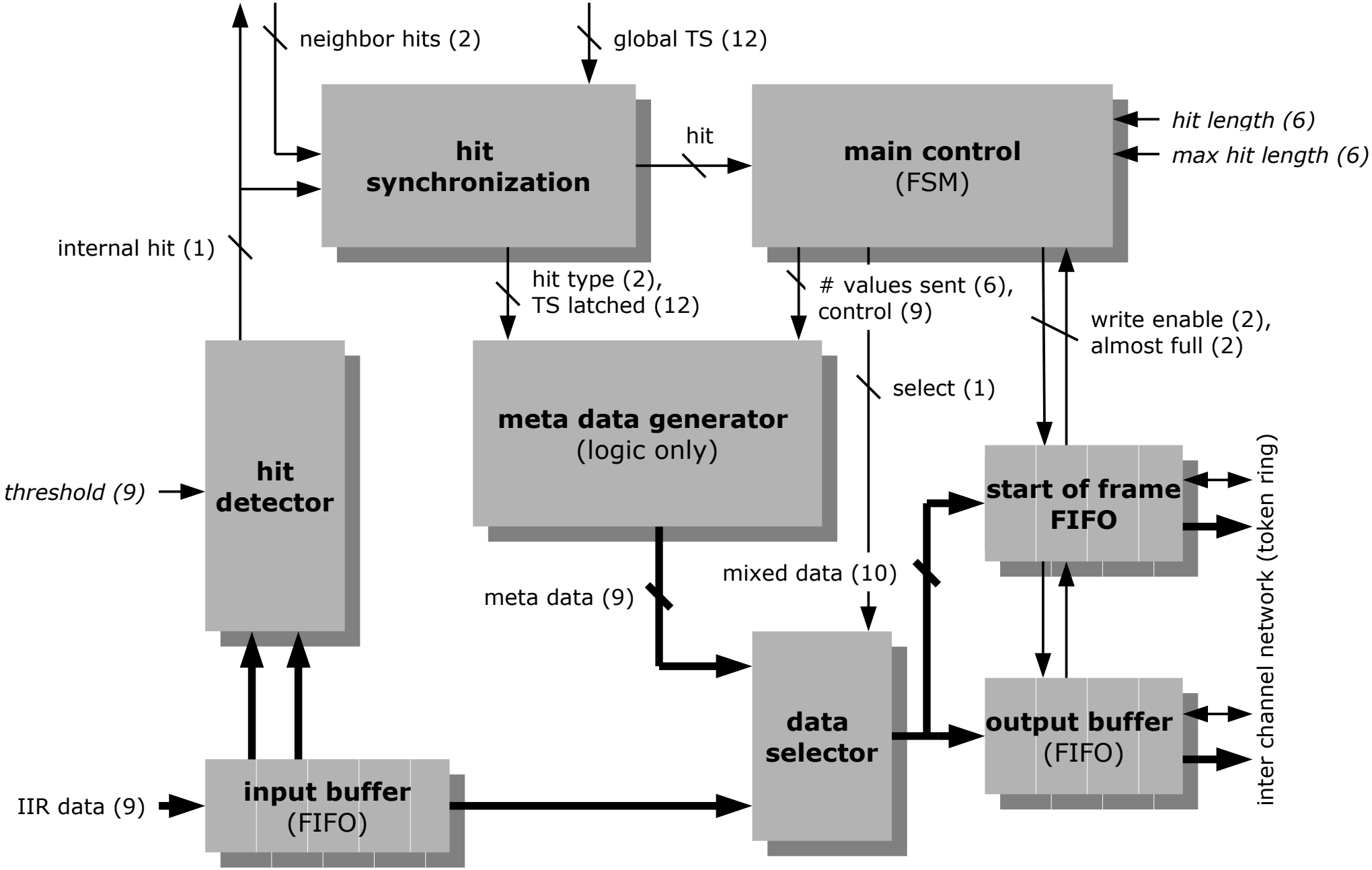
631 gates, 12500 µm² area

With channel pitch of 120 µm: multiplier size 120 x 104 µm²

=> *Only size (and power) matters!*

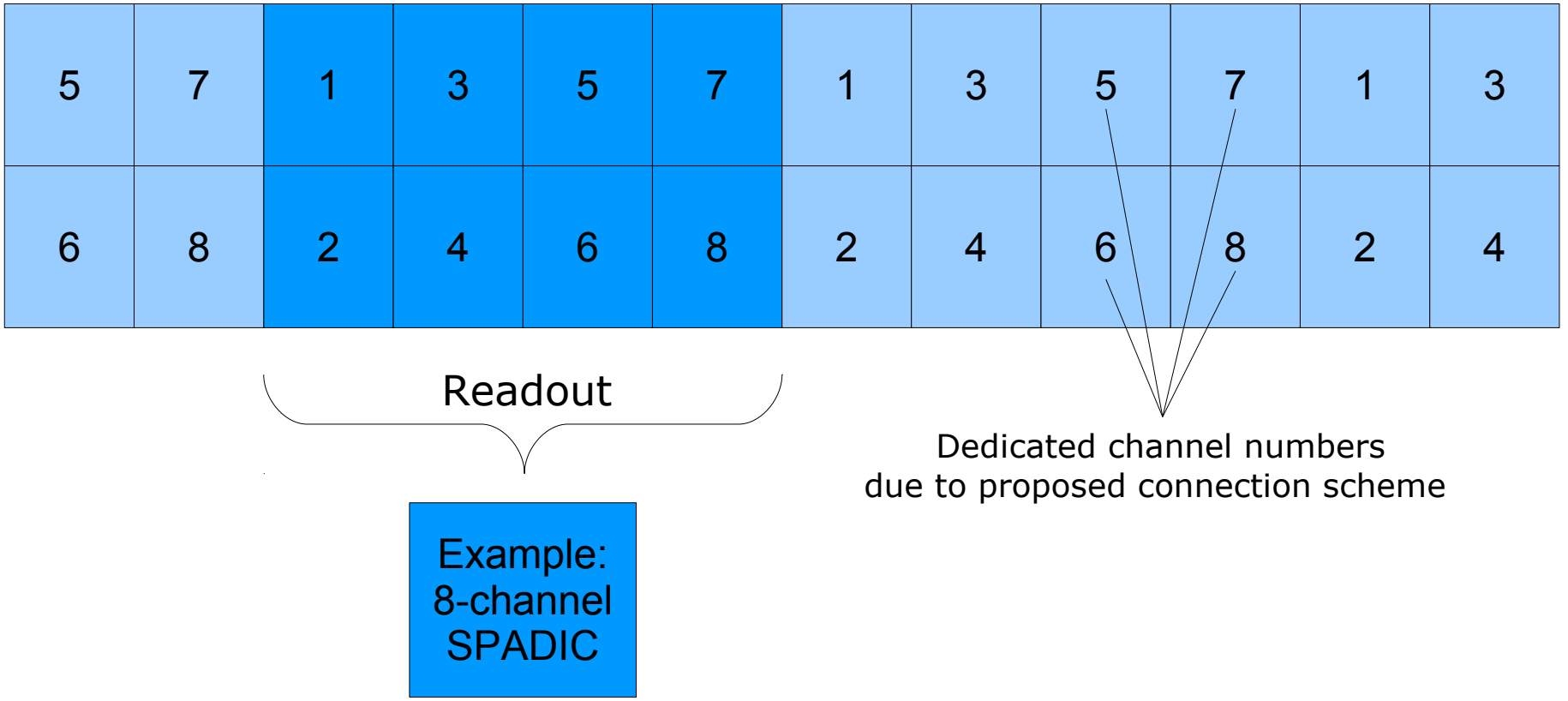
Results from Michael Krieger

Digital Hit Detector and Package Builder



Neighbor Logic

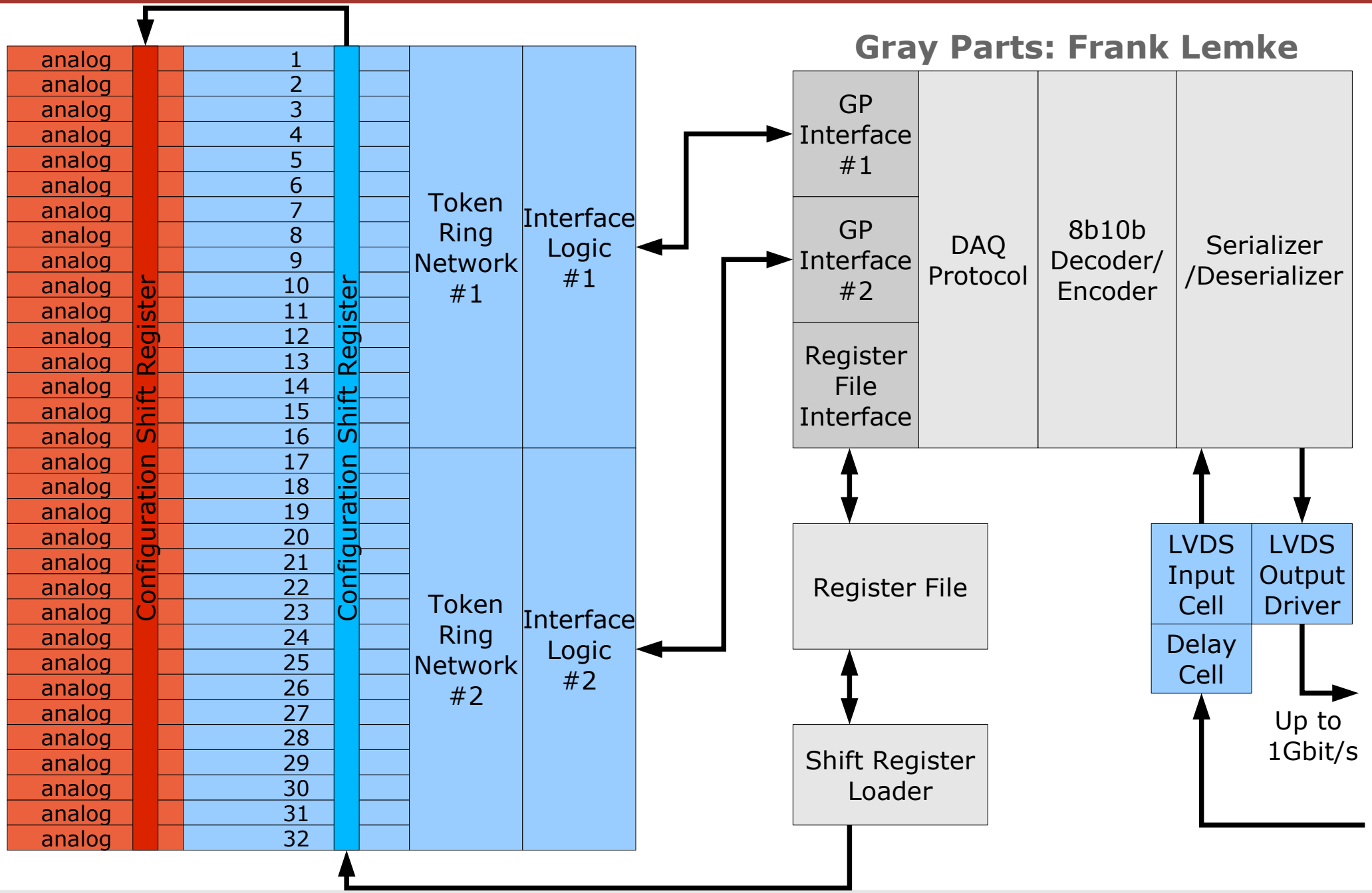
David's Pad Plane Proposal:



=> Neighbor-Chain-1: … ↔ 1 ↔ 3 ↔ 5 ↔ 7 ↔ 1 ↔ 3 ↔ …
Neighbor-Chain-2: … ↔ 2 ↔ 4 ↔ 6 ↔ 8 ↔ 2 ↔ 4 ↔ …

=> TRD: Neighbor-Relation between every second channel
=> Three neighbor-modes: off, direct and zip

Output Interface + Configuration



4. Summary

Summary

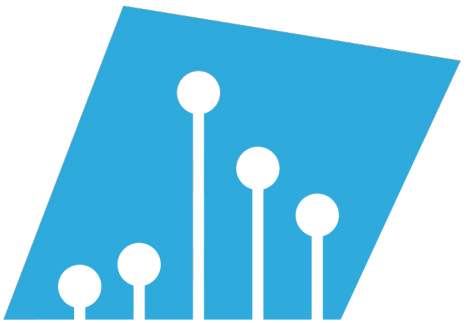
Status of SPADIC 1.0 Development

- Analog part
  - Two front-ends (positive high-gain + negative low-gain)
  - Concept and schematics close to final
  - Channel structure, pad plan and powering scheme completed
  - ADC design stays almost unchanged
  - Both front-ends must be laid out
- Digital part
  - Simulation results of IIR filter seems promising
  - IIR multiplier probably fast and small enough
  - Data gathering concept finished
  - Output logic concept finished
  - DAQ protocol under construction (Frank Lemke)

Next Steps

- Finish analog part
- Build peripheral parts (DACs, bias-diodes, IO-cells, LVDS-cells, …)
- Build first synthesized IIR filter iteration
- Start to simulate and validate digital back end (neighbor + trigger logic, package builder, output logic, …)

=> Still a lot of work that has to be done – focus goes now to digital parts



SPADIC

Self triggered Pulse Amplification and Digitization asIC

http://www.spadic.uni-hd.de