UNIVERSITÄT HEIDELBERG

SPADIC
Self triggered Pulse Amplification and Digitization asIC

SPADIC for RICH

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17th CBM CM, Dresden

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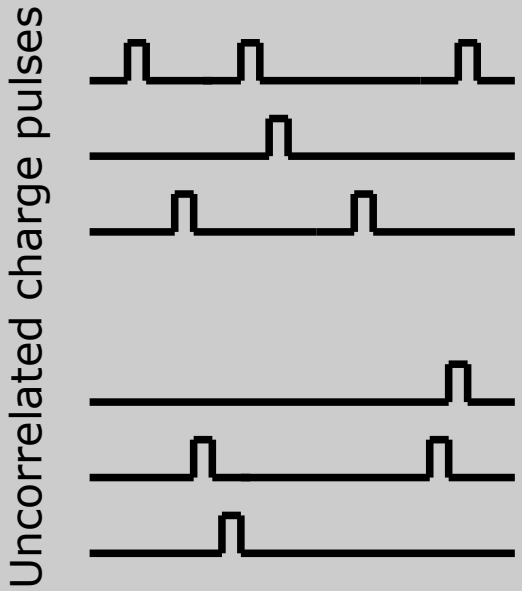
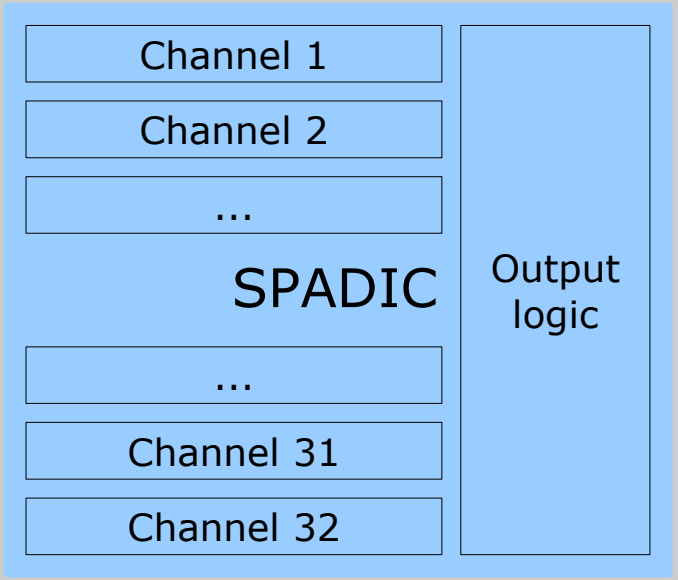
Visit http://www.spadic.uni-hd.de

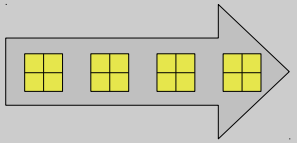
1. Planned SPADIC Architecture

Introduction to SPADIC 1.0

SPADIC: **S**elf-triggered **P**ulse **A**mplification and **D**igitization as**IC**







Output Packages @ 1Gbps (serial)

Abstract Data Flow Concept

Charge Pulse Amplification and Shaping →
Continuous Digitization →
Continuous Filtering →
Digital Hit Detection →
Package Building →
DAQ Protocol Encoding →
Fast Serial Output Interface

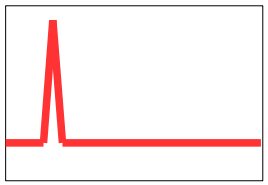
See next slides

Possible SPADIC user

- **TRD**
- Maybe RICH
- MUCH ???
- ...

The processing chain of SPADIC 1.0 – Step 1

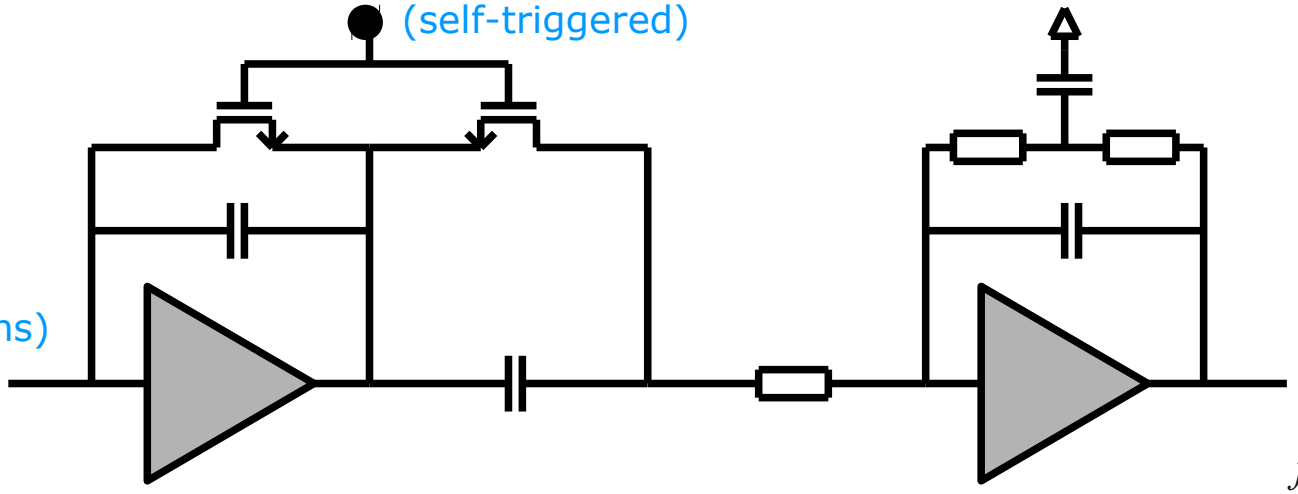
Step 1: Amplification + Shaping



Fast charge pulse from detector (< 10ns)

(RICH: negative, up to 2pF)

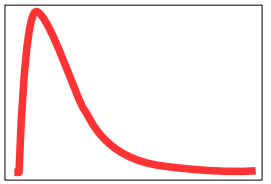
Continuous rest (self-triggered)



Charge Amplifier

2nd Order Shaper

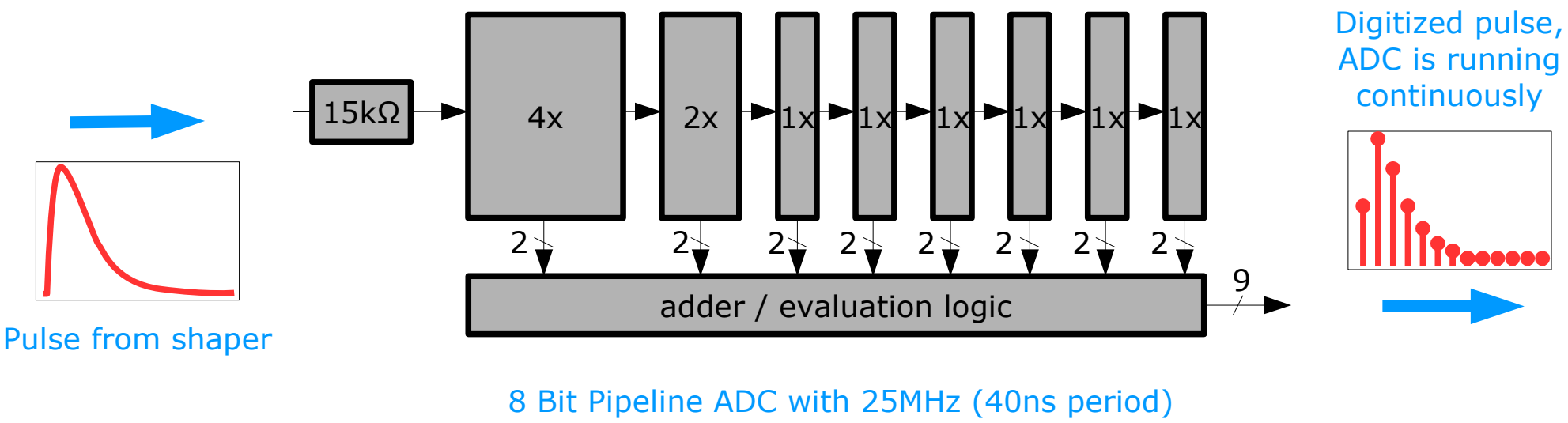
Voltage pulse, shape depends only on shaping-time:



$$f(t) = \left(\frac{t}{T}\right)^2 \exp\left(\frac{t}{T}\right)$$

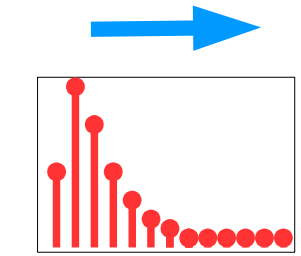
The processing chain of SPADIC 1.0 – Step 2

Step 2: Digitization



The processing chain of SPADIC 1.0 – Step 3

Step 3: Data processing + Data Gathering



Pulse from ADC

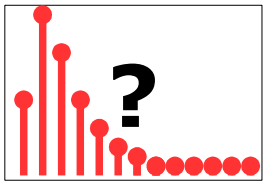
Ion-Tail IIR Filter (TRD Ion Drift)

Baseline Correction

Additional Shaping

[...]

Different data processing stages

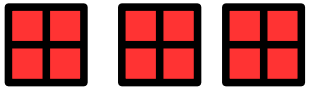


Digital Hit Detection
+
Package Builder

(scan for hits, choose data plus meta data, build package, send out)

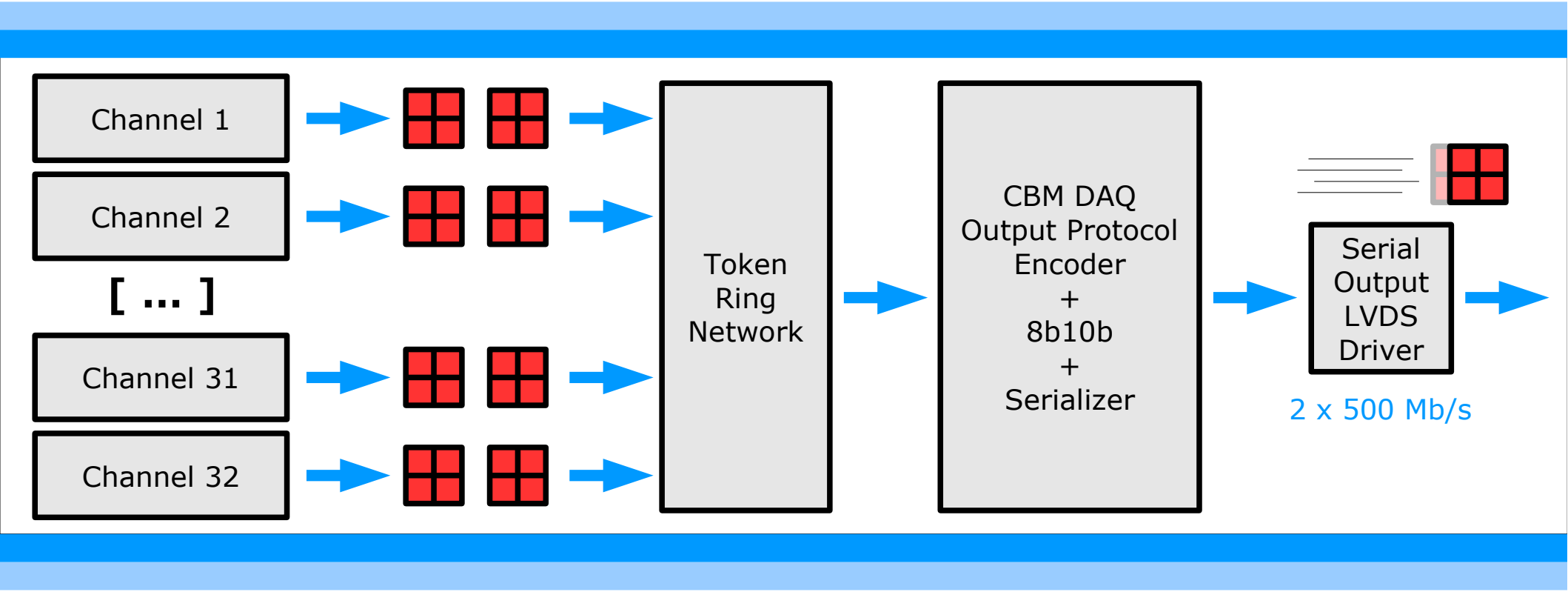
Data gathering stage

Hit packages (pulse data + meta data)



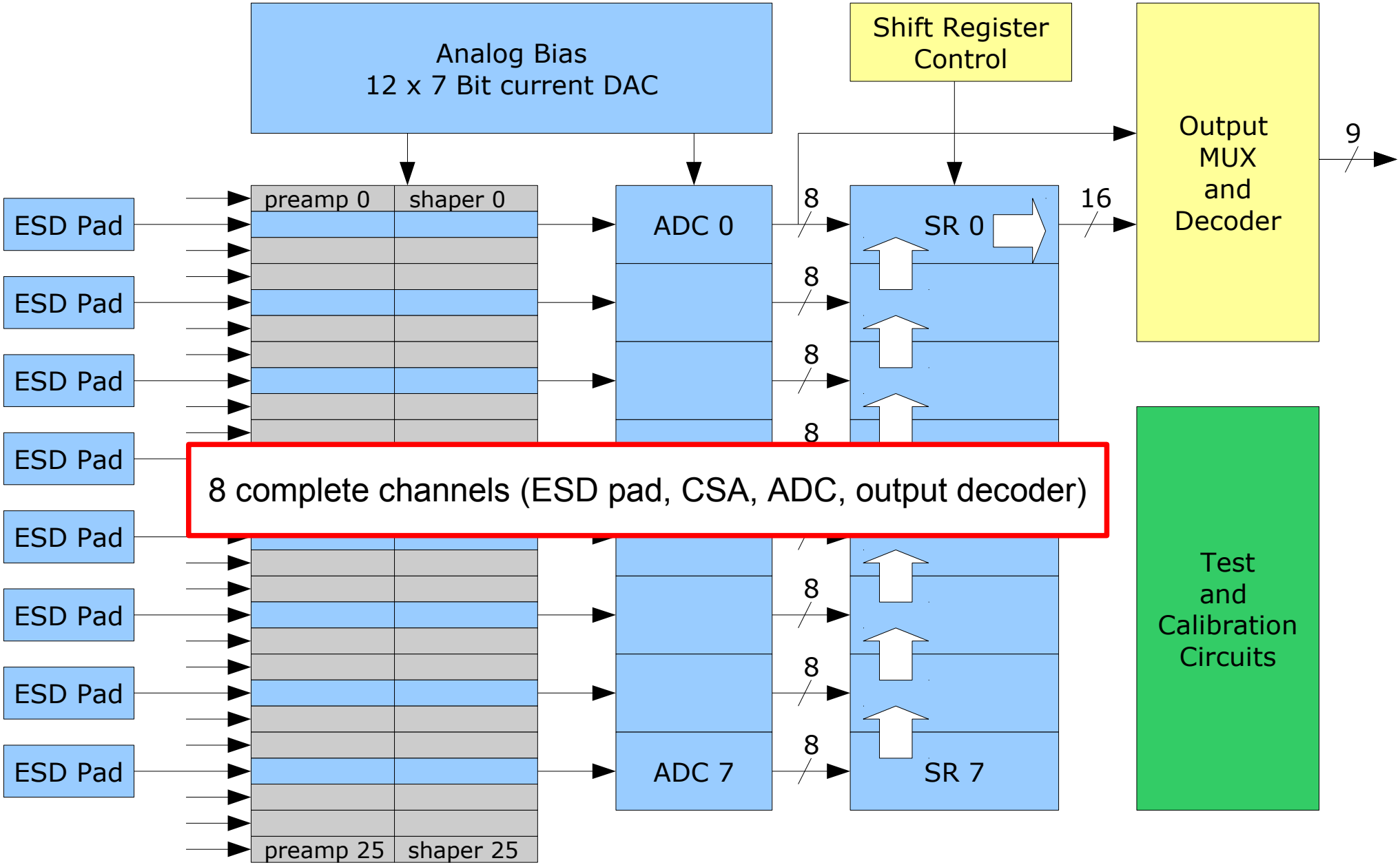
The processing chain of SPADIC 1.0 – Step 4

Step 4: Inter-Channel Network and Output Protocol

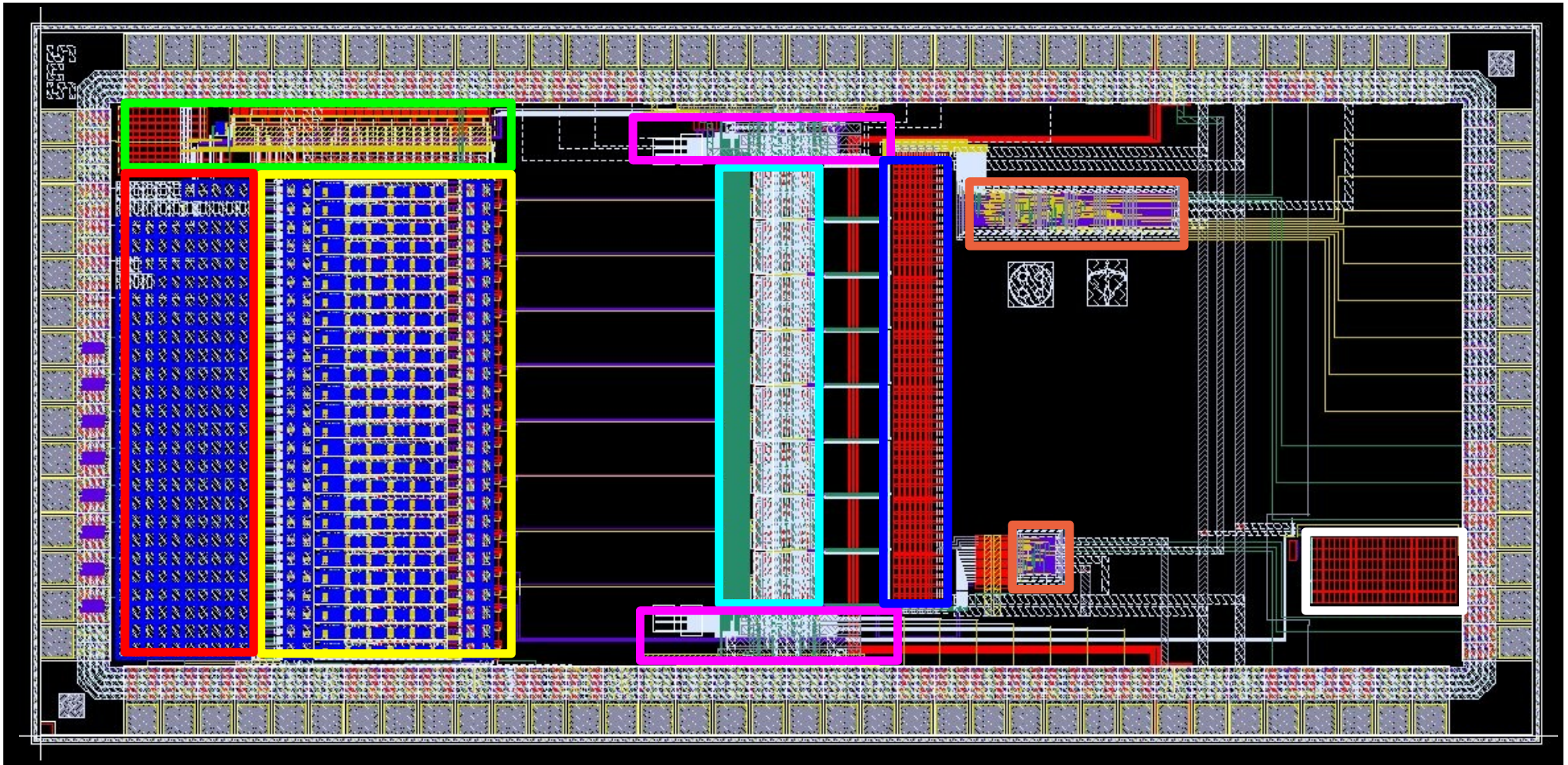


2. Latest SPADIC (version 0.3)

Block Diagram of Latest SPADIC v0.3



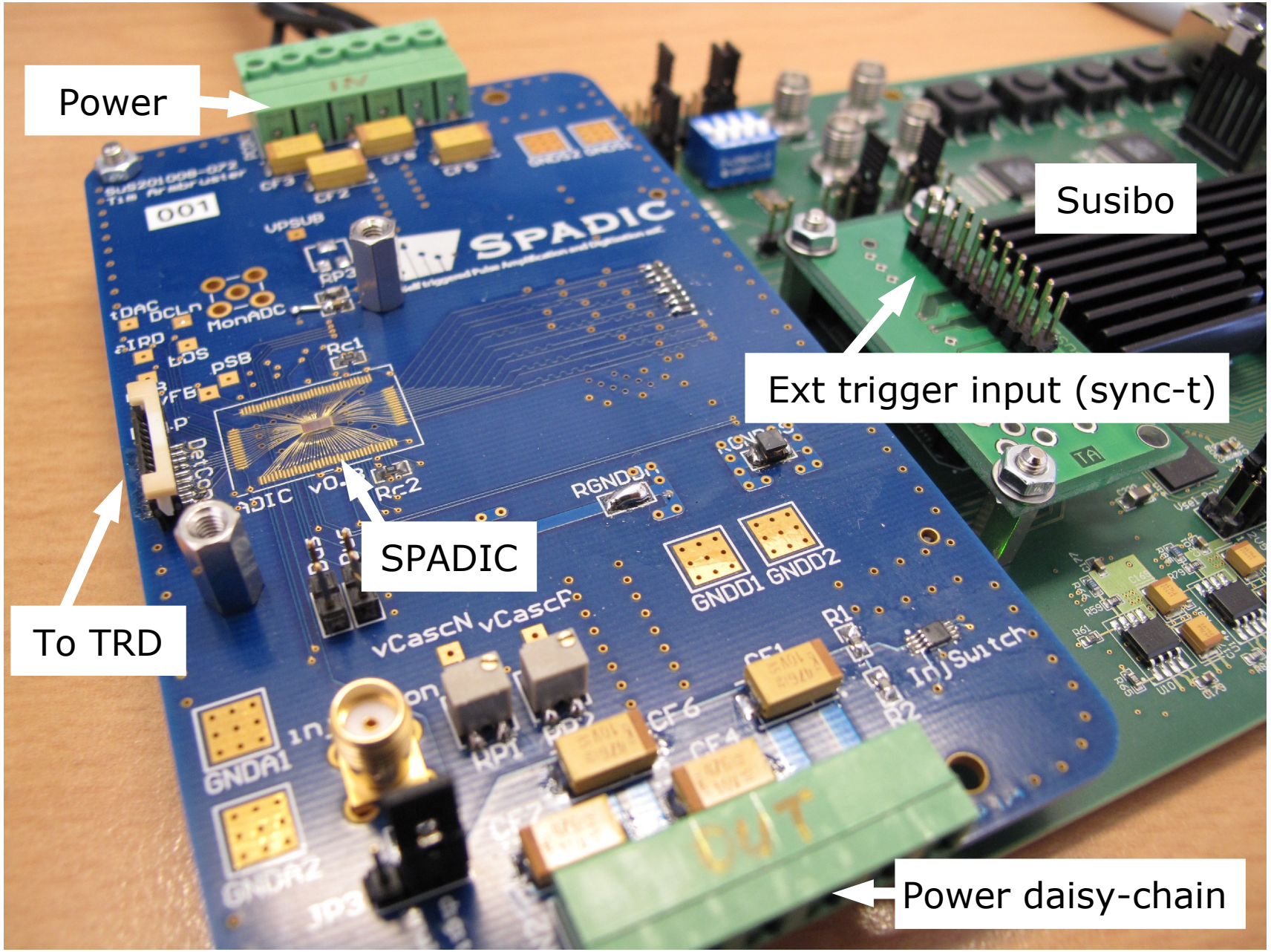
Latest SPADIC: Layout



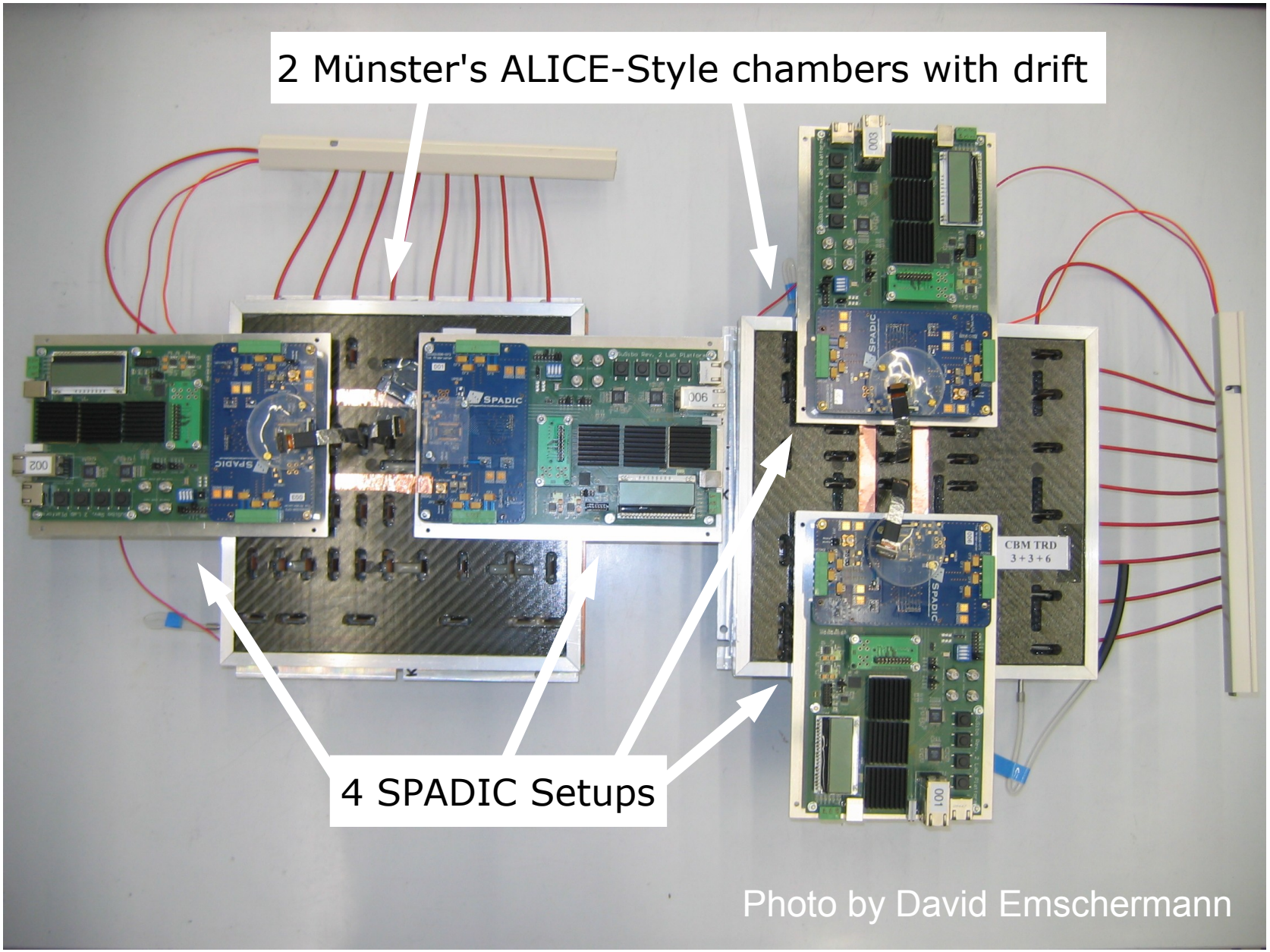
Bias circuitry (12 current DACs)
26 preamp/shaper channels
Detector capacitors (5pF per block)
8 pipelined ADCs

ADC control + bias
5.2 kBit shift register matrix
Control + readout/decoder logic blocks
Test circuits

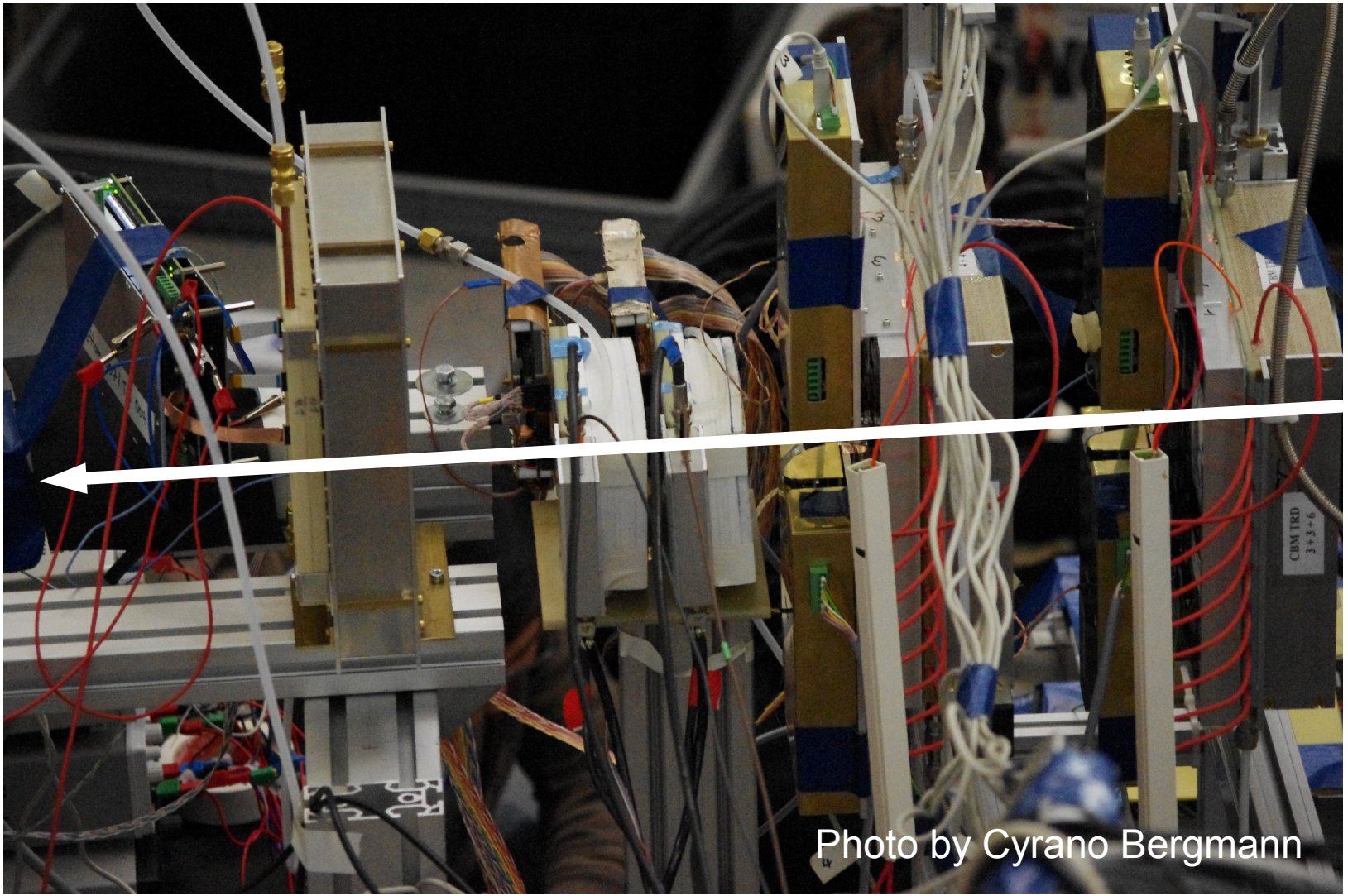
Test-Setup: SPADIC plugged on Susibo



CERN Testbeam 2010: Münster's TRD-SPADIC Setup

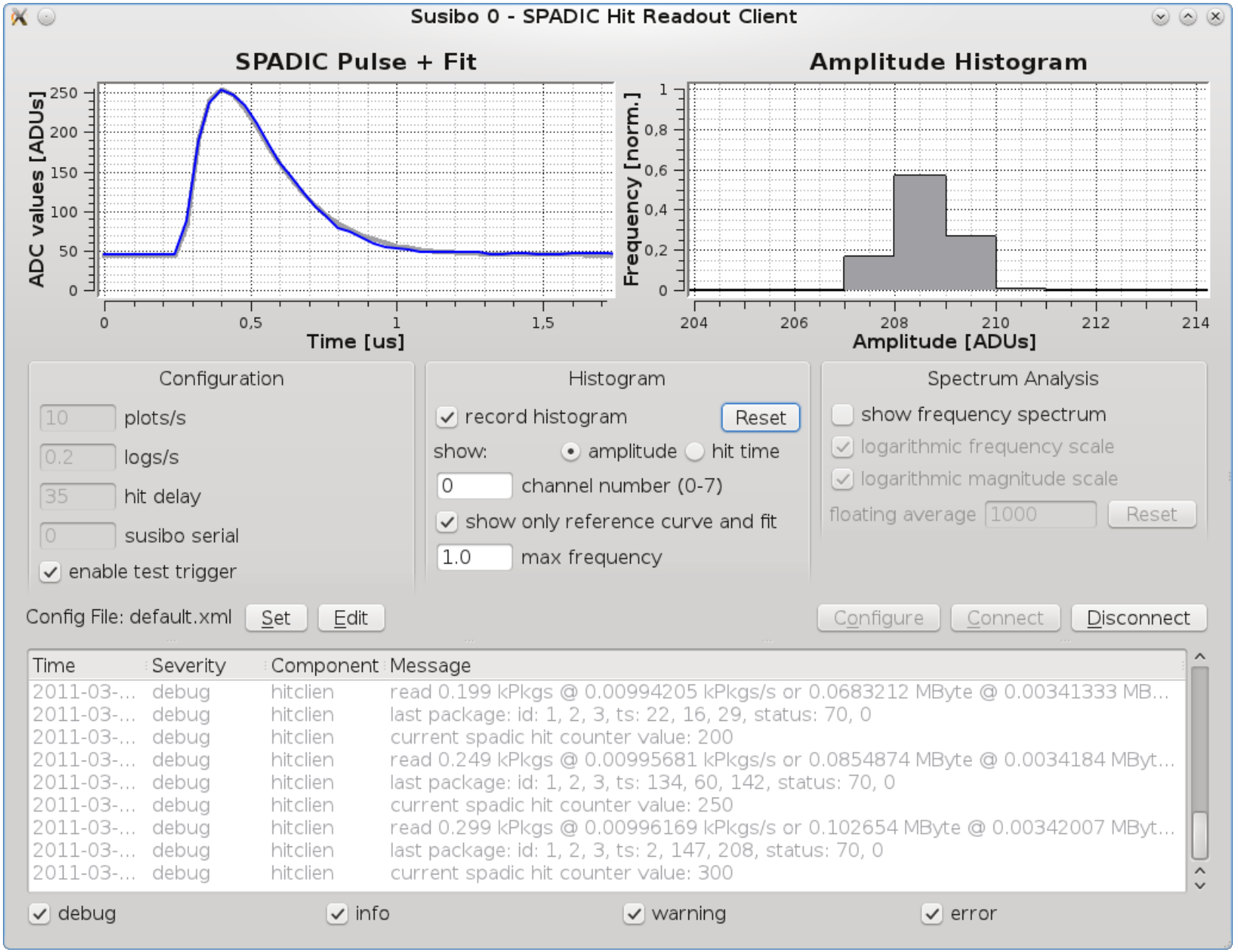


CERN Testbeam 2010



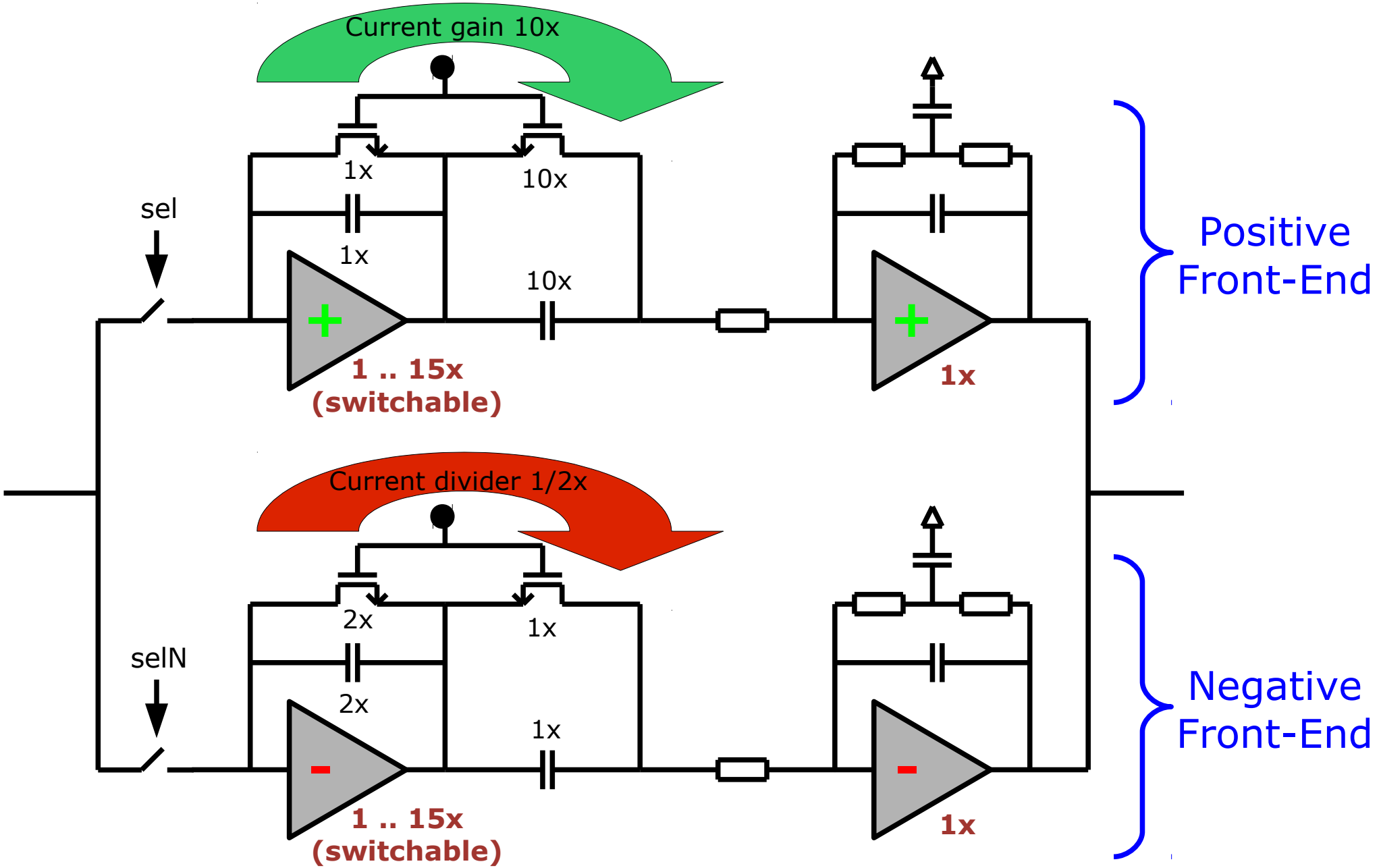
- 8 SPADIC readout setups were ready just in time
- 6 SPADIC setups were run in parallel

SPADIC Configuration, Control and Monitor Software

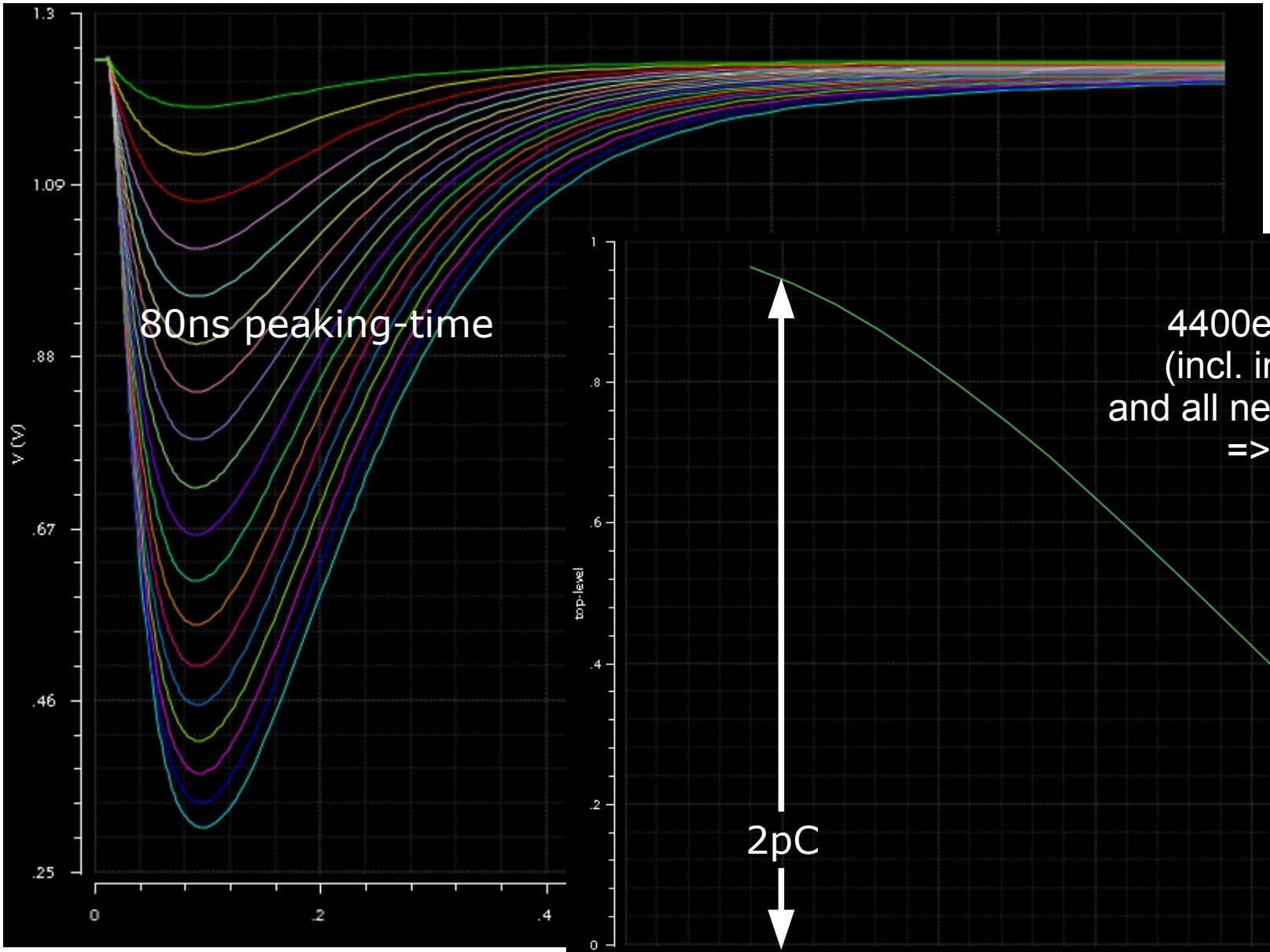


3. Status of Development

Positive Front-End Amplifier

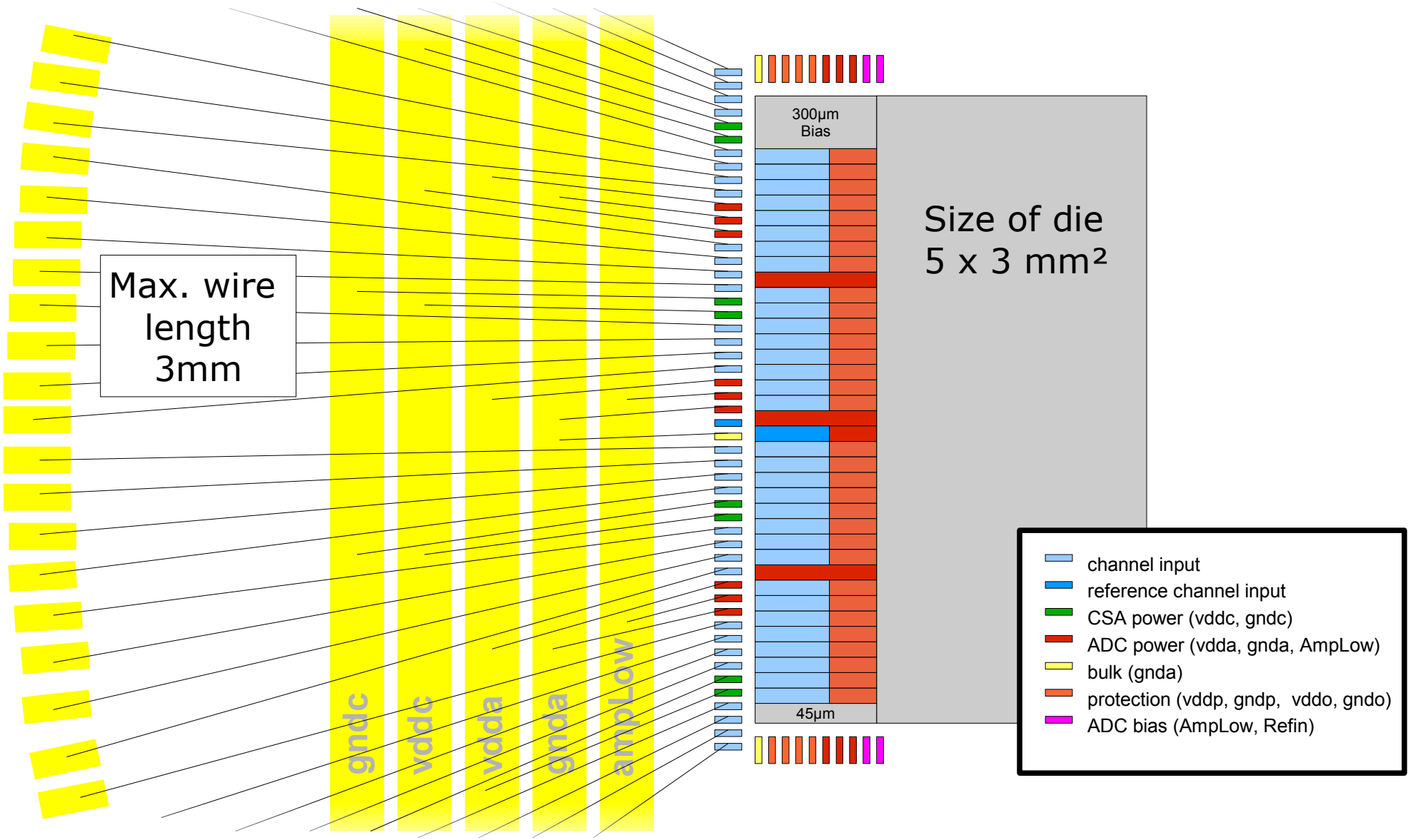


Negative Front-End (low gain)



SPADIC 1.0 FE Pad Plan

51 pads (95µm pitch), 120µm channel pitch
→ 32+1 channels, 9 x vdda/gnda/AmpLow (ADC), 8 x vddc/gndc (CSA), 1 x bulk (gnda)



Status of Digital Development

There is a lot of activity
on the digital parts, but:

Details probably here not relevant.

See FEE/DAQ talk
or
visit http://spadic.uni-hd.de

3. Summary

Summary

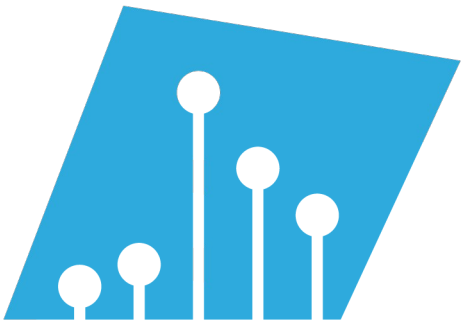
Status of SPADIC 1.0 Development

- Analog part
  - Conceptually finished
  - Dedicated RICH front-end (negative charges, 2 pF dynamic range)
  - Switchable gain in discussion (high-gain option for negative front-end)
- Digital part
  - A lot of data processing (most parts relevant for TRD only)
  - Sophisticated output protocol, 1Gbp/s max. data rate
  - Optional: Feature extraction

Next Steps

- Finish analog part (smaller adjustments, layout, …)
- Build peripheral parts (DACs, bias-diodes, IO-cells, LVDS-cells, …)
- Simulate, validate and synthesize digital parts

=> Still a lot of work that has to be done – focus goes now to digital parts



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