



CBMnet as FEE ASIC Backend

17th CBM Collaboration Meeting

P2 – FEE/DAQ/FLES

University of Heidelberg

Computer Architecture Group

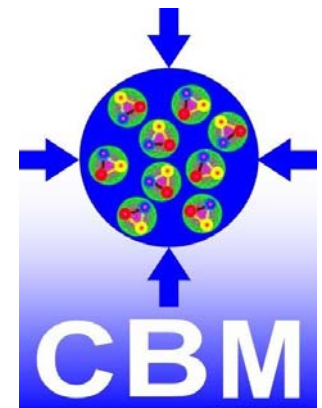
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Outline

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 - Structure
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- HUB-ASIC
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 - HUB ASIC Structure
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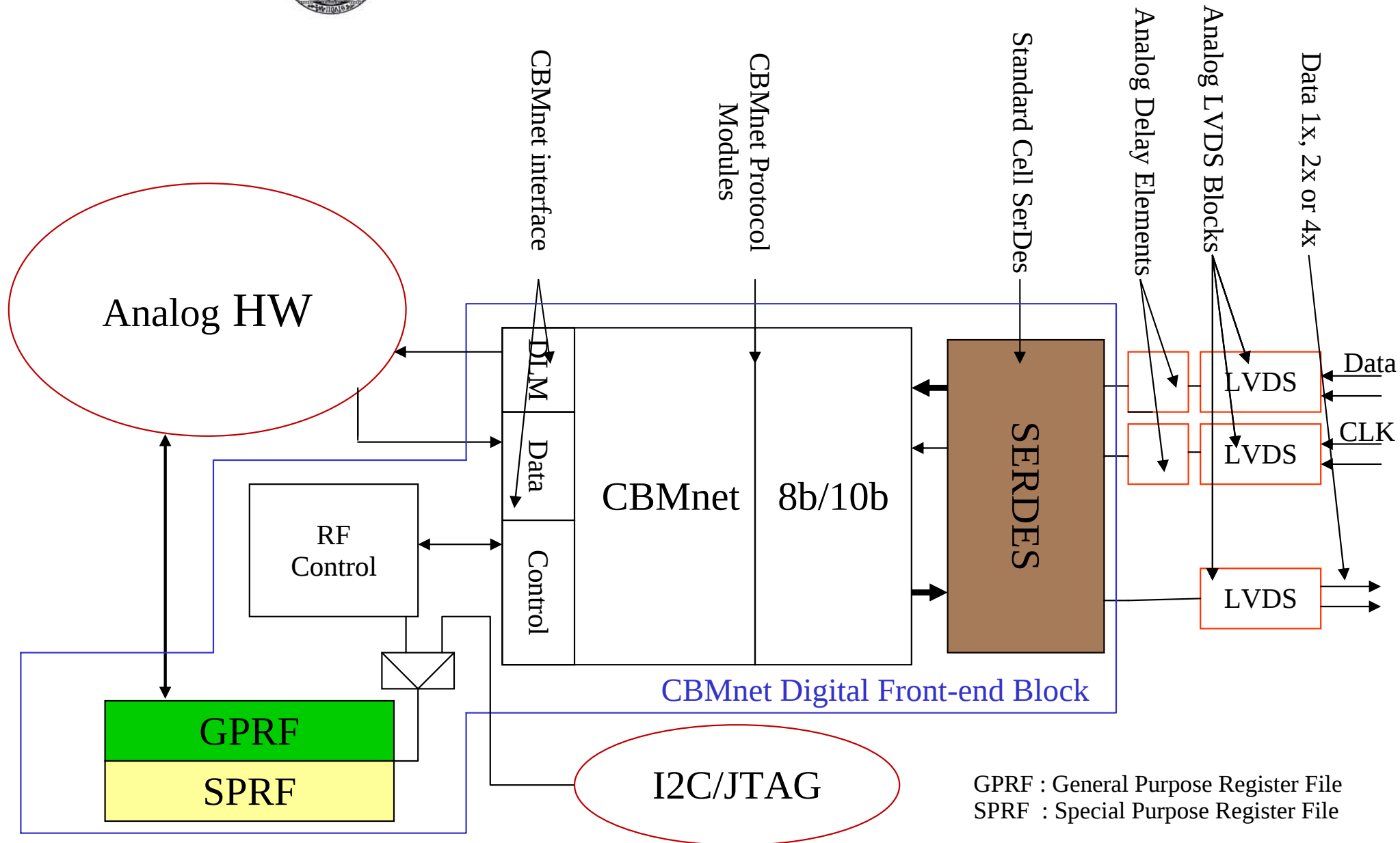


Motivation

- CBMnet delivers a CBM specific implementation
 - High Bandwidth for CBM requirements
 - Including a synchronization mechanism
 - Unified communication over one bidirectional link (possibly unbalanced)
- ⇒ Creation of a standardized CBMnet front-end ASIC building block
 - Integration into different types of front-ends possible
 - Generalized easy to use interface
 - One DAQ frontend read-out chain used in several parts of the experiment



Front-end ASIC CBMnet Structure





Features of CBMnet

CBMnet V1.0 Features	Planned additional CBMnet V2.0 extensions
• Communication over one optical link supporting DTM, DCM and DLM • Optimized data utilization about 91 % (about 73 % considering 8b/10b) • Optimized easy to use Interface • Highly modular CBM LP code structure • Special adapted routing scheme • Fast and efficient administration packets • Retransmission for Control Packets • System wide clock recovery with low jitter • Deterministic link latency feature for well defined Deterministic Latency Messages	• Lane handling for unbalanced communication • Support for large messages within hardware • Planned data loss strategy in cases of overloads at the end of epochs • Communication also reliable for data stream • Meta data detection adaption to find Meta data within message streams in early system stages

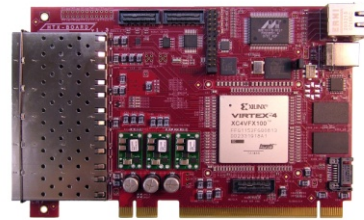


Existing operational Modules

- CBMnet V1.0 stable working within several FPGA solutions
- Changes for V2.0 can thereby be tested efficiently
- All modules are ASIC ready implemented
- Only XML description for RF required



Readout Controller



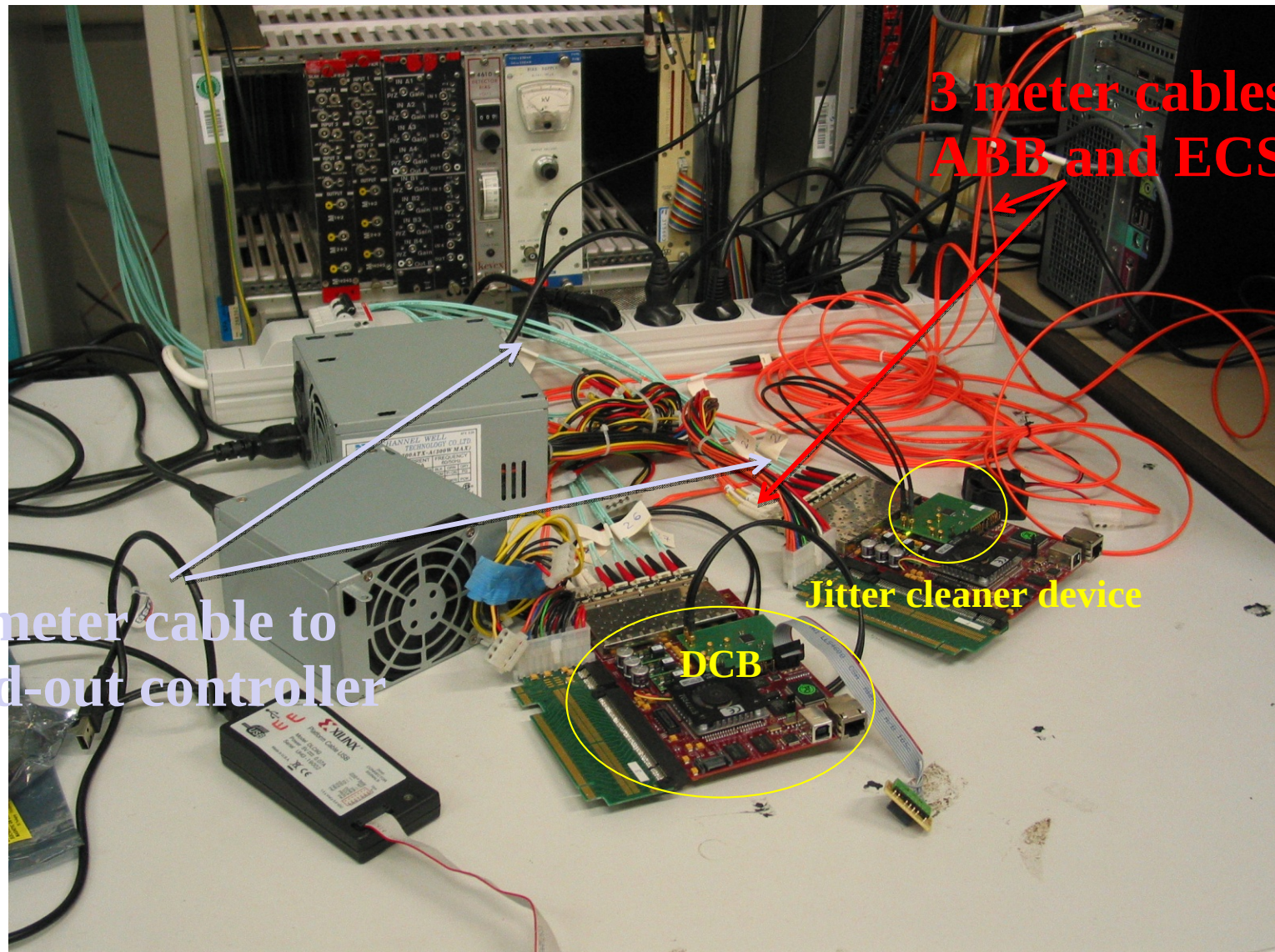
Data Combiner Board



Active Buffer Board



Cosy Beamtime December 2010



3 meter cables to
ABB and ECS

50 meter cable to
read-out controller

Jitter cleaner device

DCB



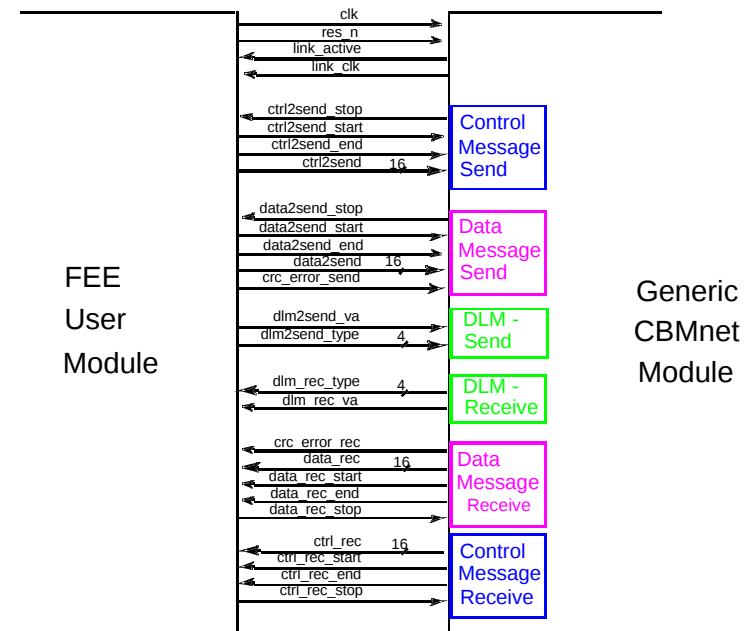
Functions under Development

Digital design parts under construction

- Register File Control Module
- CBM V2.0 protocol changes
- SERDES Modules

Analog parts required for CBMnet read-out

- Delay Cells
- LVDS Cells



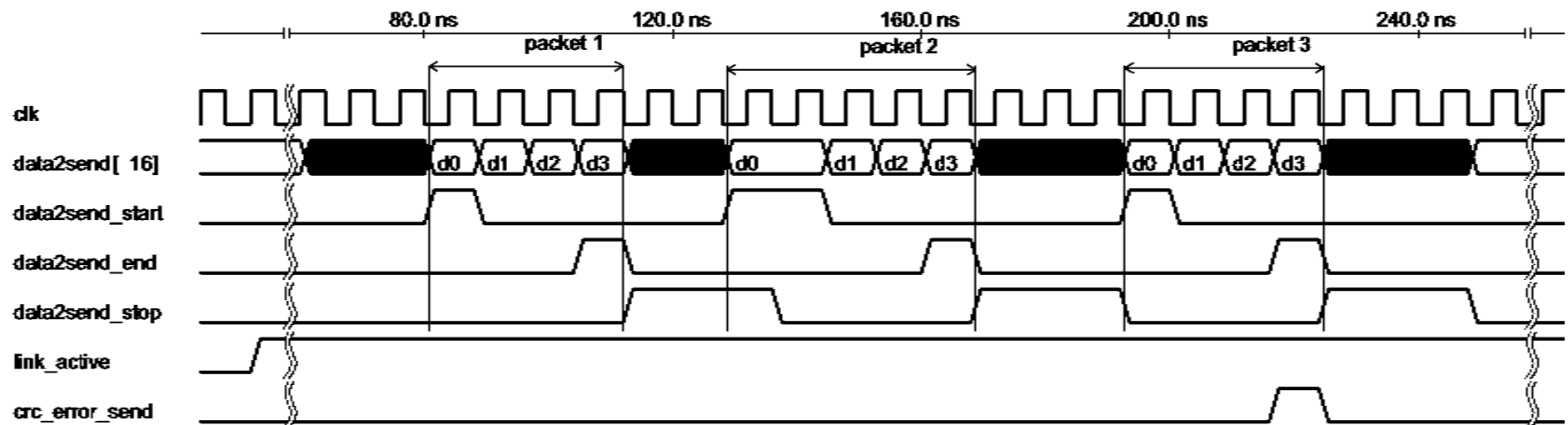
⇒ Generic CBMnet control block for FEE ASICs

⇒ First implementation for SPADIC together with Tim Armbruster



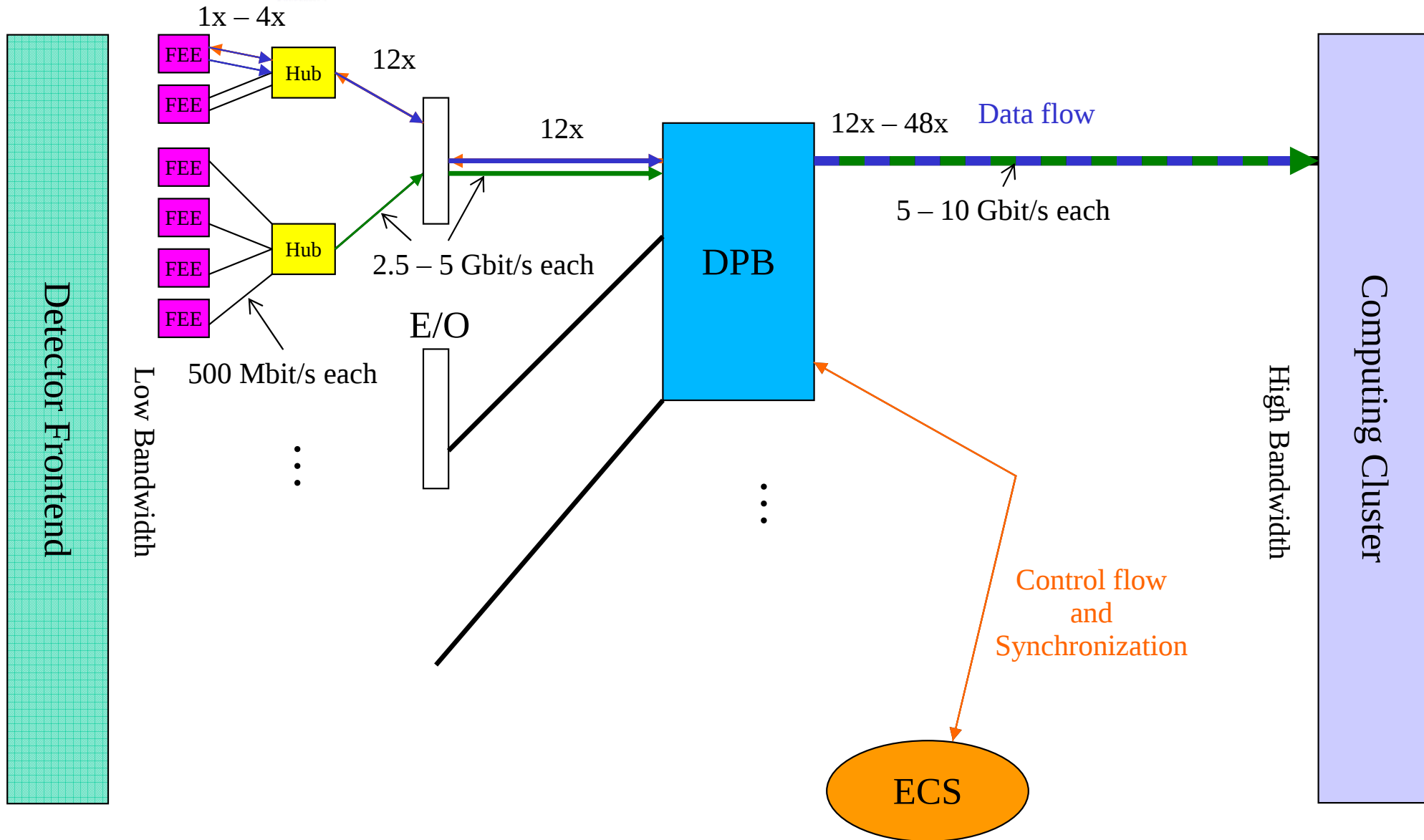
Interface - Data Send Example

- Interface optimized for easy and efficient data transmission
- Variant of valid-stop synchronization
- All protocol specific features like initialization, retransmission are not visible for users



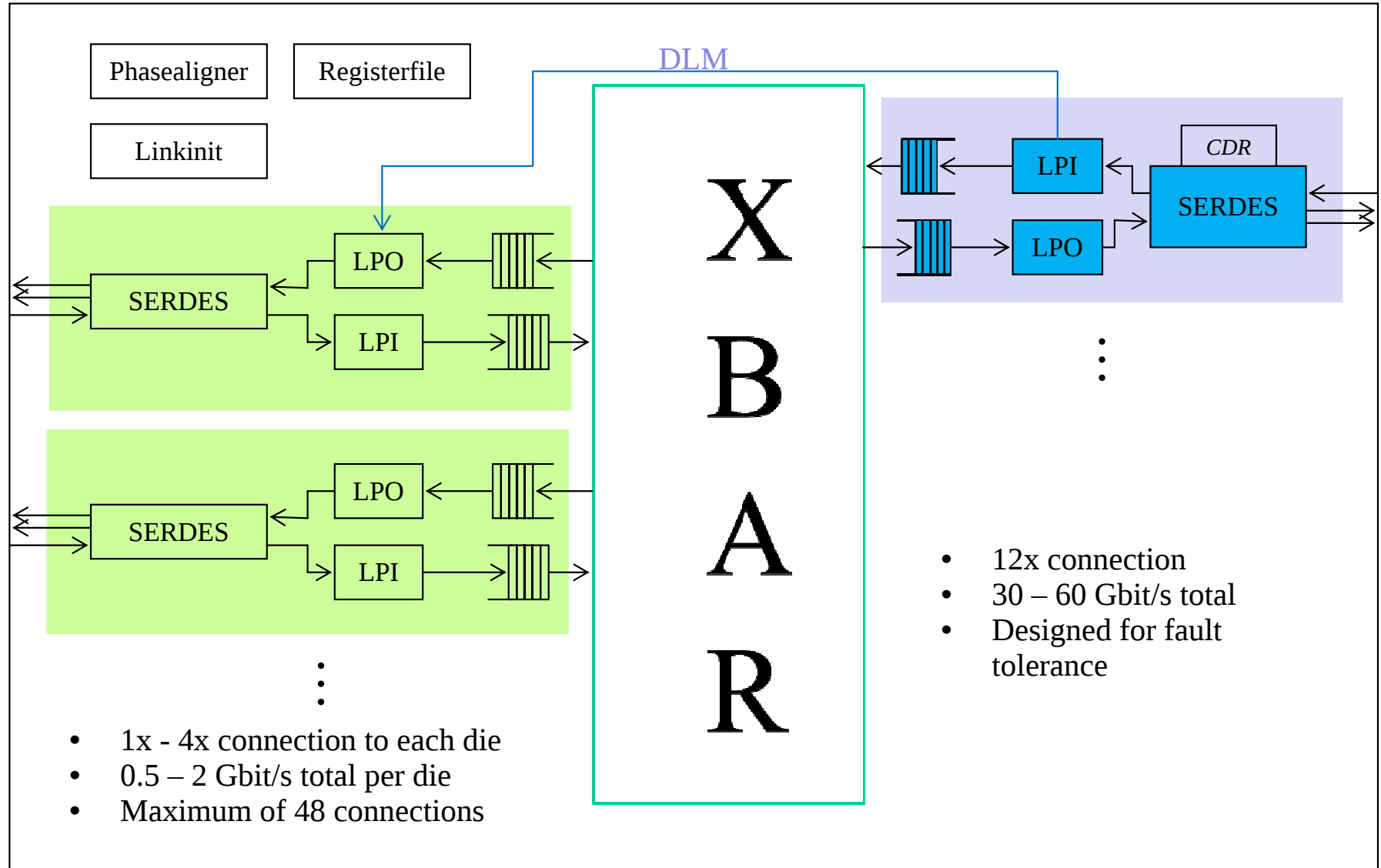


CBMnet Structure





HUB ASIC Structure





Workpackages

Design tasks

- Analysis and adaption of CBM link port
- CBM protocol V2.0 has to be made ASIC ready
- Dynamic configuration for 1x, 2x, 4x
- Serializer and CDR at 2.5 Gb/s 5Gbit/s (CBM group in India)
- Clock distribution uses clock line at 500MHz
- Serializer at 500Mb/s interface, 8B/10B coded, phase alignment
- Low level initialization and hub configuration
- Special crossbar implementation
- Complete deterministic design
- Fault correction, redundancy for lanes etc.



Workpackages

Backend tasks

- Process technology decision
- Collection of IPs and libs
- Integration and backend design
- Radiation tolerant design

Test & Verification tasks

- Verification
- FPGA prototyping (in cooperation with KIP/Frankfurt)
- ASIC prototyping (ZITI and CBM group India)

Other tasks

- Project planning
- Coordination



Conclusion & Outlook

- CBMnet prototyping was successful
- ⇒ CBMnet logic will be included into SPADIC front-end ASIC
- ⇒ Generation of reusable front-end ASIC read-out building block

- HUB CBM planning has to be continued
- Boundary conditions has to be solved



Thank you for
your attention !

Questions ?