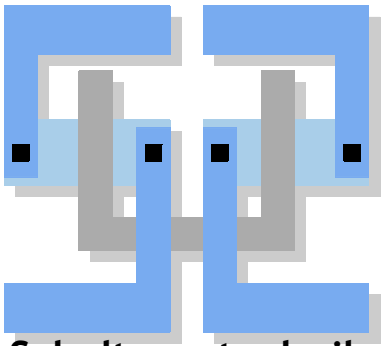
UNIVERSITÄT HEIDELBERG

SPADIC
Self triggered Pulse Amplification and Digitization asIC

Design Tips for Low Noise Readout PCBs

Or: How black magic can lead to success



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SuS Monday Meeting

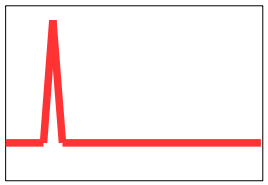
April 2011

Visit http://www.spadic.uni-hd.de

1. Reminder: SPADIC Readout ASIC

The processing chain of SPADIC 0.3 – Step 1

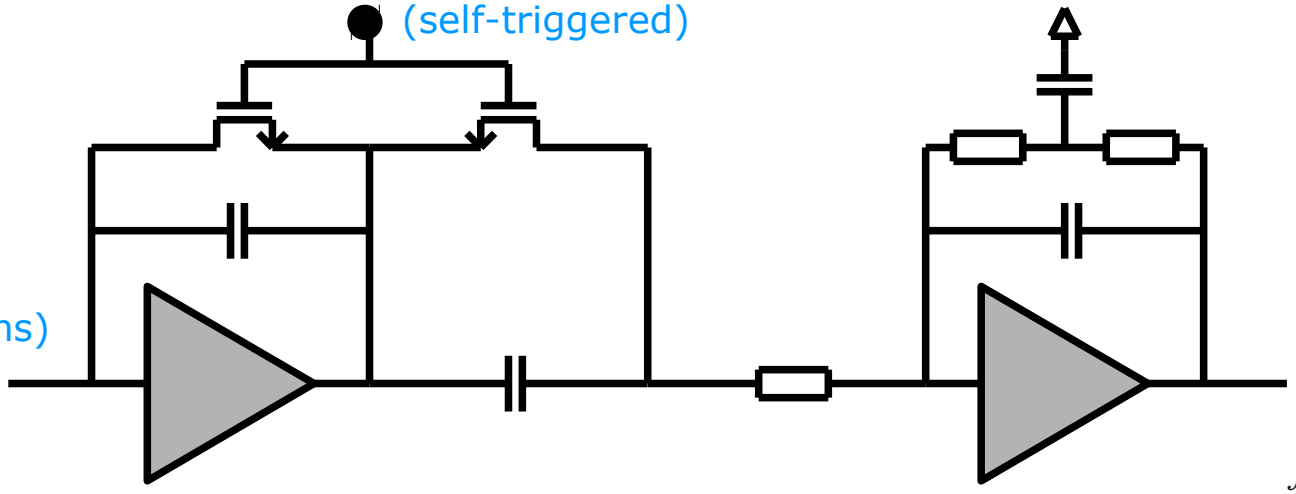
Step 1: Amplification + Shaping



Fast charge pulse from detector (< 10ns)

(RICH: negative, up to 2pF)

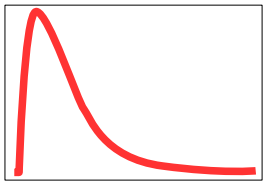
Continuous rest (self-triggered)



Charge Amplifier

2nd Order Shaper

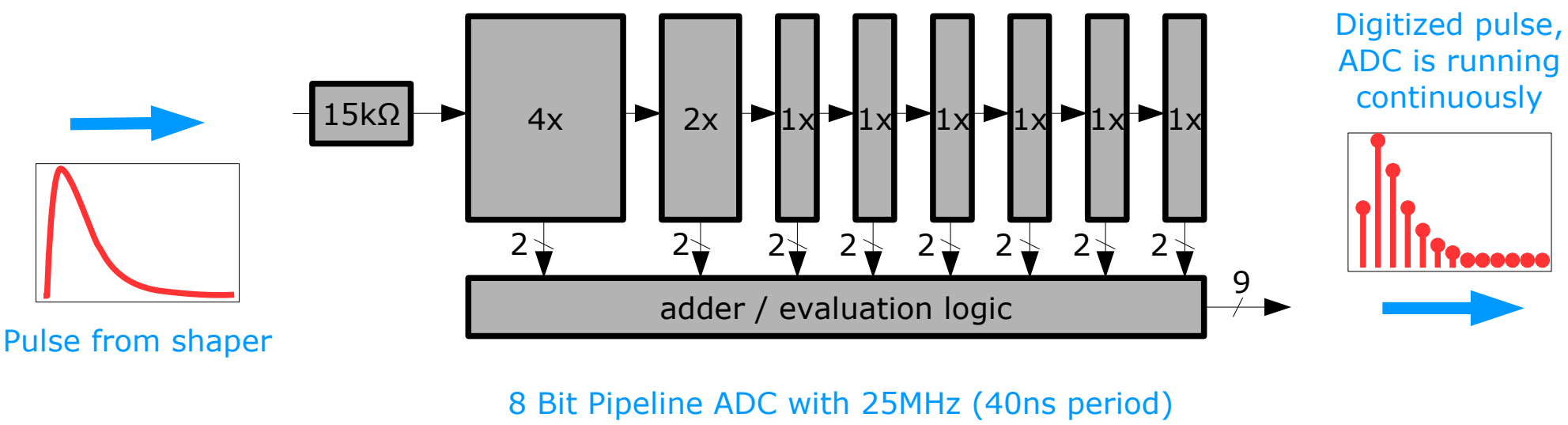
Voltage pulse, shape depends only on shaping-time:



$$f(t) = \left(\frac{t}{T}\right)^2 \exp\left(\frac{t}{T}\right)$$

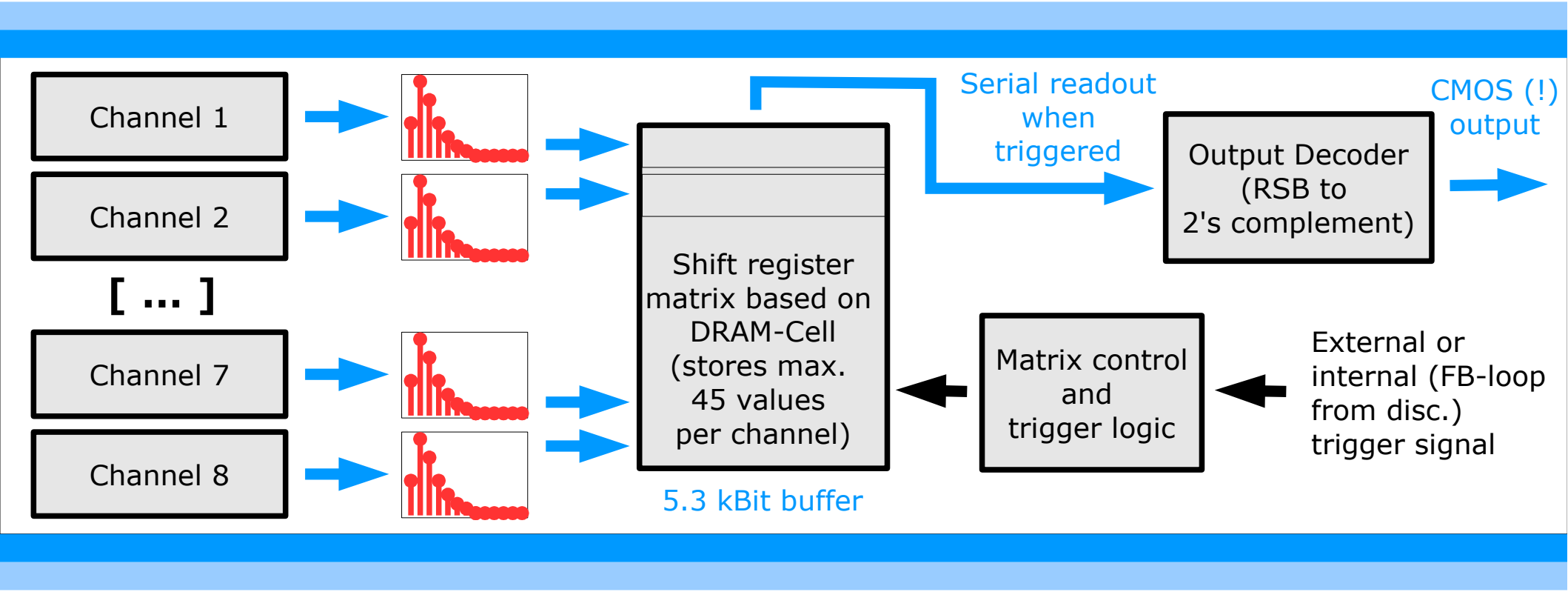
The processing chain of SPADIC 0.3 – Step 2

Step 2: Digitization

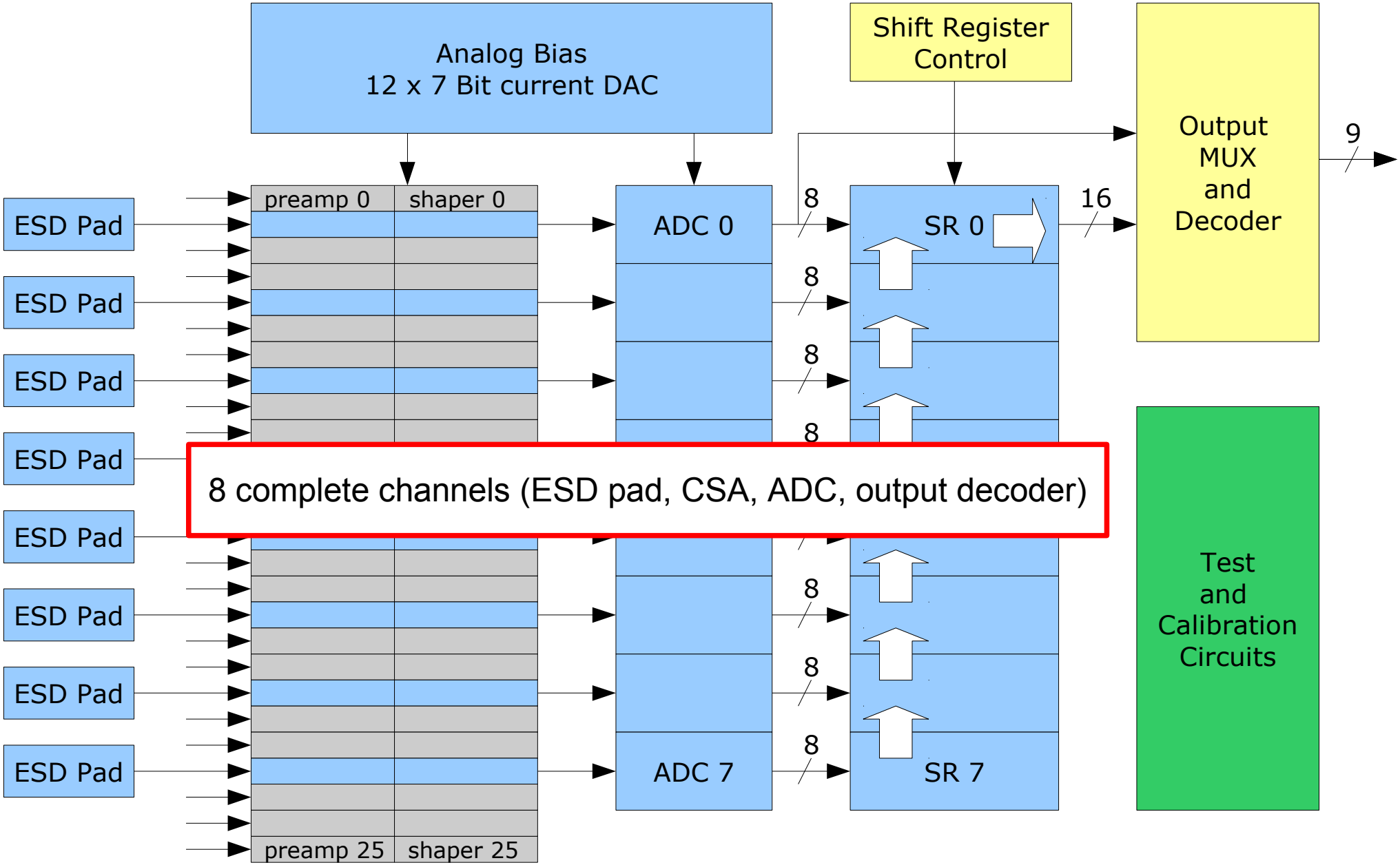


The processing chain of SPADIC 0.3 – Step 3

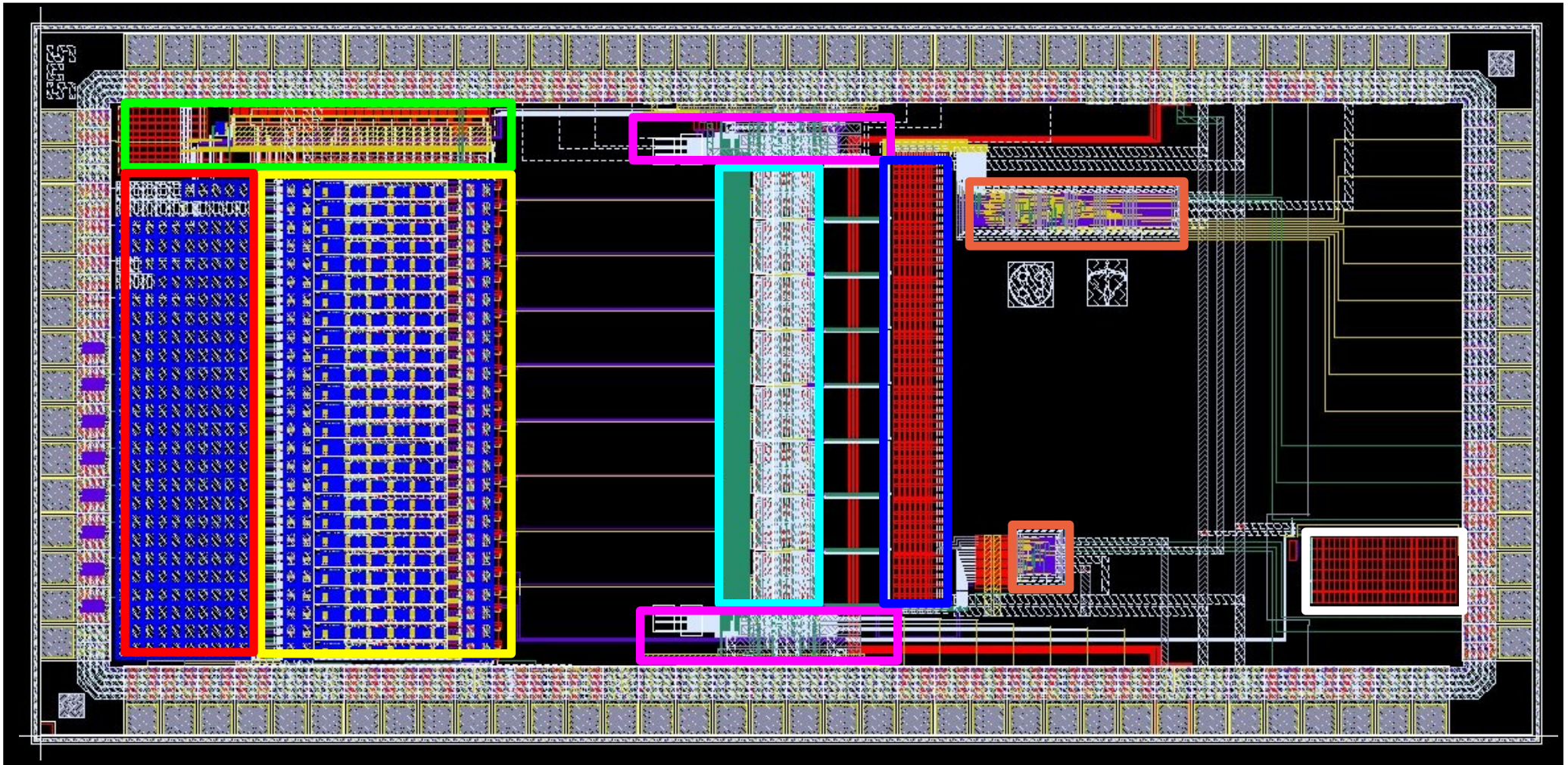
Step 3: Buffering Matrix, Trigger Control and Output Decoder



Block Diagram of Latest SPADIC v0.3



Latest SPADIC: Layout

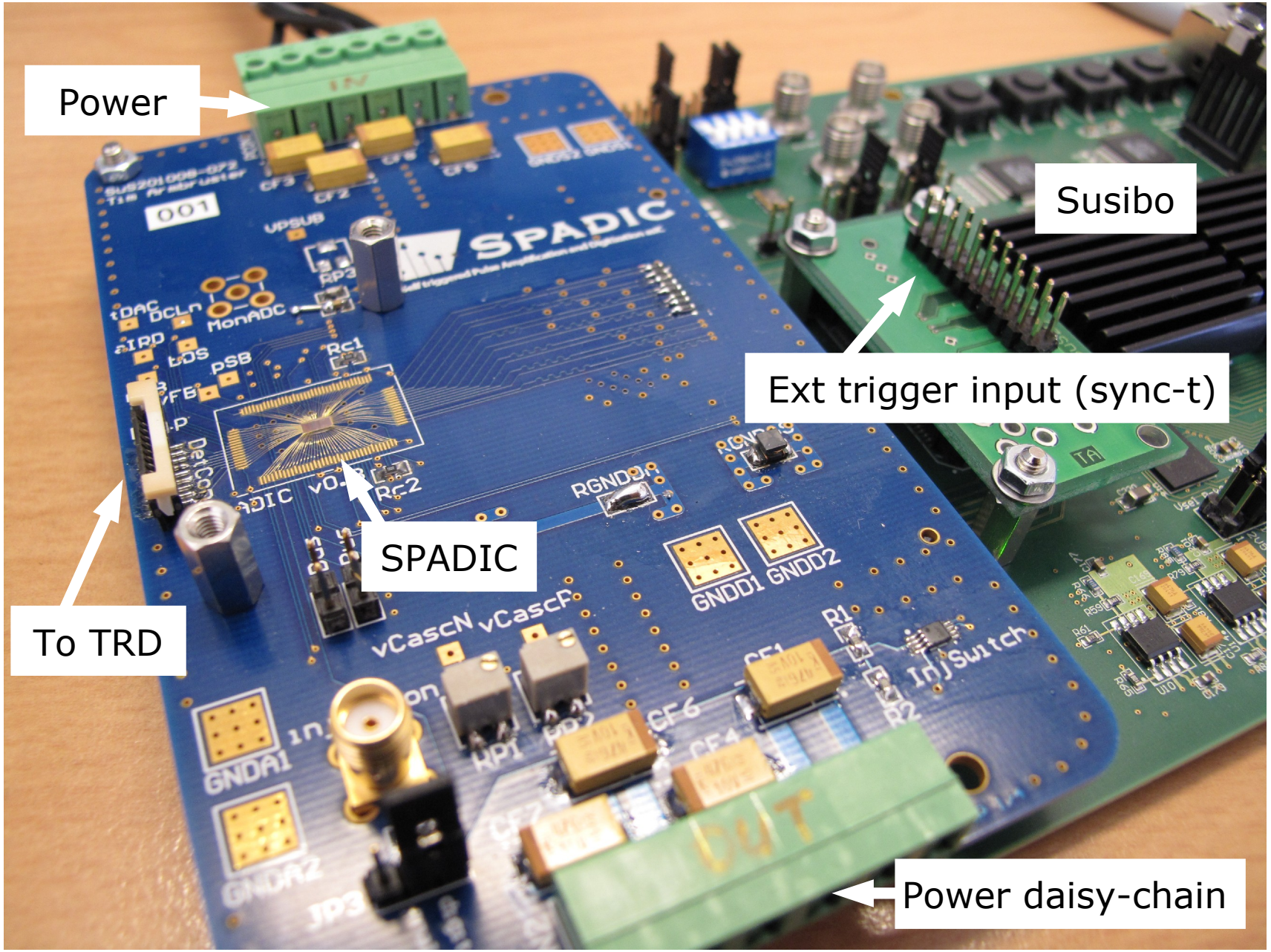


Bias circuitry (12 current DACs)
26 preamp/shaper channels
Detector capacitors (5pF per block)
8 pipelined ADCs

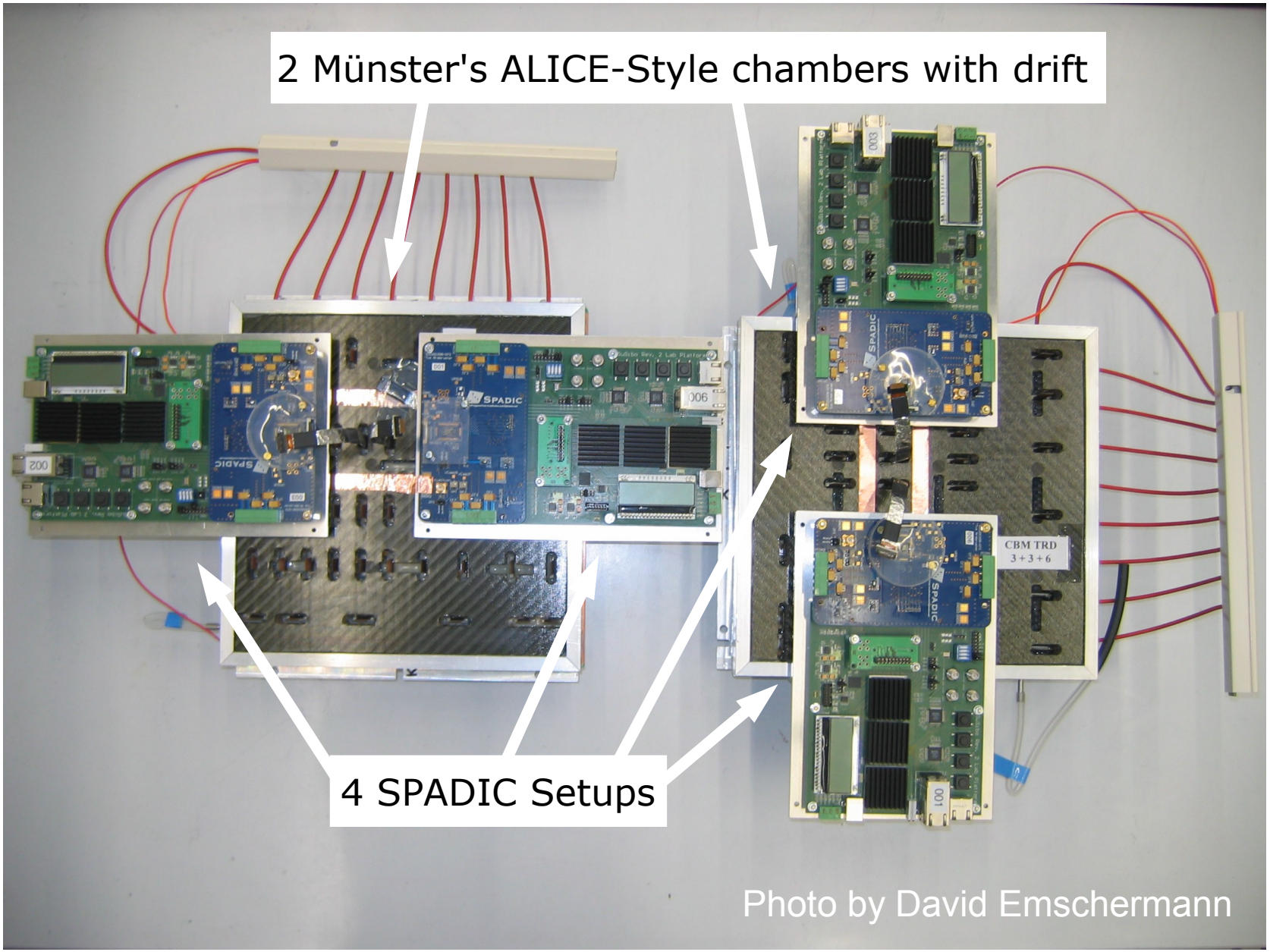
ADC control + bias
5.2 kBit shift register matrix
Control + readout/decoder logic blocks
Test circuits

2. Starting Point: Noisy Setup

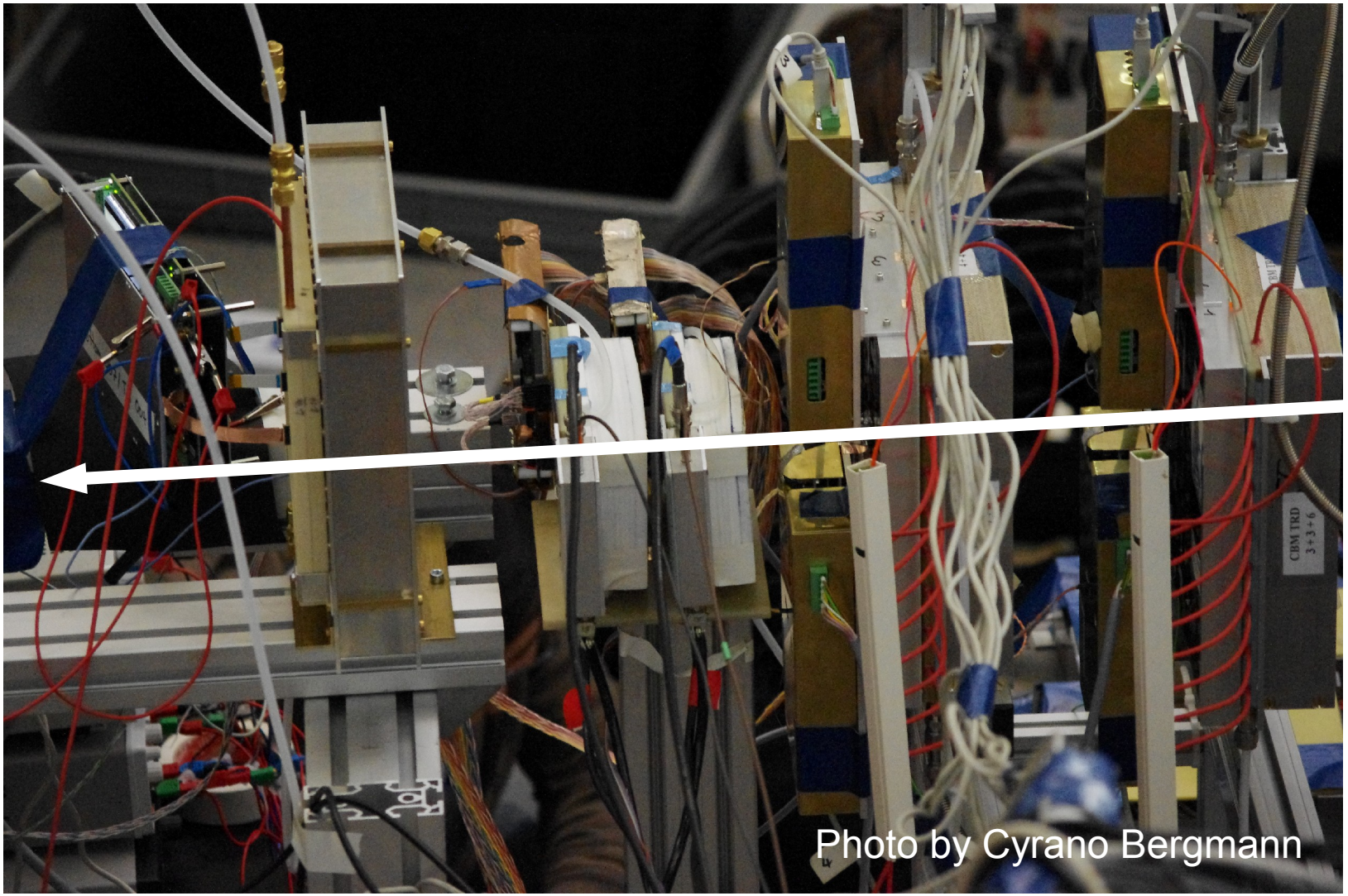
Test-Setup: SPADIC plugged on Susibo



CERN Testbeam 2010: Münster's TRD-SPADIC Setup



CERN Testbeam 2010



- 8 SPADIC readout setups were ready just in time
- 6 SPADIC setups were run in parallel

Video: Setup Connected to Pad-Plane, Internal Test-Trigger

http://www.youtube.com/watch?v=qsUtSE-T2YI

Problem 1: Pick-up Noise

Problem

- Setup very sensitive to pick-up noise due to external disturbing sources. Stable as long as no detector is connected.

Possible Reason(s)

- Very long connection chain (8mm bonding-wire, 1cm wire on PCB, unshielded 9-pin connector, 10cm flex flat cable, unshielded 9-pin connector, 2cm wire on PCB)
- No consistent grounding scheme (both for PCB and chip)

Possible Solutions / Next Steps

- After a lot of trial and error, one can usually find a more or less stable setup
- Shielding: Seems to help!?
- Minimize length of connection chain (e.g. better PCB footprint)
- Develop more consistent grounding scheme (very important)
- Gather experience with the next SPADIC 0.3 PCB iteration

Problem 2: Baseline-Shift

Problem

- Baseline-shift (offset of pulses jumps) when some external load is connected. Shifts in both(!) directions (up/down) have been observed. Probably no impact on noise (but on dynamic range).

Possible Reason(s)

- Theoretically and from simulation: Some leakage current (several 10nA) can cause such a behavior. But for instance the TRD pads are well isolated. True reason hard to find – no good idea so far.

Possible Solutions / Next Steps

- Better grounding scheme (PCB and chip) might help here as well
- Isolation of analog input cells (leakage via protection circuitry?)
- Good ideas are very welcome!
- Check whether this problem still exists on the next SPADIC 0.3 PCB iteration (see later)

Problem 3: Too Strong Output Driver

Problem

- CMOS Output driver too strong. They cause power glitches which leads to different internal problems (e.g. loss of configuration).

Possible Reason(s)

- CMOS :-)

Possible Solutions / Next Steps

- Only LVDS on SPADIC 1.0
- Buffer on next SPADIC 0.3 readout board
- Latest SPADIC 0.3 readout board uses resistors to limit current (patch)

Problem 4: Broken Setups

Problem

- After some time, several SPADIC 0.3 Rev.2 boards stopped working. Symptoms: Much too much current flow, analog part still works (but noisy), digital part still works, but ADC seems to be death. Some users reported to have heard (!) discharges. No visible damage.

Possible Reason(s)

- Cross-current between power domains
- Electrostatic discharge
- ESD circuitry not sufficient
- Faulty operation

Possible Solutions / Next Steps

- Test: Better powering scheme on next SPADIC 0.3 readout board
- Use voltage regulators (less cables, less operational problems, more stable power signals)
- Try to use only power supplies with accurate current protection!

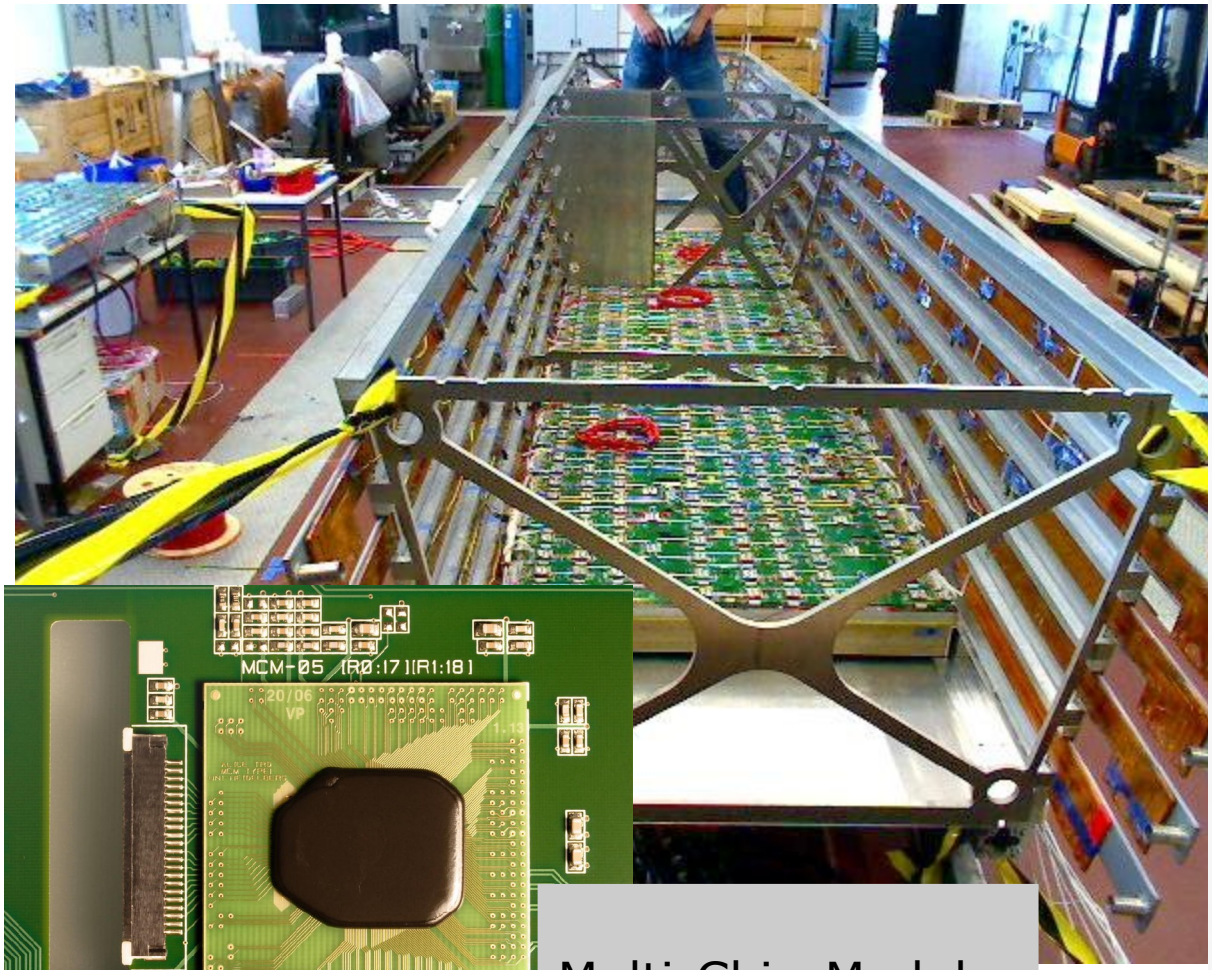
3. The Ideas and Improvements

Meeting at GSI

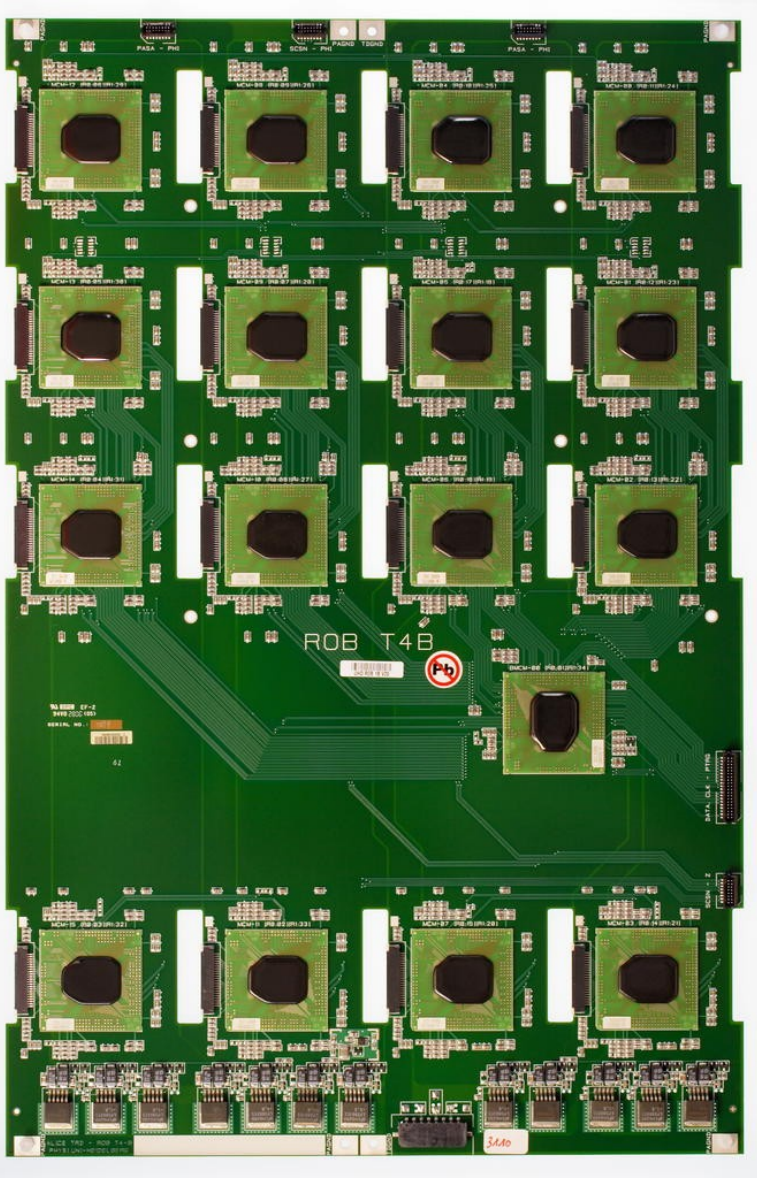
Dr. Ivan Rusanov from GSI → had a lot of good tips

Source: http://www.gsi.de

Ivan's PCB (ALICE TRD)



Multi-Chip-Module:
TRAP + PASA

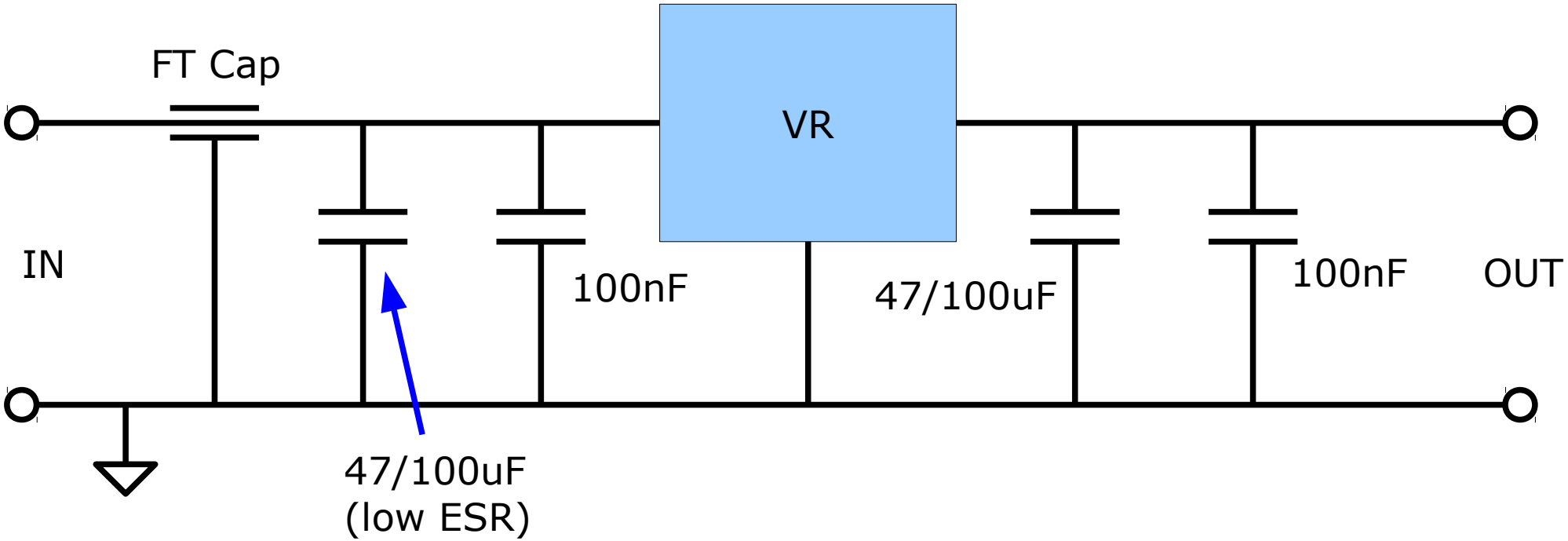


Source: http://physi.uni-heidelberg.de

SPADIC PCB Improvement #1: Voltage Regulators

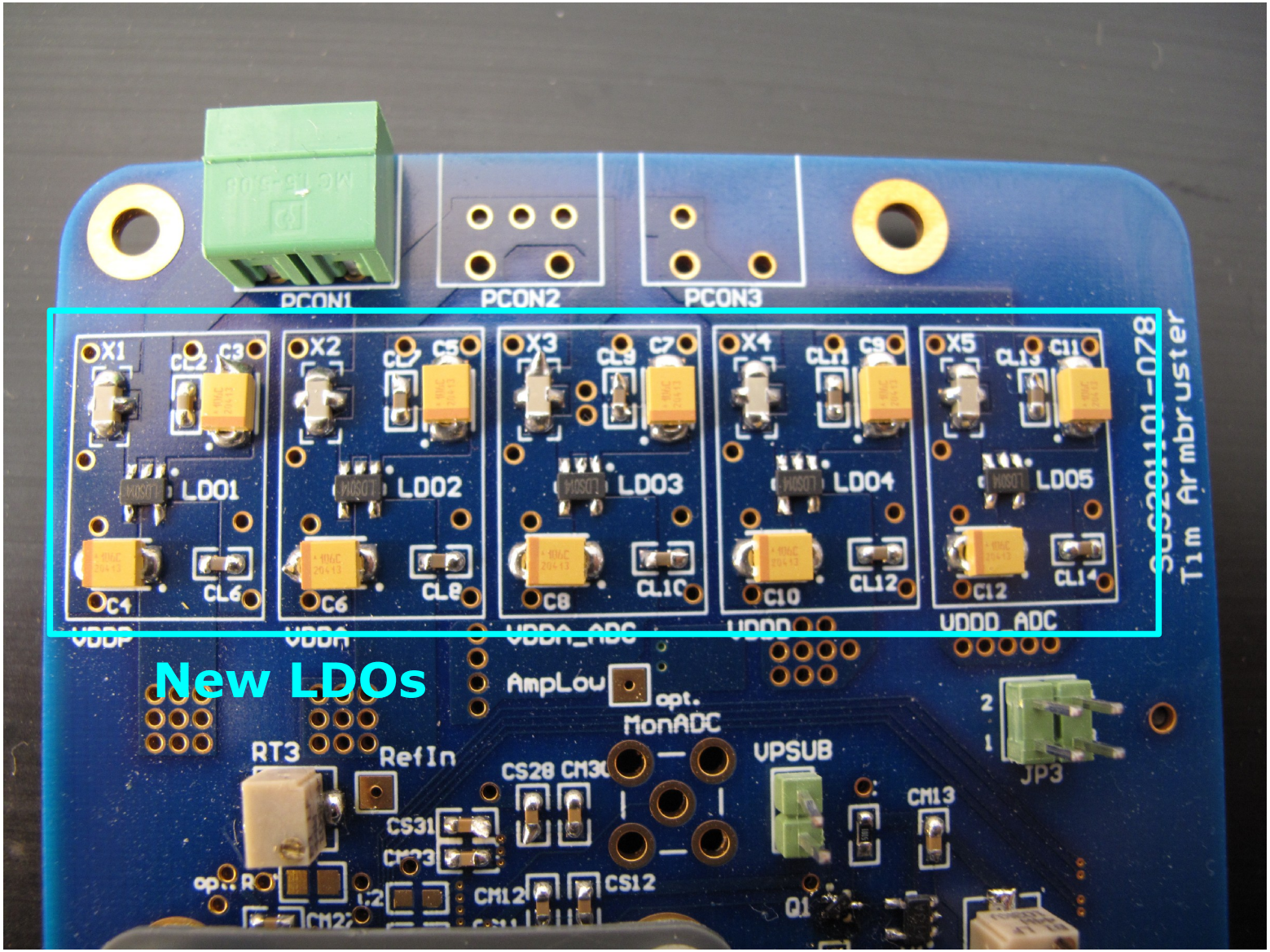
Tip from Ivan Rusanov (GSI)

4 Power Domains: Preamp 1.8V, ADC analog 1.8V, ADC digital 1.8V, Digital 1.8V
3 Ground Domains: Pramp, ADC+Digital, Susibo
3 Bias-Voltages with current flow: AmpLow, RefIn, VPSUB

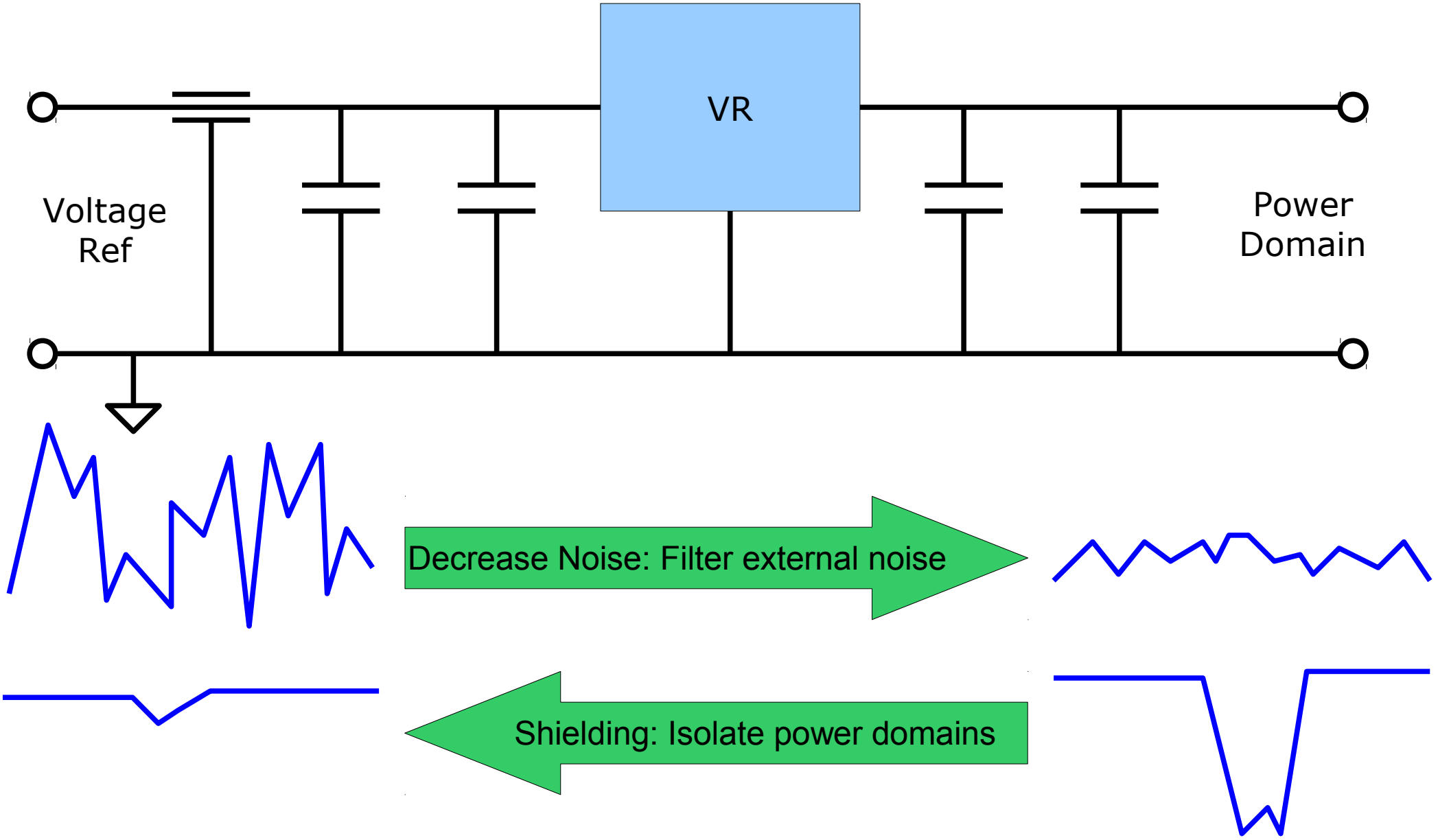


Use a voltage regulator for each power domain!
→ decrease voltage drop in power-daisy-chain

SPADIC PCB Improvement #1: Realization

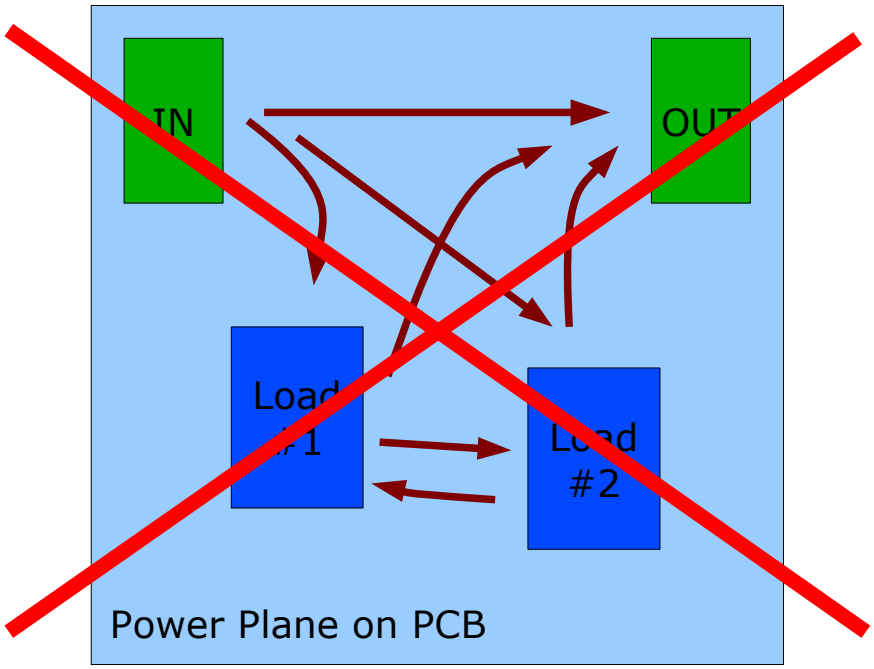


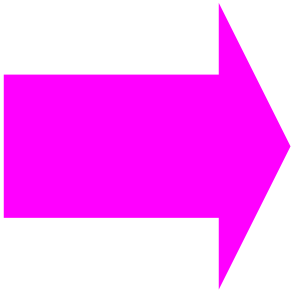
SPADIC PCB Improvement #1: Theory

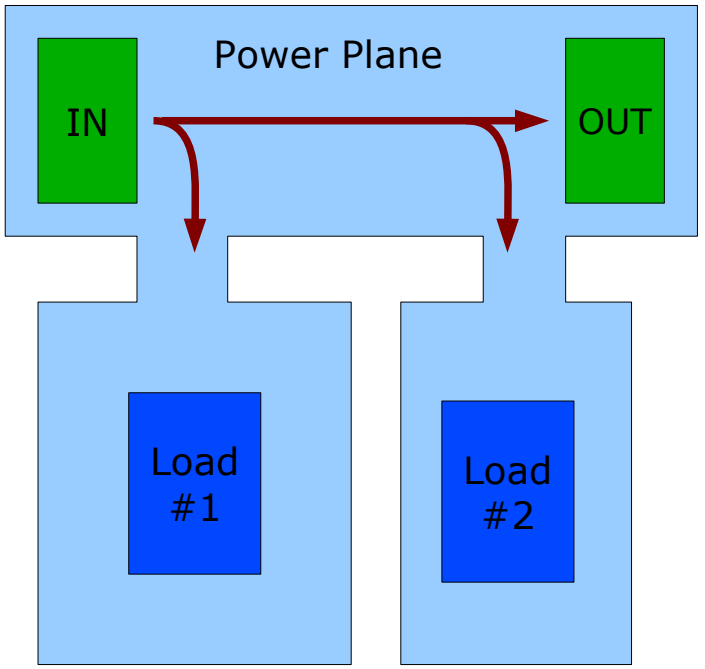


SPADIC PCB Improvement #2: Regulate Current Flows

Tip from Ivan Rusanov (GSI)



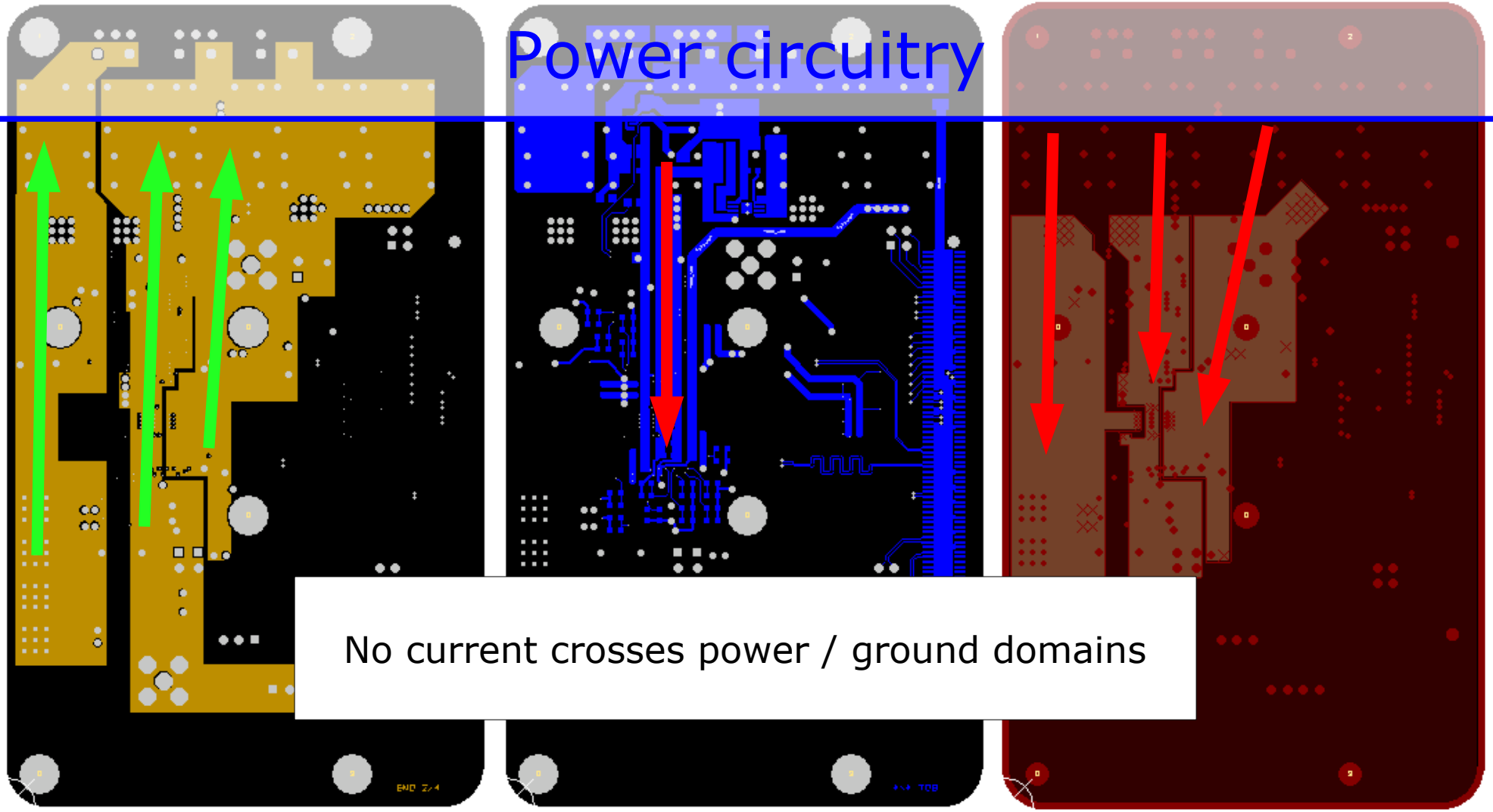




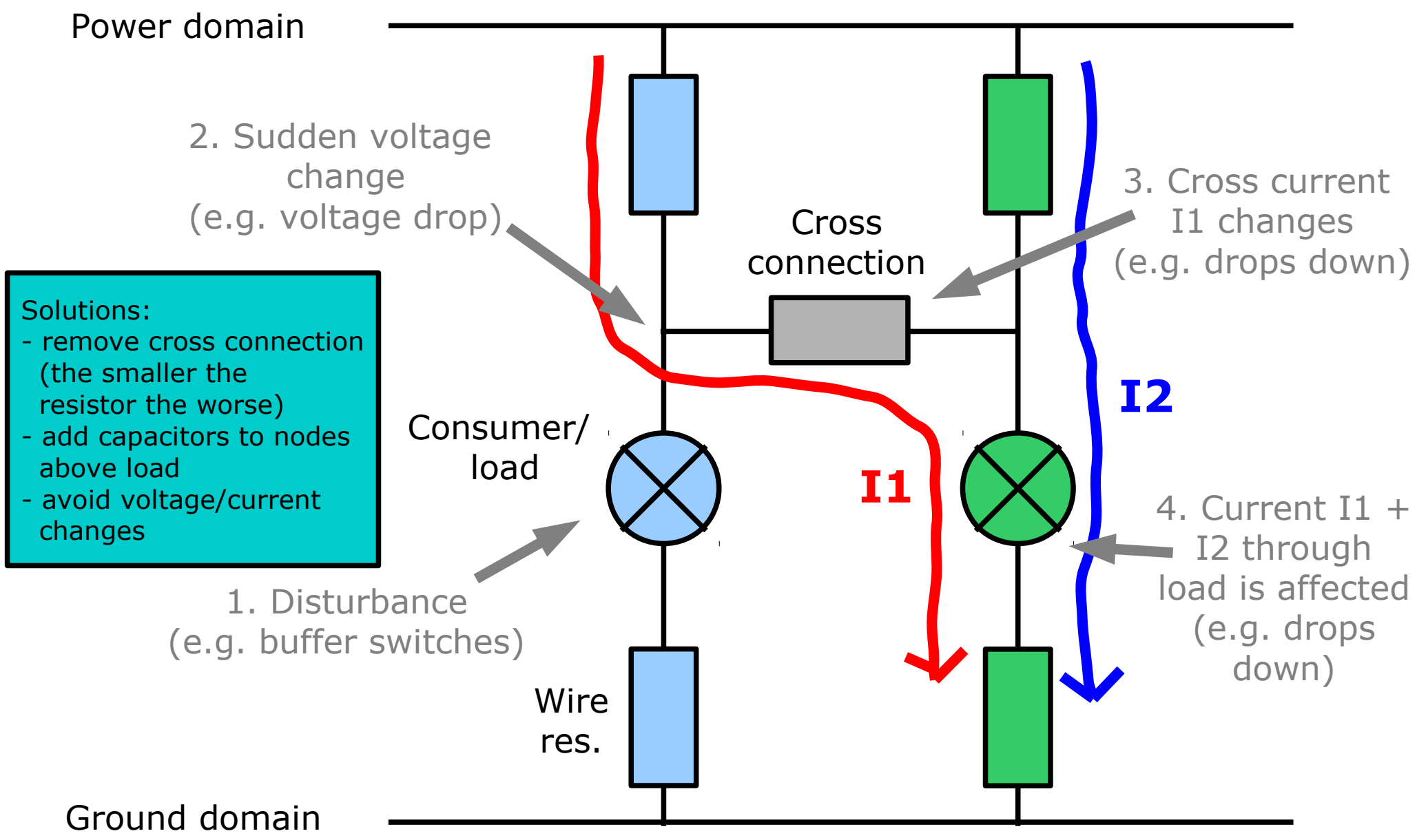
(Same scheme for current sink on a different layer)

Clearly regulate current flows
→ Remove possible sources for power/ground loops!

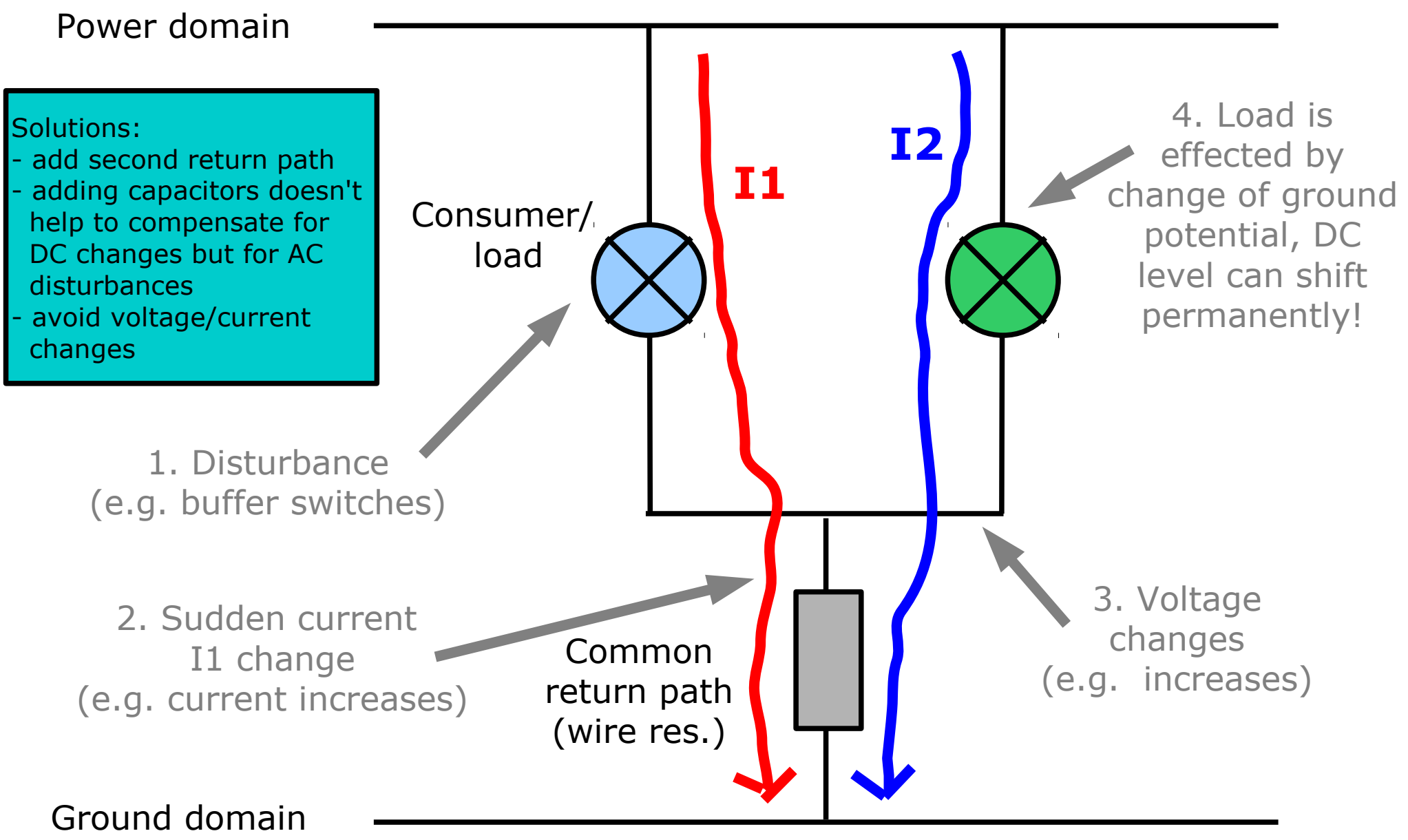
SPADIC PCB Improvement #2: Realization



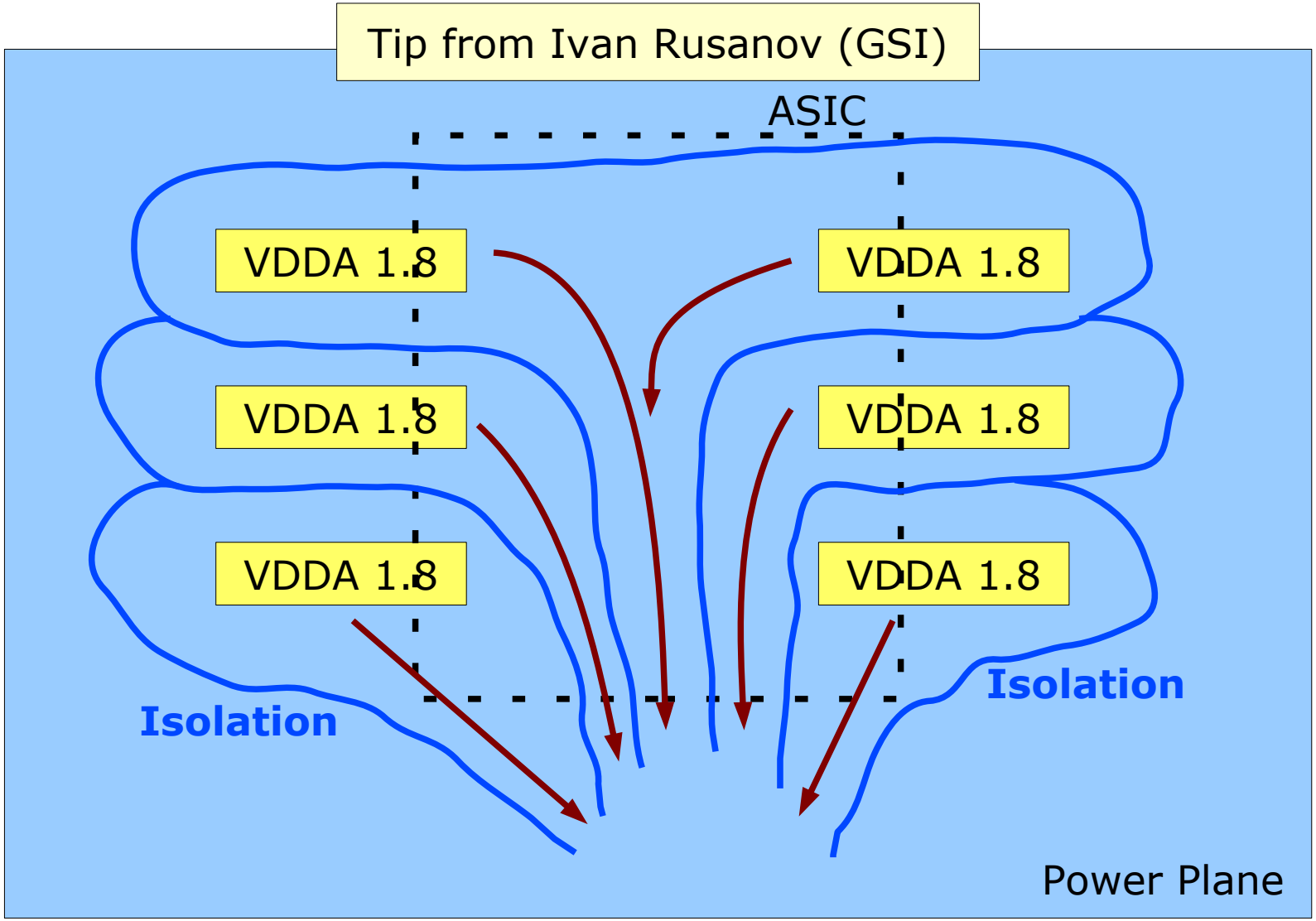
SPADIC PCB Improvement #2: Theory Example 1



SPADIC PCB Improvement #2: Theory Example 2

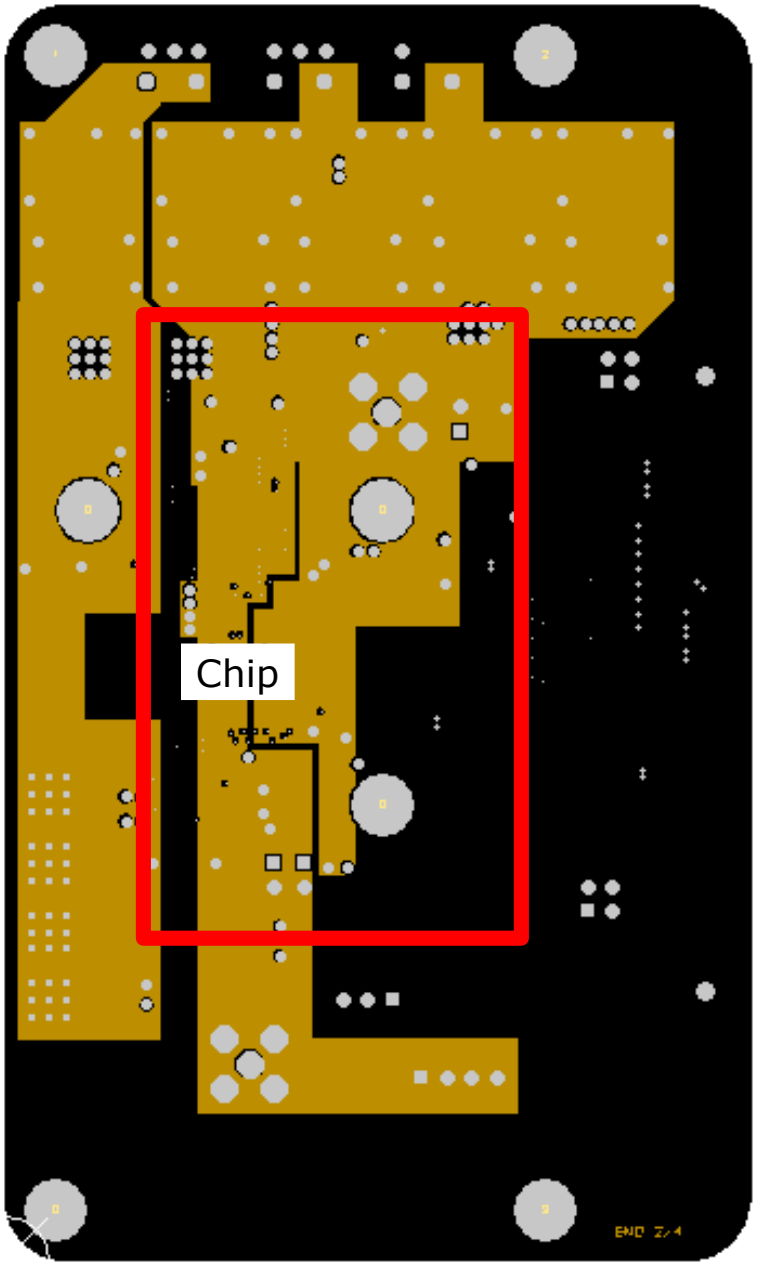


SPADIC PCB Improvement #3: Current Flows Next to Chip



Semi-isolate power pins of same domain to remove direct currents
→ Remove possible sources for power/ground loops!

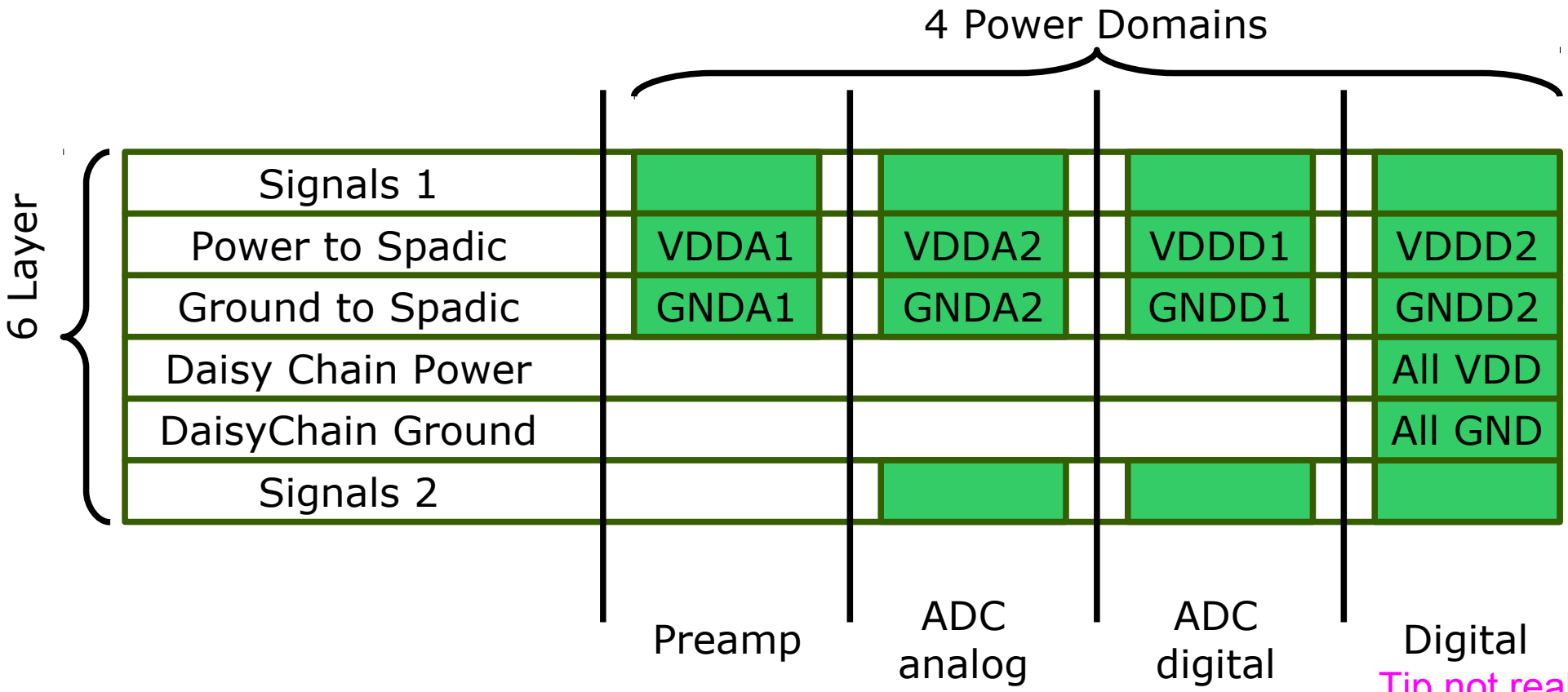
SPADIC PCB Improvement #3: Realization



Some theory as #2!

SPADIC PCB Improvement #4: New Layer Stack

Tip from Ivan Rusanov (GSI)

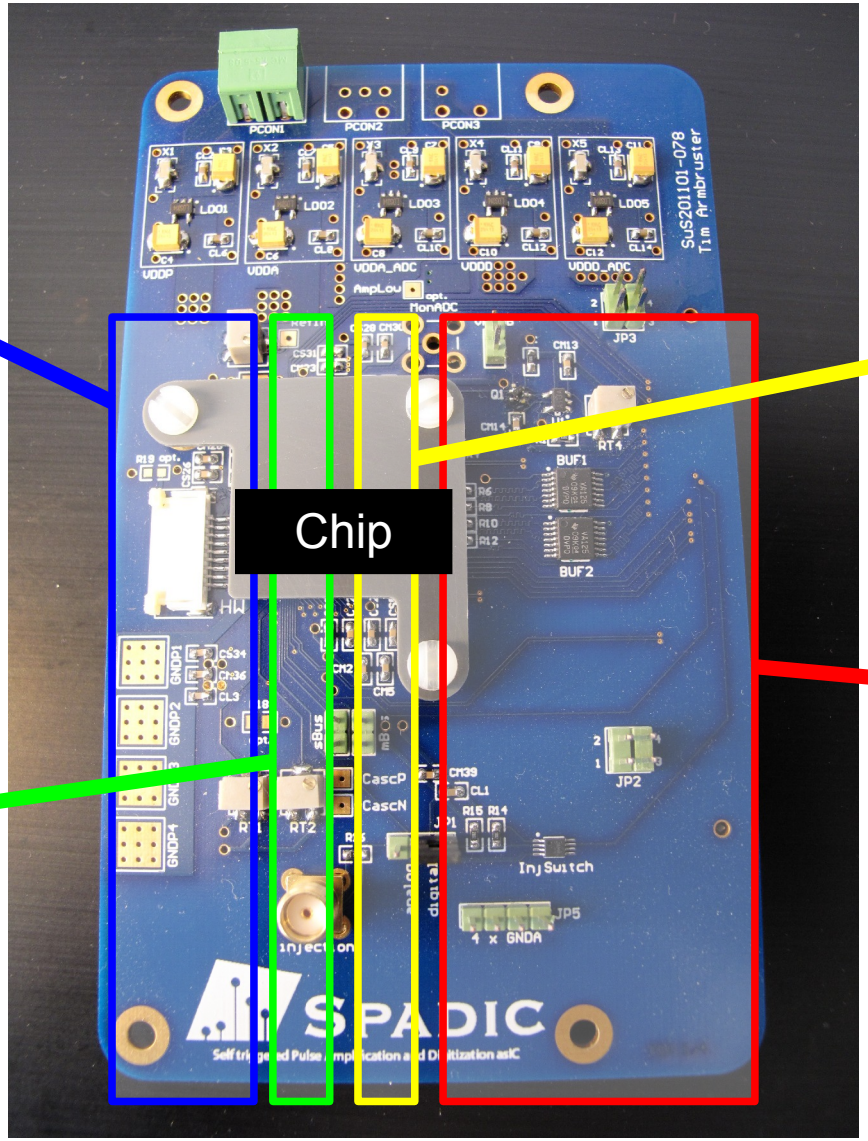


Tip not realized, no daisy chain powering any more

Two additional layers for daisy chain powering

→ Clear separation of power domains in all directions!

SPADIC PCB Improvement #4: Realization



Analog preamplifier

digital ADC

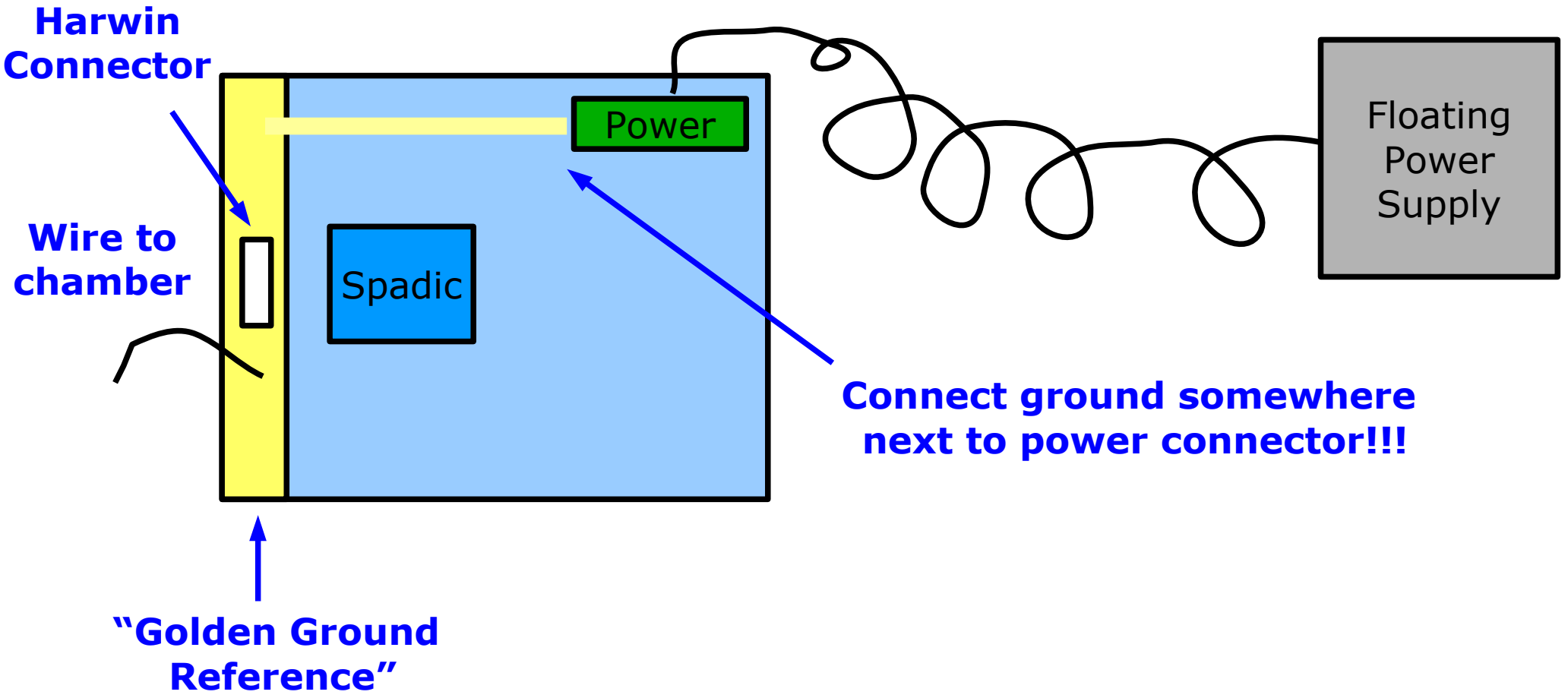
Misc digital (s-cell + PCB stuff)

Analog ADC

Sensitivity

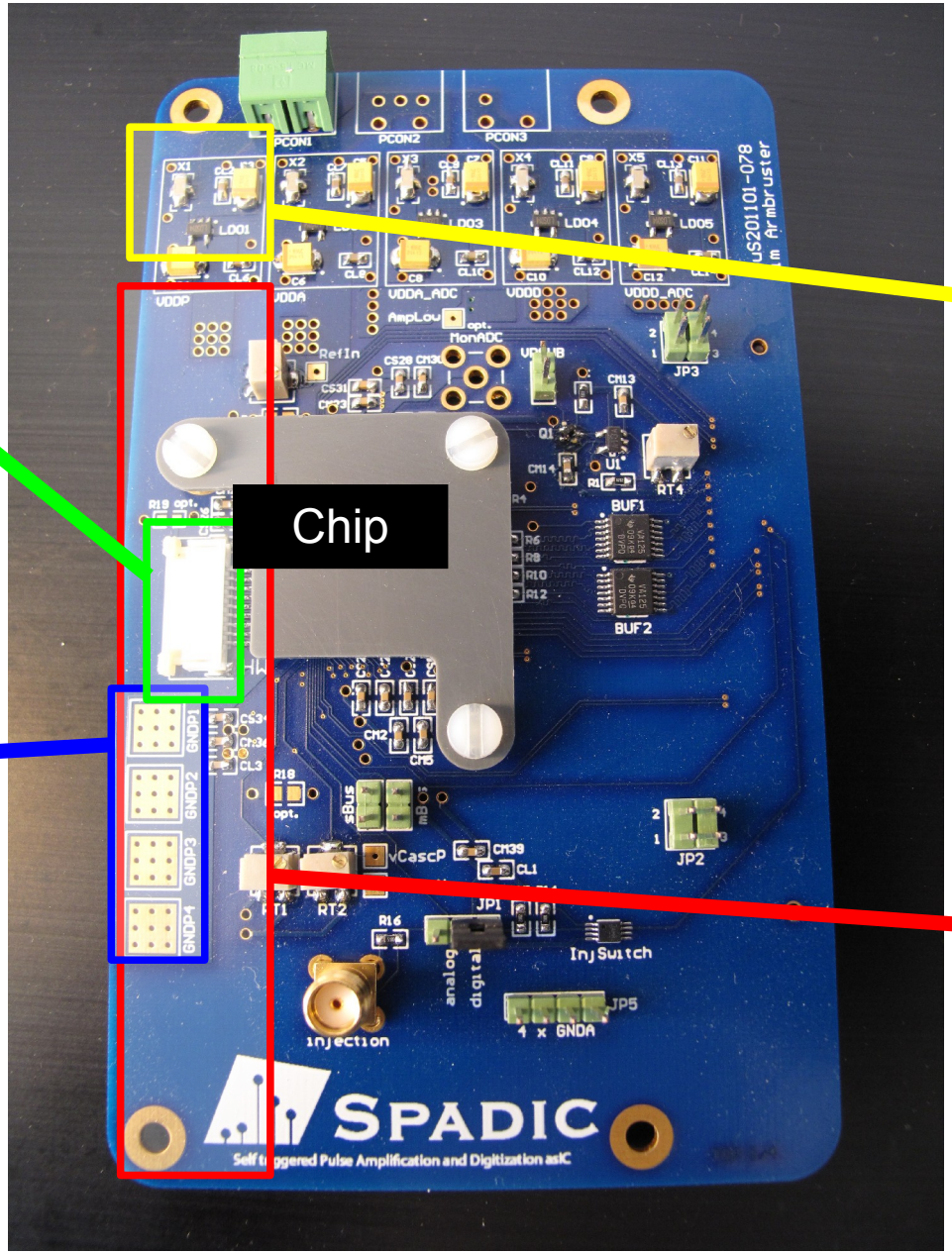
SPADIC PCB Improvement #5: Global Ground Reference

Tip from Ivan Rusanov (GSI)



Geometrically set the analog power reference close to the SPADIC input
→ Well defined "Golden Ground"

SPADIC PCB Improvement #5: Realization



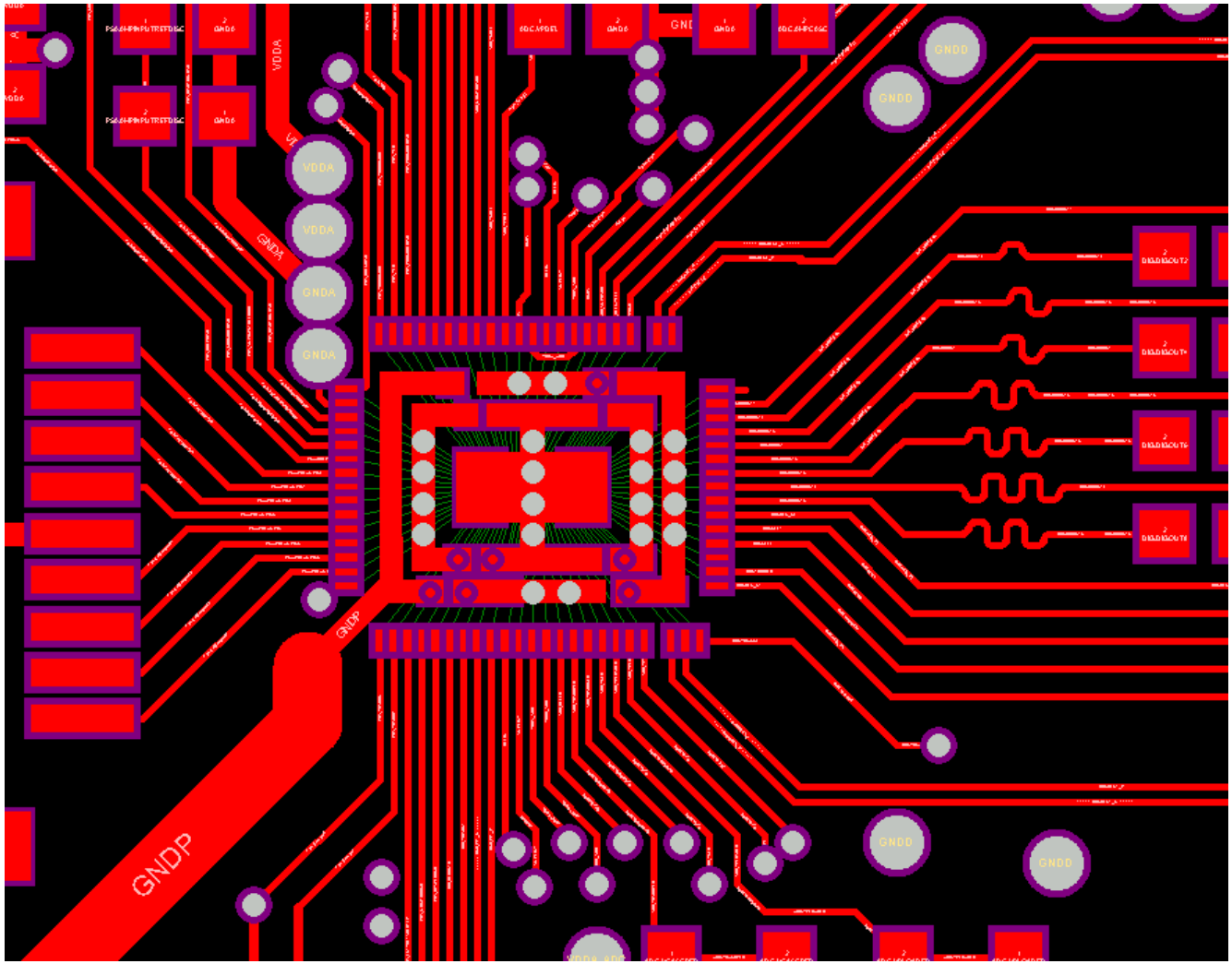
Harwin connector (capton cable to TRD chamber)

Absolute ground reference pads (preamp ground) 0.0V

Connection to other ground domains - here and only here

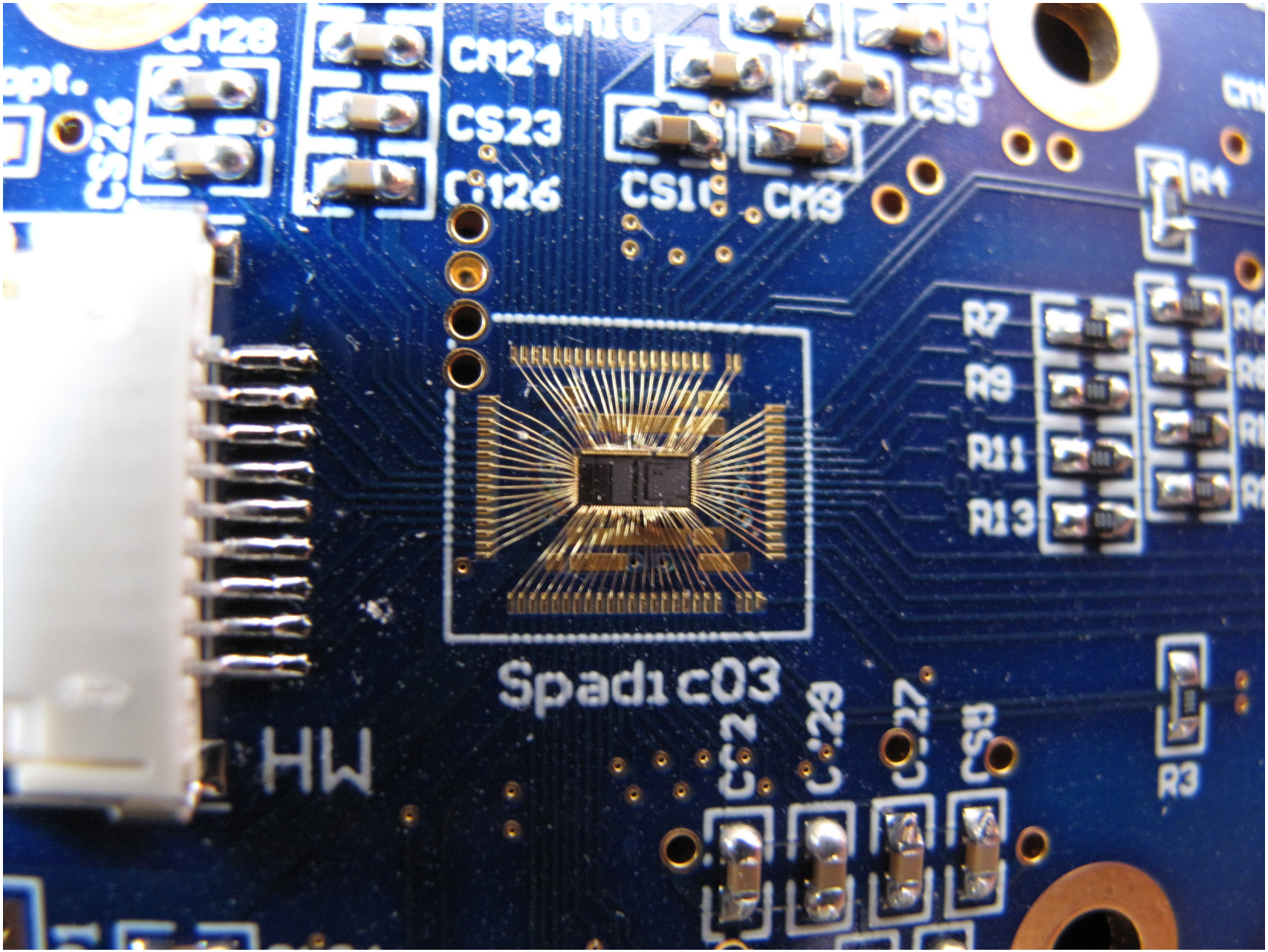
Absolute ground reference pad-plane

SPADIC PCB Improvement #6: Better Footprint



Usage of power rings, well separated power domains, shorter bonding wires, much more relaxed bonding angles

SPADIC PCB Improvement #6: Realization



4. Results

Video: Setup Connected to Pad-Plane, Internal Test-Trigger

http://www.youtube.com/watch?v=tK7Hm2MSg3Y

5. Summary: Design Methodology

Deviated Abstract Design Methodology (1/2)

Proposal: Design methodology for low-noise setups

1) Define power domains
- a) For instance: low noise analog, general purpose analog, standard cell digital, digital io, …
- b) Separate of course different voltage levels (1.8V, 2.5V, ...)
- c) Separate wherever critical dependencies in-between components might be (signal crosstalk, power-drop shielding, parts very sensible to a certain power net, analog vs. digital in general, …)
- d) Separate wherever cross-currents shall be avoided!

2) Define ground domains
- a) Also separate wherever critical dependencies in-between components might be
- b) Don't hesitate to separate wherever it might help - ground nets will be connected again later

3) Define which power domain shall refer to which ground domain
- a) A ground domain can belong to several power domains but mostly not the other way around

4) Assign components to the defined power/ground domains
- a) Add each component to a domain where it neither negatively affected nor affects negatively
- b) For Instance: A strong CMOS buffer can be added to a already noisy digital domain but a sensible amplifier must be added to a low-noise analog domain
- c) If necessary, separate components further into sub-parts (e.g. ASIC)

5) Choose one ground domain to be the absolute ground node (0.0V)
- a) For instance: Choose the most sensitive ground reference (e.g. amplifier input ref-ground)

6) Locally define the position of the absolute ground node (0.0V)
- a) For instance: next to power connector on PCB, nearby connection wire to detector, …
- b) Note: always try to imagine that all other node – even ground nodes – refer to this node
- c) Note: at this point all power and ground domains should meet later on
- d) Leave enough place for the power circuitry and power connectors

Deviated Abstract Design Methodology (2/2)

7) Place components separated by domains
- a) Maximize spacing between most sensible parts
- b) Try to create a "sensitivity gradient"
- c) For instance: Left hand side "sensible analog", middle "misc analog", right hand side "digital"
- d) Avoid domain crossings as much as possible and avoid loops!
- e) All domains must meet somewhere nearby the absolute ground note

8) Add decoupling capacitors (if not already considered)
- a) The smaller the capacitor, the closer it should be placed to the component
- b) E.g: 10uF nearby connector, 100nF to the power line, 1nF directly next to the comp. pin(s)

9) Route all signal wires

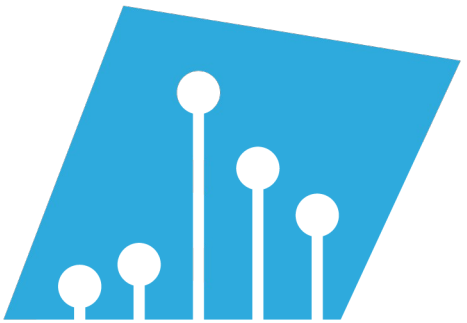
10) Connect components to its power and ground domains
- a) Use large planes whenever possible or at least maximize the width of all power buses
- b) All power buses/planes must meet nearby the absolute ground note

11) Add power circuits using linear regulators
- a) Use the power circuit described further above
- b) Use one power circuit for each power domain, if possible or at least for all sensitive domains

12) Inter-connect ground planes nearby the power circuitry
- a) To stay flexible connect ground planes via large zero-Ohm resistors
- b) Connect just before linear regulator inputs

13) Add Power connectors
- a) Optimum: connect one power connector to each power circuit input
- b) In principal one can also share one power connecter between several or even all power circuits

Theoretical goal: One and only one closed loop for each component group of the same type, starting from the absolute ground reference, going through a linear regulator (+ filter) and coming back via some dedicated ground domain without touching or crossing any other domain.



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