



Status of SPADIC 1.0



Tim Armbruster

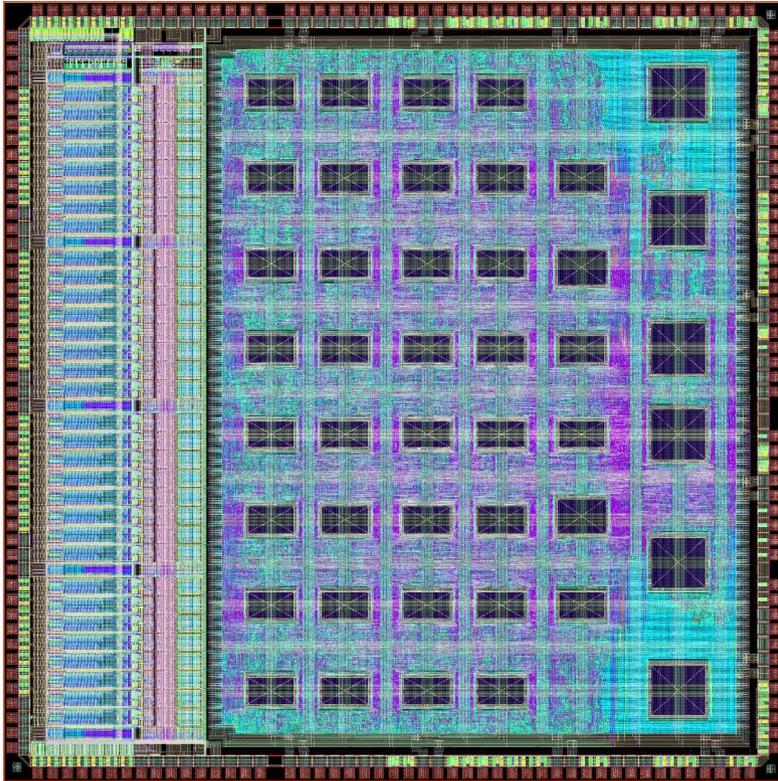
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19th CBM Collaboration Meeting GSI

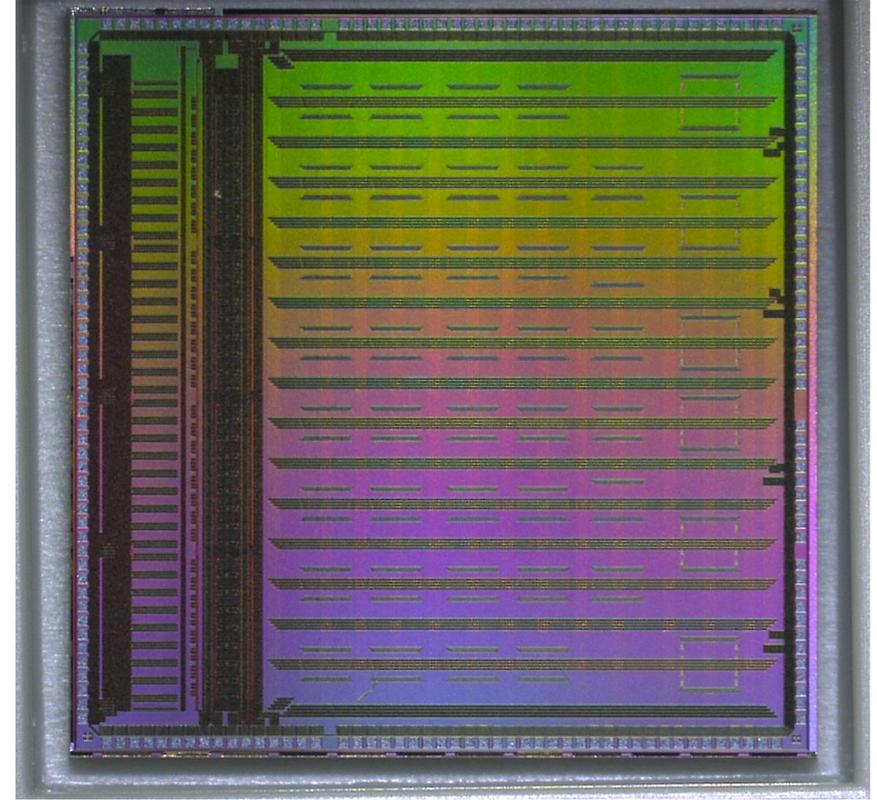
March 2012

Visit <http://www.spadic.uni-hd.de>

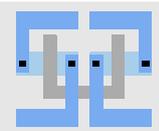
Back from Factory 02/2012



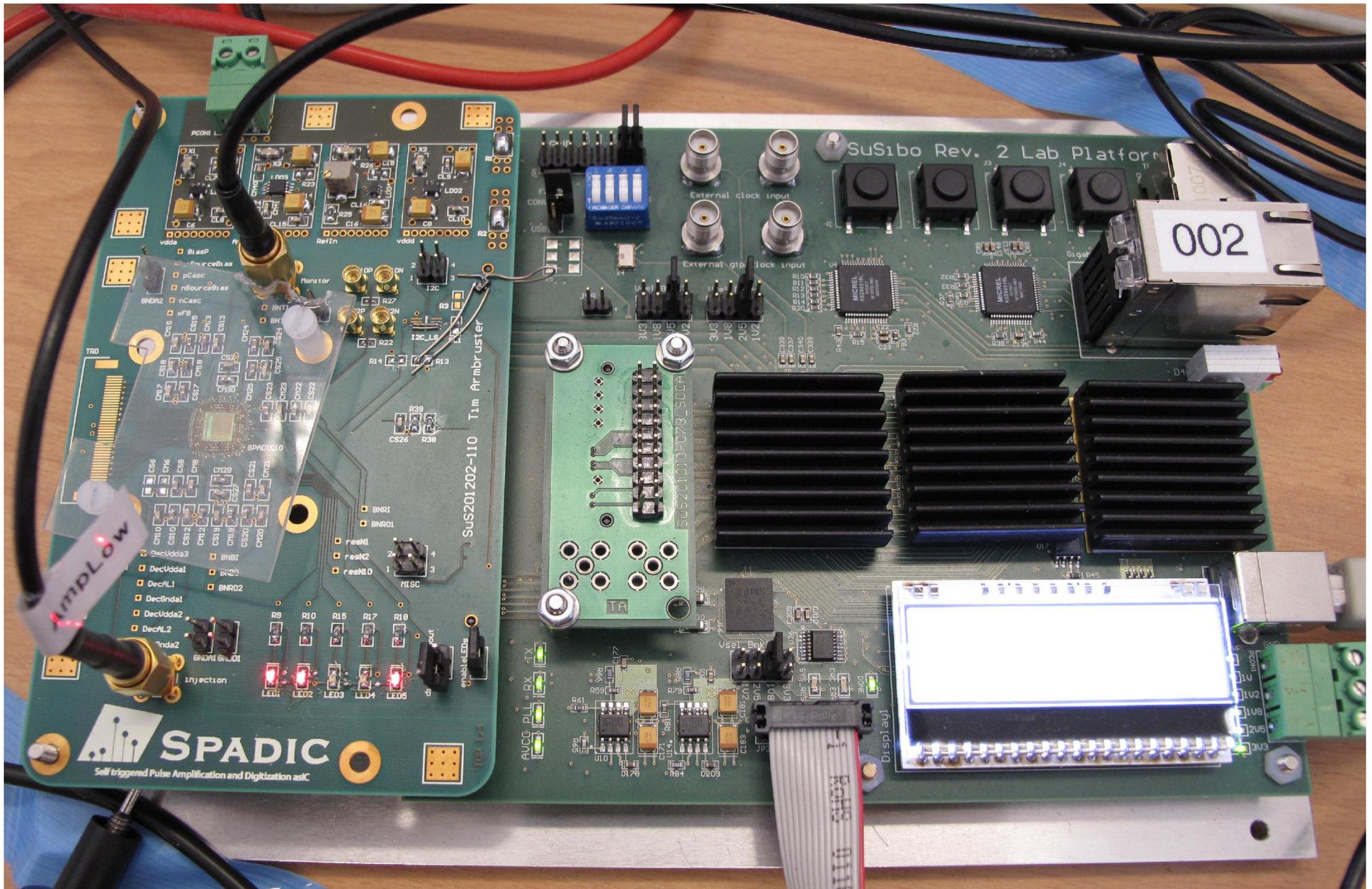
Layout



Photo

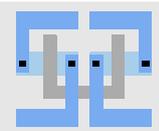
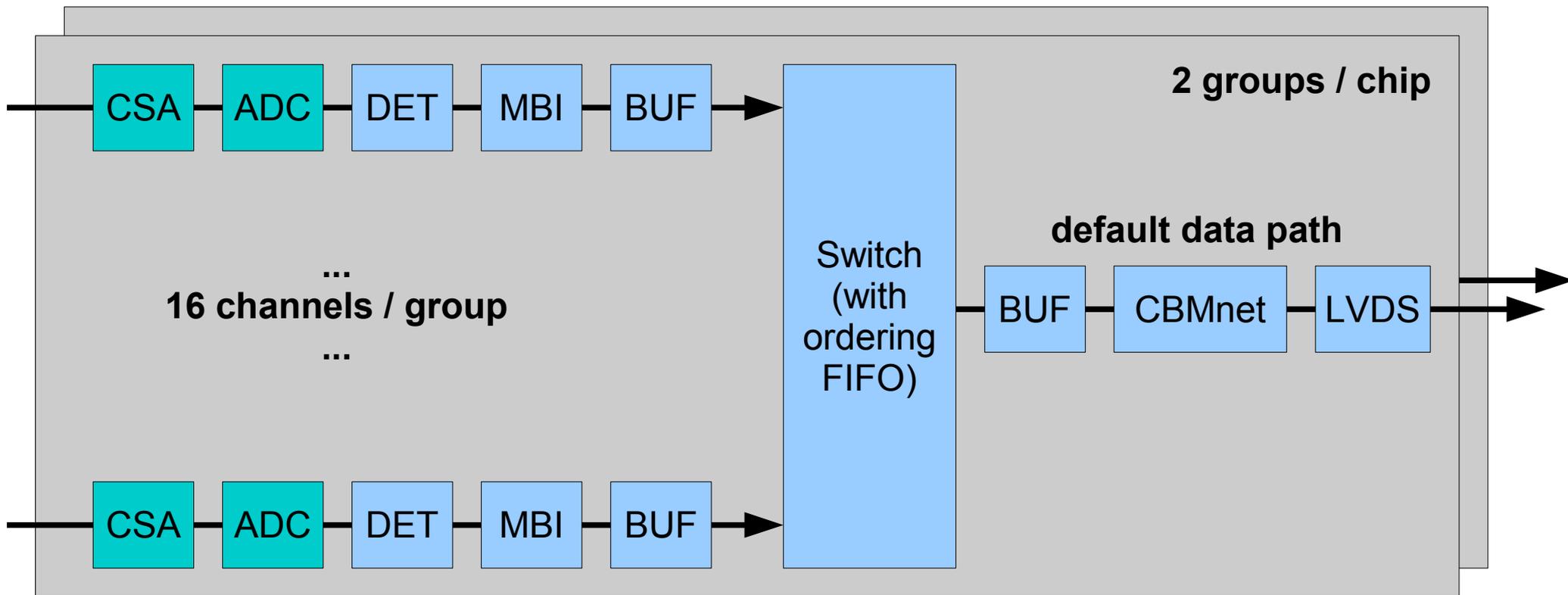


New Setup: Susibo 2.0 + 4 Layer PCB

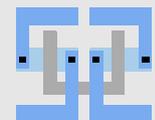
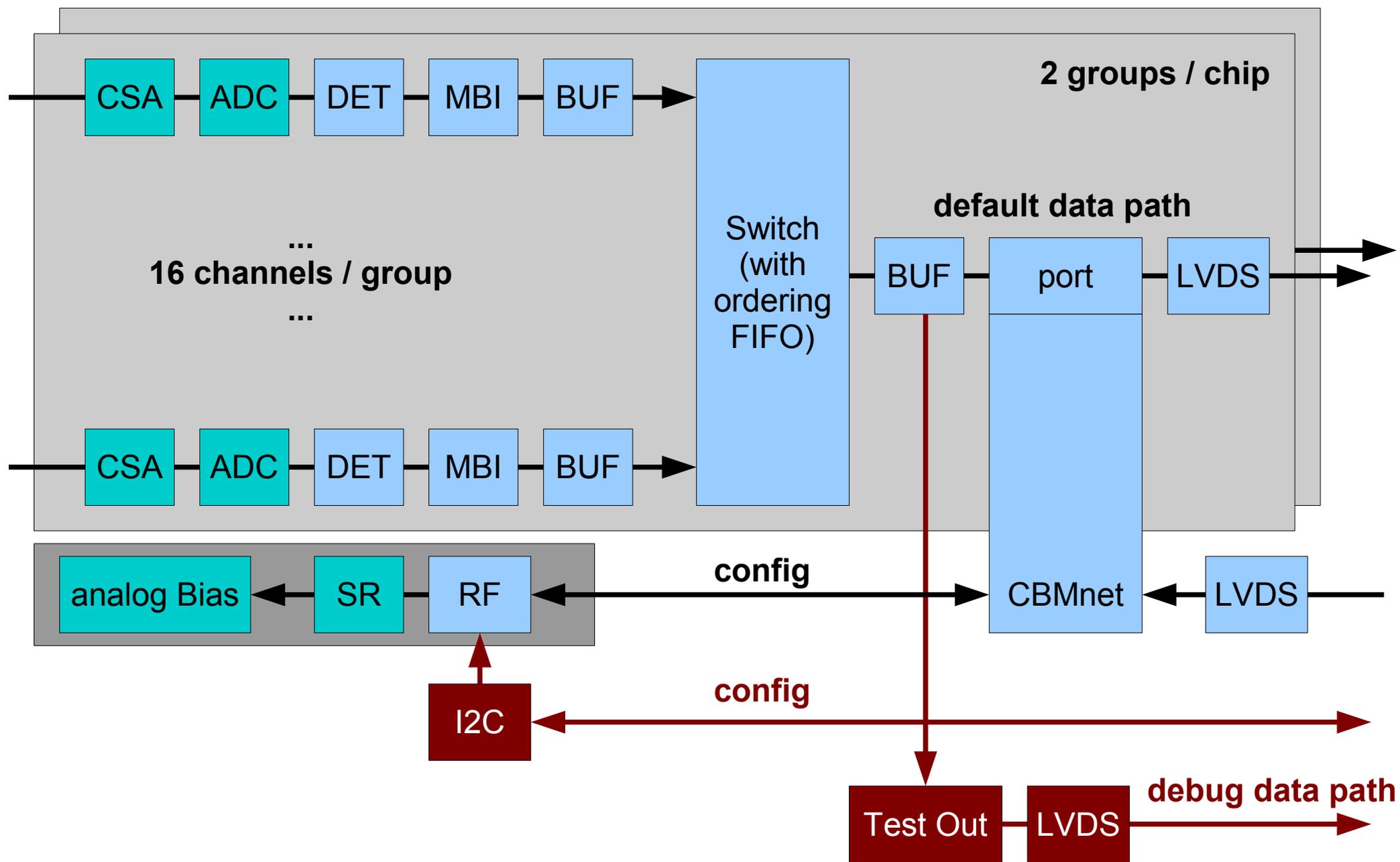


Reminder: SPADIC 1.0 Data Path

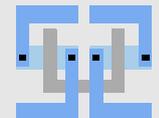
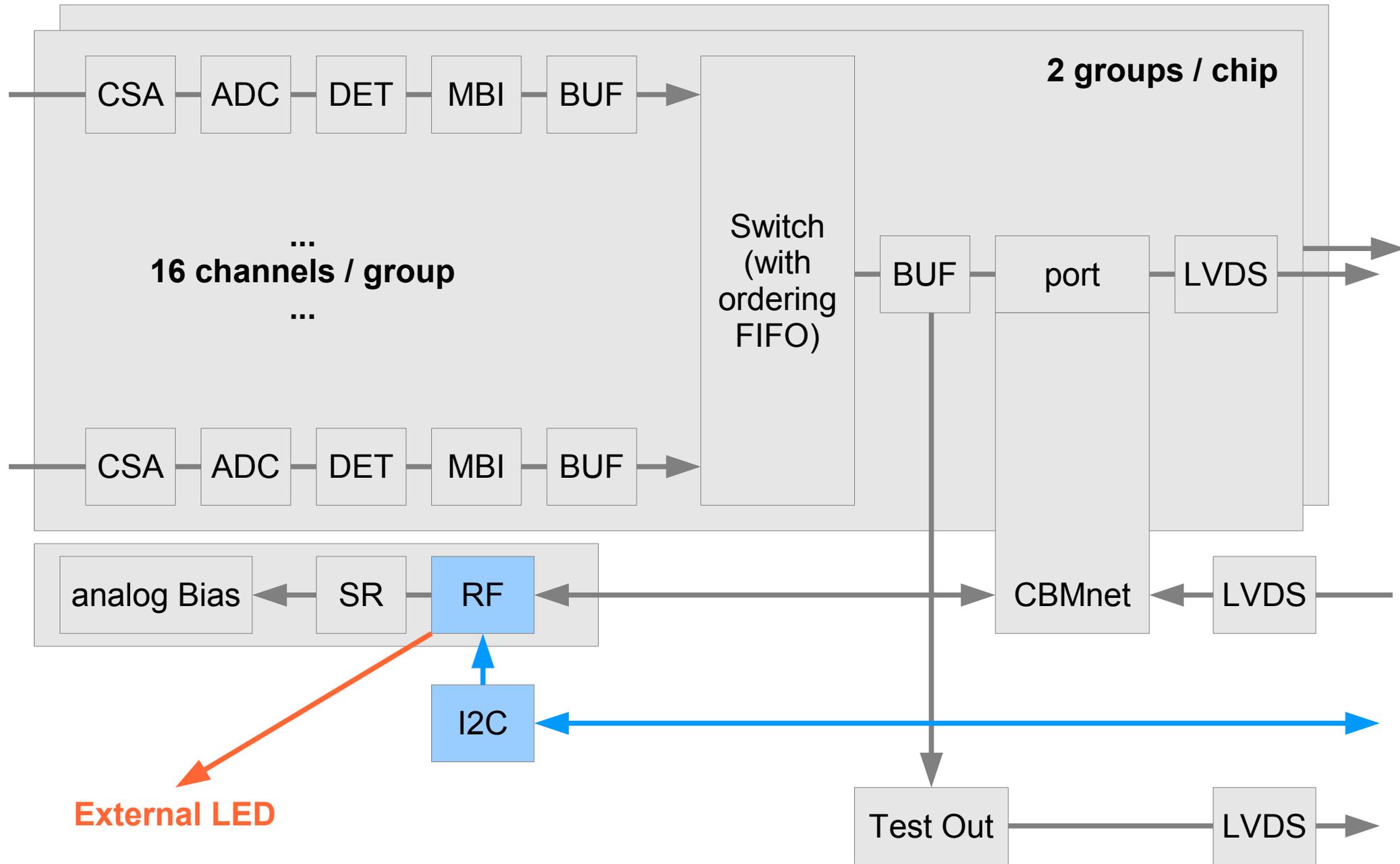
SPADIC: **S**elf-triggered **P**ulse **A**mplification and **D**igitization as**IC**



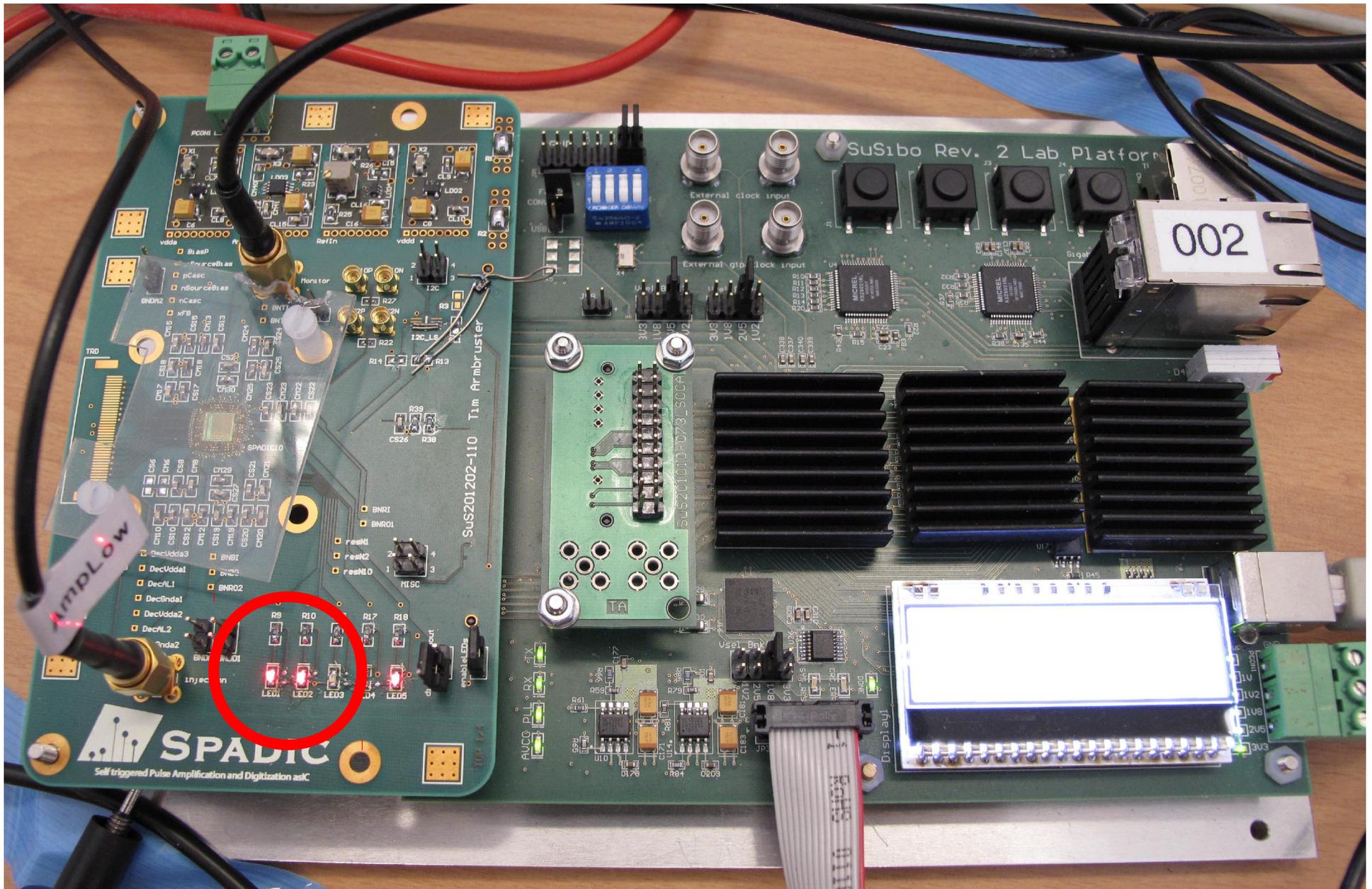
Status: CBMnet not ready yet → fall-back readout



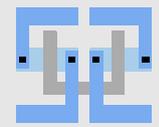
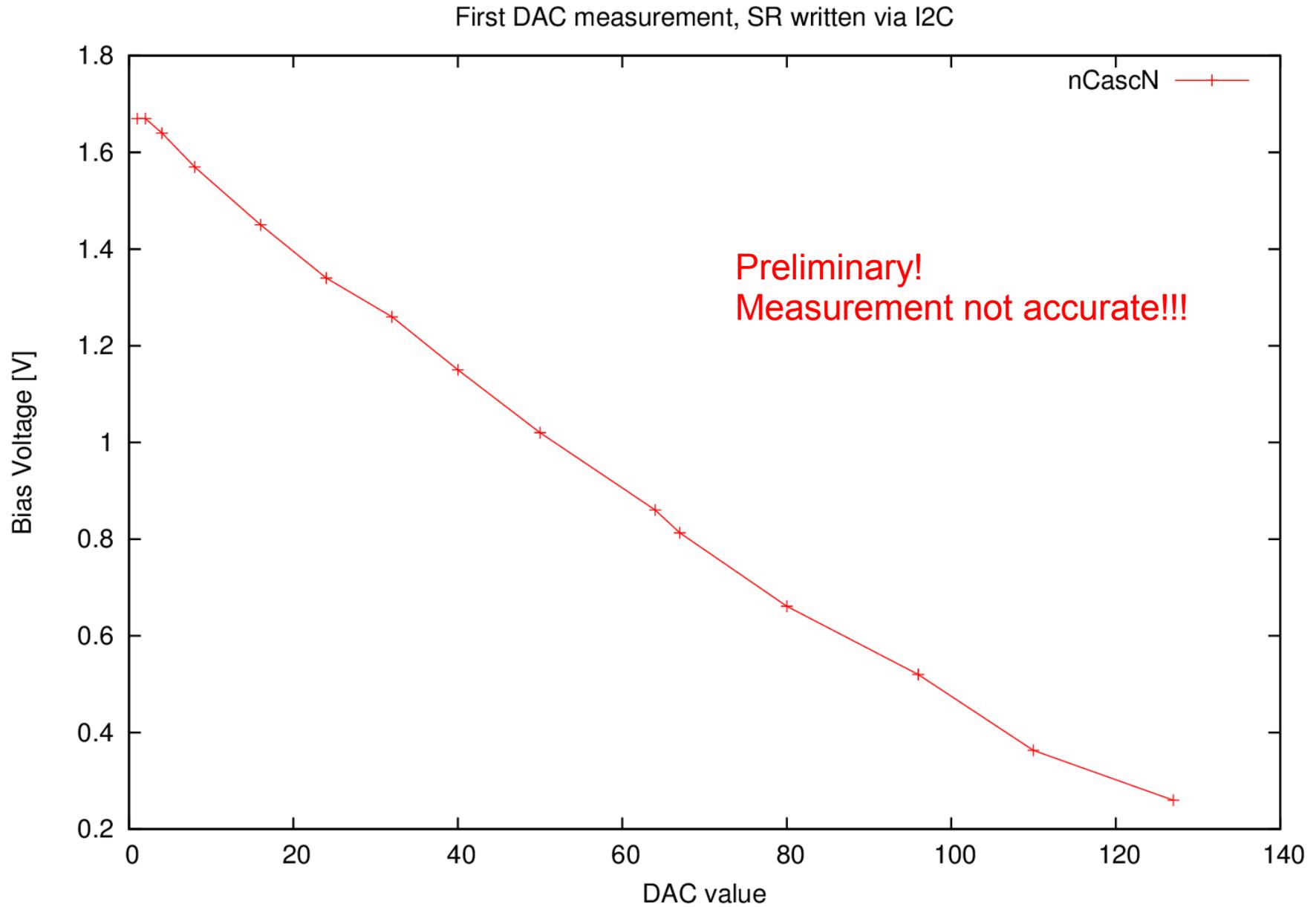
Test 1: Write Register of RF



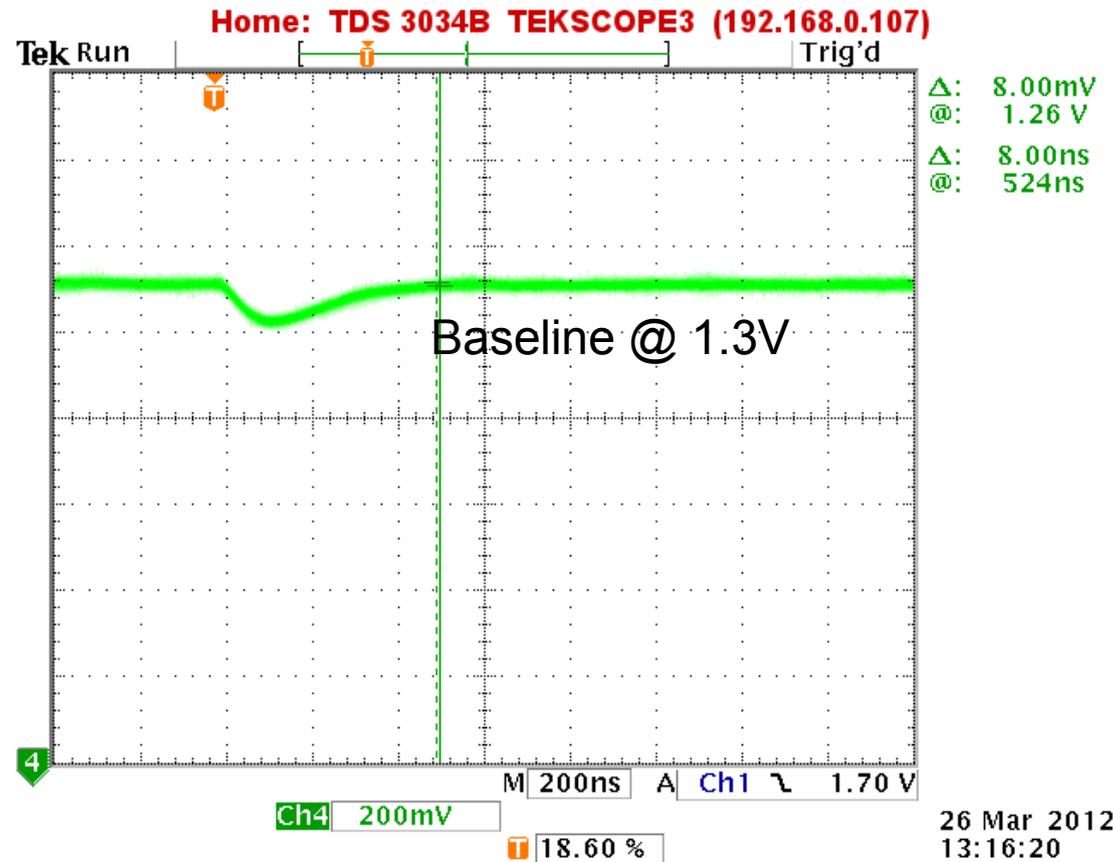
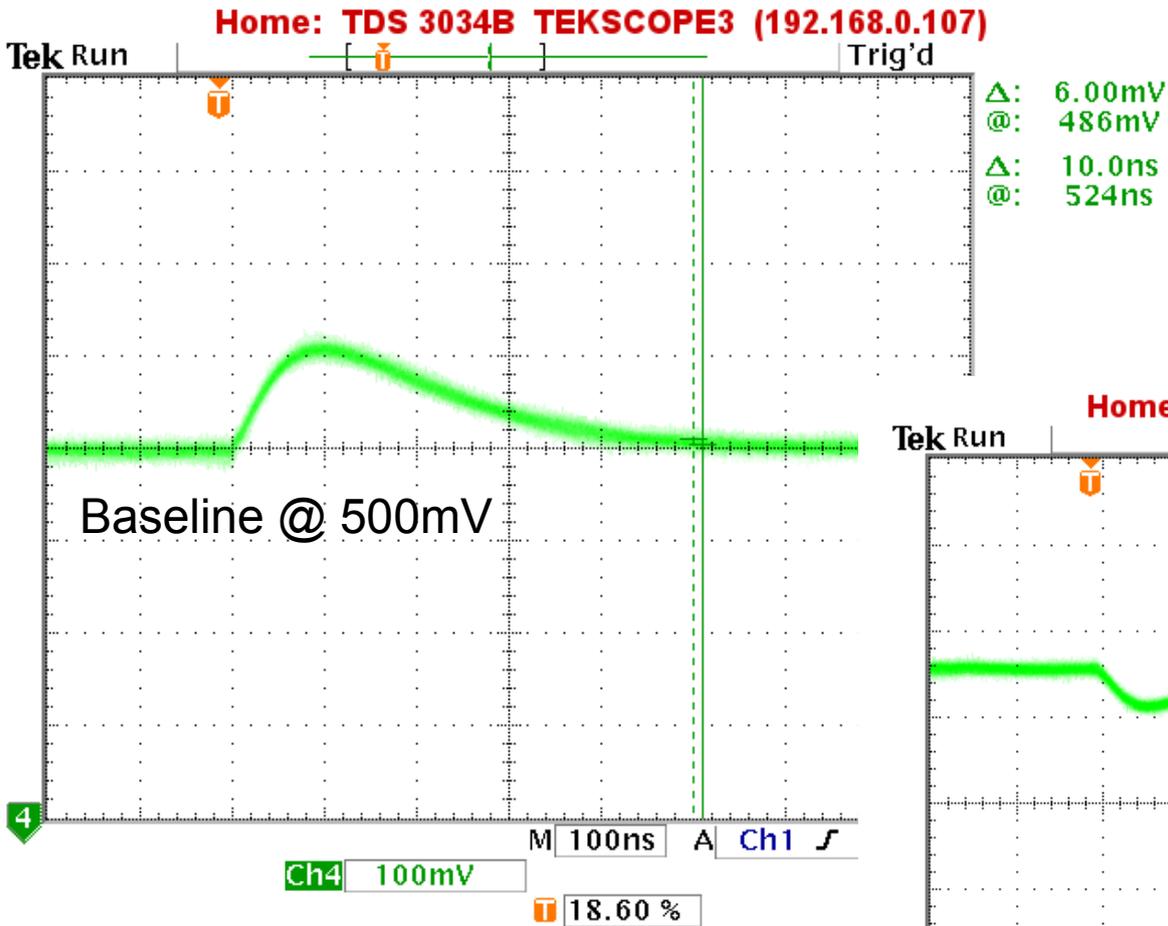
Test 1: Write Register of RF (connected to LED)



Test 2: DAC transfer characteristics



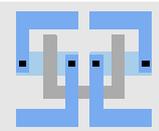
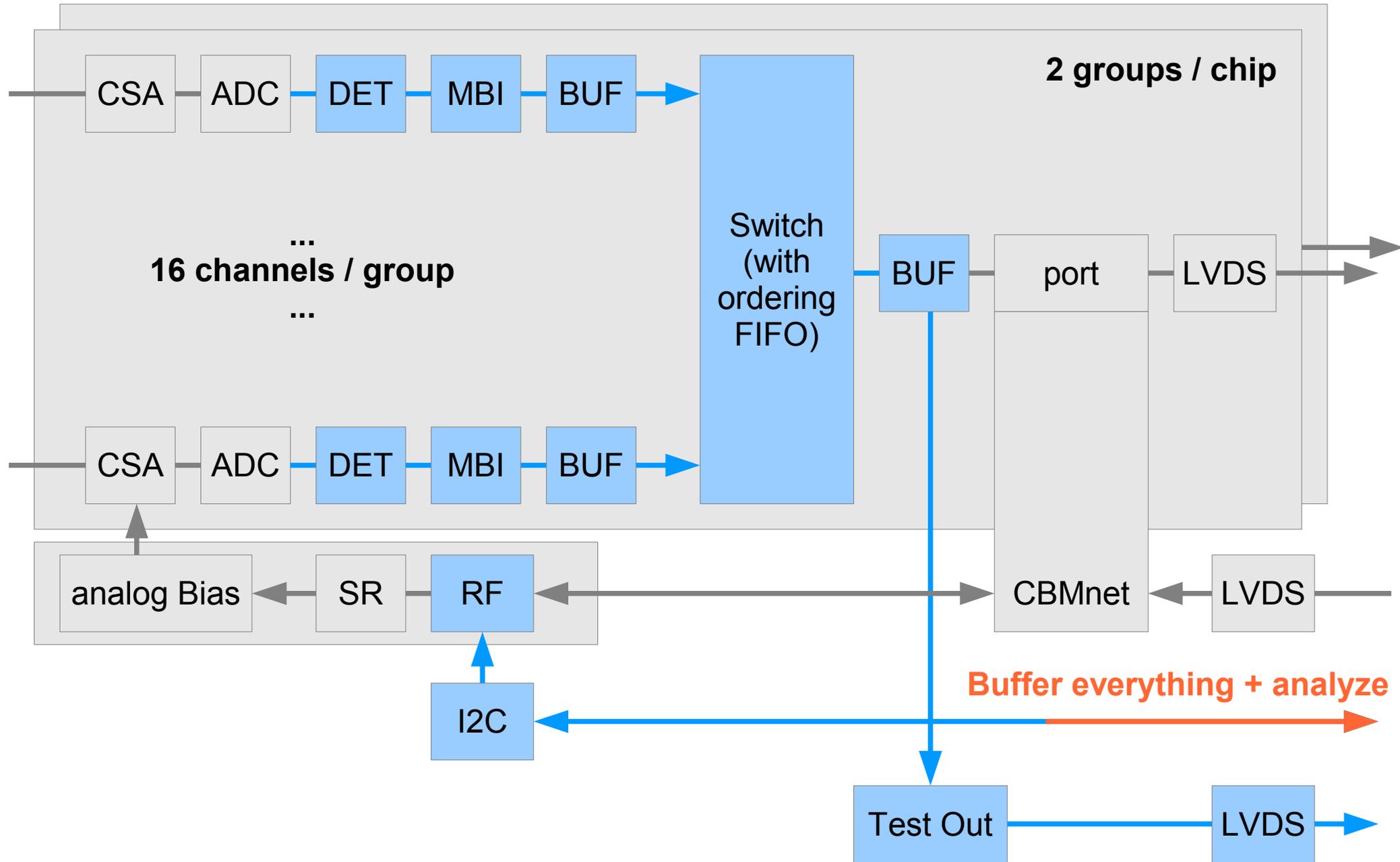
Test 3: CSA



Preliminary!
Measurement not accurate!!!
Via monitor bus only!
Bias not optimal!

26 Mar 2012
13:16:20

Test 4: Read-out everything DIRECTLY after releasing reset



Test 4: "Read Initial Trash"

read10 (~/asics/spadic10/...ent susibo/data/te...)

Datei Editieren Werkzeuge Synta

```

1 bfa0 0fb3 df1f ff01 bf90
2 bf3a af7a 0f01 143f 0f80
3 2f54 ef55 dfaf bdfb 0fb3
4 5f25 df07 8f90 af2a bf22
5 8f0b 753f 0f80 bf2a 0f80
6 bf2a 0f80 ef53 3f80 2f56
7 88fa 2f54 bfa4 5f27 b4fa
8 3f80 bf2a ff91 df2b df92
9 df92 3fa6 0fb3 55eb df37
10 df2f df92 9fa5 ff50 bf5a
11 bf6a 9f3b ef9f 5eaf caf7
12 bf7a af2a af6a 0f80 6f55
13 7f55 9fa5 0fb3 efa4 3f80
14 bf32 8f93 0fb0 df1f 5f39
15 7f99 69f5 9f5a 9f5a 9f3a
16 0f80 af7a 0f80 7f57 ef57
17 4fa5 57ea 0fb3 df3b 5fb0
18 5fa4 af74 edef 4fa4 0fa4
19 bf26 af50 9f27 3f9f ff93
20 ef97 c038 1f9e c0ff
21
22 8011 900b a000 0001 01c3 73fb 7eee 3b9d 6753 3c00 b310
23
24 8012 900b a000 01ff 0143 53eb 5aed 3b5d 576b 3a00 b310
25
26 8014 900b a000 01ff 0143 52ea 5abd 2f57 55ea 7a00 b310
27
28 8015 900b a000 01ff 0143 536b 5add 375b 56eb 3a00 b310
29
30 8017 900b a000 01ff 0143 53eb 7afd 3f5f 57eb 7a00 b310
31
32 801a 900b a000 01ff 0143 53eb 7afd 3f5f 57eb 7a00 b310
33
34 8010 900b a000 01ff 0143 53eb 7afd 3f5f 57eb 7a00 b310
35
36 8013 900b a000 01ff 0143 53eb 7afd 3f5f 57eb 7a00 b310
37
38 8016 900b a000 01ff 0143 53eb 7afd 3f5f 57eb 7a00 b310
39
40 8019 900d aff8 0bf5 1552 56aa 32d5 265a 54cb 2a00 b310
41
42 801b 900d aff8 0bfd 0753 54ea 3a99 2552 54aa 2a00 b310
43
44 801c 900d aff8 0bf5 155a 569b 2295 3552 56aa 3200 b310
45
46 801d 900d afff 7bf5 054a 52a9 2a53 14ca 3299 2600 b310
47
48 801e 900d aff8 03f9 165a 56ab 2ad5 355a 56ab 2a00 b310
49
50 8010 9016 a56b 3a00 2f57 554a 7a00 2f55 15ca 5200 b310

```

Preamble	Payload	Type	Description
1000	ssss ssss iiii	start data message	s: 8 bit group-id, i: 4 bit channel-id
1001	tttt tttt tttt	time-stamp	t: 12 bit time-stamp
1010	rrrr rrrr rrrr	raw data	r: 12 bit raw data
1011	pppp pphh -sss	end of data message ¹	p: 6 bit data values, h: 2 bit hit-type, s: 3 bit stop-type
1100	-- bbbb bbbb	buffer overflow ¹	b: 8 bit lost hits
1101	eeee eeee eeee	epoch marker ¹	e: 12 bit epoch
1110	dddd dddd dddd	extracted data	d: 12 bit extracted data
1111	tttt iiii iiii	information ¹	t: 4 bit info-type, i: 8 bit depends on info-type
0	ddd dddd dddd dddd	continuation	d: 15 bit continued (meta/raw) data

Reset released

e.g.:

“Normal Message” of channel 17:
 Time-Stamp 11 (440ns after reset)
 12 x 9 bit raw data (yet random)
 Internally triggered, normal stop

or

“Normal Message” of channel 30
 Time-Stamp 13 (520ns after reset)
 12 x 9 bit raw data (yet random)
 Internally triggered, normal stop

Some packages (since ADCs are not configured yet and typically produce a strange start-up sequence)

Test1 ... Test4 => Promising results!

Some milestones reached:

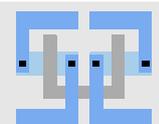
- Digital part can already be clocked and reset @ 200MHz
- I2C core works (little bug in I2C pad, but workaround found)
- RF works
- Tricky chain RF → SR in analog part works
- Analog CSA (both polarities) work
- FIFO (unknown SRAMs!!!) work
- Hit-Detection seems to work
- Message protocol seem to work

Next steps:

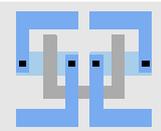
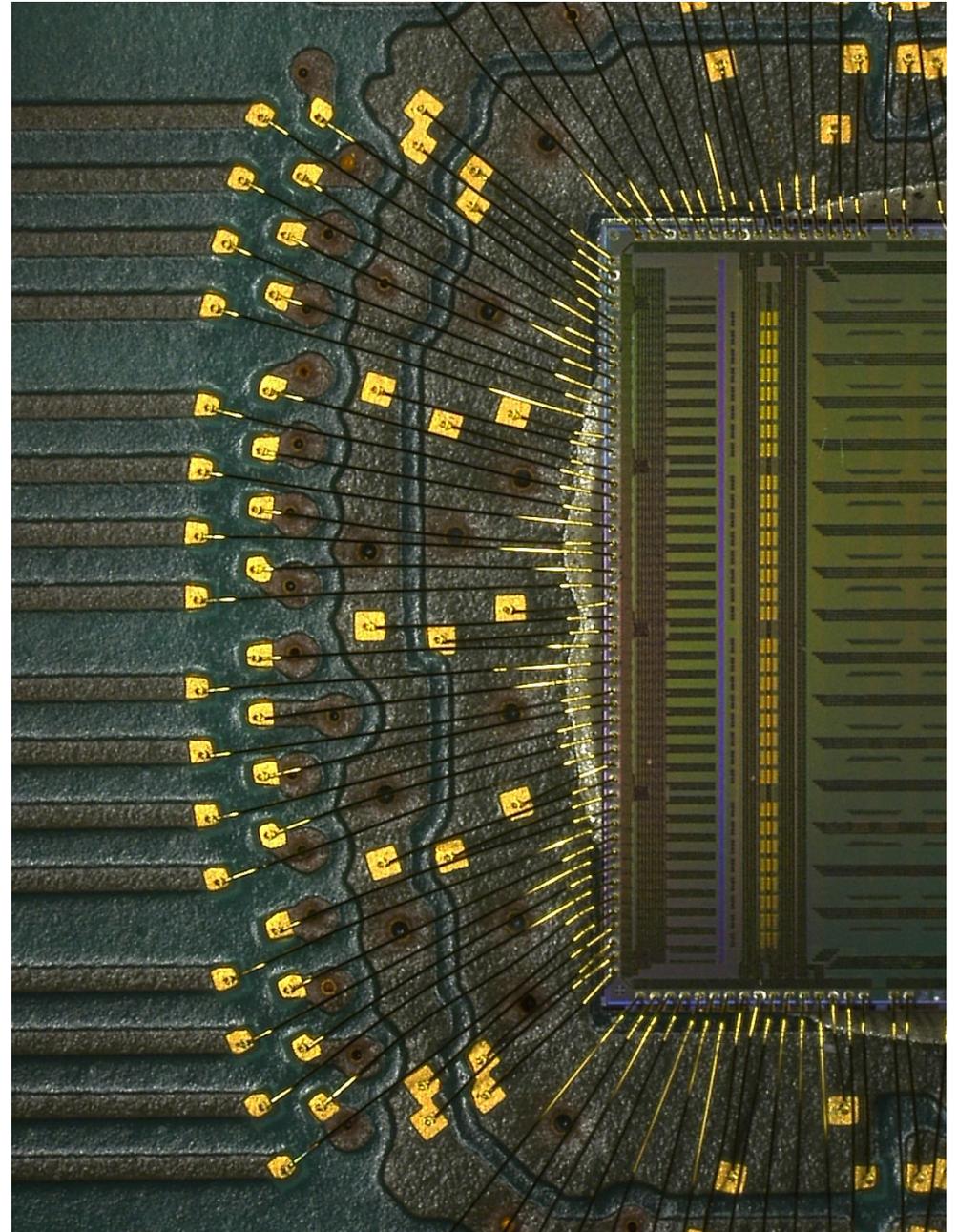
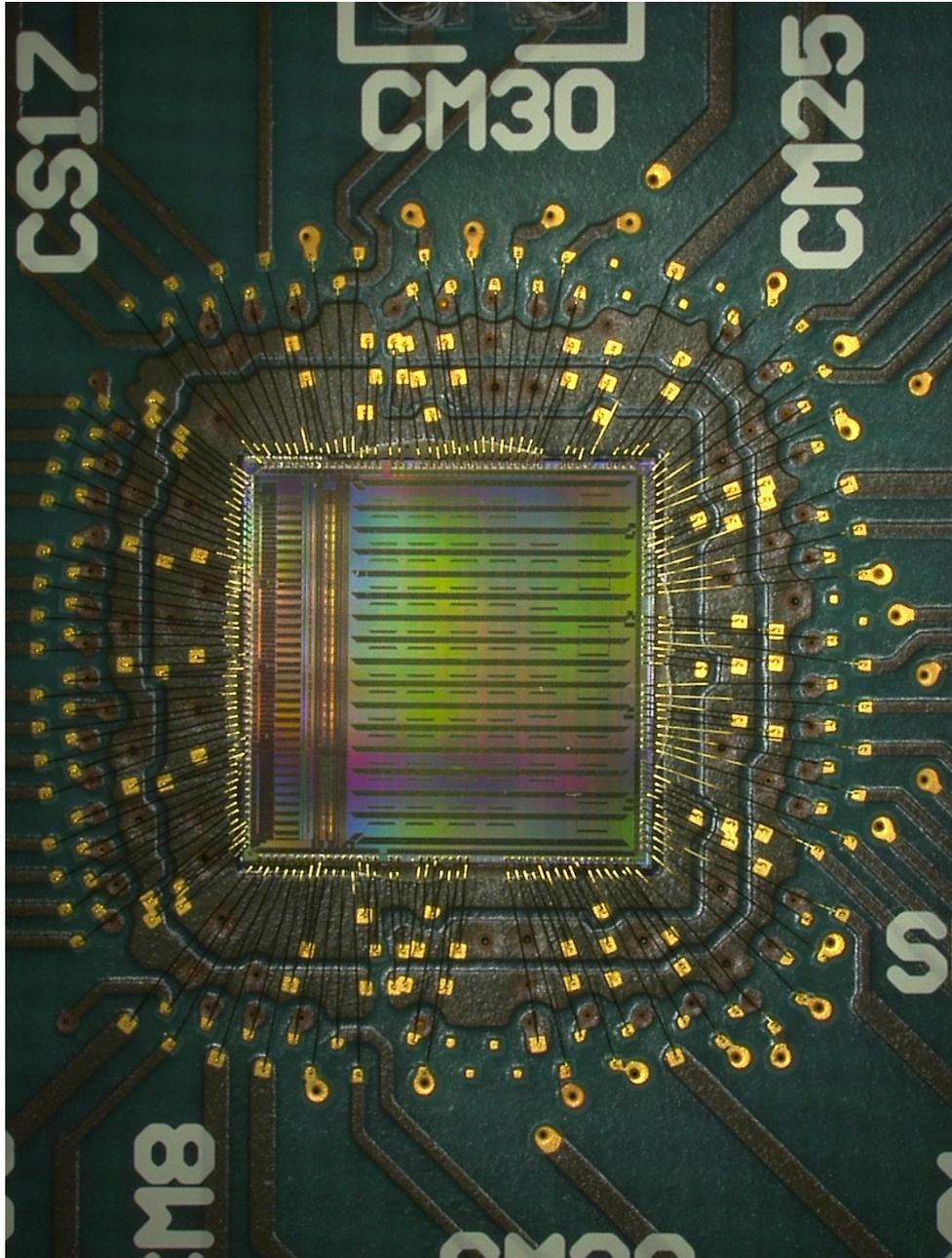
- improve readout software
- set bias voltages, start ADCs
- build CBMnet core for FPGA, test CBMnet link
- put everything together
- characterize everything
- ...

Very promising results → but yet no final conclusion possible:

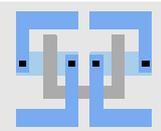
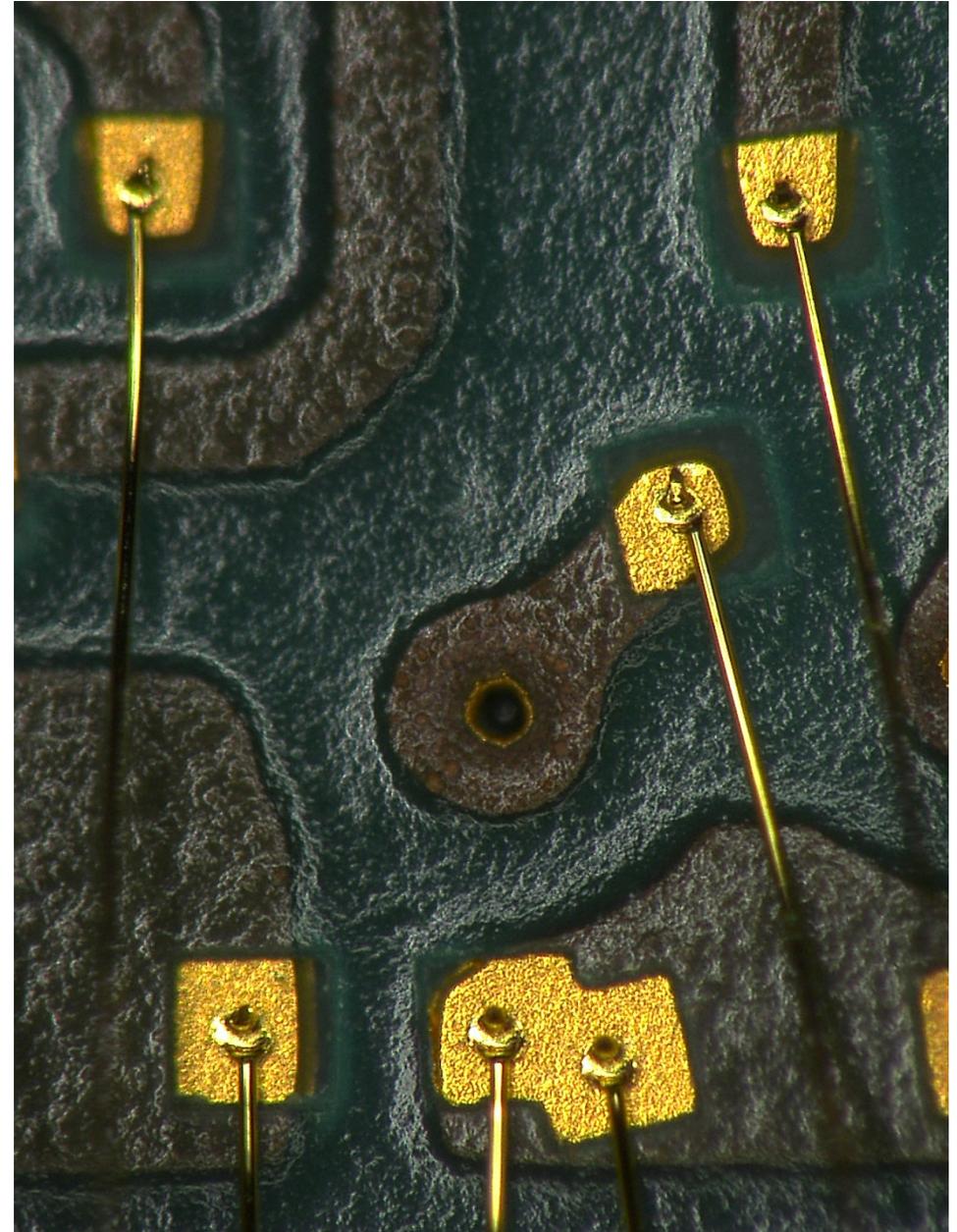
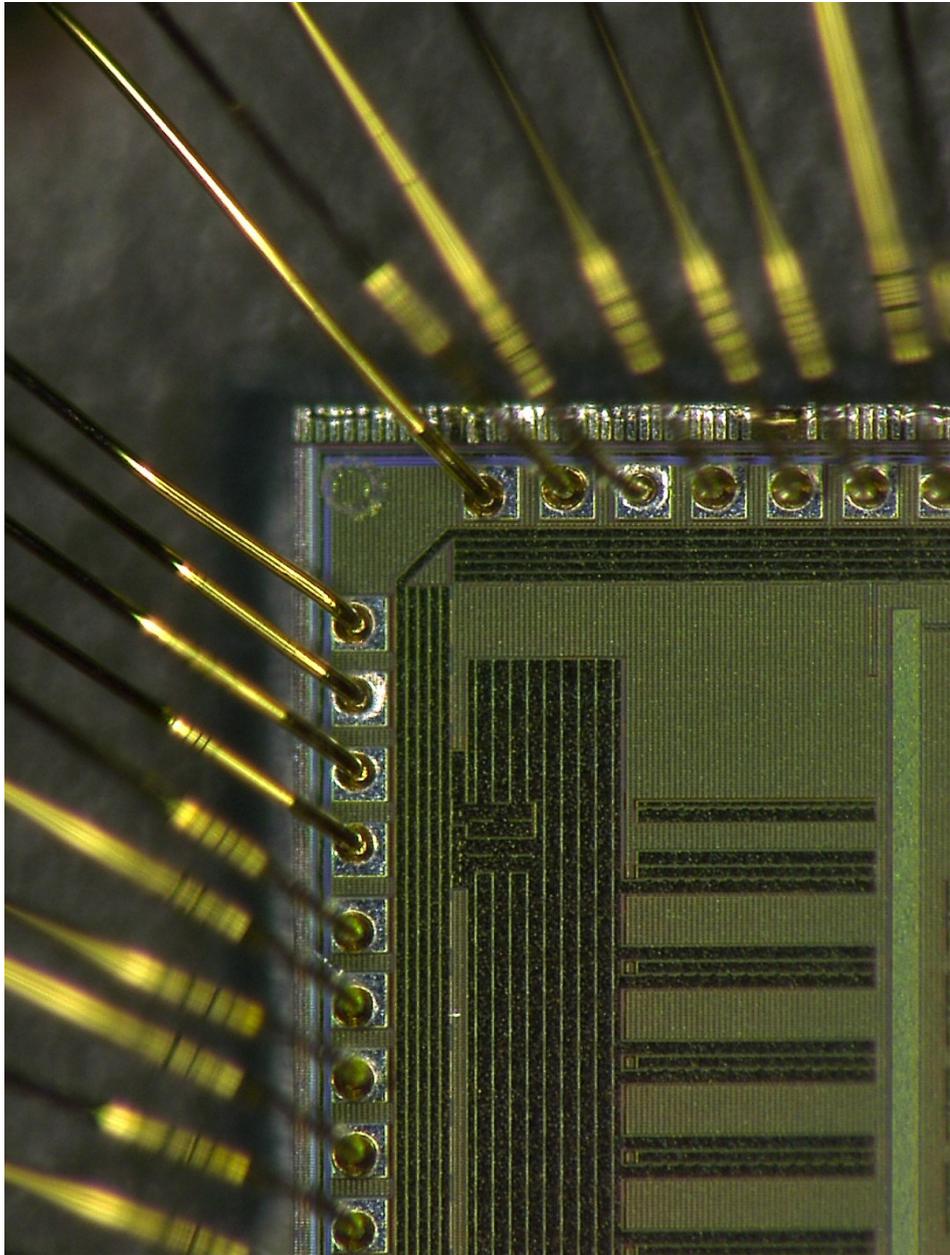
Status: "SPADIC 1.0 {works; works not}"



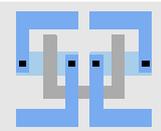
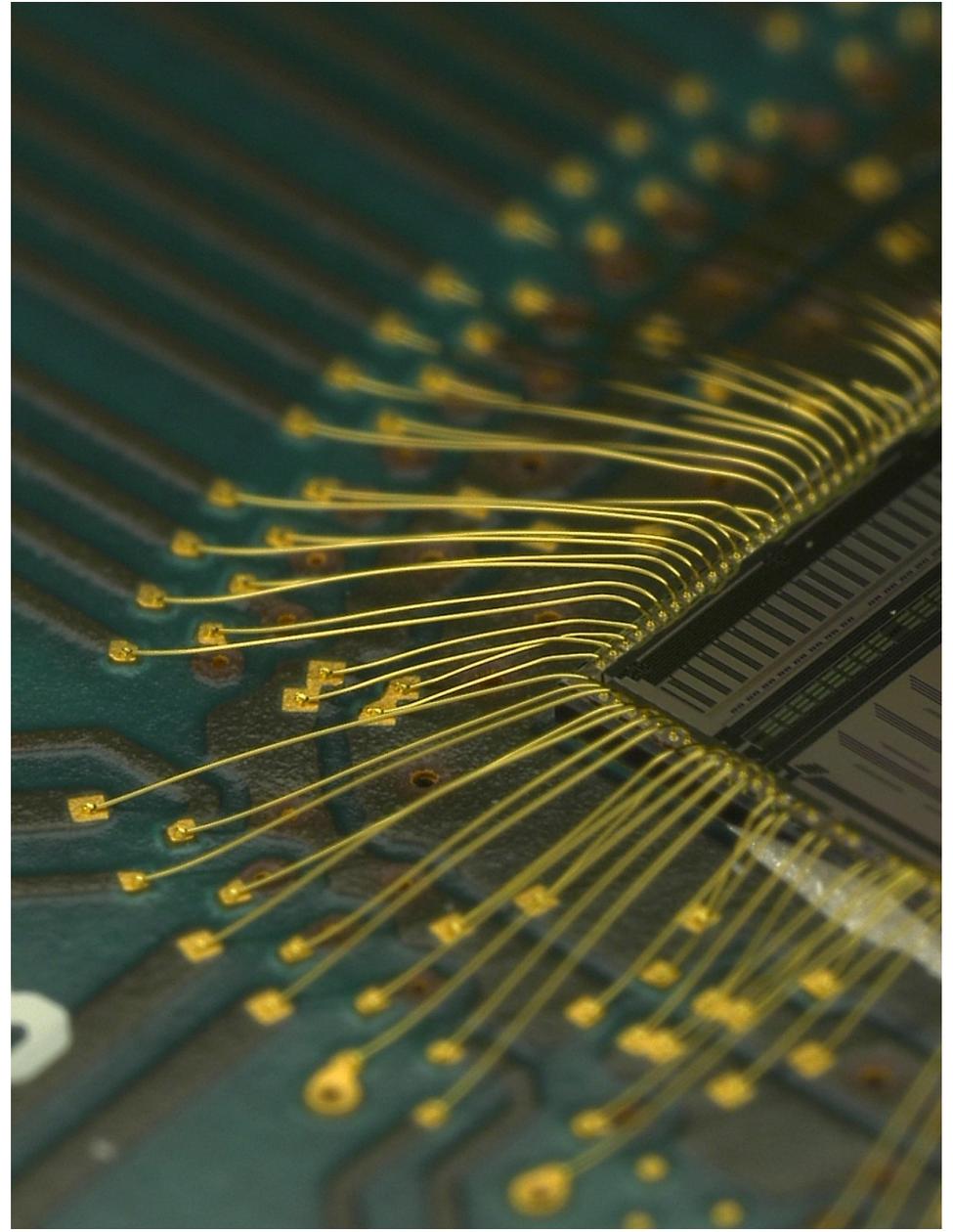
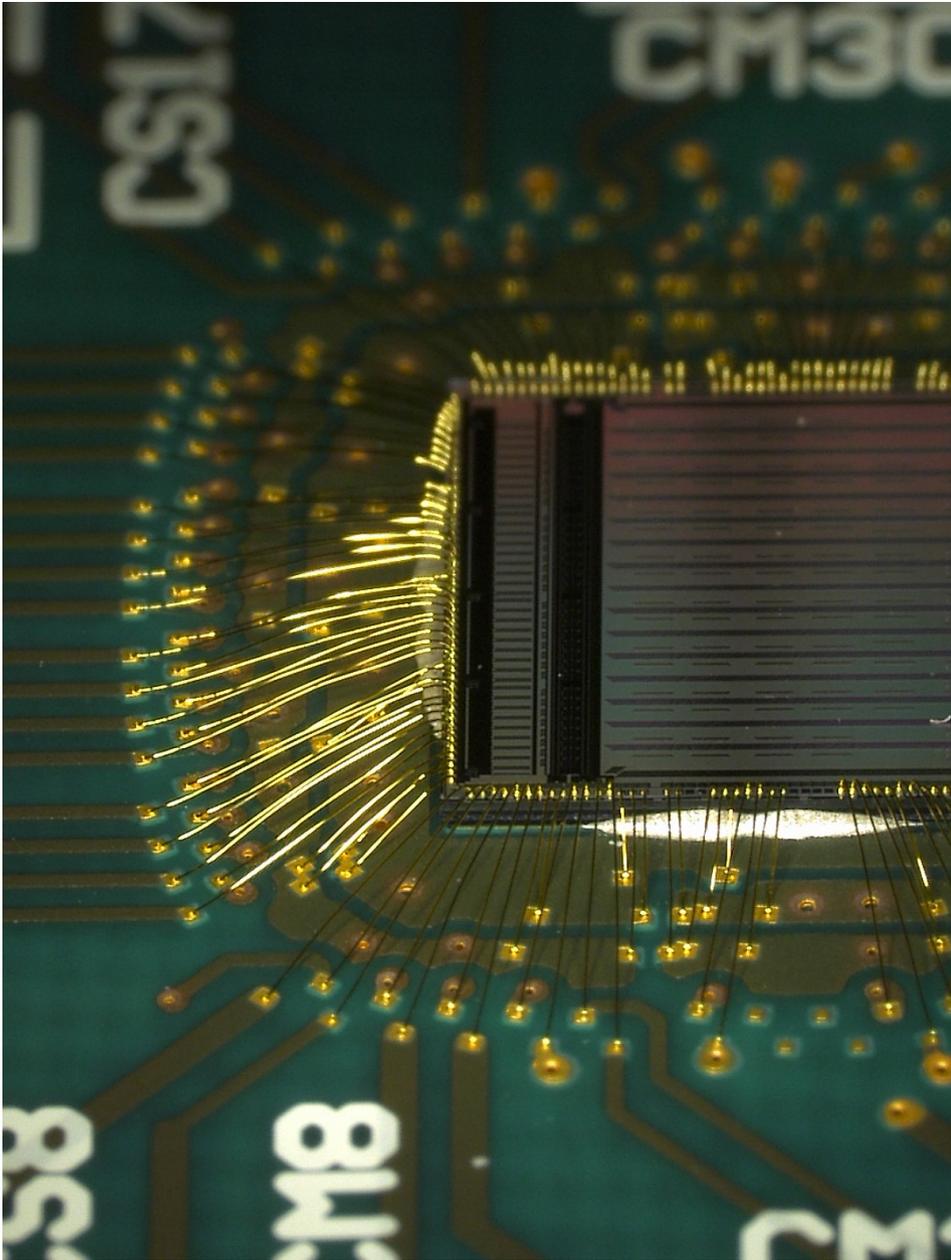
Some Impressions (1/3)

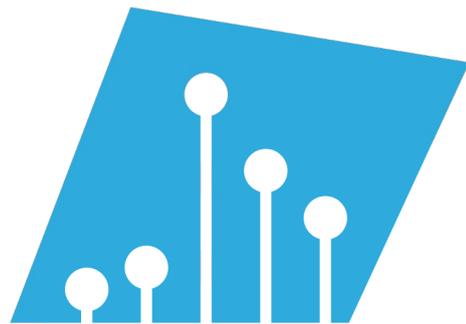


Some Impressions (2/3)



Some Impressions (3/3)





SPADIC

Self triggered Pulse Amplification and Digitization asIC

<http://www.spadic.uni-hd.de>