UNIVERSITÄT HEIDELBERG

SPADIC
Self triggered Pulse Amplification and Digitization asIC

Status of SPADIC 1.0

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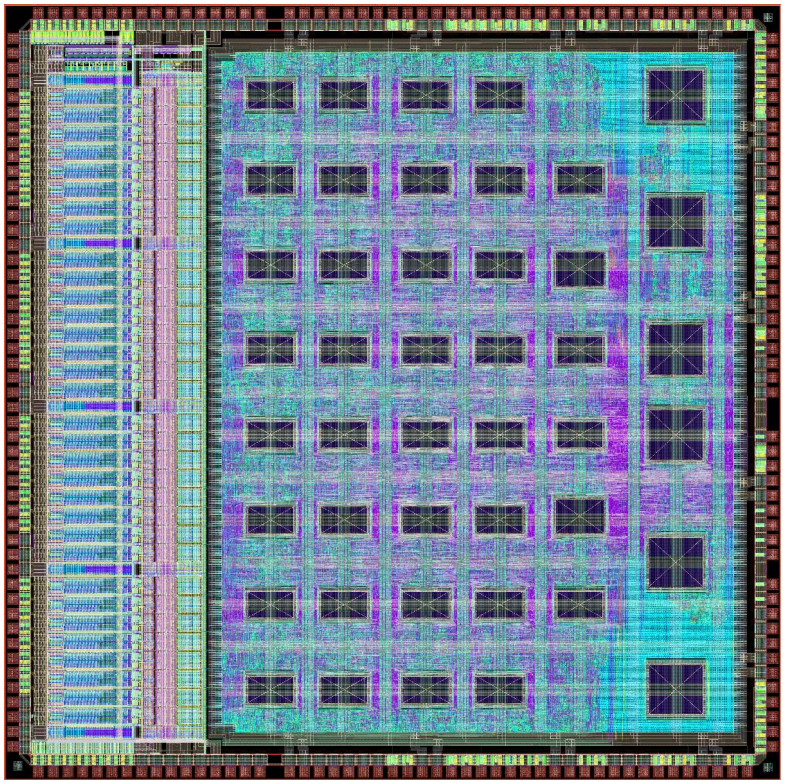
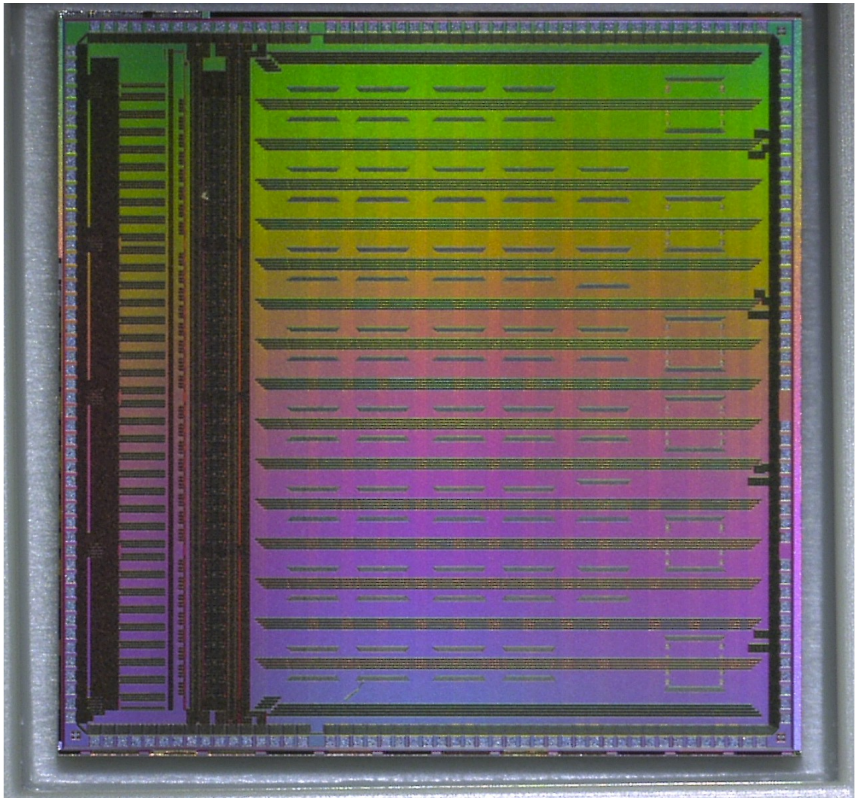
19th CBM Collaboration Meeting GSI
March 2012

Visit http://www.spadic.uni-hd.de

Back from Factory 02/2012

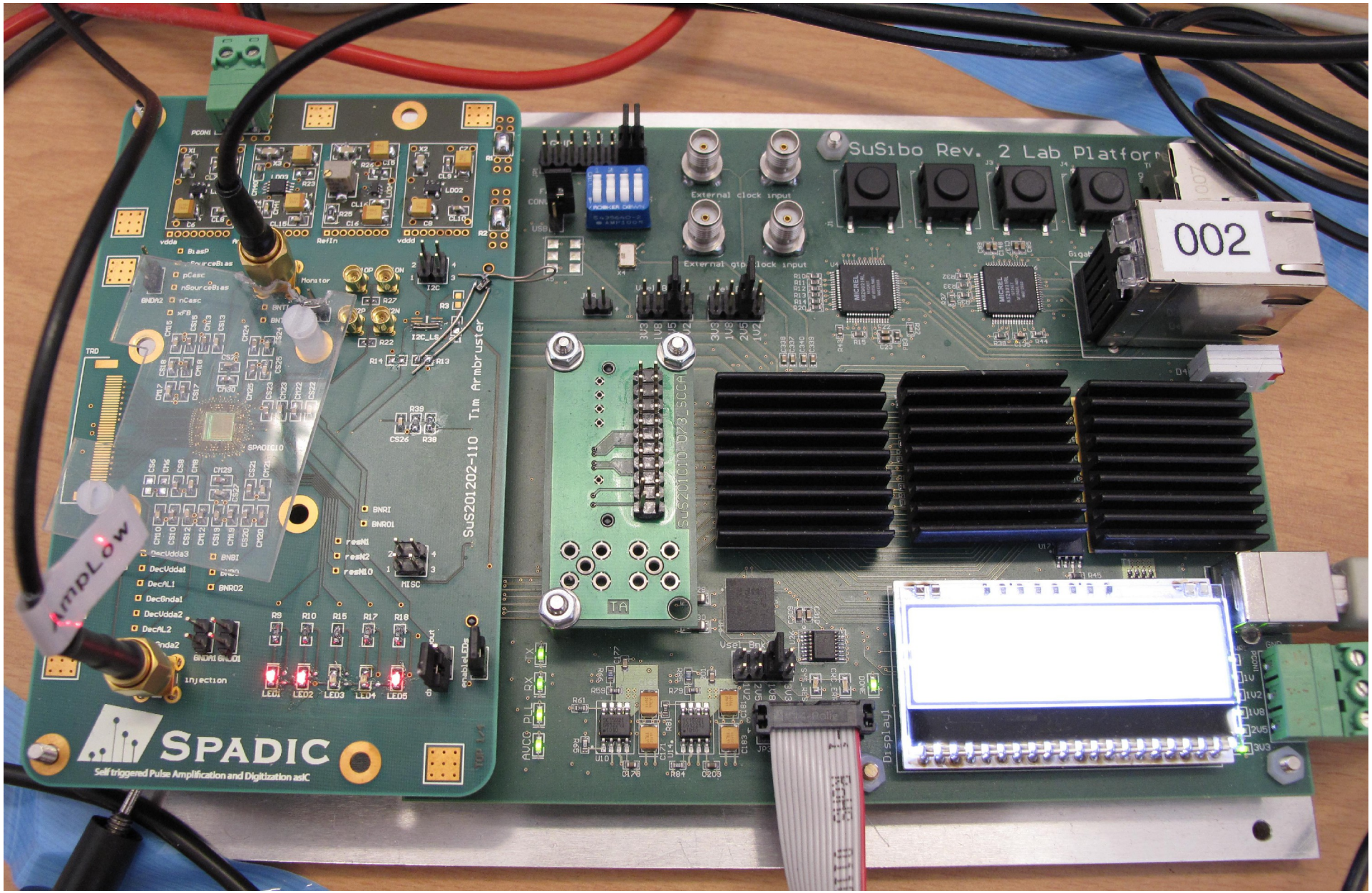


Layout



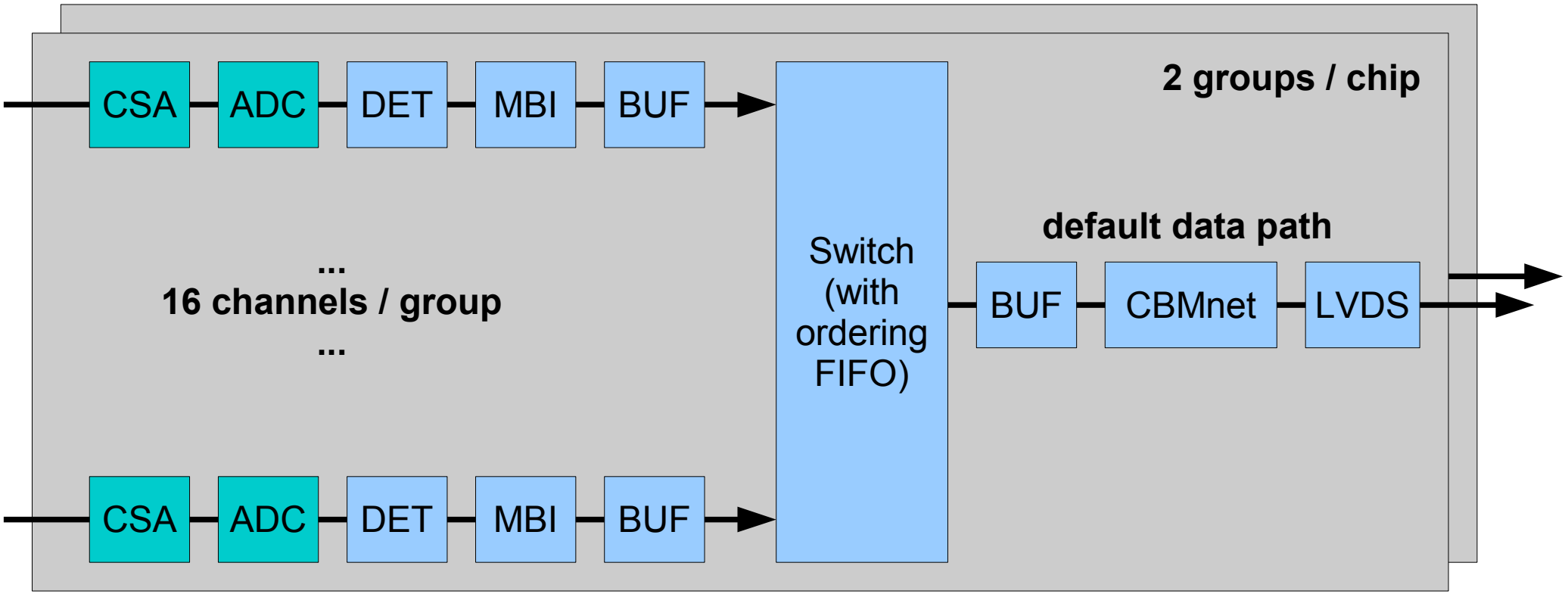
Photo

New Setup: Susibo 2.0 + 4 Layer PCB

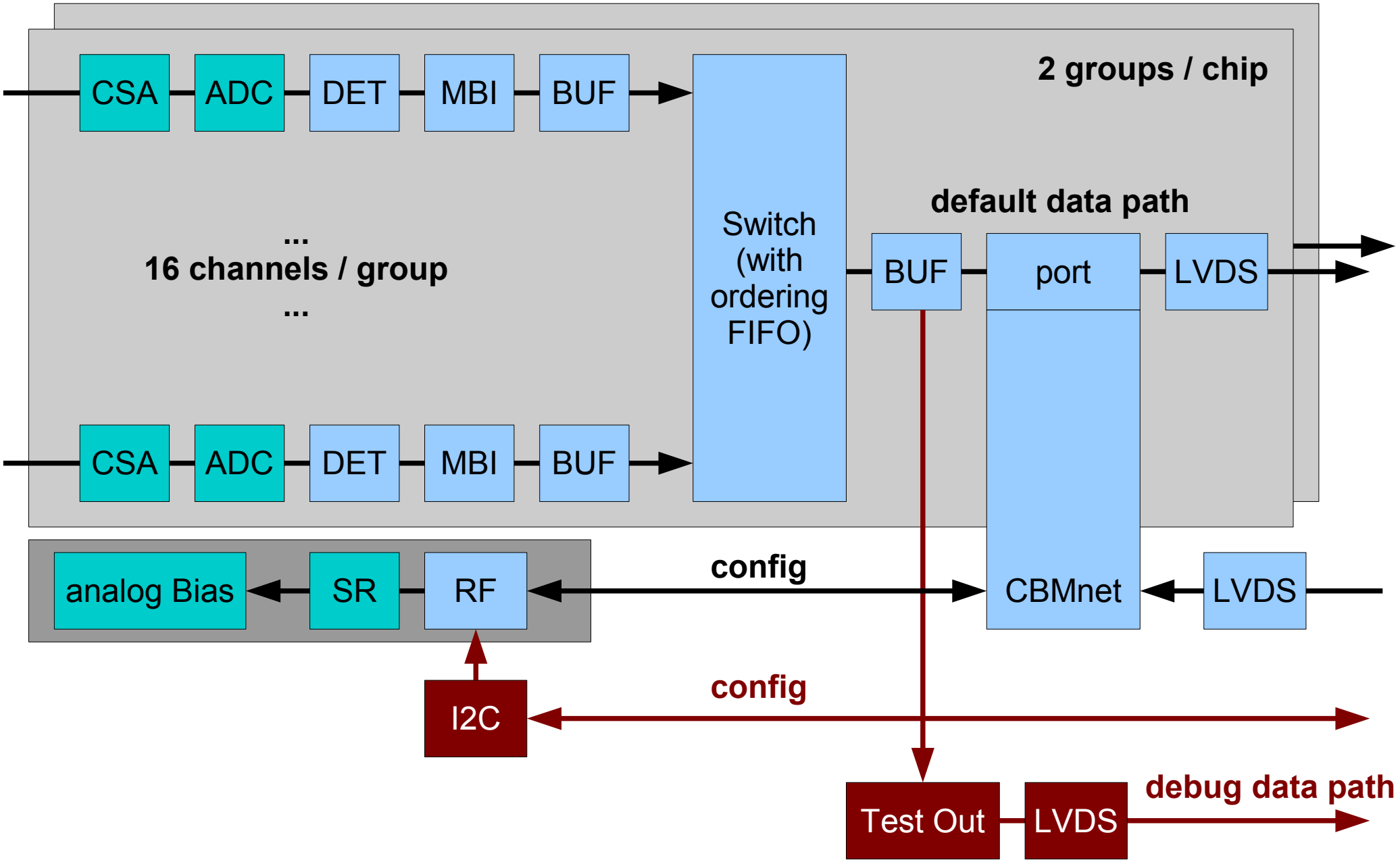


Reminder: SPADIC 1.0 Data Path

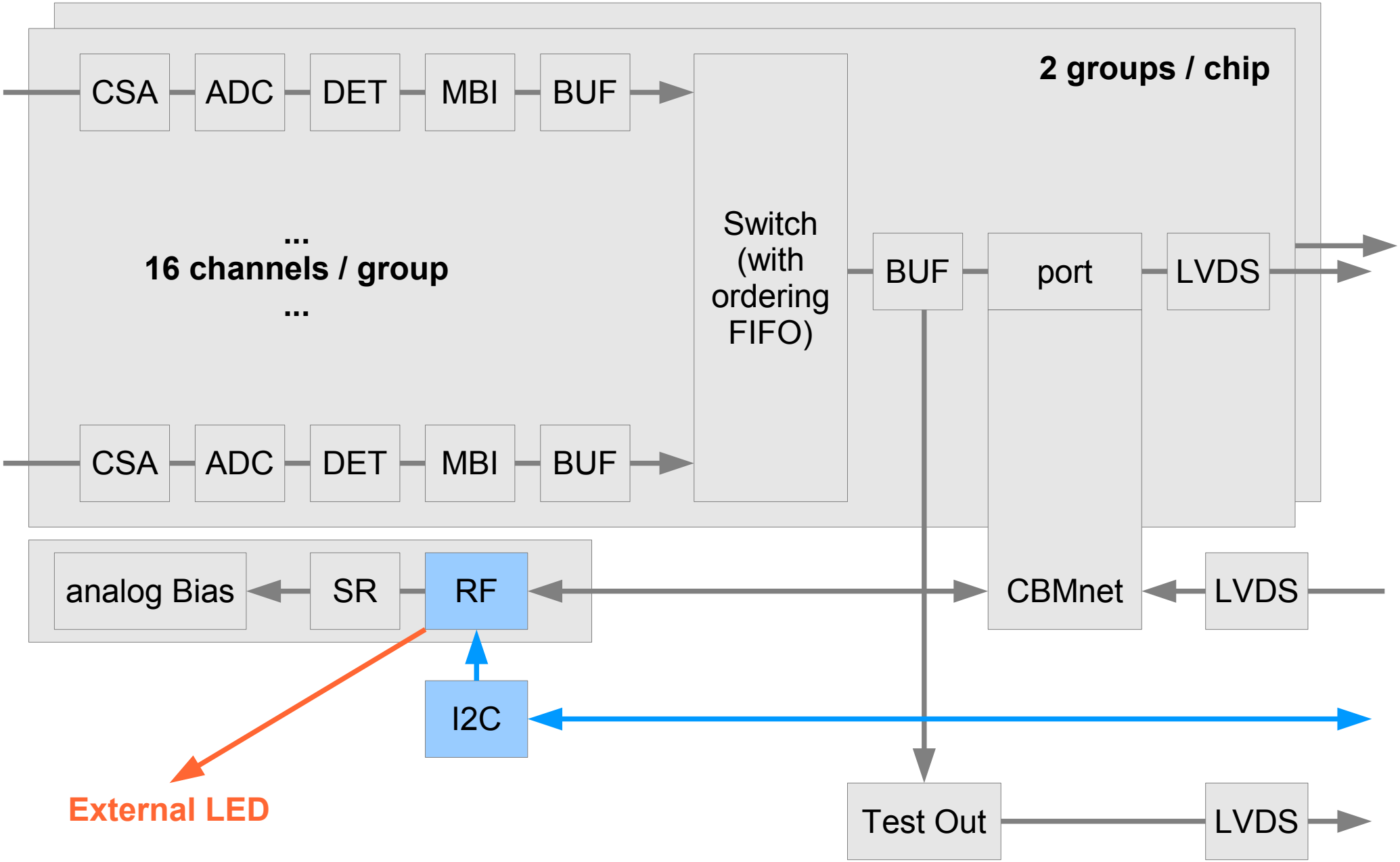
SPADIC: **S**elf-triggered **P**ulse **A**mplification and **D**igitization as**IC**



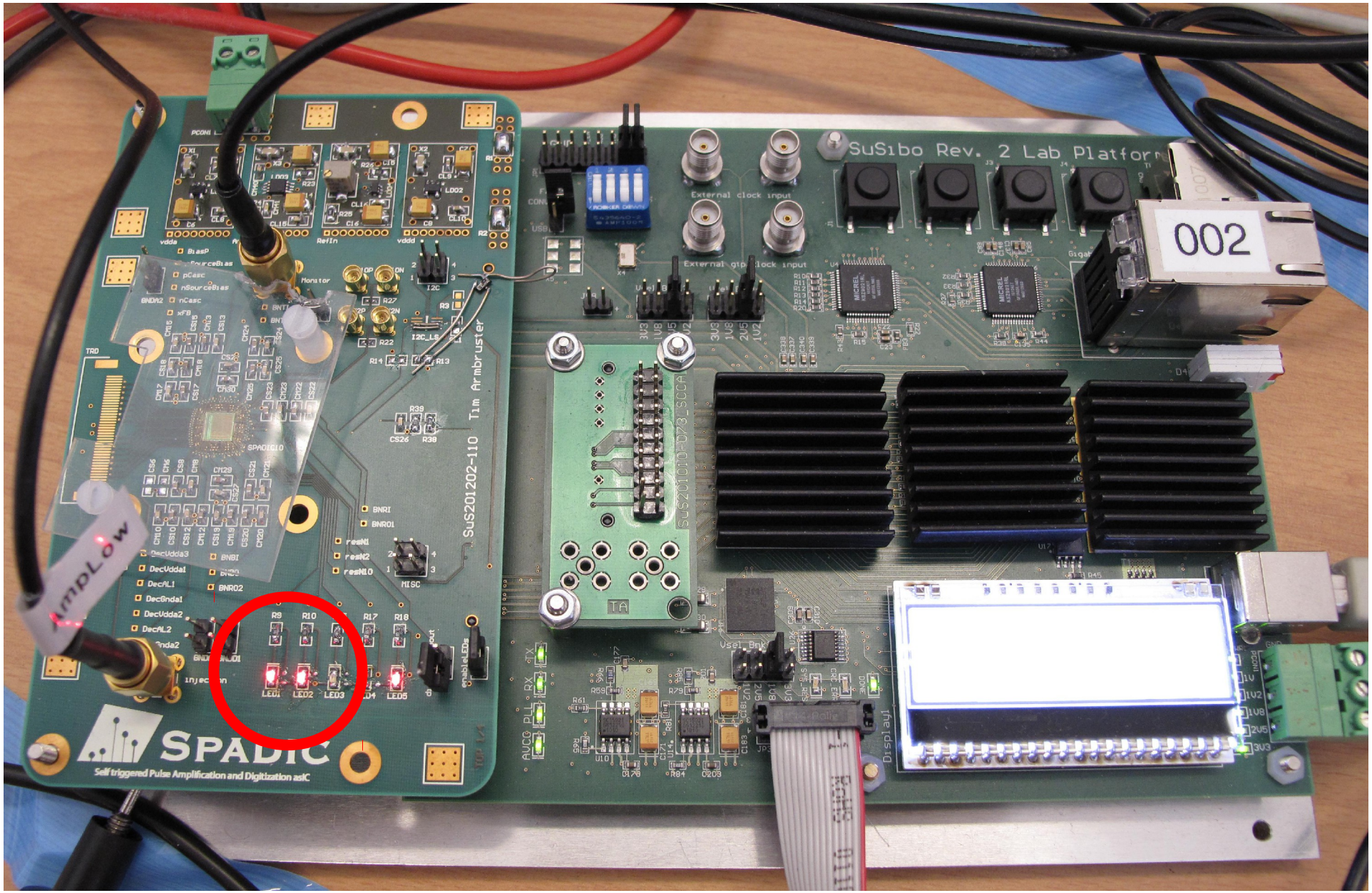
Status: CBMnet not ready yet → fall-back readout



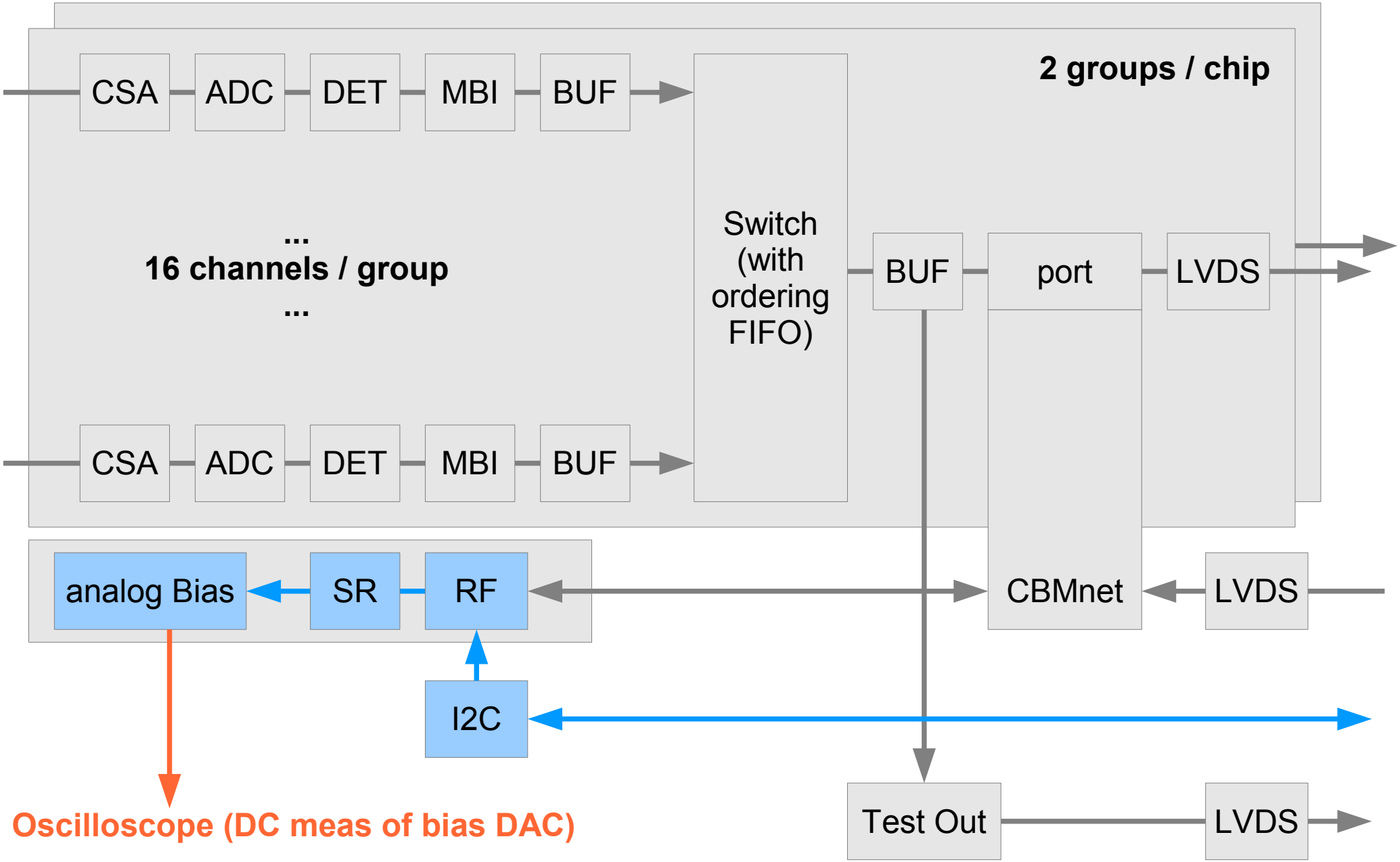
Test 1: Write Register of RF



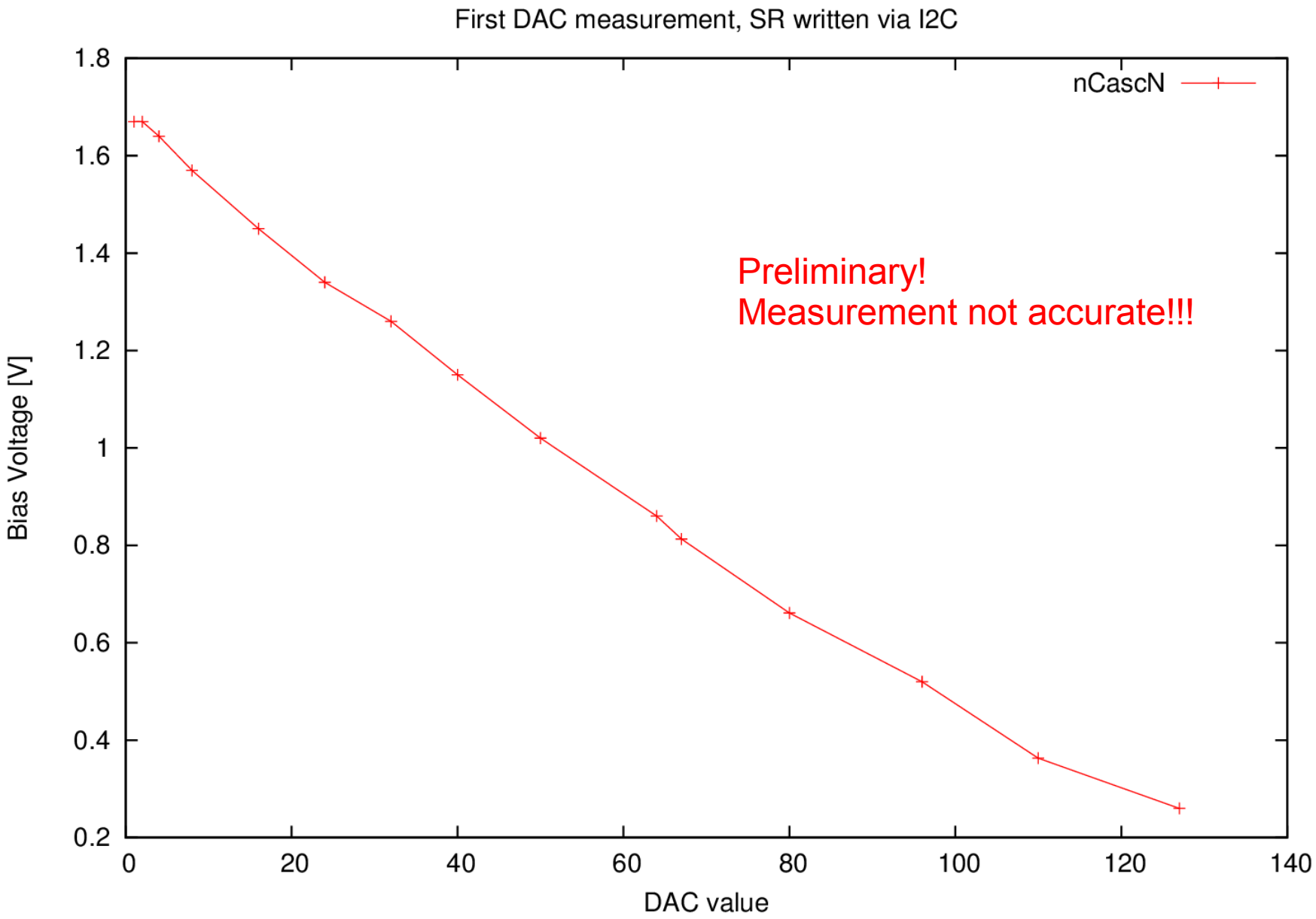
Test 1: Write Register of RF (connected to LED)



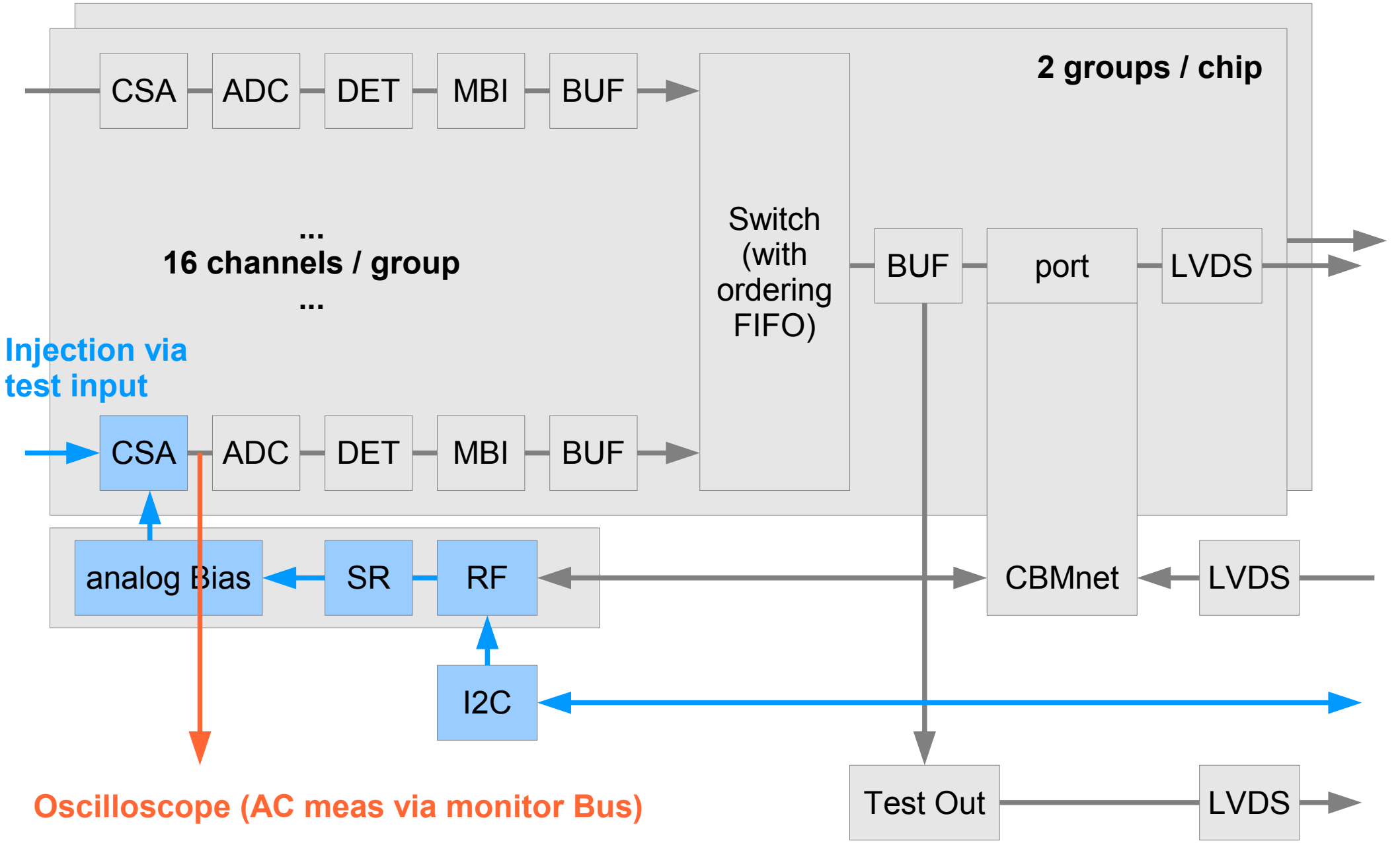
Test 2: Write analog SR → set some DAC value



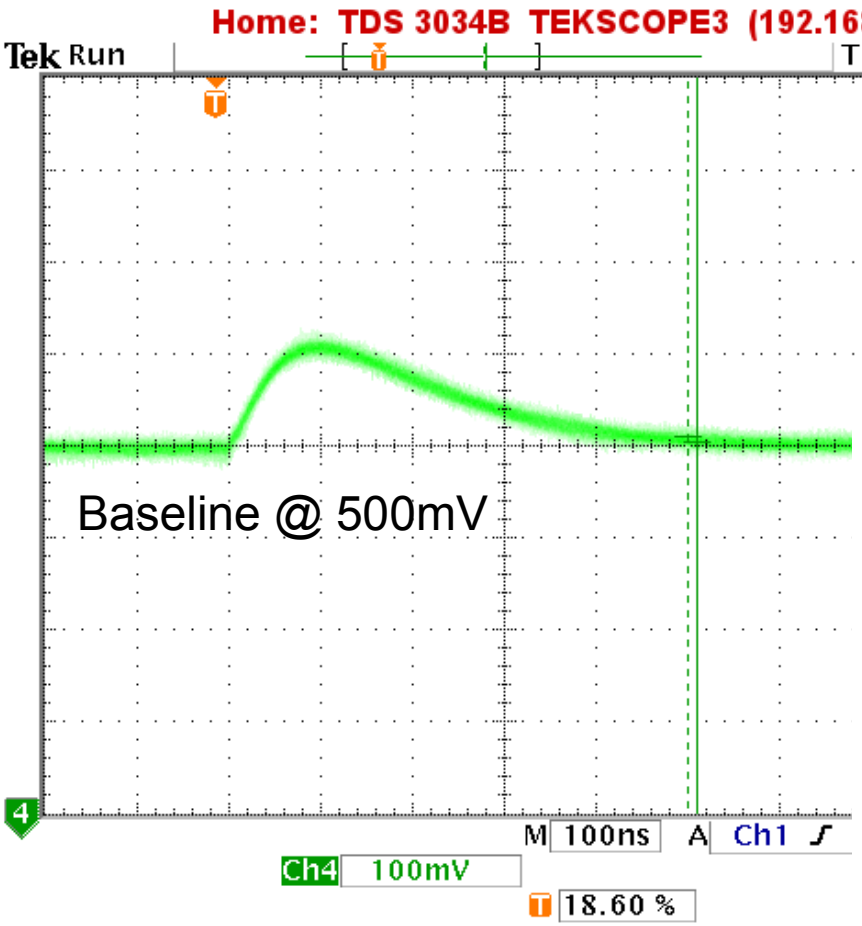
Test 2: DAC transfer characteristics

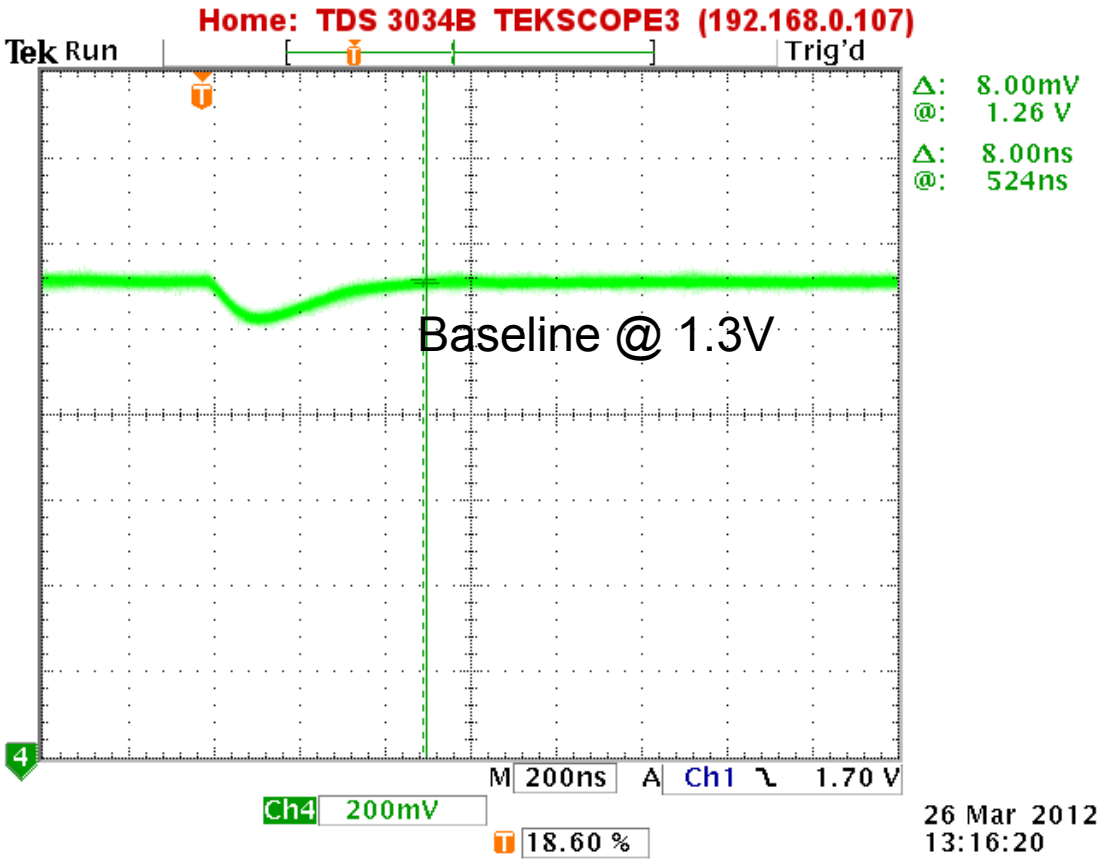


Test 3: Run CSA (pos + neg)



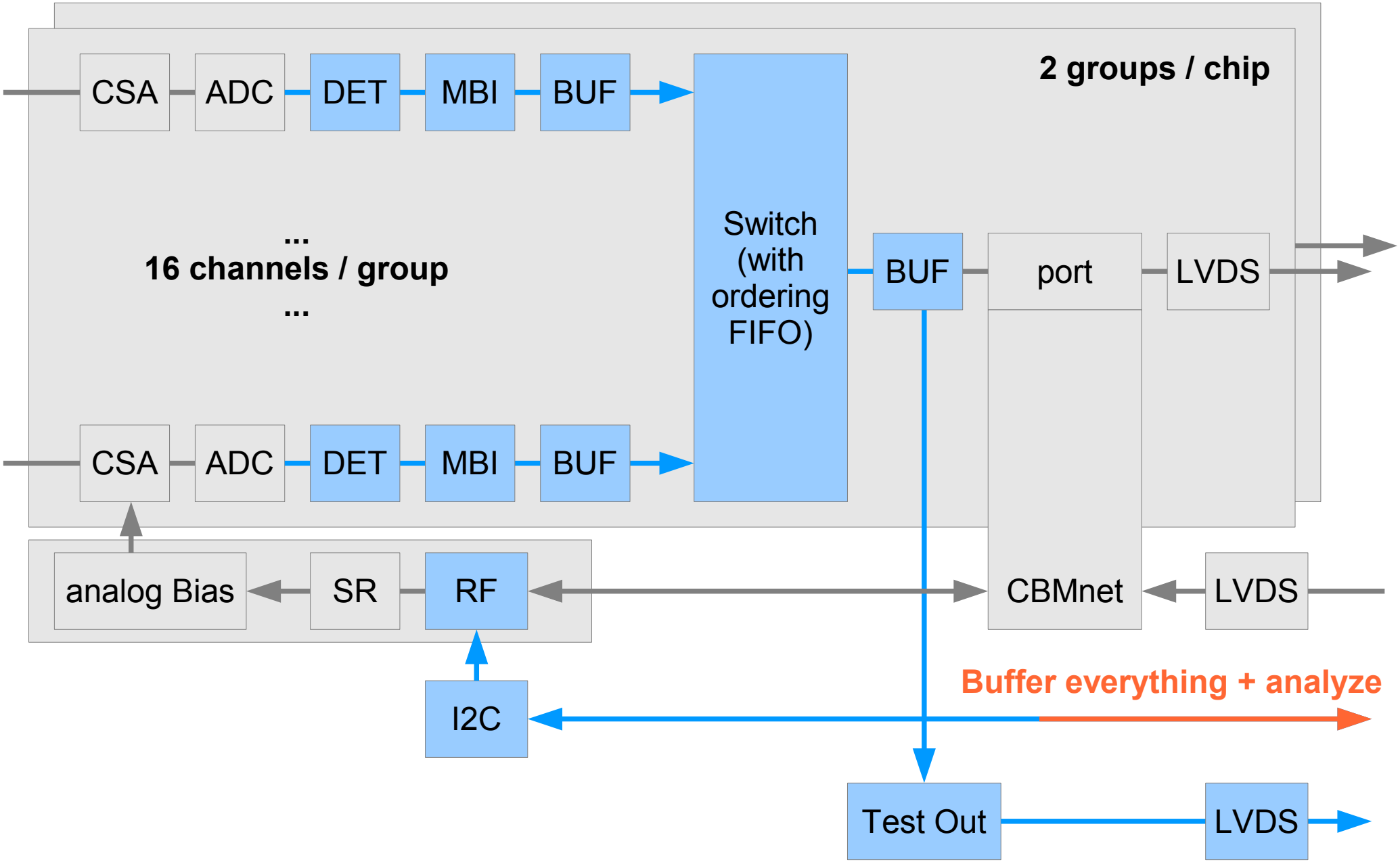
Test 3: CSA



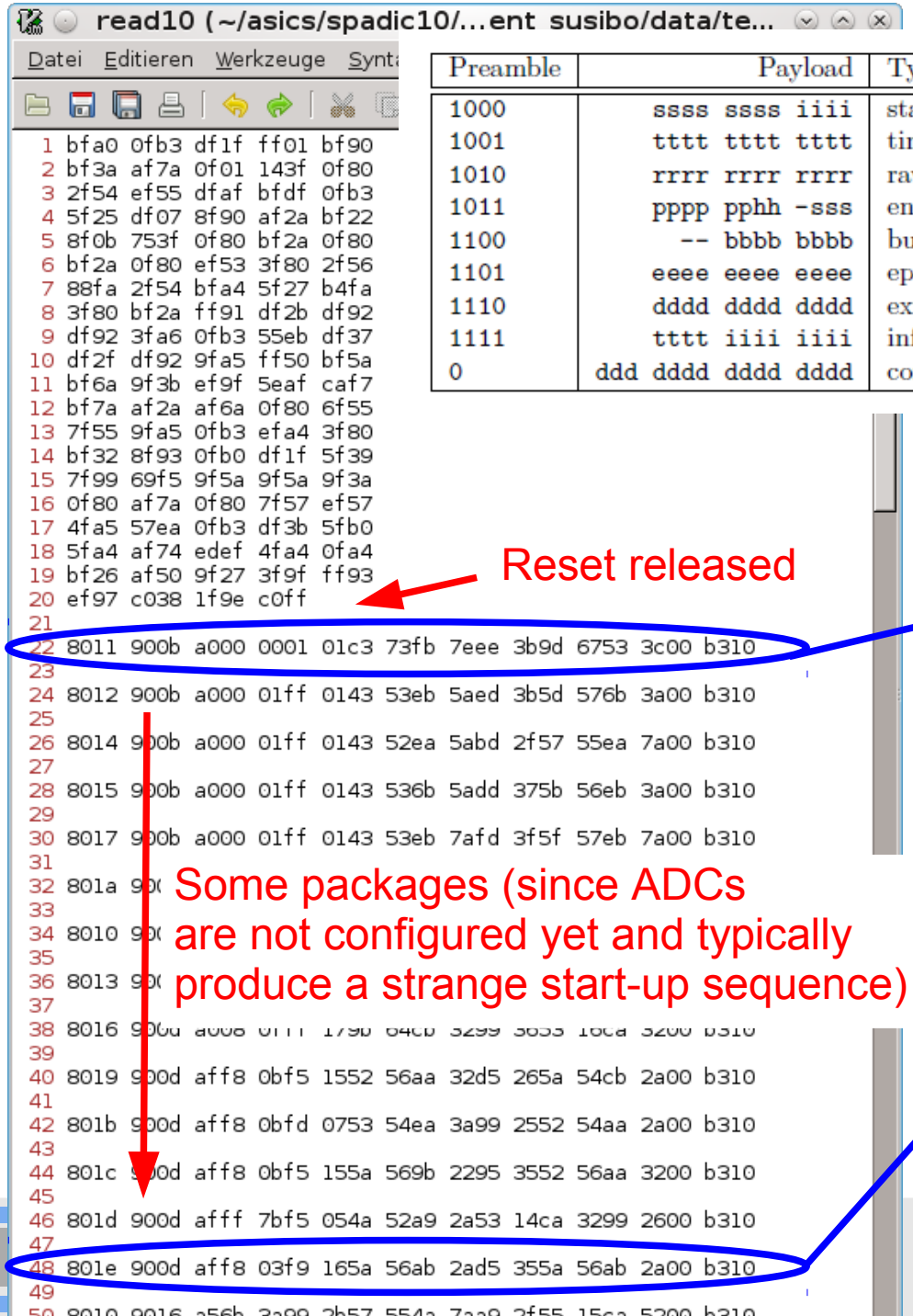


Preliminary!
Measurement not accurate!!!
Via monitor bus only!
Bias not optimal!

Test 4: Read-out everything DIRECTLY after releasing reset



Test 4: “Read Initial Trash”



Preamble	Payload	Type	Description
1000	ssss ssss iiii	start data message	s: 8 bit group-id, i: 4 bit channel-id
1001	tttt tttt tttt	time-stamp	t: 12 bit time-stamp
1010	rrrr rrrr rrrr	raw data	r: 12 bit raw data
1011	pppp pphh -sss	end of data message[1]	p: 6 bit data values, h: 2 bit hit-type, s: 3 bit stop-type
1100	-- bbbb bbbb	buffer overflow[1]	b: 8 bit lost hits
1101	eeee eeee eeee	epoch marker[1]	e: 12 bit epoch
1110	dddd dddd dddd	extracted data	d: 12 bit extracted data
1111	tttt iiii iiii	information[1]	t: 4 bit info-type, i: 8 bit depends on info-type
0	ddd dddd dddd dddd	continuation	d: 15 bit continued (meta/raw) data

Reset released

Some packages (since ADCs are not configured yet and typically produce a strange start-up sequence)

e.g.:

“Normal Message” of channel 17:
Time-Stamp 11 (440ns after reset)
12 x 9 bit raw data (yet random)
Internally triggered, normal stop

or

“Normal Message” of channel 30
Time-Stamp 13 (520ns after reset)
12 x 9 bit raw data (yet random)
Internally triggered, normal stop

Test1 ... Test4 => Promising results!

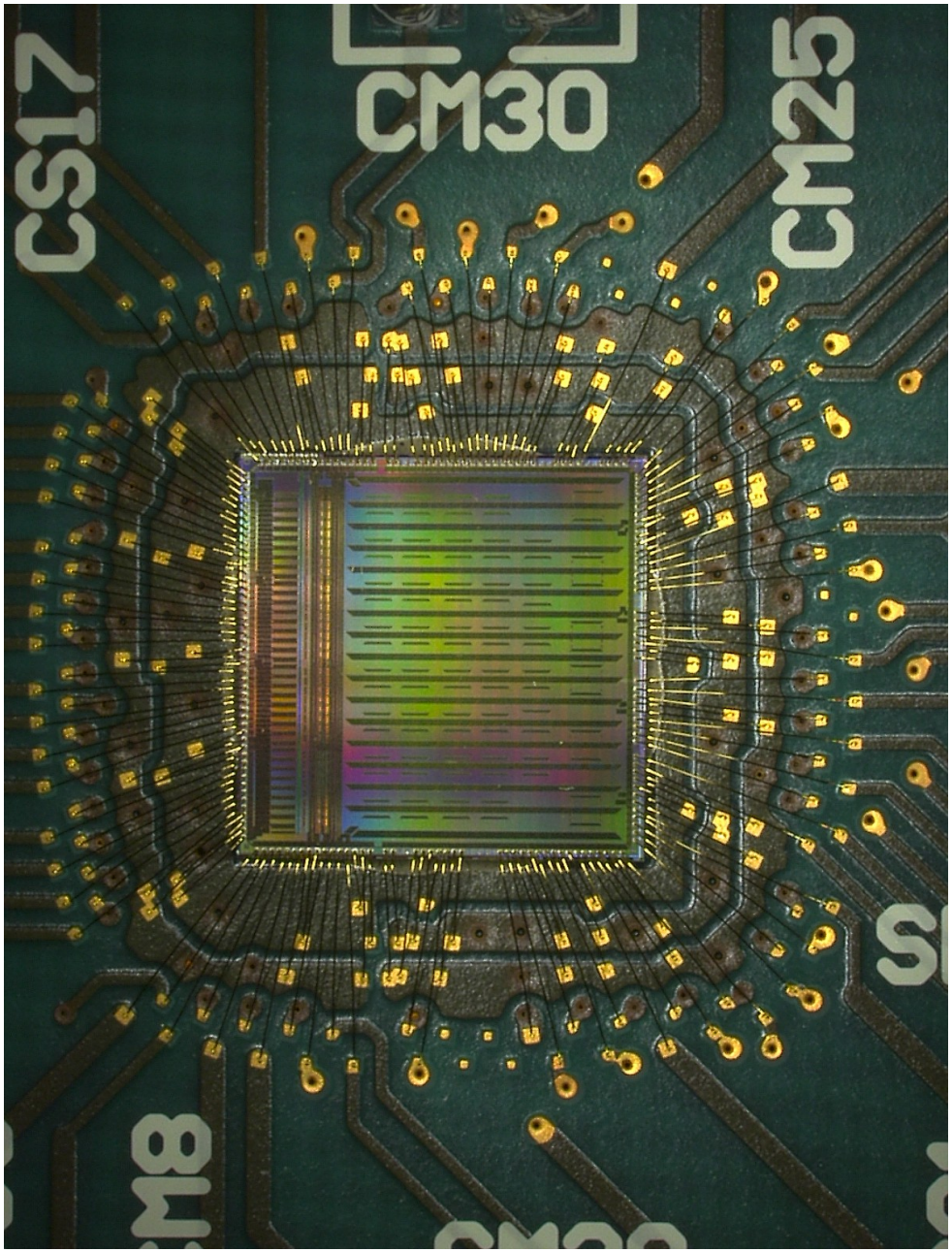
Some milestones reached:
- Digital part can already be clocked and reset @ 200MHz
- I2C core works (little bug in I2C pad, but workaround found)
- RF works
- Tricky chain RF → SR in analog part works
- Analog CSA (both polarities) work
- FIFO (unknown SRAMs!!!) work
- Hit-Detection seems to work
- Message protocol seem to work

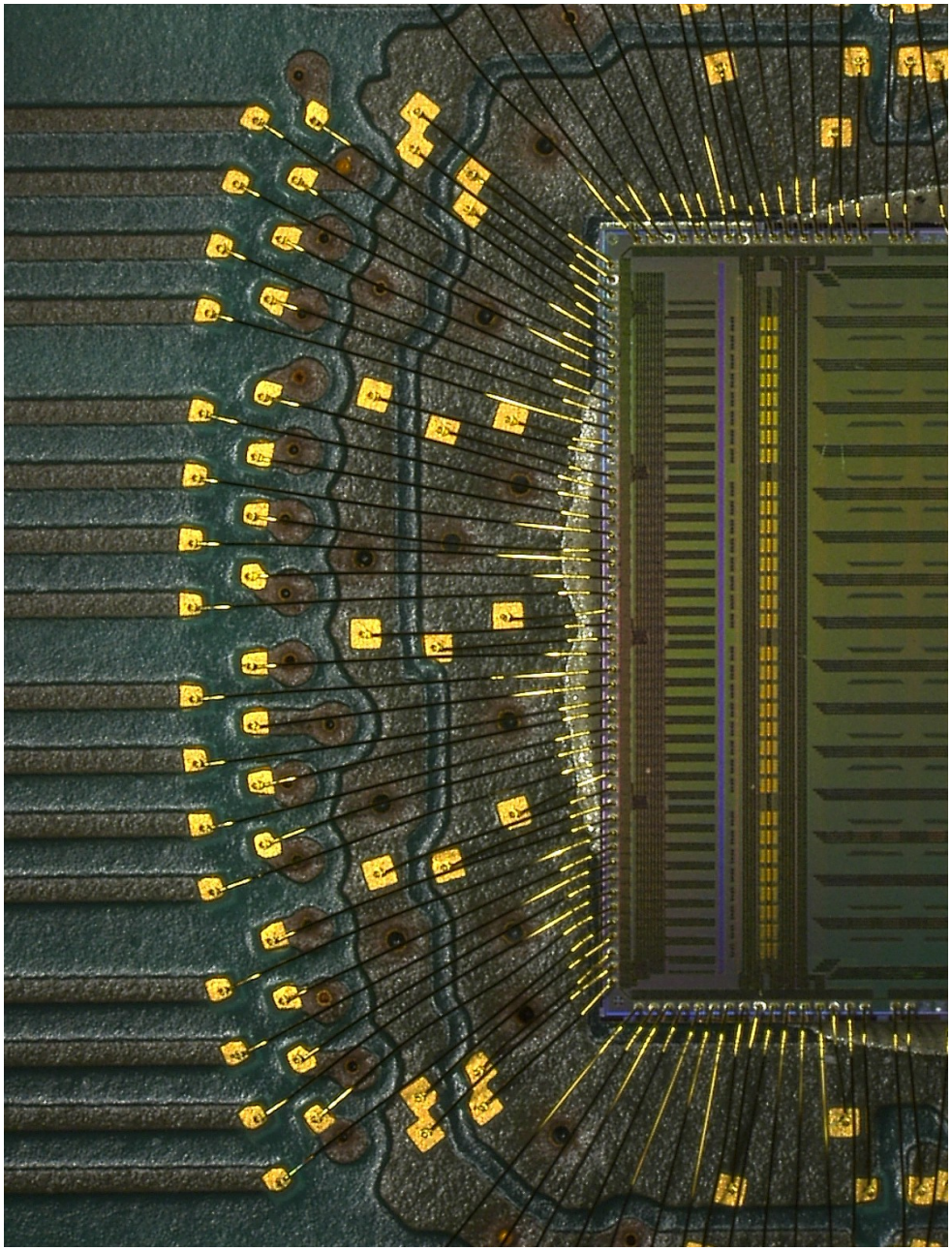
Next steps:
- improve readout software
- set bias voltages, start ADCs
- build CBMnet core for FPGA, test CBMnet link
- put everything together
- characterize everything
- ...

Very promising results → but yet <u>no final conclusion</u> possible:

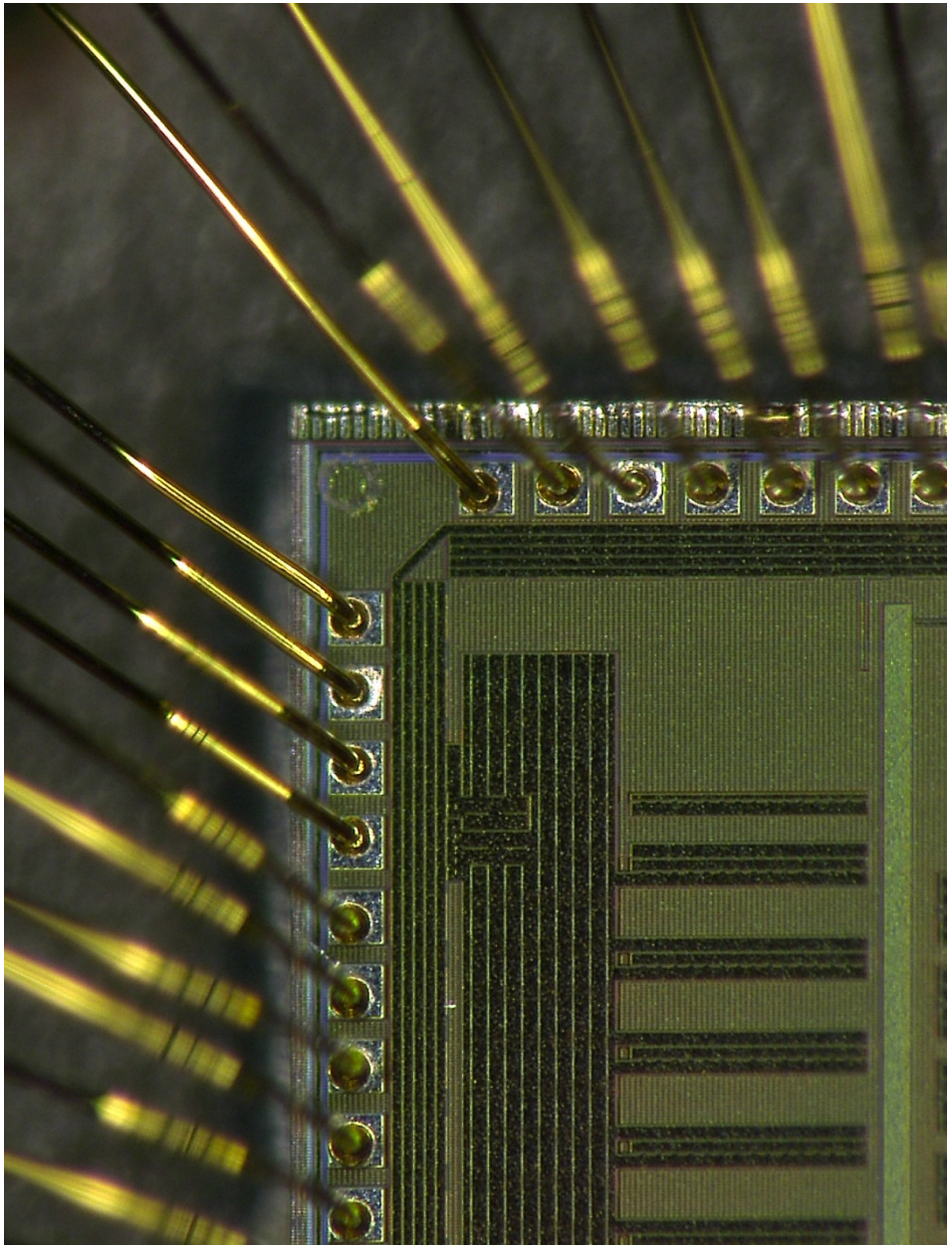
Status: "SPADIC 1.0 {works; works not}"

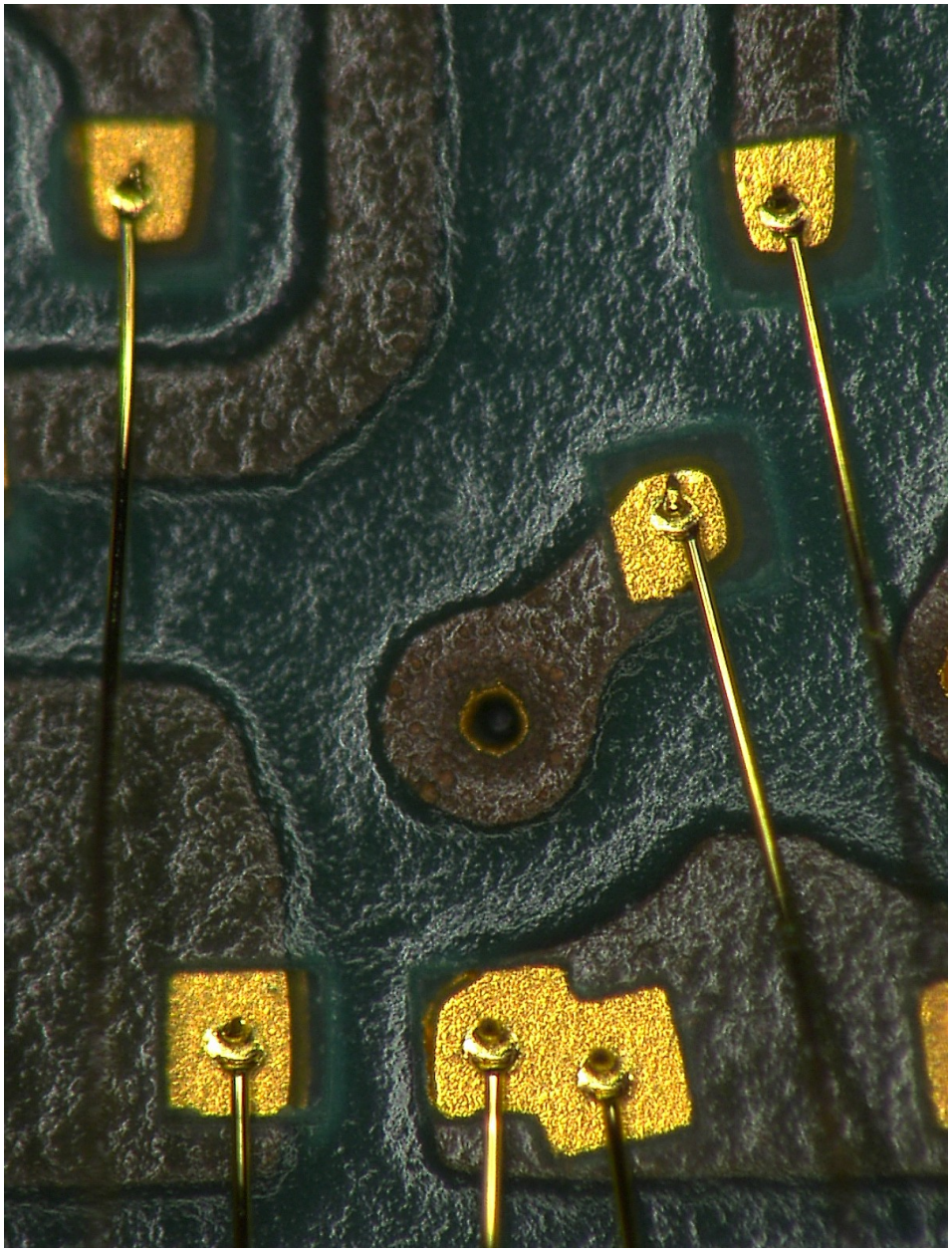
Some Impressions (1/3)



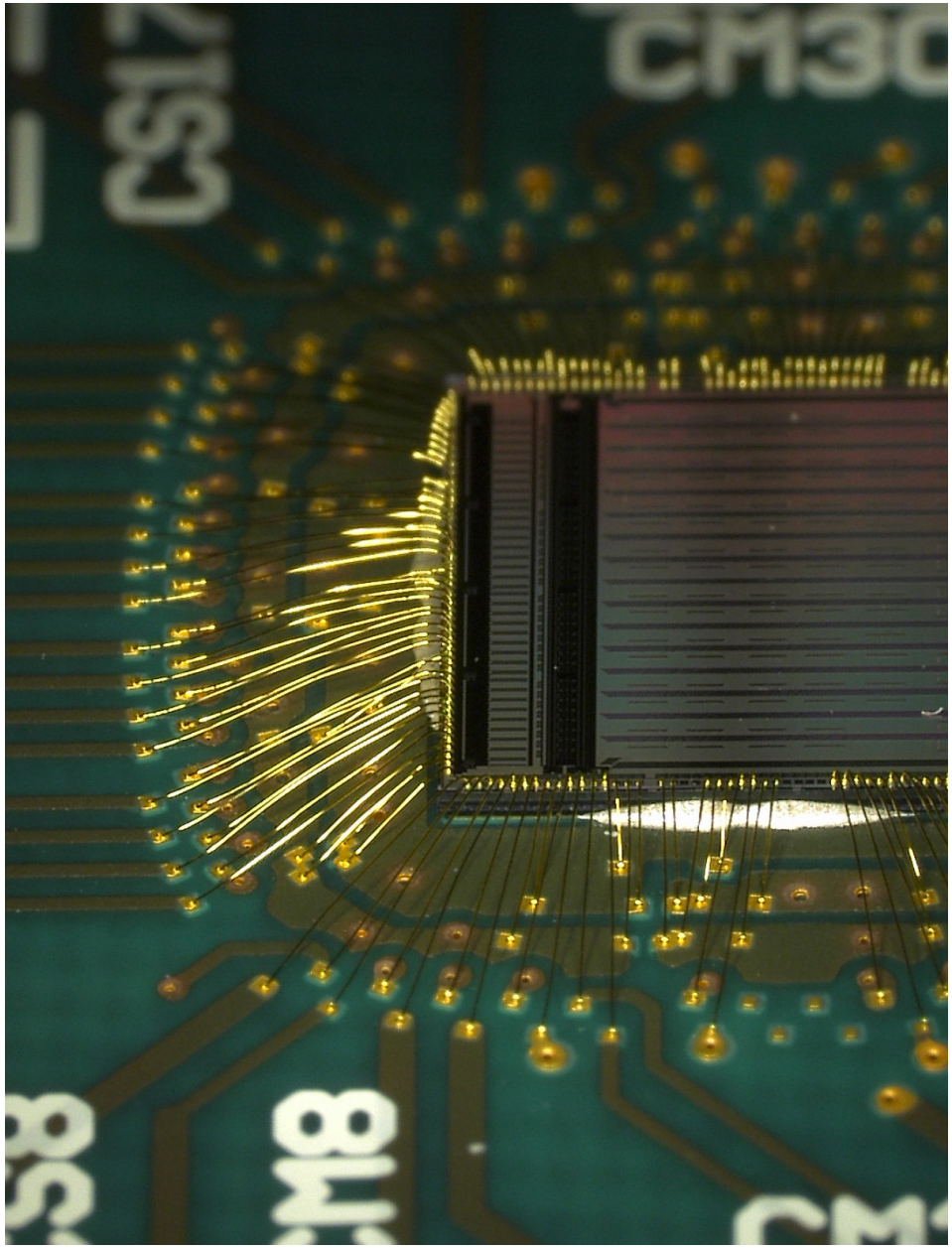


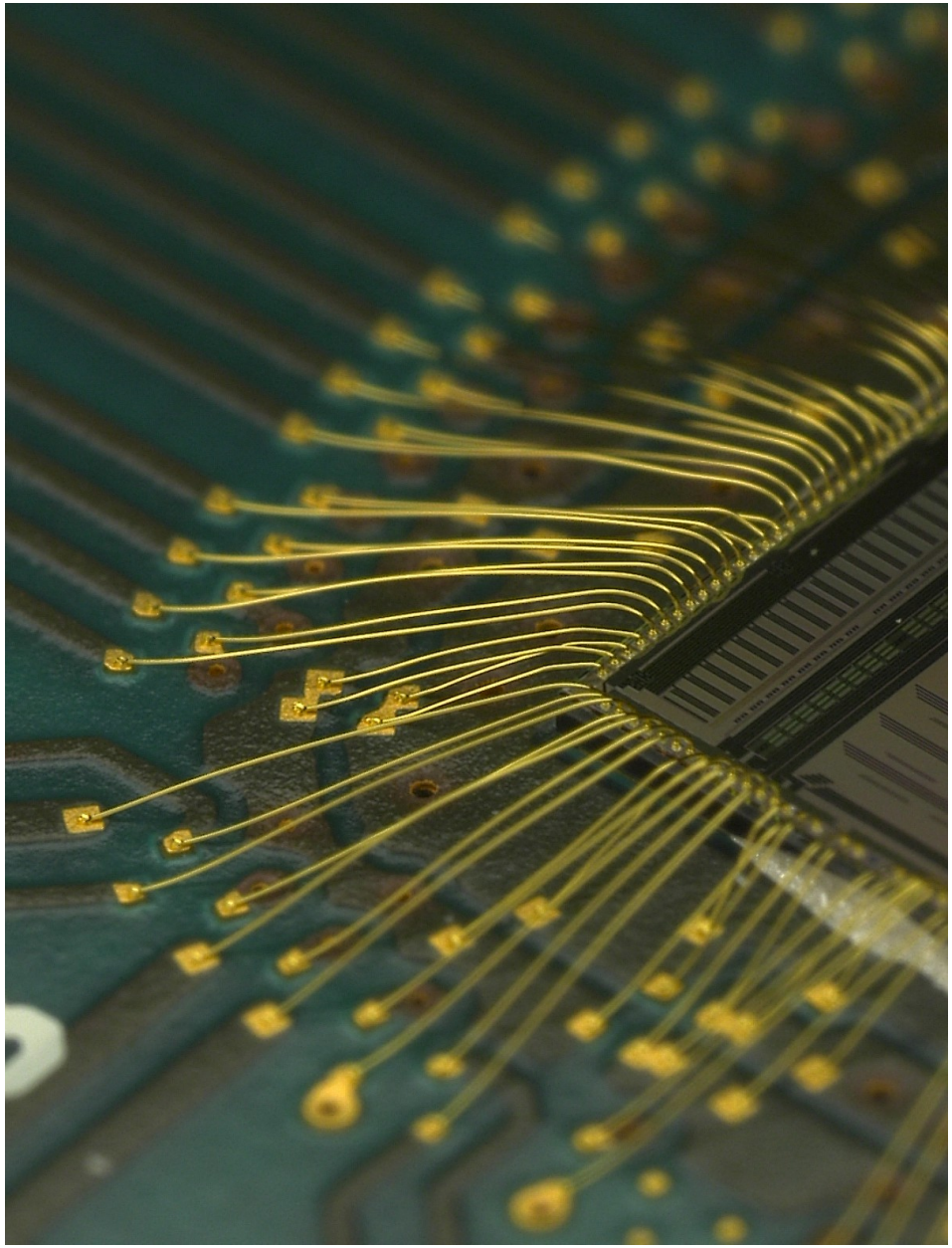
Some Impressions (2/3)

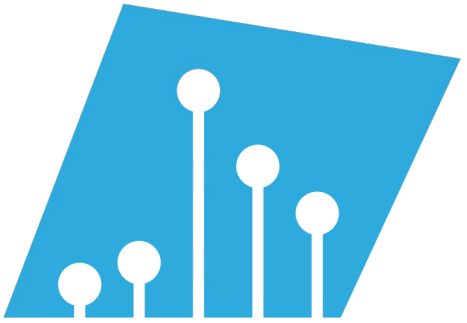




Some Impressions (3/3)







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