UNIVERSITÄT HEIDELBERG

SPADIC
Self triggered Pulse Amplification and Digitization asIC

Status of SPADIC 1.0

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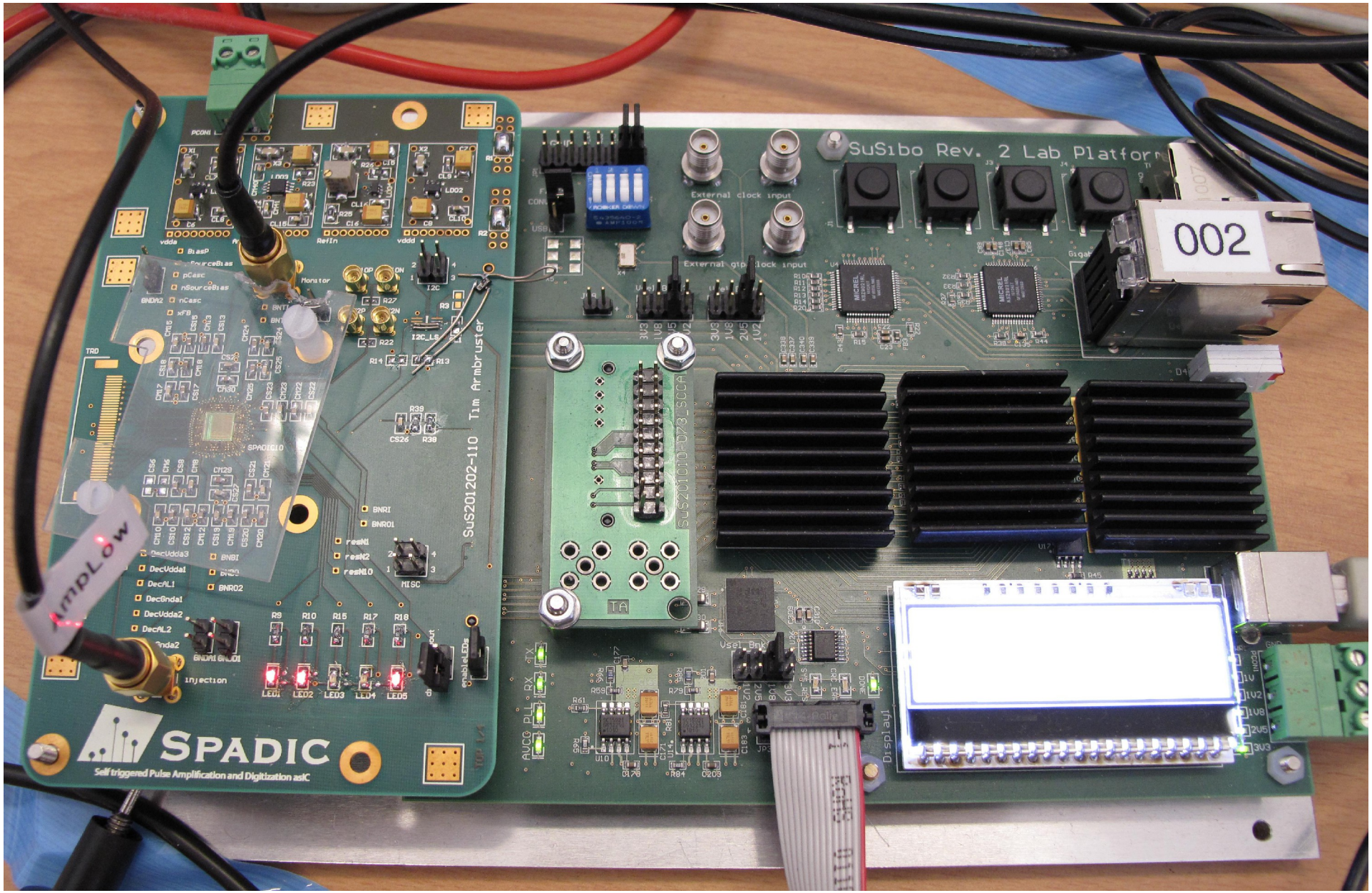
CBM DAQ Meeting GSI

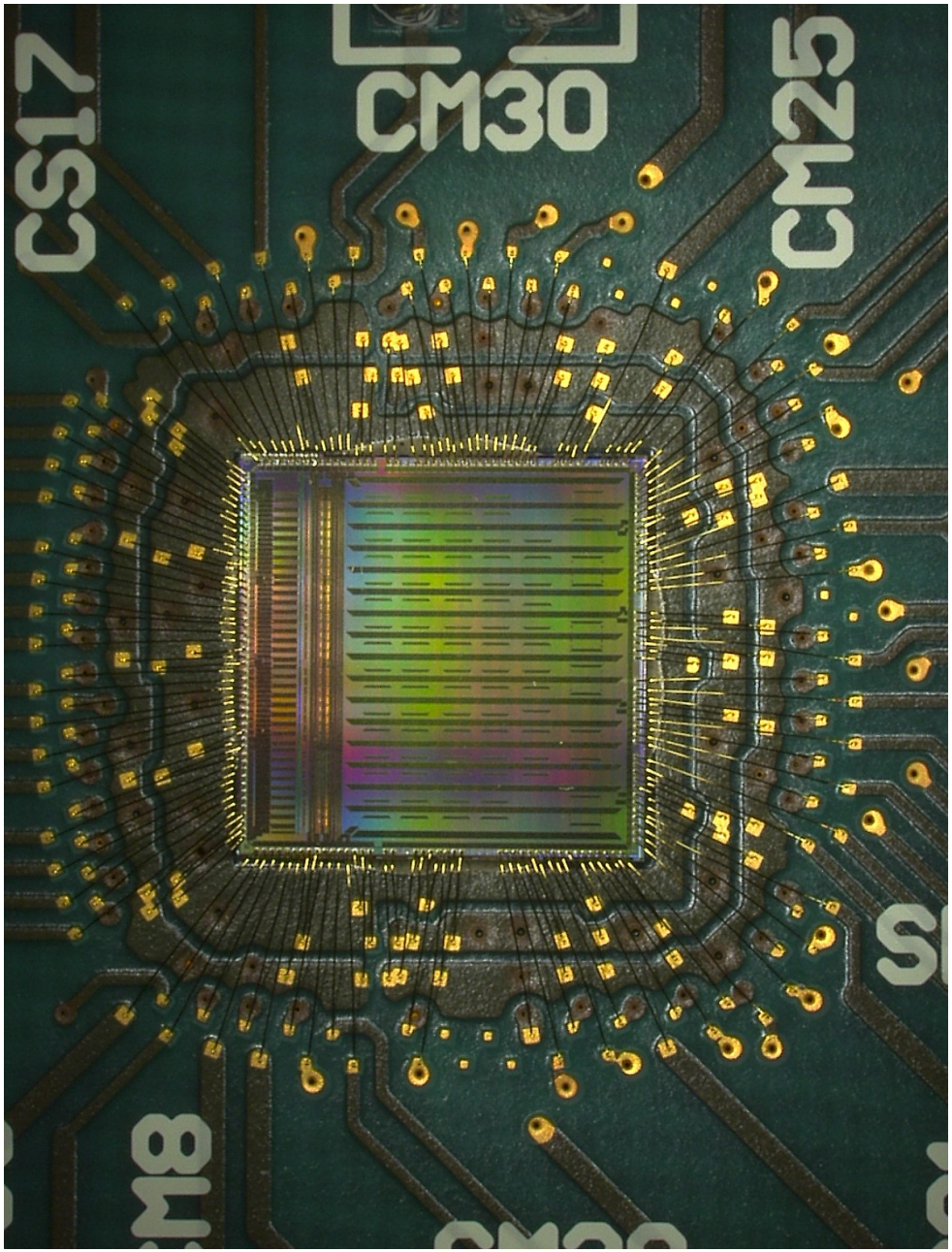
May 2012

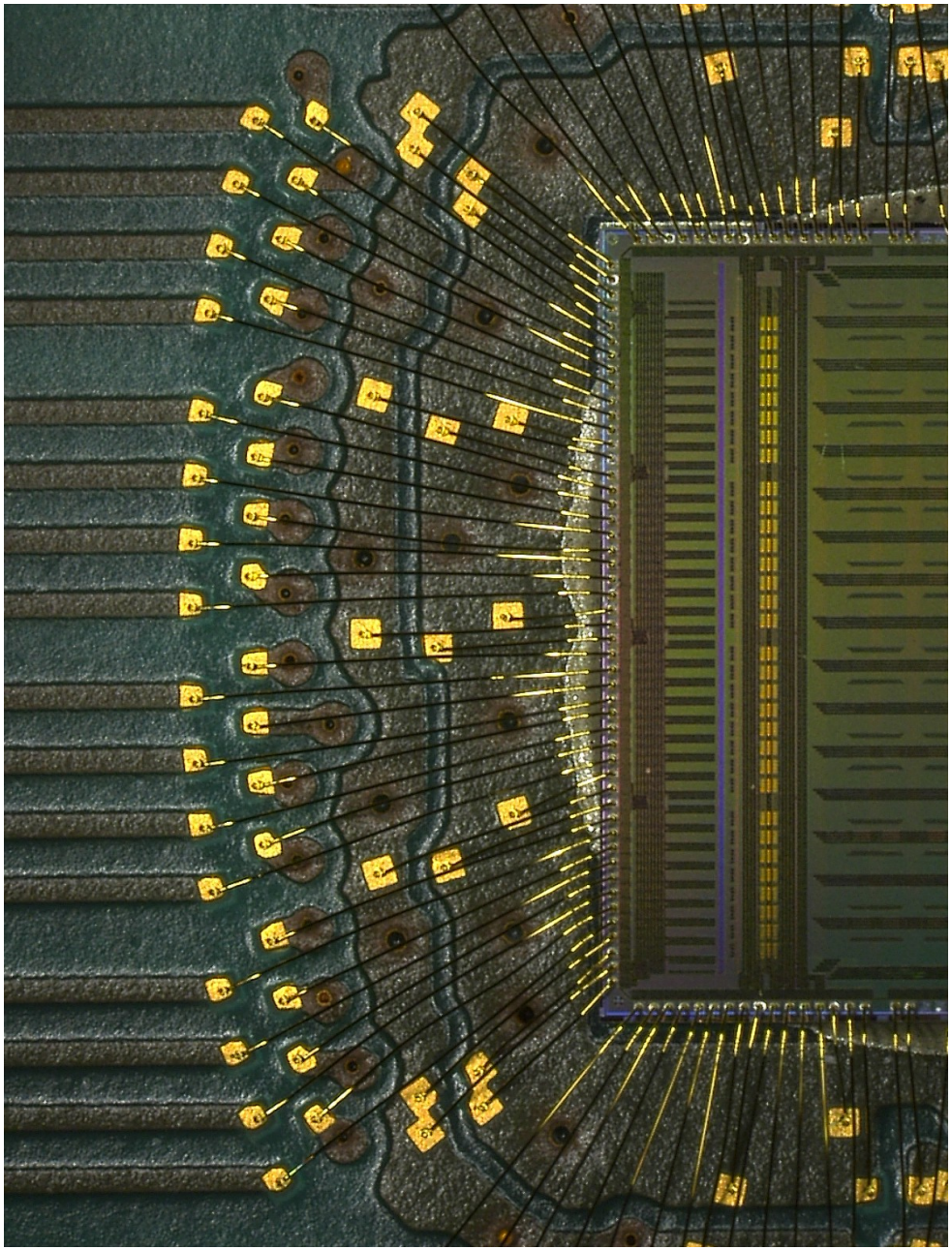
Visit http://www.spadic.uni-hd.de

1st SPADIC 1.0 Setup: Susibo 2.0 + 4 Layer PCB



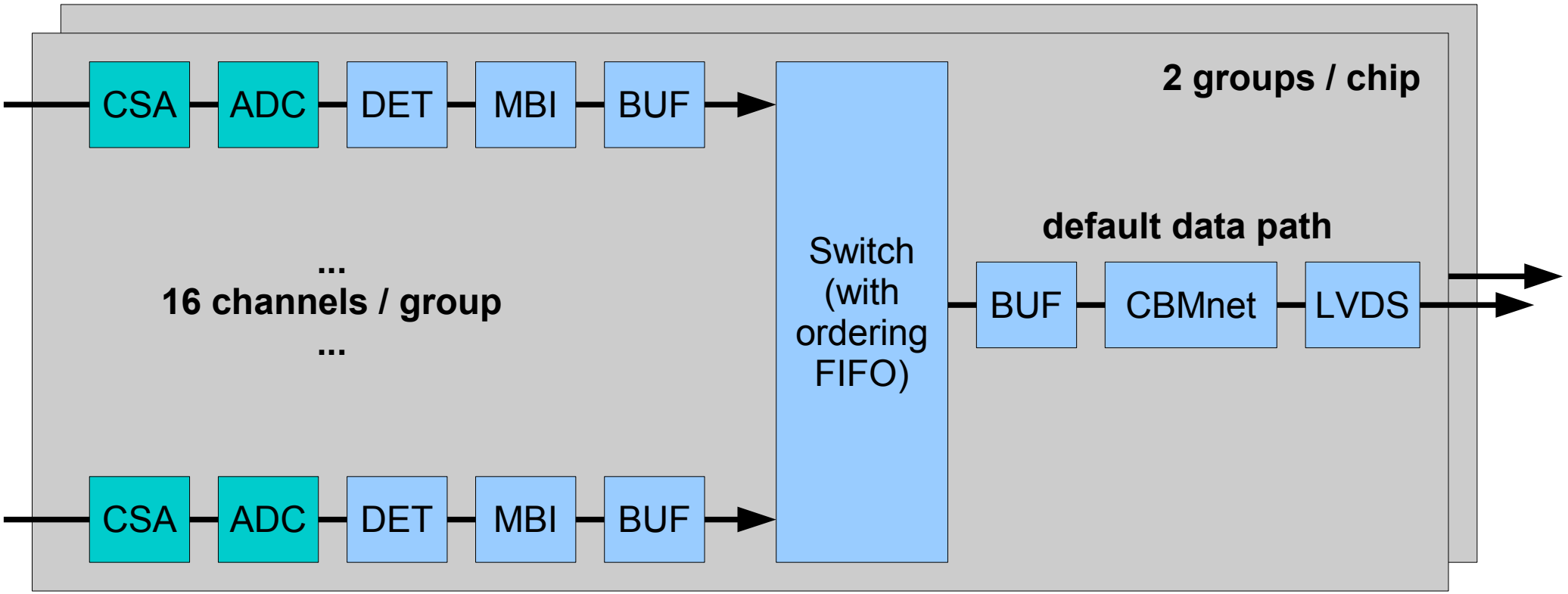
Some Impressions



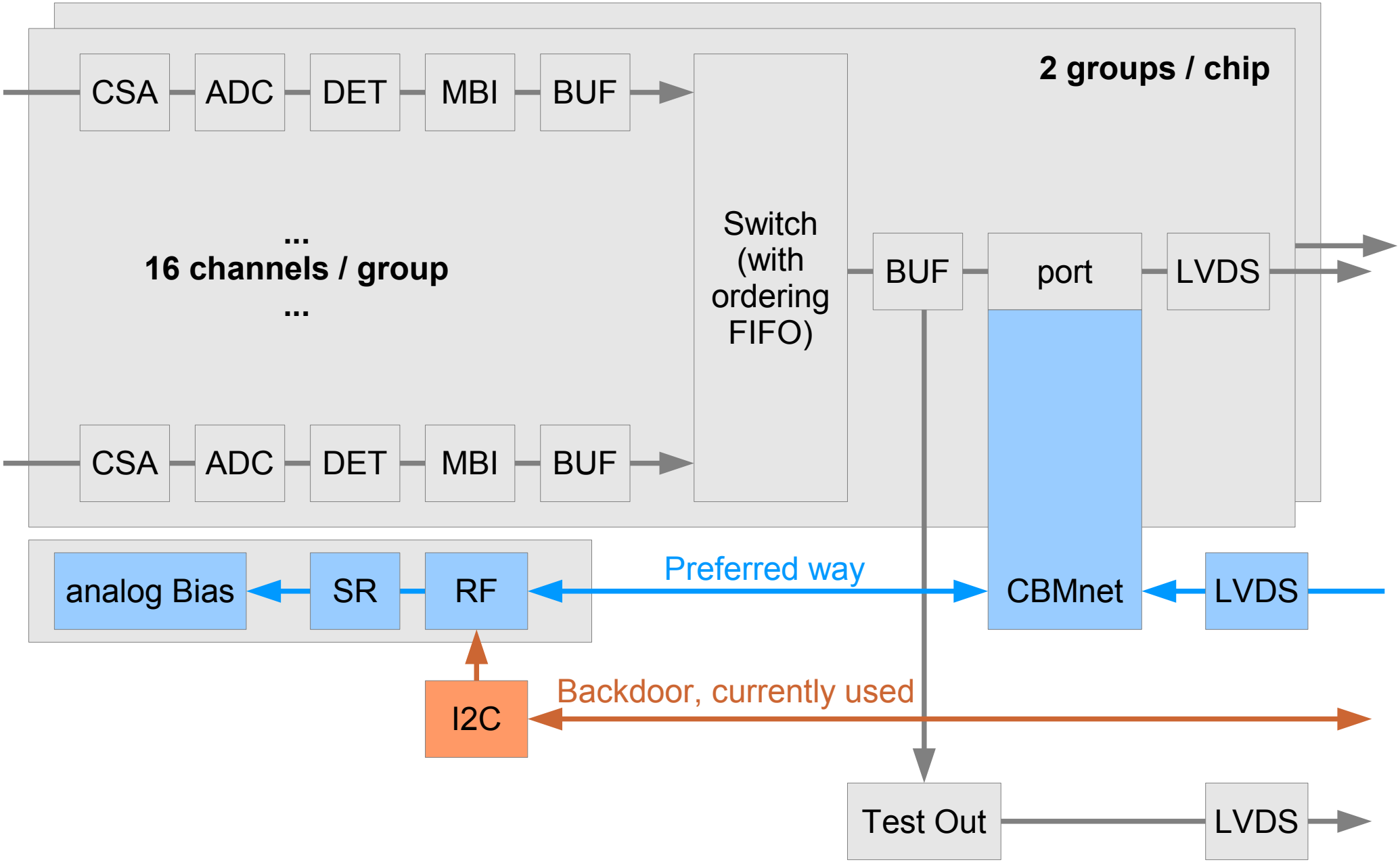


Reminder: SPADIC 1.0 Data Path

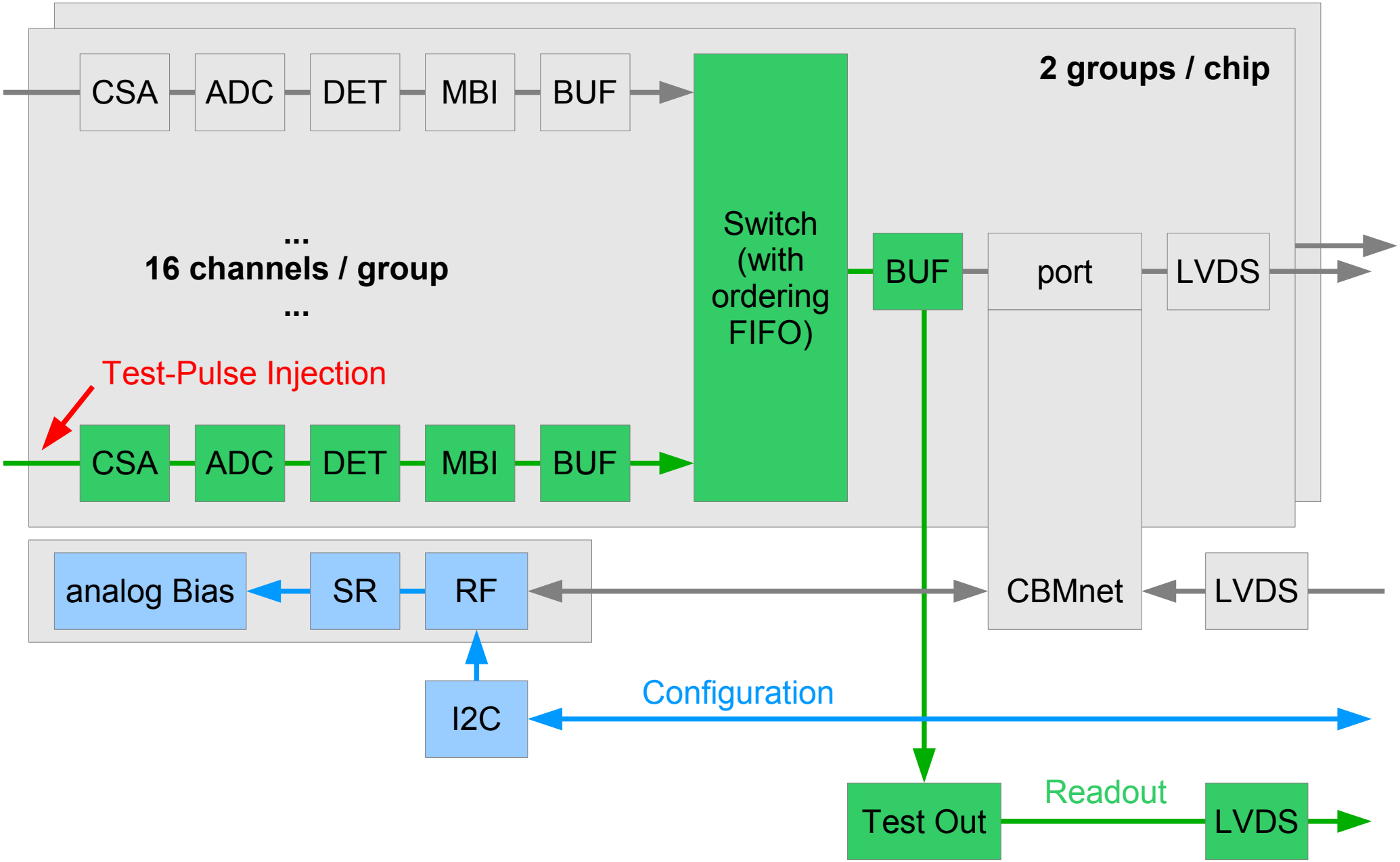
SPADIC: **S**elf-triggered **P**ulse **A**mplification and **D**igitization as**IC**



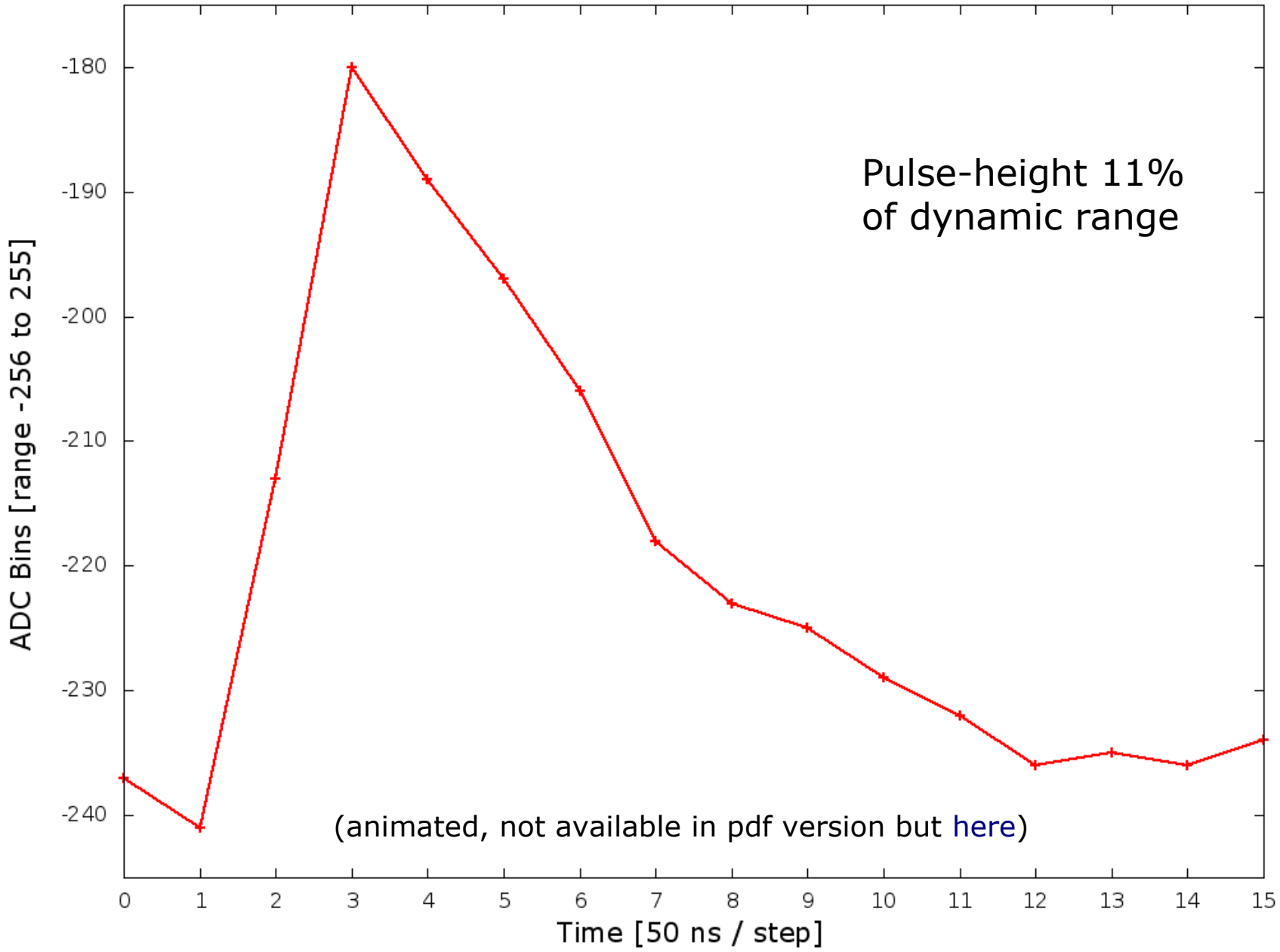
Writing the Configuration ...



First SPADIC Hits: Using Analog Test Injection



First SPADIC 1.0 Hits



Next PCB Iteration

Long Todo-List:

- I2C patch, with jumper to disconnect transistor
- LDO enable pins (think about proper way how to connect grounds)
- new LDOs
  - digital: more current, new footprint (e.g. NCV8570B) >= 300mA
  - new AmpLow LDO from e.g. 3V to 300mV (currently it's 5.5V to 300mV)
- LVDS impedance control not important -> cheaper and thicker PCB
- think about fuse (not so important)
- maybe add-on carrier board for ASIC (proper connector important)
- remove MMCX
- newer bonding diagram, maybe buried vias
- second power connector (optional) for digital part
- add one or two LEDS that can be controlled via FPGA
- think about LVDS AC coupling
- add HDMI type1 connector -> CBMnet
- Lattice Ispac power up chip or equivalent (or analog ADM1184) …

Michael K. can start as soon as we know CBMnet is working @ full speed!

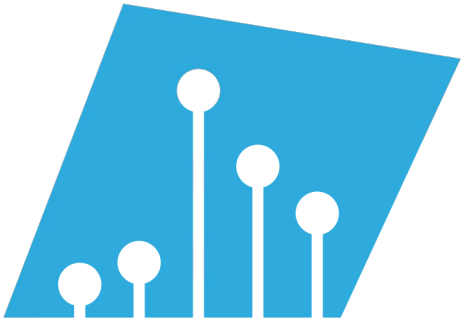
Open SPADIC 1.0 Tasks

Open SPADIC tasks for beam-time in October, incomplete (!) list:

- **Characterization of SPADIC 1.0** → Michael Krieger (+ myself)
- **Next SPADIC 1.0 PCB Iteration** → Michael Krieger (+ myself)
- **SPADIC 1.0 USB Library** → Michael Krieger (+ myself)
- **SPADIC 1.0 Documentation** → Michael Krieger (+ myself)
- **SPADIC 1.0 DAQ Library** → ???, can probably use most parts of USB Lib
- **CBMnet link to SPADIC testing** → Sven Schatral + Frank Lemke
- **CBMnet link characterization** → Sven Schatral + Frank Lemke
- **SPADIC 1.0 monitor + user software** → Cruz Garcia (+ Jano Gebelein?)
- **Integration to DAQ/DABC** → Sergey Linev + Jörn Adamczewski-Musch
- **Hardware chain FEE to "FLES"** → ???
- […]

Assembly:

- How many FEE boards / SPADIC 1.0 setups required?
  - Beam-Time
  - Test-Setup for the lab
- Who organizes the bonding?
- Who organizes the assembly (buy and solder components, testing)?



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