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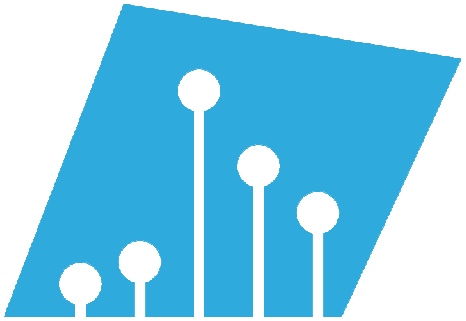


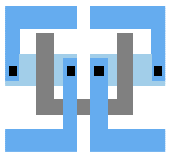
SPADIC 1.0

Self triggered Pulse Amplification and Digitization asIC

Multi-Channel Charge Pulse Amplification, Digitization and Processing ASIC for Detector Applications

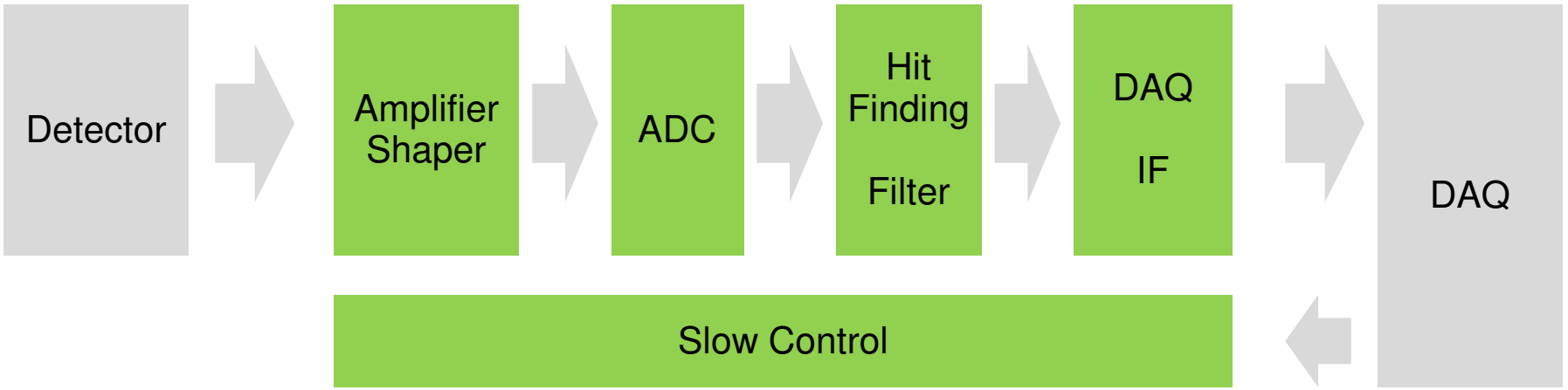
Peter Fischer
for
Tim Armbruster, Michael Krieger and Ivan Peric

Heidelberg University



Motivation

- Asynchronous detector applications need specialized readout
  - Auto detection of hits
  - Large data volume sent to online / offline processing
- Existing solutions (still) require several chips
- Want to connect the chip ‘directly’ to the DAQ network



- Main SPADIC Application: TRD of CBM @ FAIR @ GSI
- Other sub-detectors (RICH) are interested

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SPADIC 1.0 Overview

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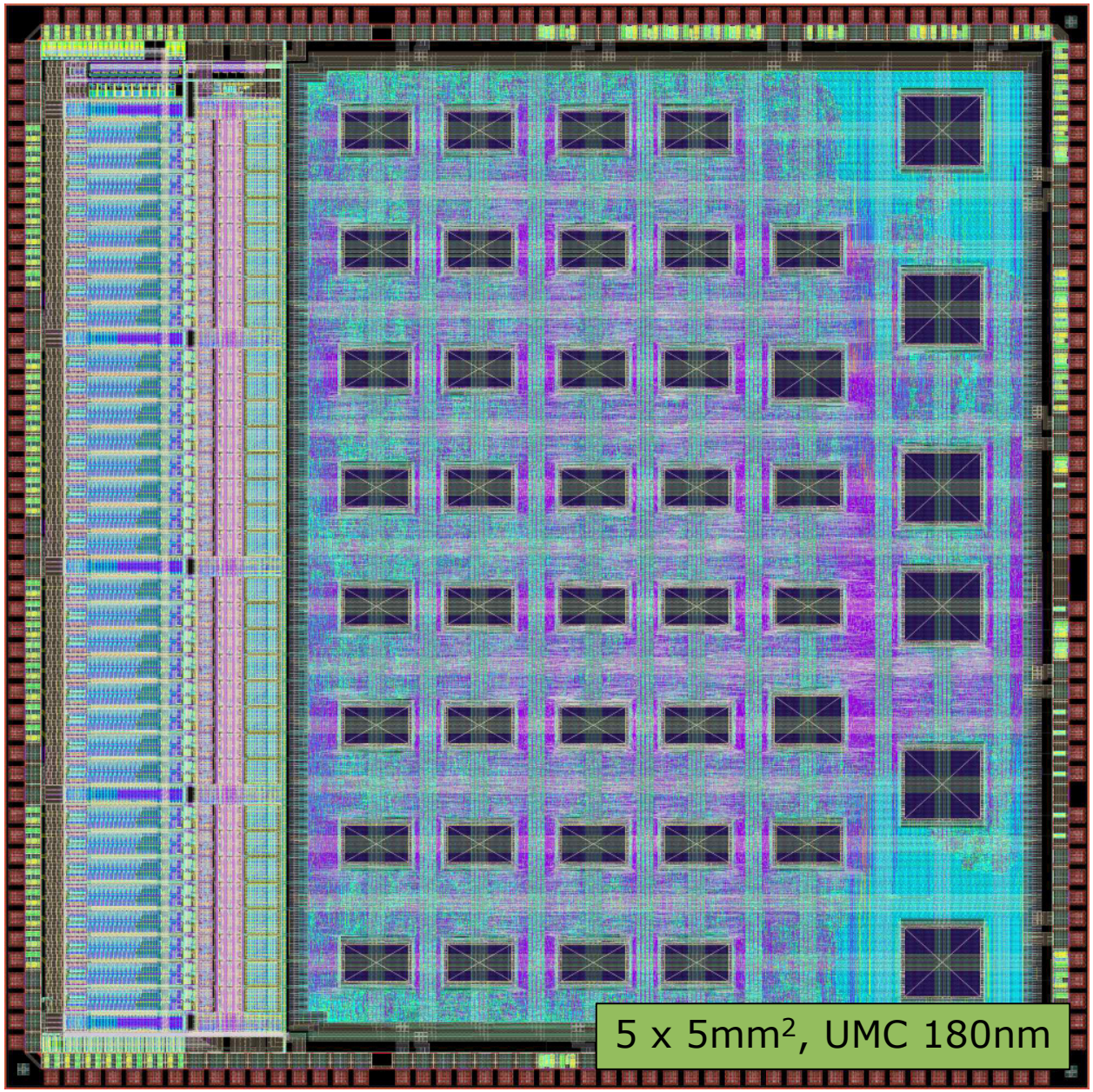
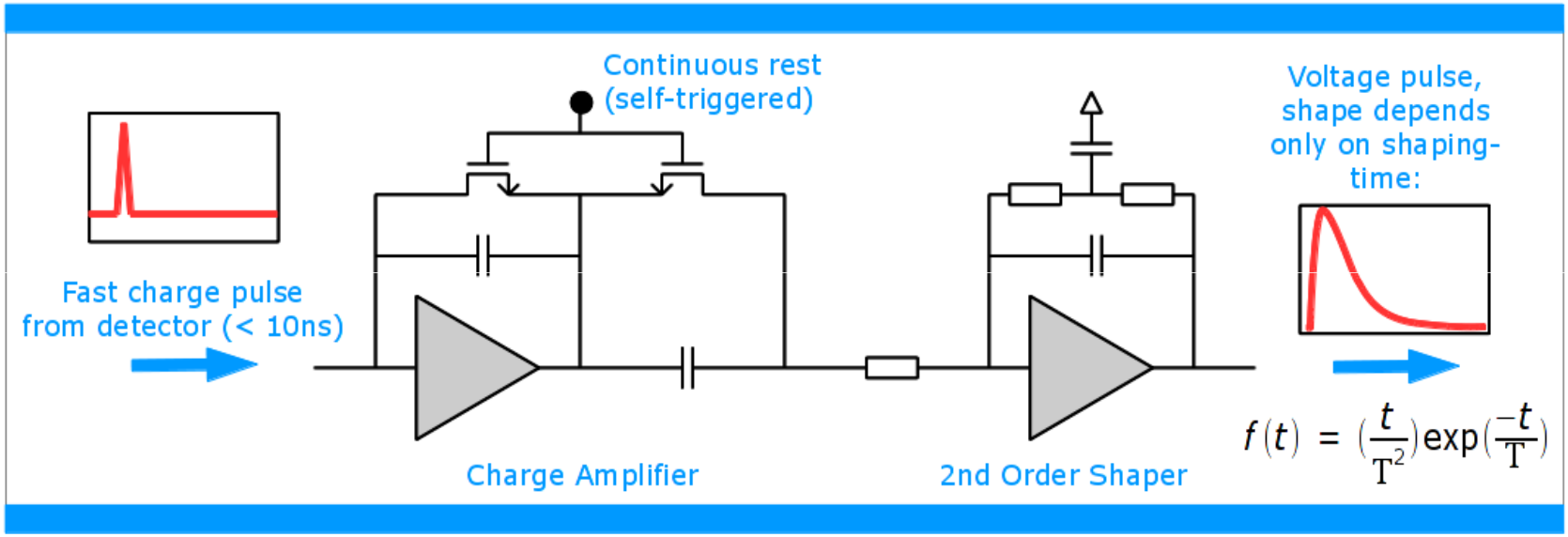
32 channels

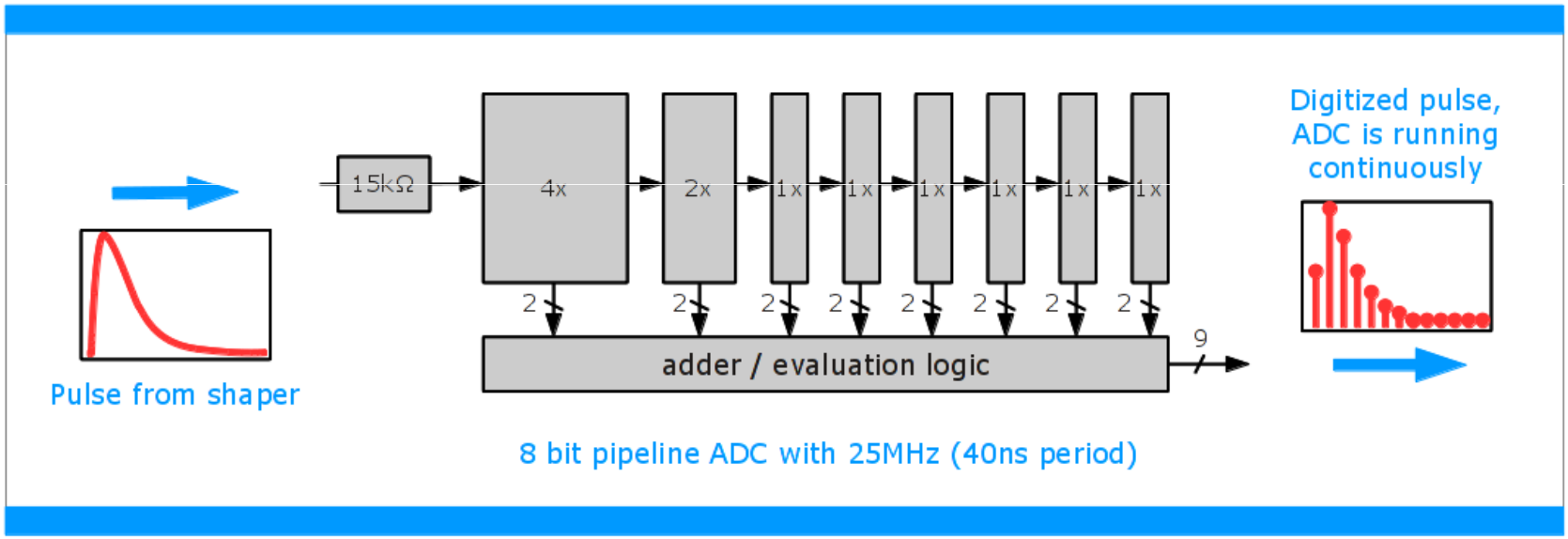
Per channel:
- **Two** CSAs (both polarities)
- pipeline ADC, ENOB ~ 8 bit
- IIR filter
- Autonomous hit detection
- Complex package builder
- Neighbor readout
- Time Stamp

Readout:
- FIFO buffer per channel
- Preserved Timestamp-order
- Injection of Epoch Events
- CBMnet 2.0 protocol
- 2 LVDS outputs @ 500Mbps

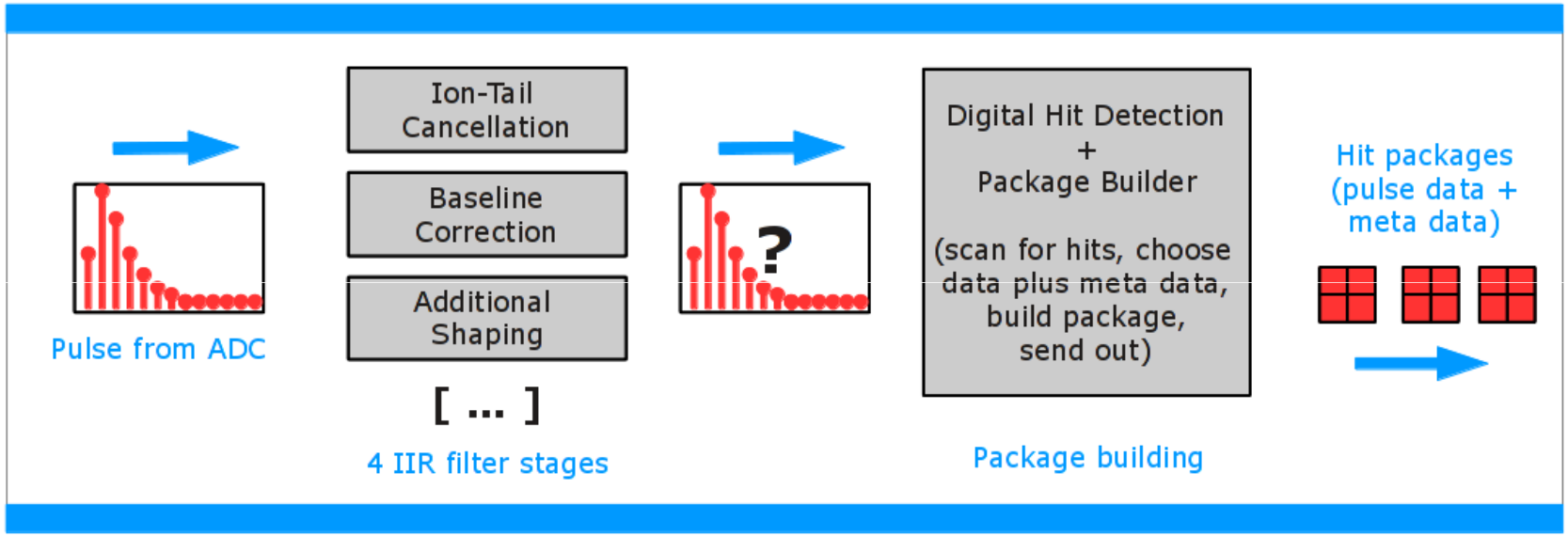


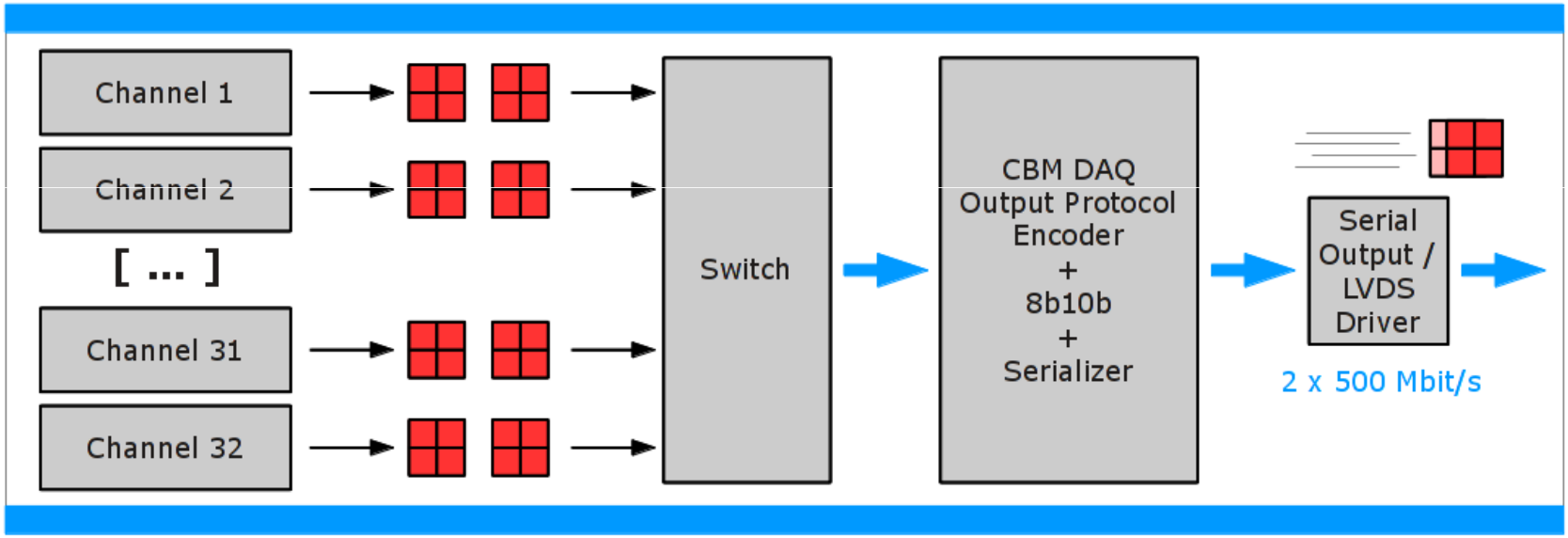
Data-Flow


Continuous rest
(self-triggered)
Voltage pulse,
shape depends
only on shaping-
time:
Fast charge pulse
from detector (< 10ns)
Charge Amplifier
2nd Order Shaper
$f(t) = (\frac{t}{T^2})\exp(\frac{-t}{T})$

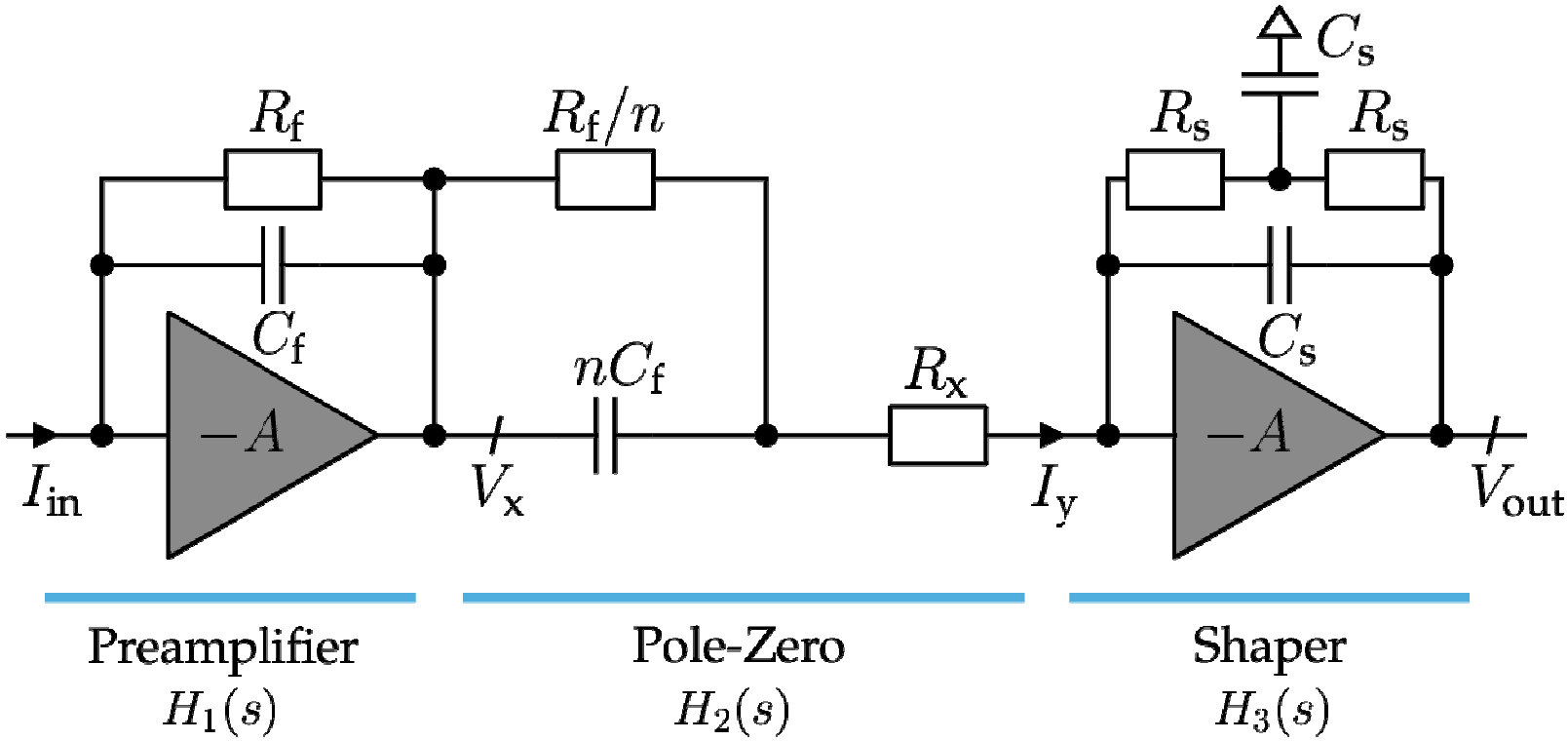

15kΩ
4x
2x
1x
1x
1x
1x
1x
1x
2
2
2
2
2
2
2
2
9
adder / evaluation logic
Digitized pulse,
ADC is running
continuously
Pulse from shaper
8 bit pipeline ADC with 25MHz (40ns period)

Data-Flow


Pulse from ADC
Ion-Tail Cancellation
Baseline Correction
Additional Shaping
[...]
4 IIR filter stages
?
Digital Hit Detection + Package Builder
(scan for hits, choose data plus meta data, build package, send out)
Package building
Hit packages (pulse data + meta data)

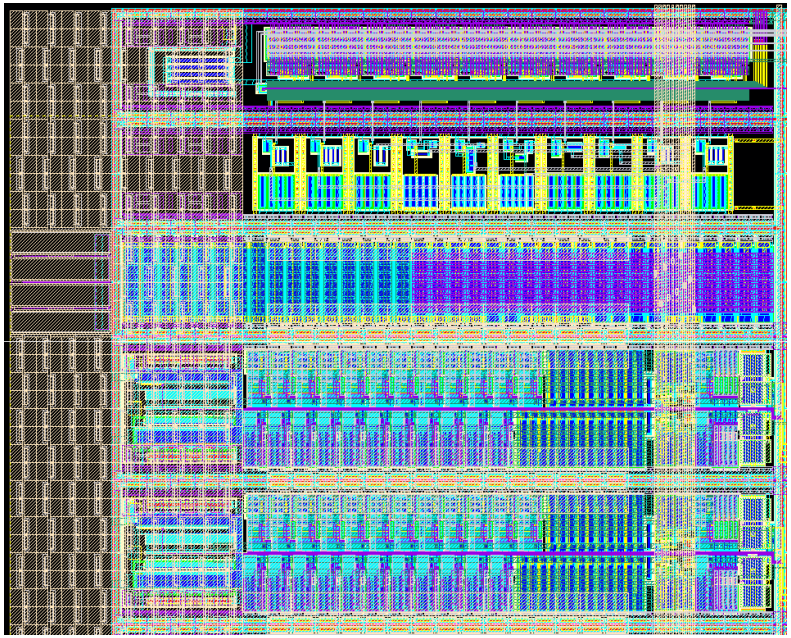

Channel 1
Channel 2
[...]
Channel 31
Channel 32
Switch
CBM DAQ Output Protocol Encoder + 8b10b + Serializer
Serial Output / LVDS Driver
2 x 500 Mbit/s

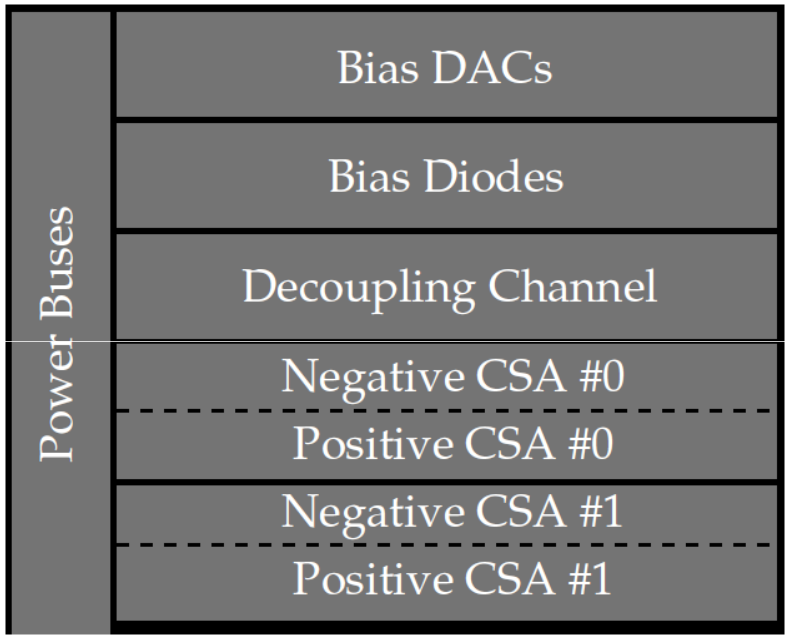
Charge Amplifiers

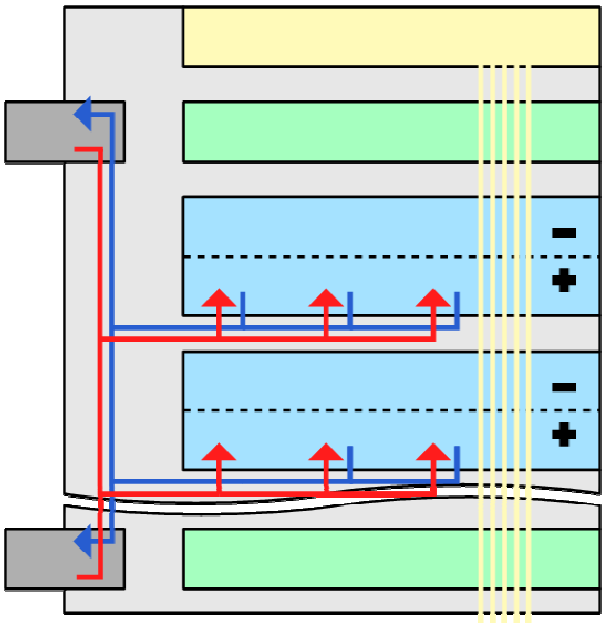


- Two CSAs: positive and negative polarity (input range 75 fC), single ended
- Shaping-time: **80ns** (simple CR-RC shaper)
- Noise: 700e @ 30pF (sim.), previous ASIC: **800e @ 30pF** (measured)
- Power: **4mW** (positive), 10mW (negative, not optimized)
- Layout: 440µm x 60 µm (each polarity)
- Features: Power disable, modular & scalable layouts and schematics

Charge Amplifiers







bias channel/bus

decoupling channel

pos./neg. CSA

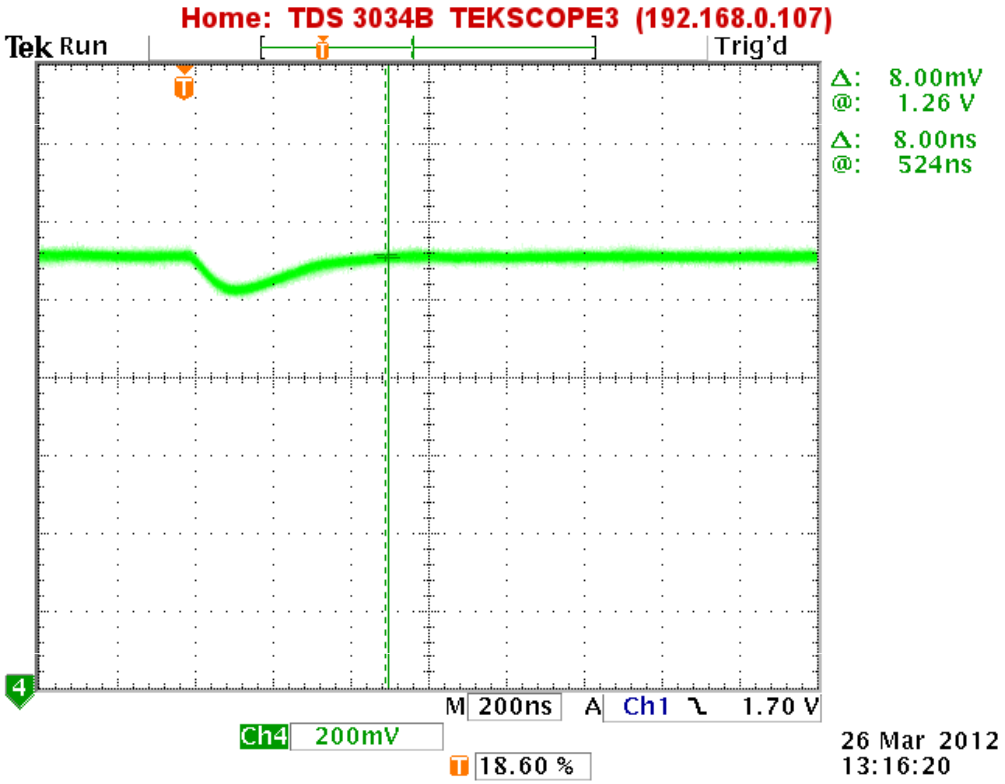
power buses

to power pad

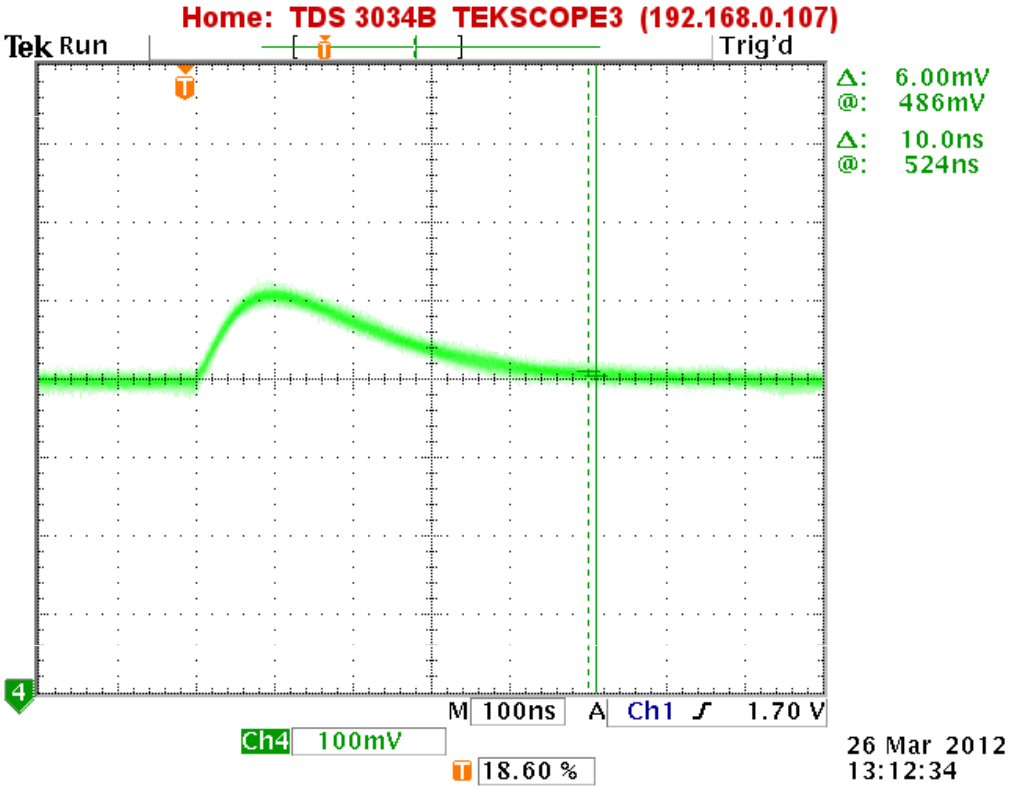
current flow

Charge Amplifier Output Signals

- Measured via monitor bus (slow, noisy) as a proof of operation

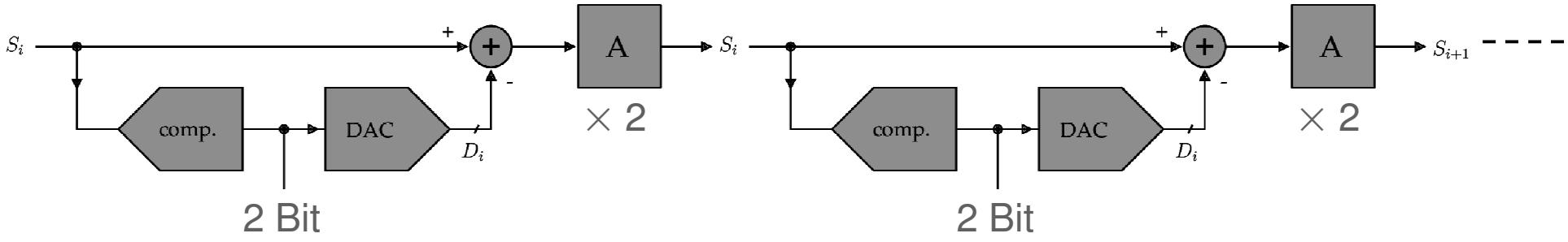


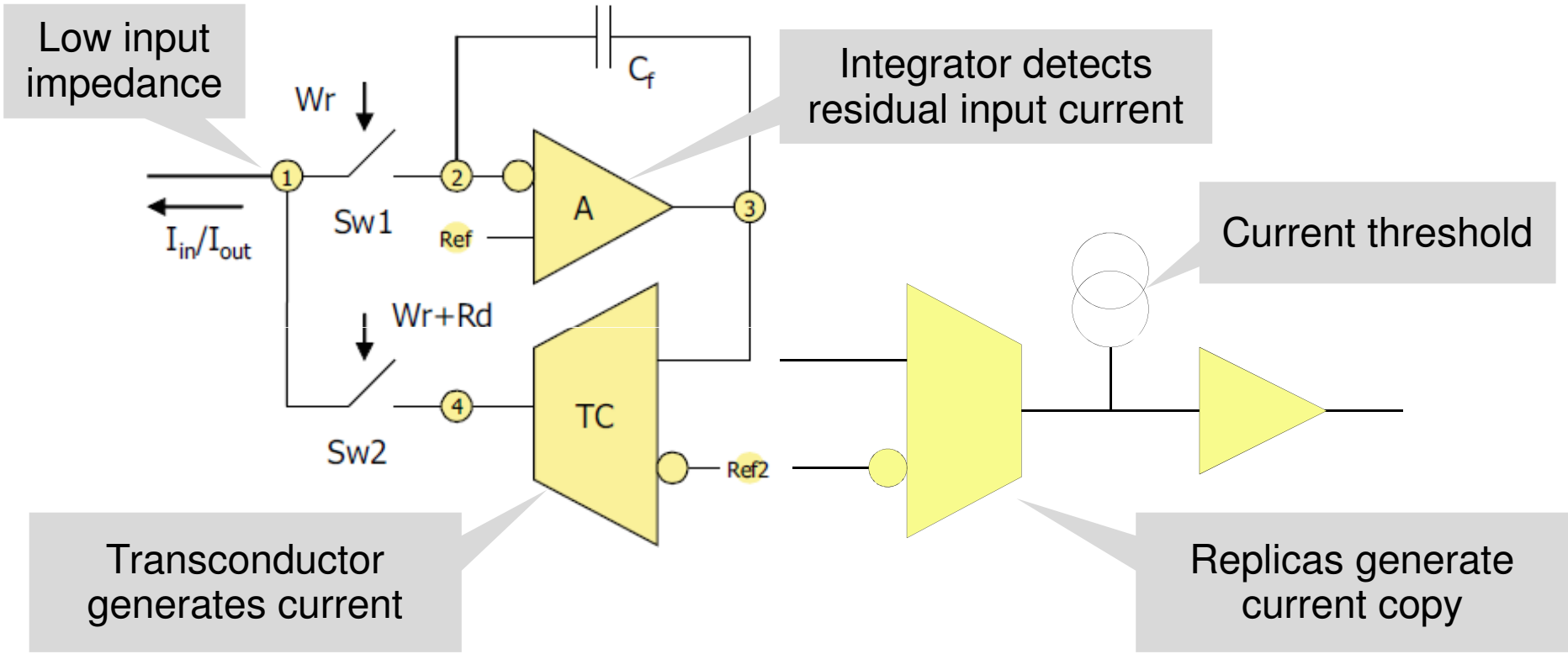
Negative polarity FE



Positive polarity FE

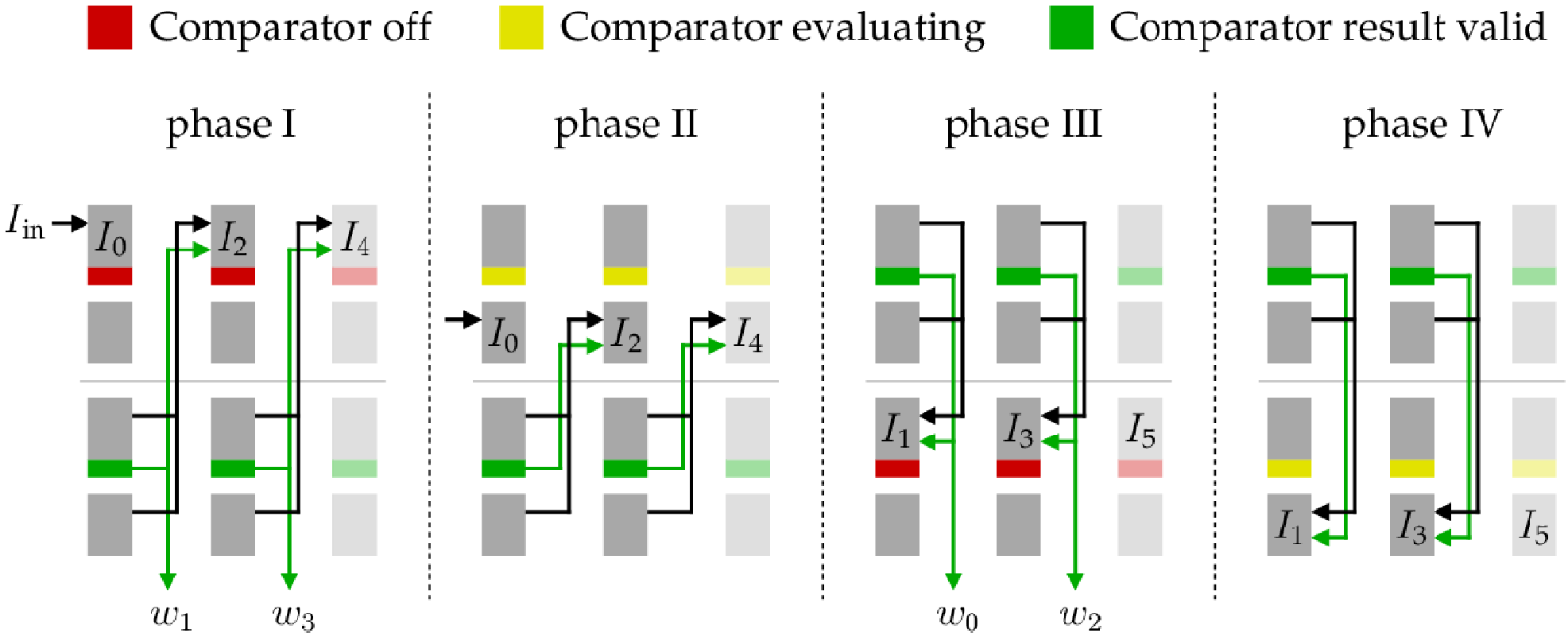
- **Pipelined** Design using **Current Mode Storage cells**





Pipeline ADC

- Signal doubling by use of 2 storage cells / stage & current addition
- Noise of first stages is decreased by higher power there
- 8 pipeline stages of 1.5 bit with error correction
- 9 bit (**ENOB ~8**), **25 MS/s**, **4.8 mW**. Rad-hard layout, Size: 400 x 300 µm²



Pipeline ADC Transfer

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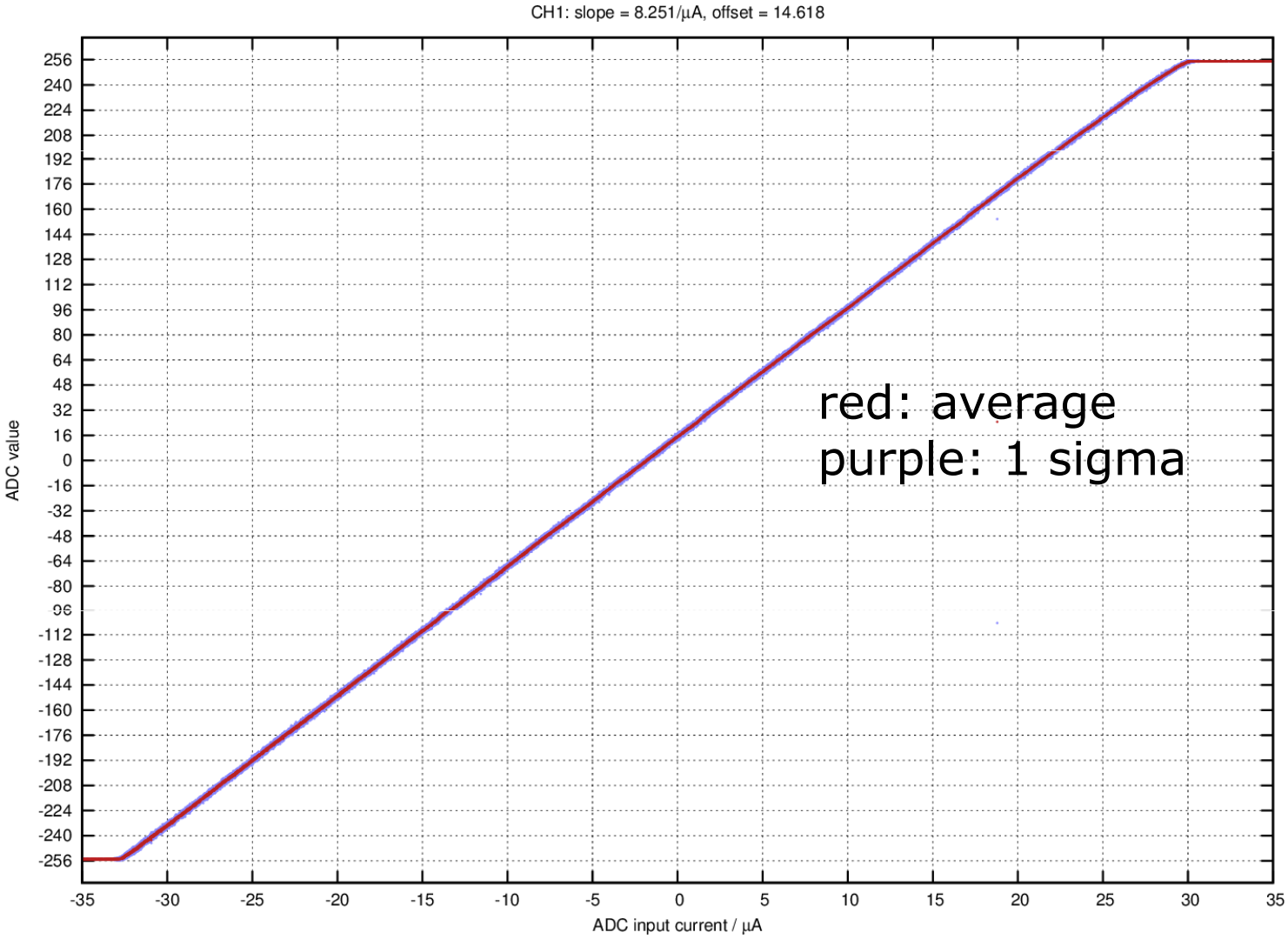
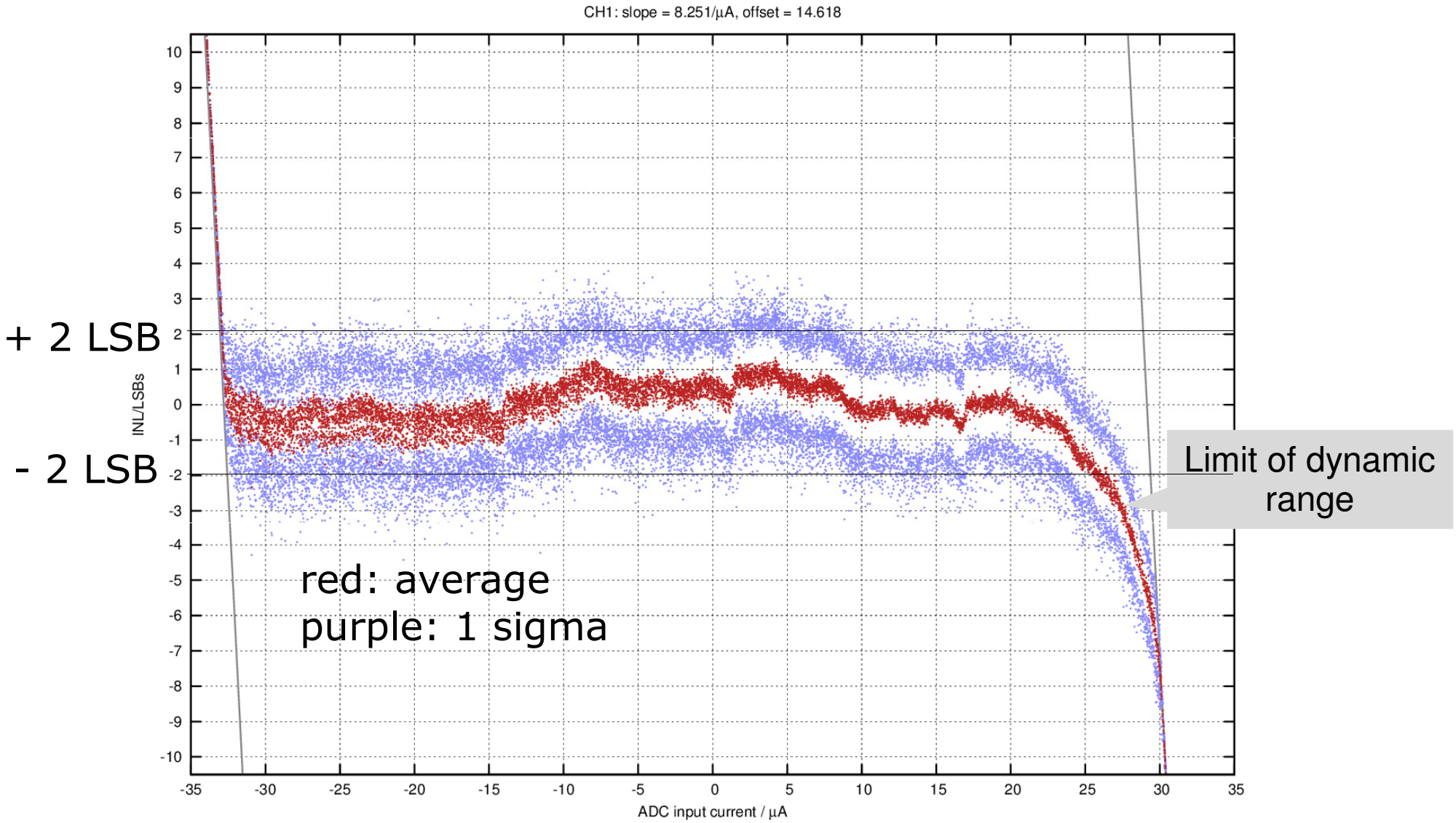
- Measured at 20 MSps, 9 Bit Mode (-255..256)

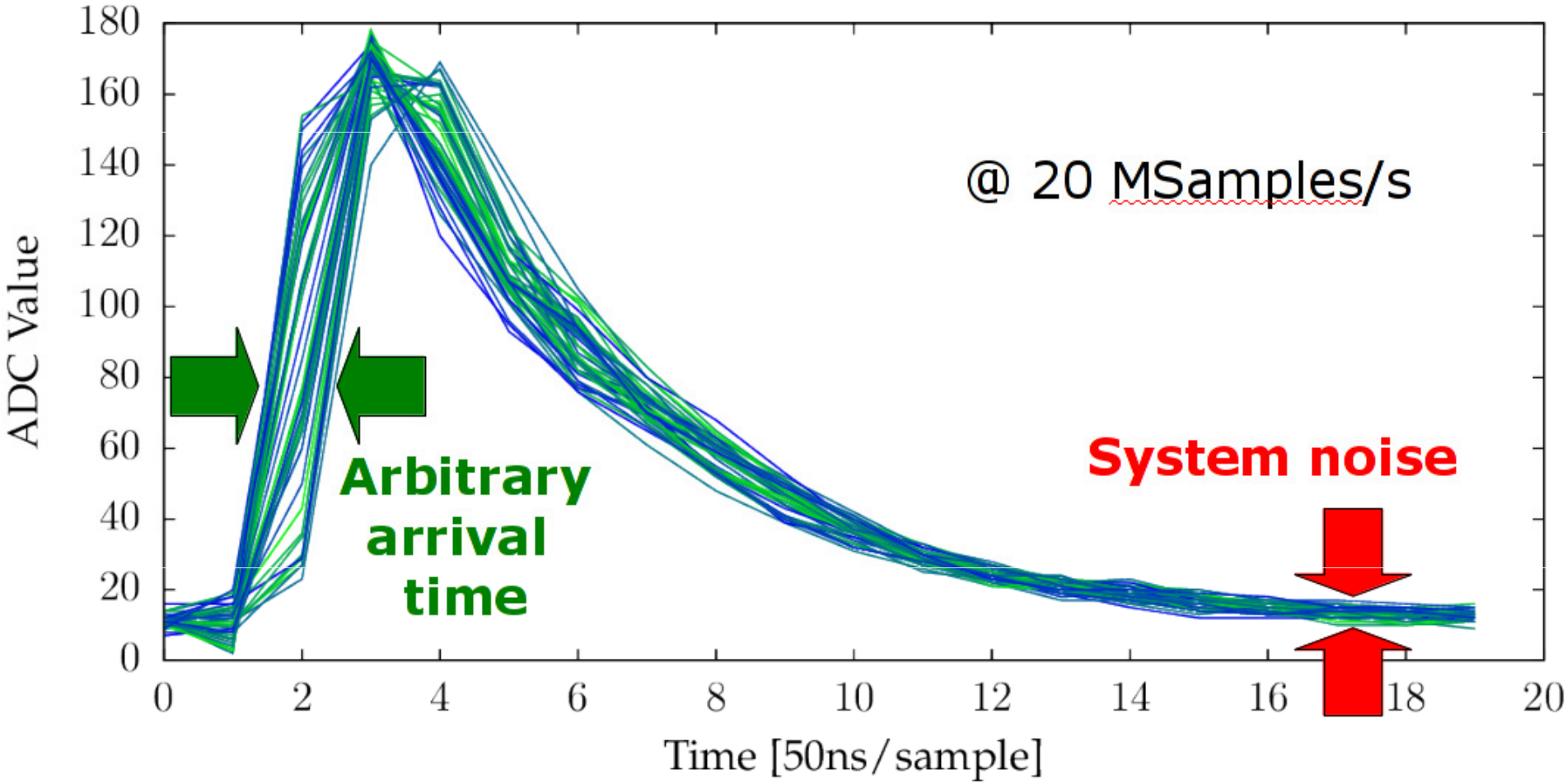


Pipeline ADC INL

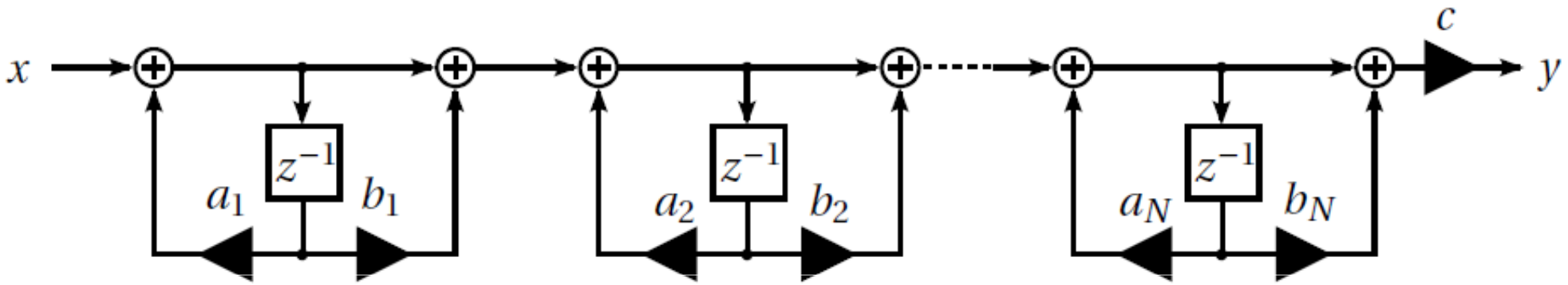
- INL @ 20 MSps, 9 Bit mode:

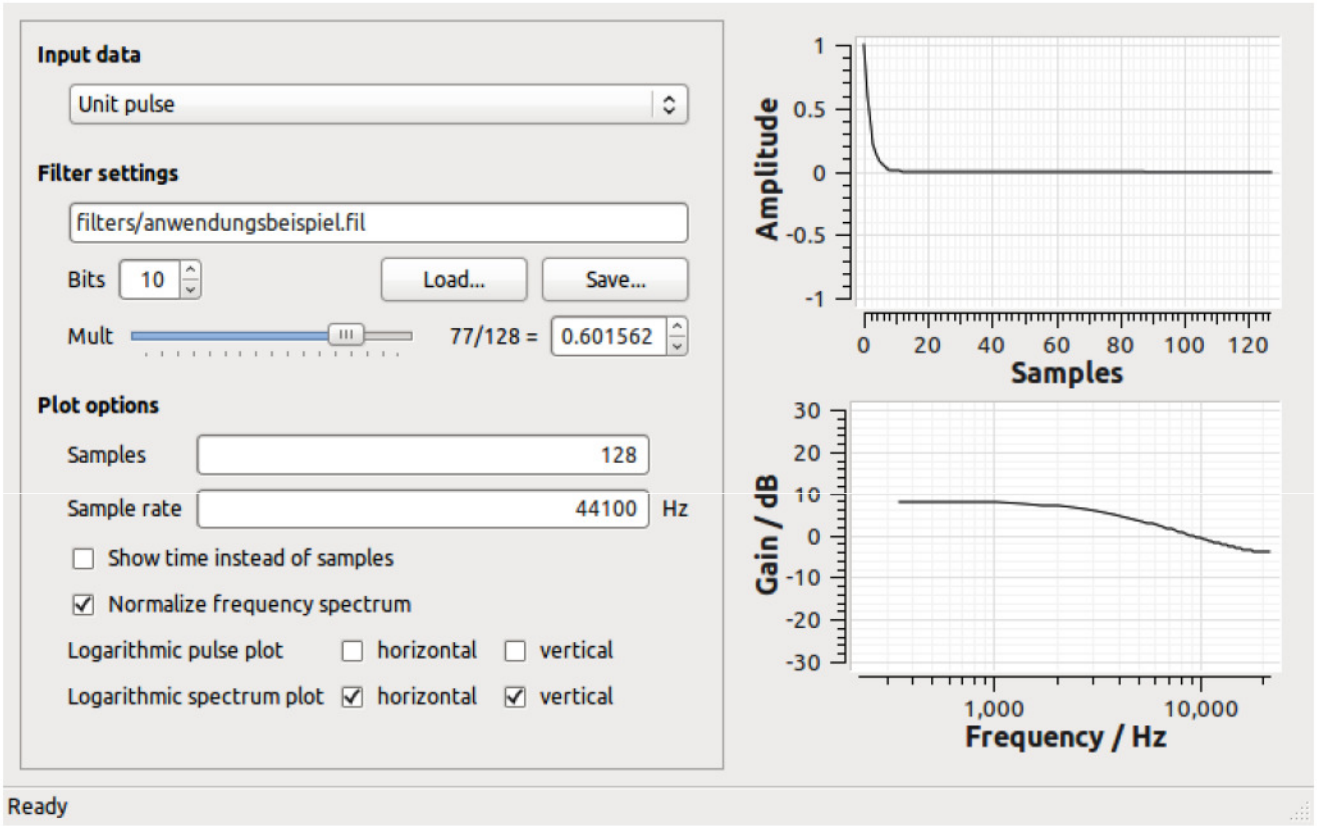


Digitized Pulses



IIR Filter





Configuration/Simulation Software

Main Purposes

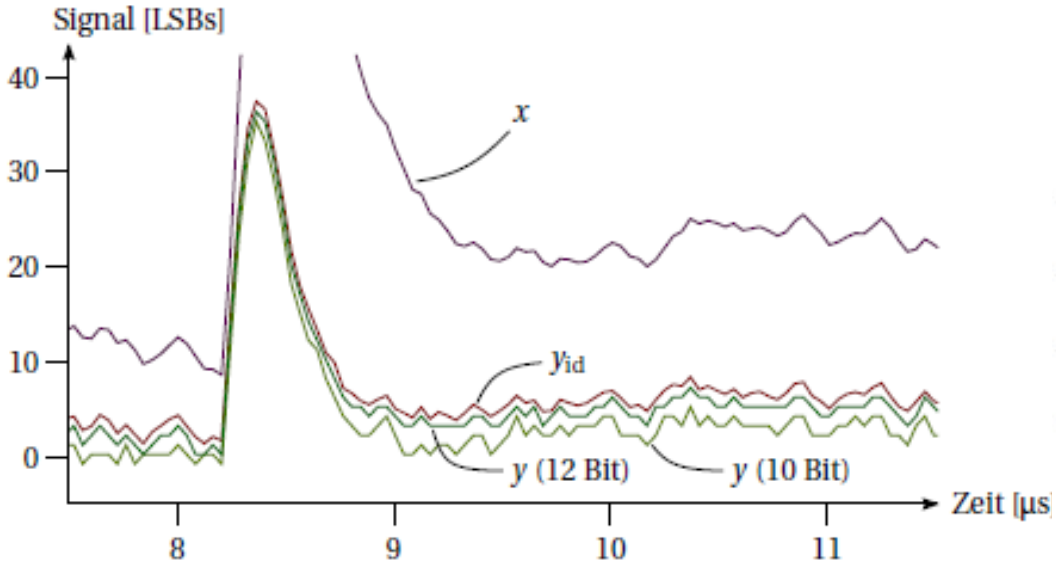
- Ion-tail cancellation (MWPC)
- Baseline stabilization
- Pulse inversion (required for negative front-end)

Structure

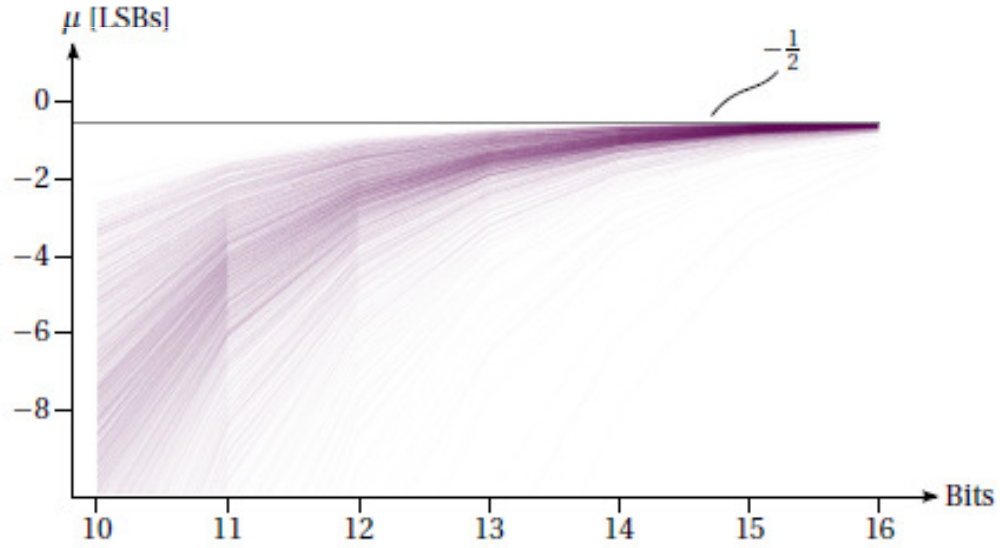
- Four 1st order stages
- 25MHz max.

IIR Filter Optimization

- Determine **quantization errors** introduced by internal bit widths
- Choose bits width as small as possible to simplify the multipliers



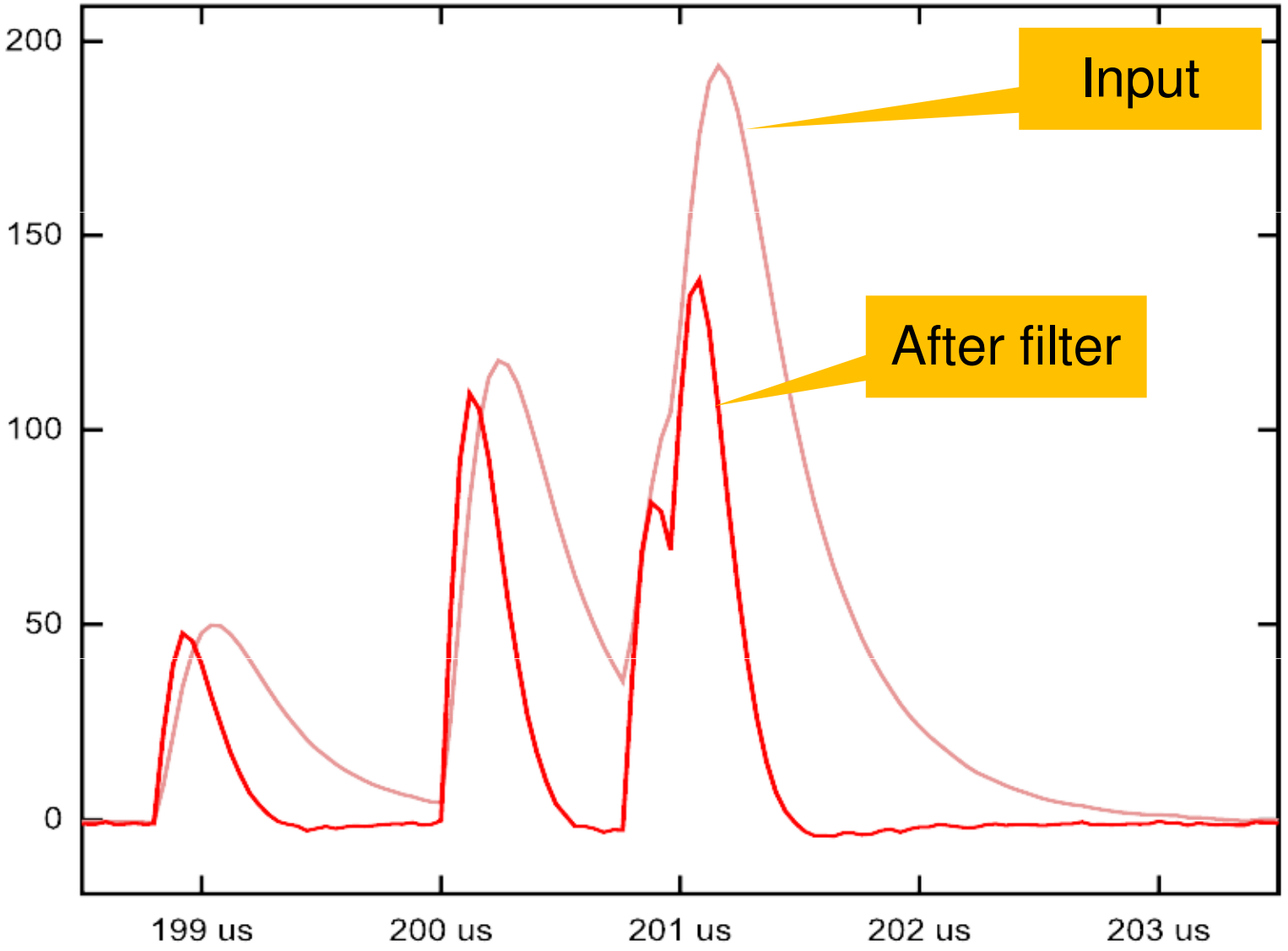
Pulses @ different bit widths



Quantization Error for different filter settings vs. Bit width

- Our conclusion: **16 bit internal resolution** (very generous)
  8 bit coefficients

Ion Tail Cancellation / IIR Filter Simulation



Ion Tail Cancellation / IIR Filter Simulation

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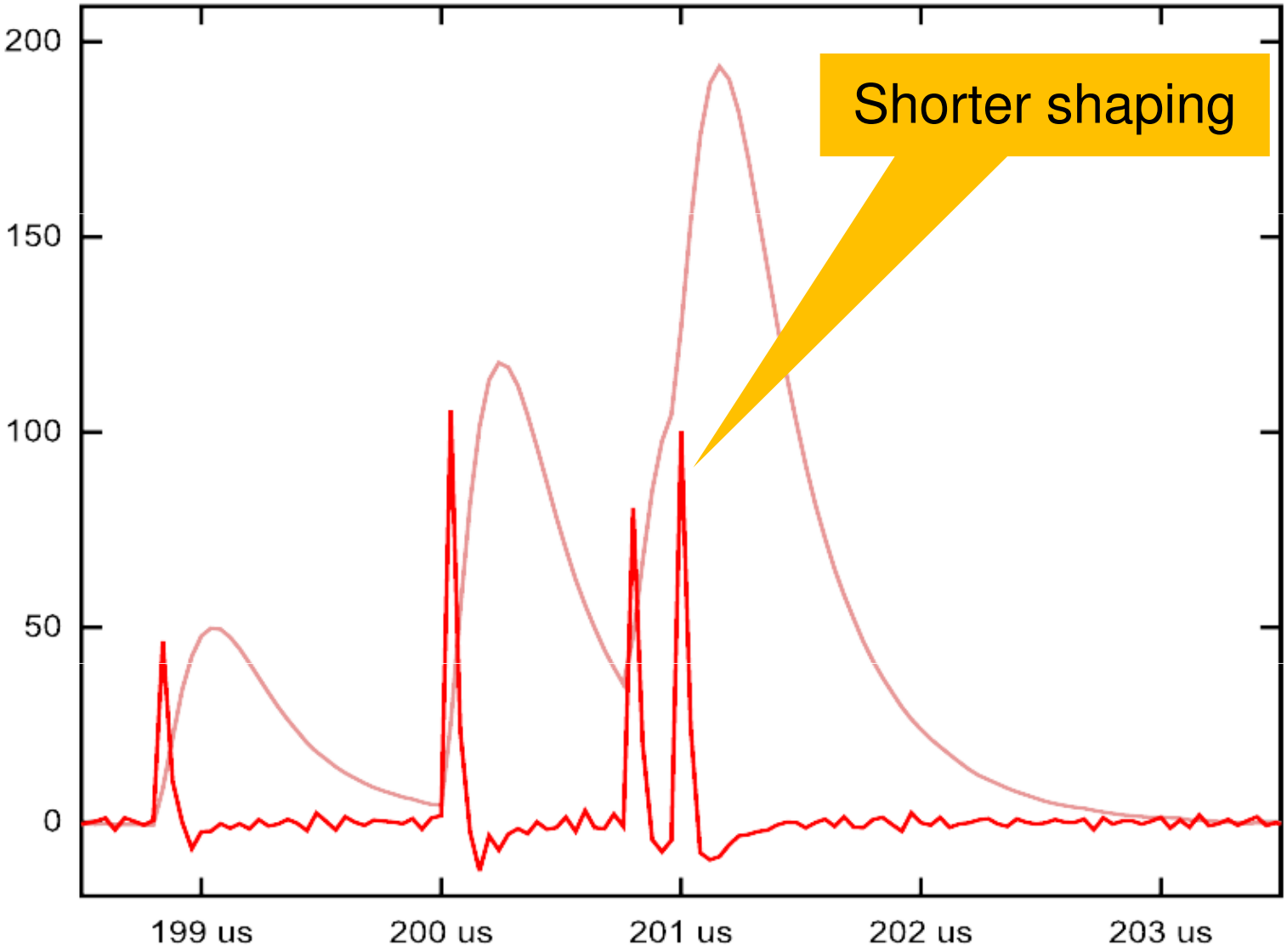
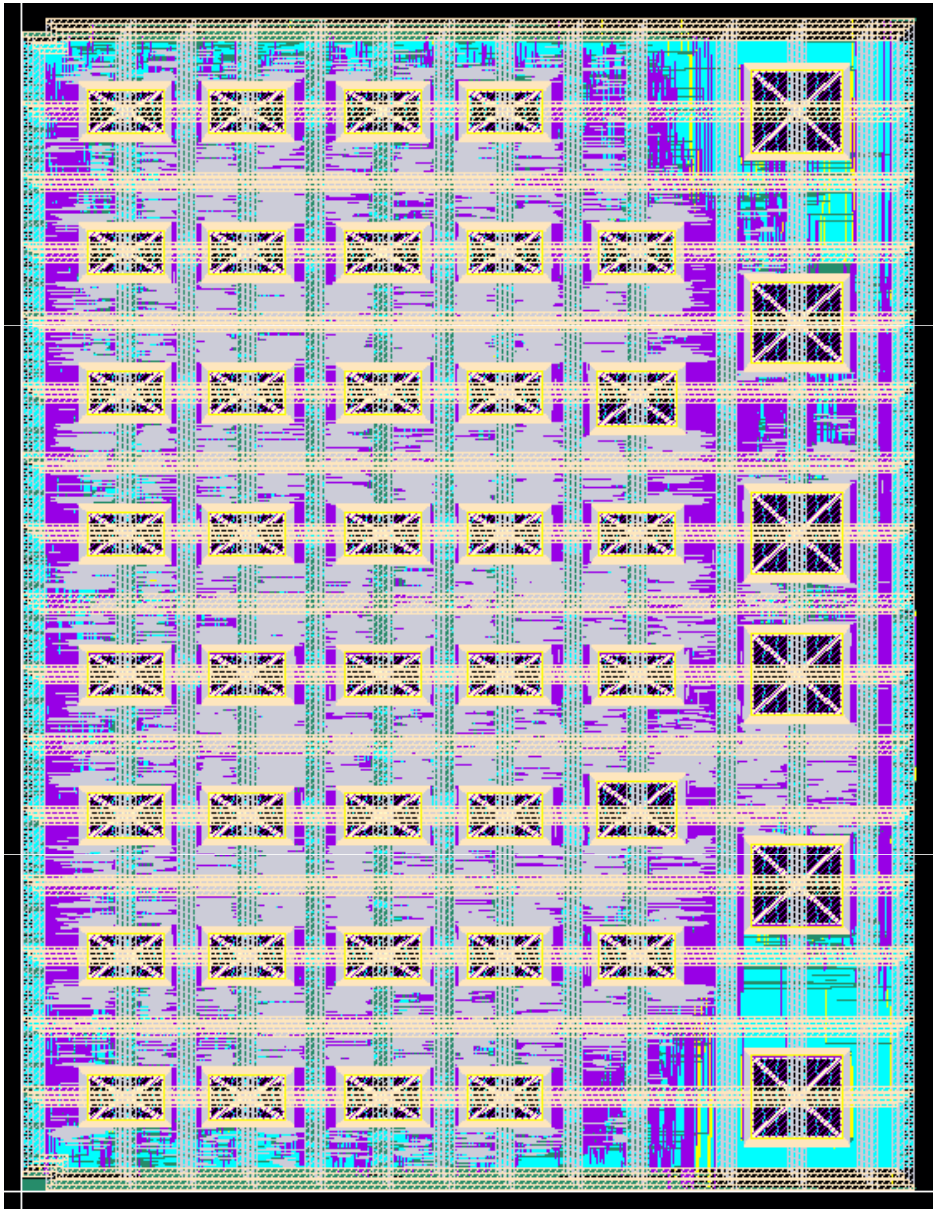
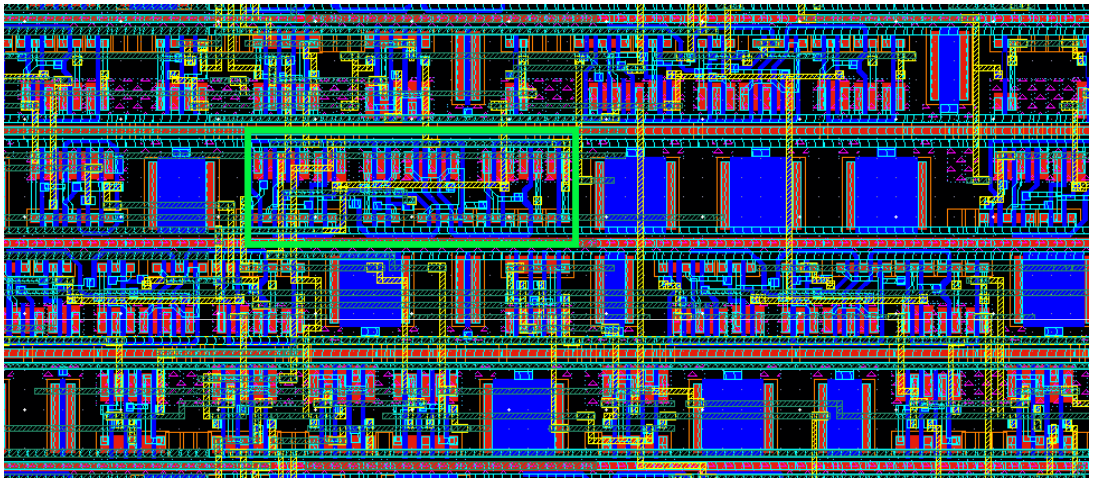


The Digital Part



Complete: 3.5 mm x 4.5 mm



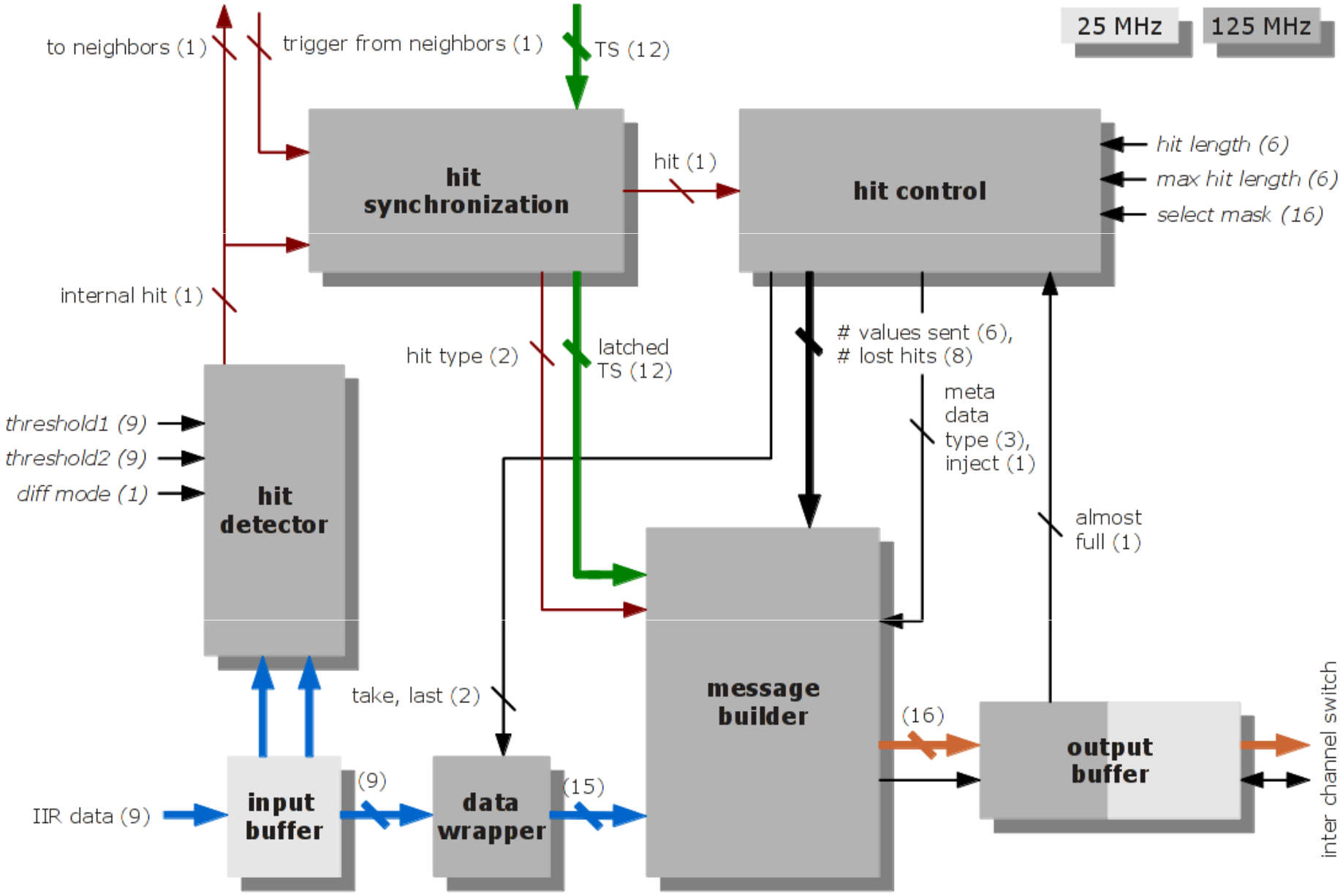
Cut-out: 14.4 µm x 5.76 µm (green: DFF)

- 250 MHz reference via CBMnet, other frequencies internally derived
- 3 CLK domains: 250 / 125 / 25 MHz

- 2.5 million transistors, 23k FF, 81k gates, total wire length: 14.4 m
- Home-made standard cell library
- 44 Faraday SRAMS (for FIFOs)

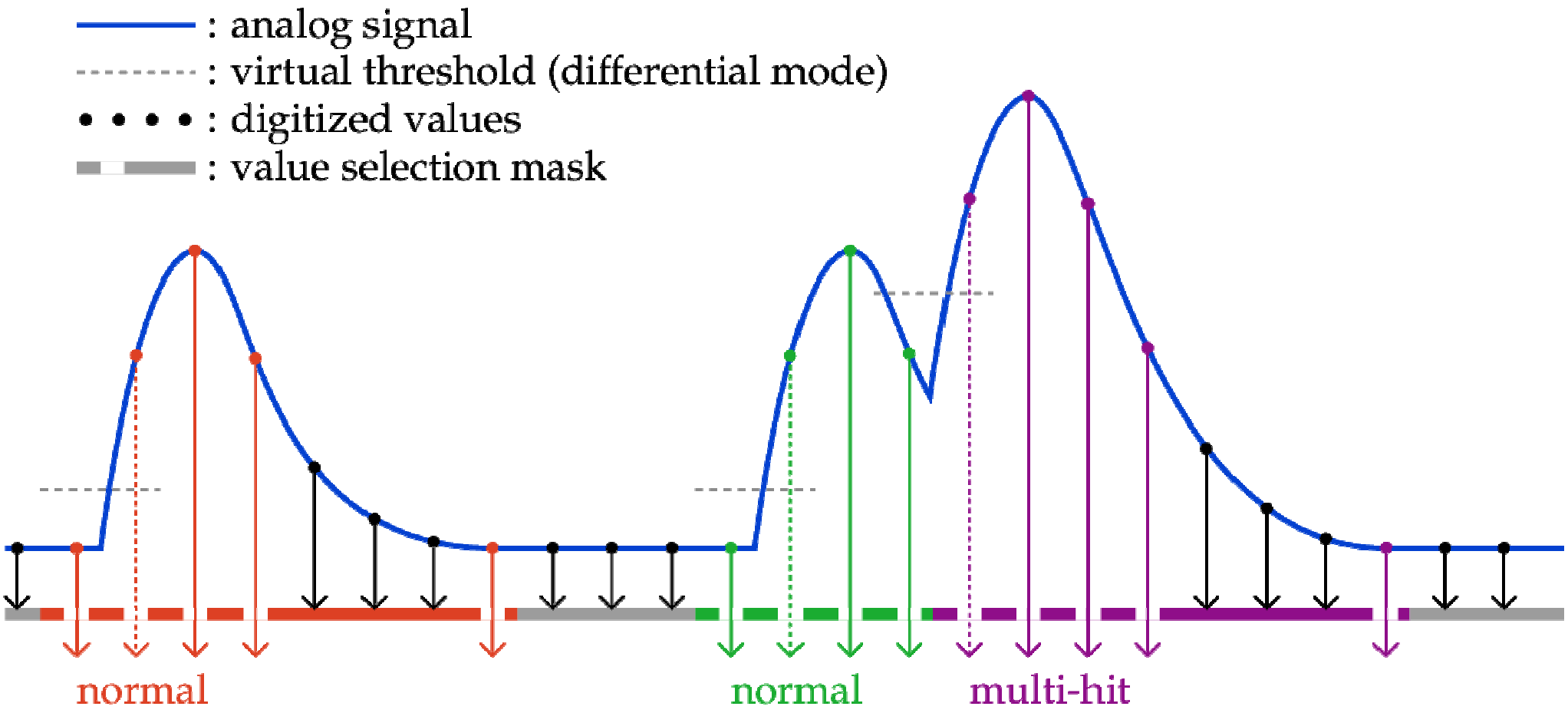
- Power (@ 200 MHz): 600 mW

Hit Detector and Message Builder



Hit Selection Logic

- Allows to pick a set of 'interesting' points in the pulse



Message Format Definition

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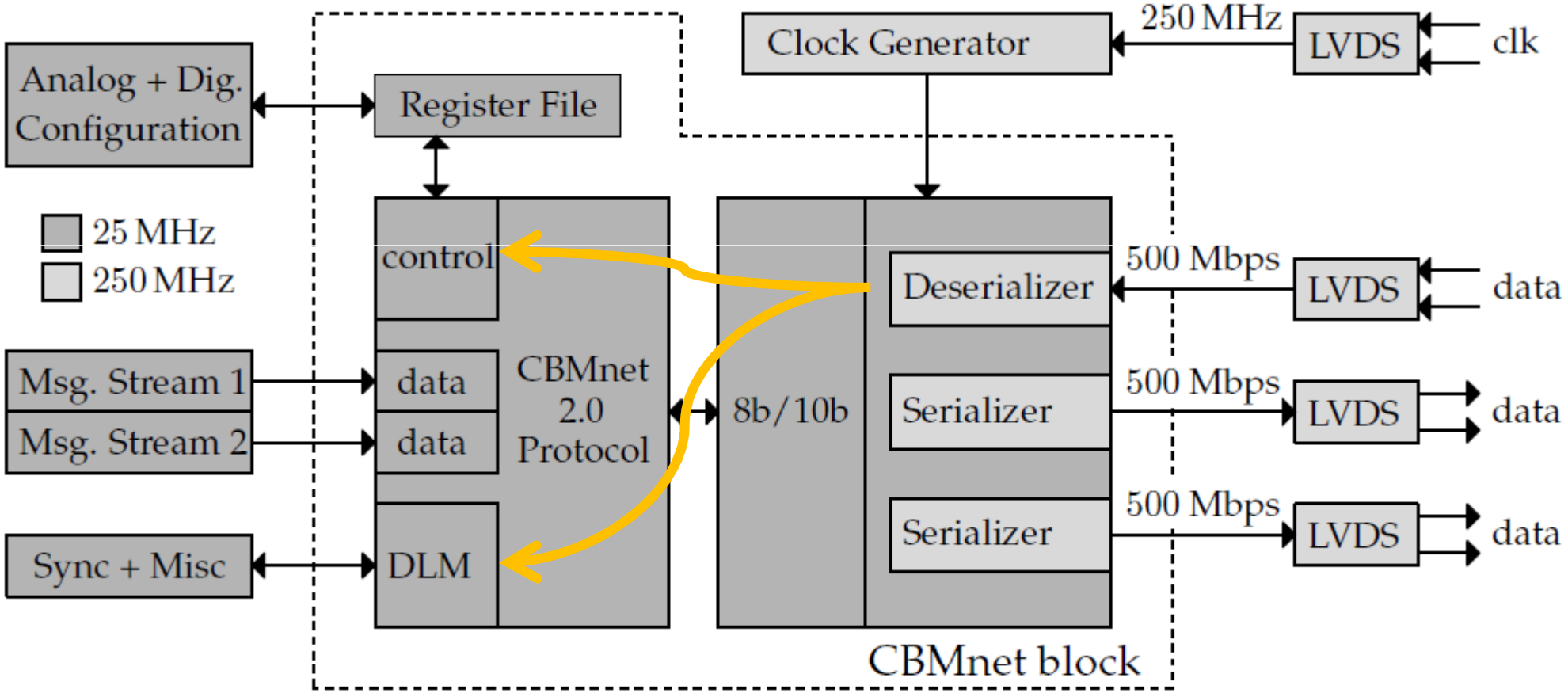
Data words	Interpreted content
1000 0000 0111 0010	Start of message - group: 7, channel: 2
1001 0011 0010 1010	Time-stamp - counter value: 810
1010 1111 1110 1000	Begin of raw data - sample 1, sample 2
0000 0101 1111 1100	Continuing raw data - sample 2, sample 3
0000 0000 1000 0011	Continuing raw data - sample 4, sample 5
0111 0000 0000 0000	Continuing raw data - sample 5, unused
1011 0001 0101 0000	End of message - ADC samples: 5, internally triggered, unused, normal stop

Benefits:

- Very reliable definition (each word has a preamble)
  - Bit-flips or loss of whole words are only a problem in the local context
  - Message stream can always be re-synchronized, even if whole words are lost
- Large number of predefined messages (normal, epoch, info, error, warning, …)
  - Easily adjustable/extendable
- Suitable for on-the-fly stream analysis (e.g. monitor time-stamps, count hits, ...)

CBMnet



Features:

- 2 x 500 Mbps downstream, 1 x 500 Mbps upstream (serial links, DDR)
- Automatic link initialization and management
- Only 4 LVDS pairs required (data, control and synchronization shared)
- **Deterministic Latency Message**: Fixed latency through network (sync, trigger,..)
- Reliable Link: Retransmission, 8b/10b, CRC, ...

Channel Message Switch + Epoch Channel

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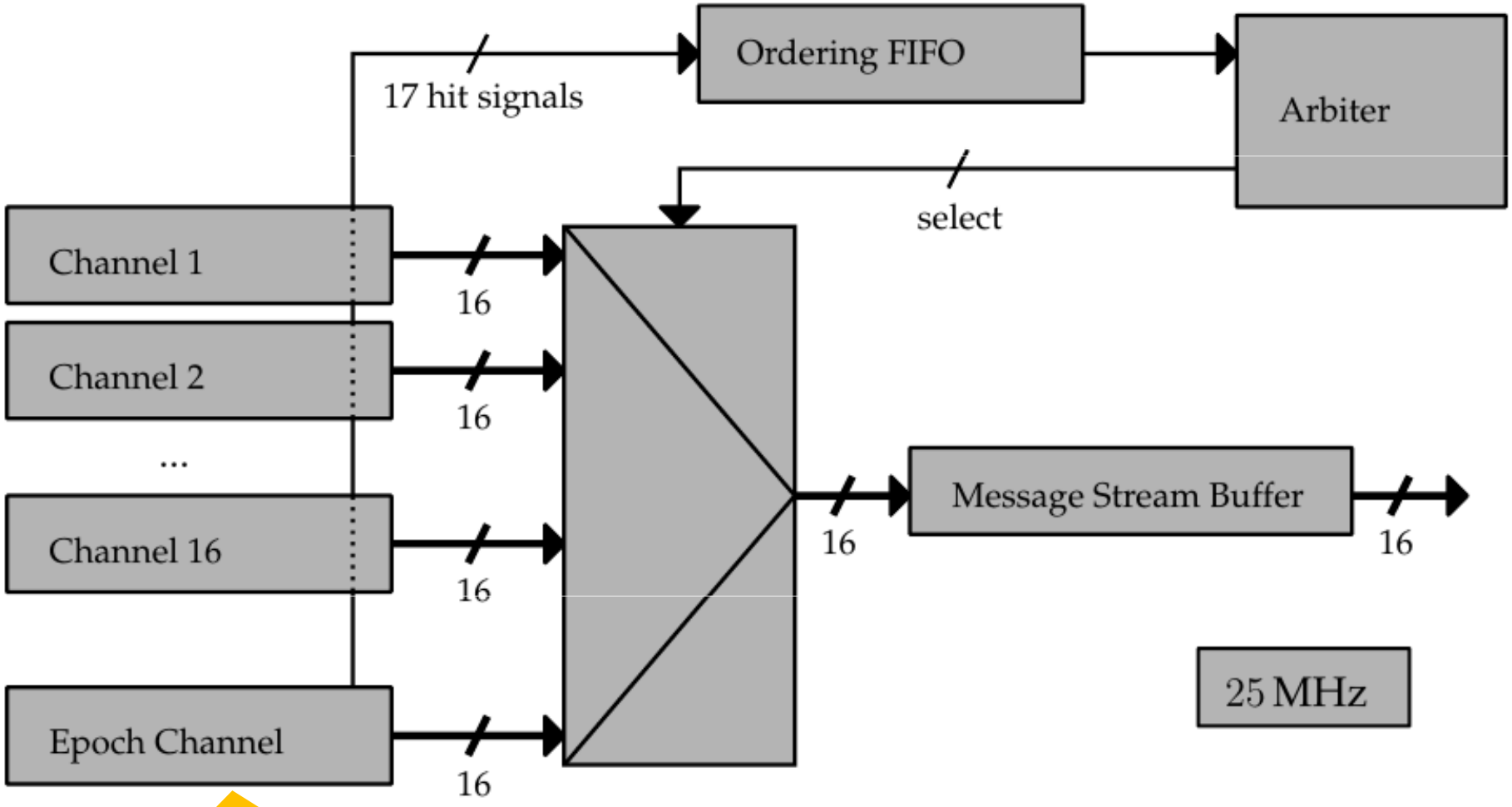
- Epoch Events flag when time stamp counter wraps



Epoch generation

SPADIC 1.0 Lab Setup

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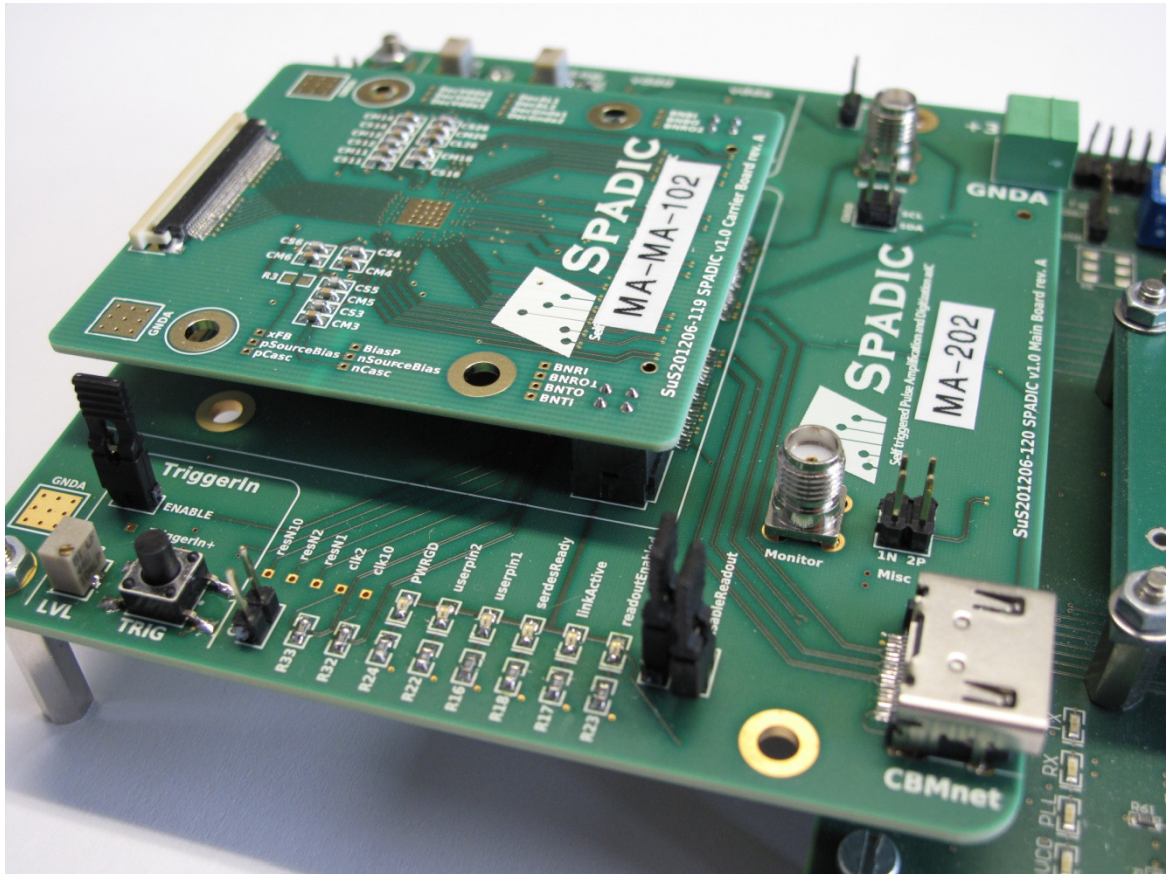
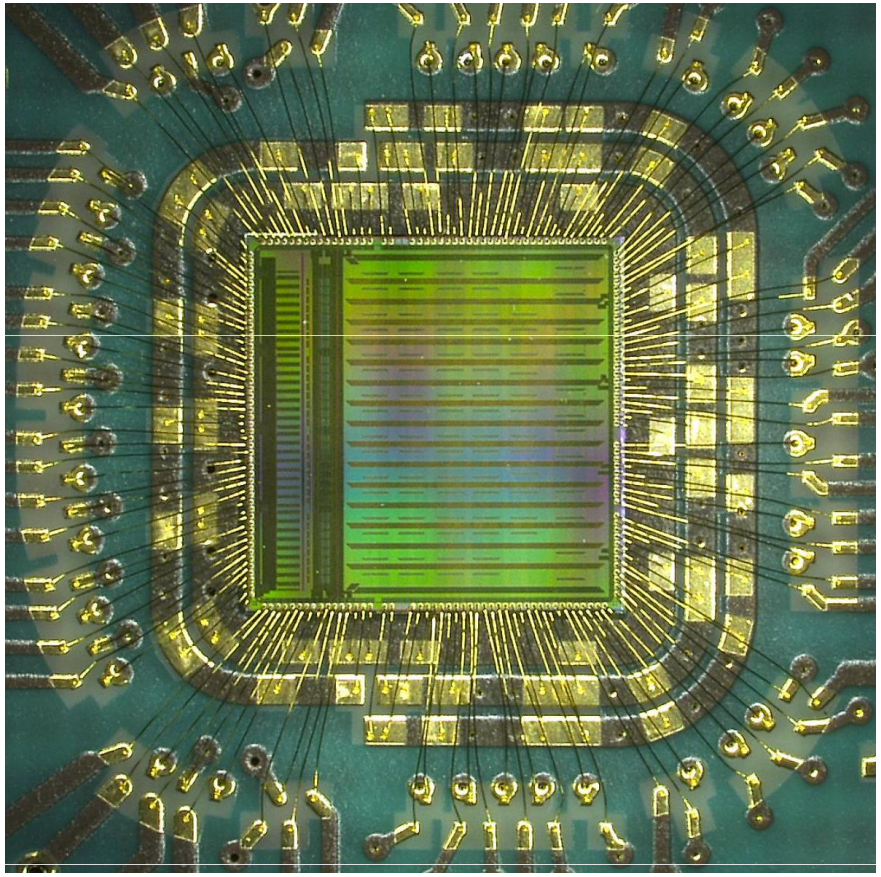
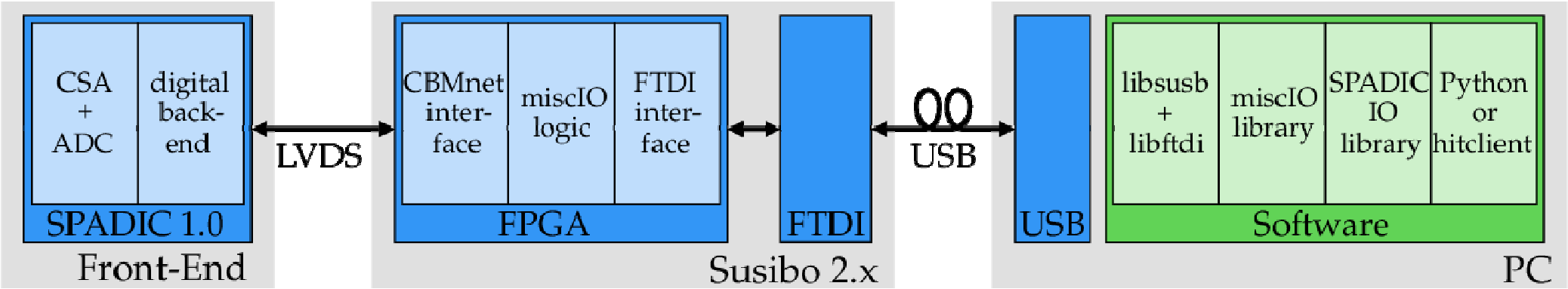
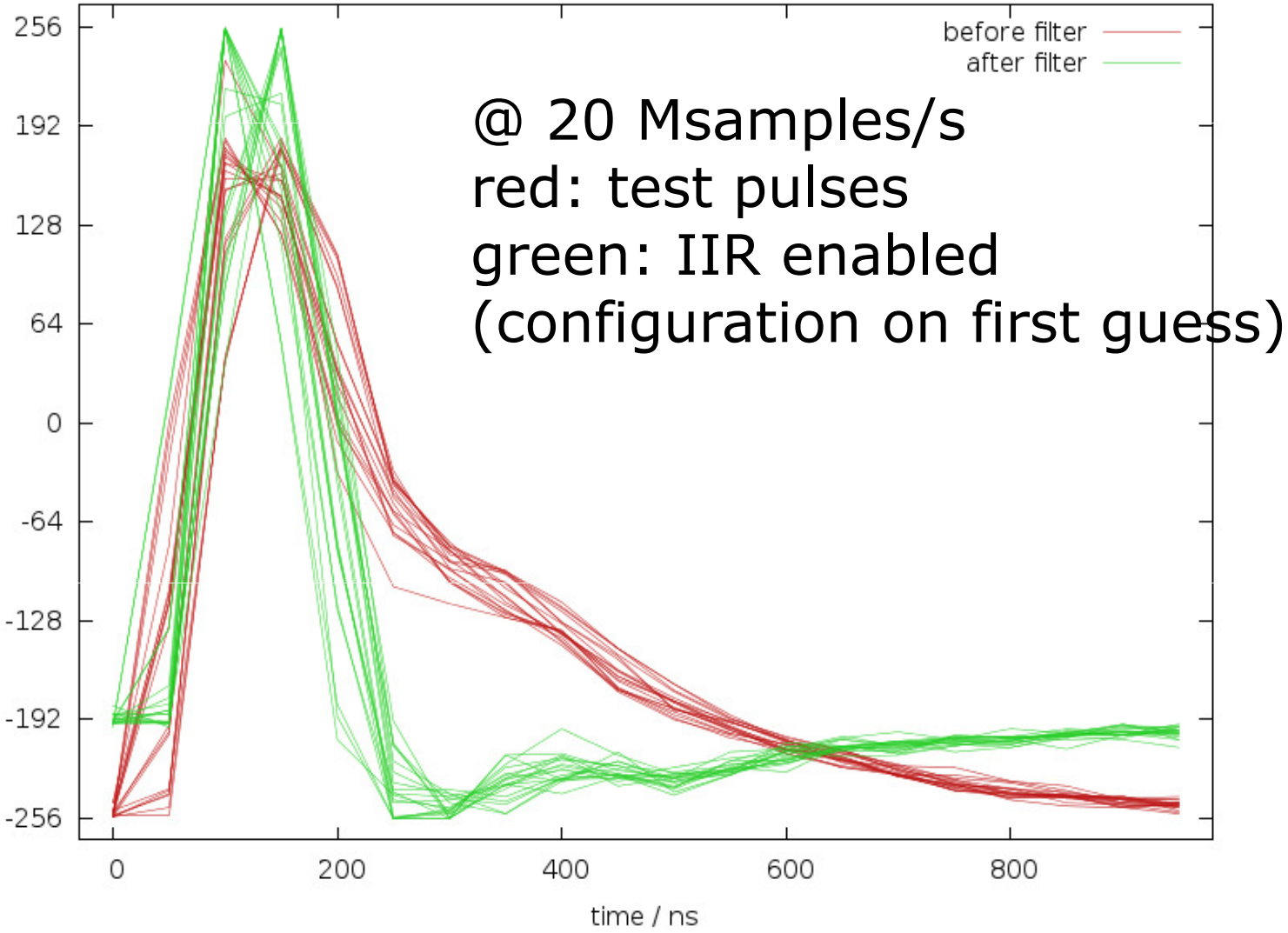






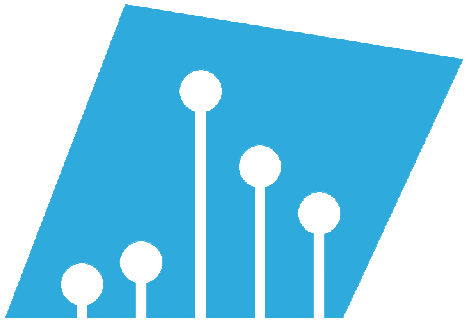
First Full System Measurement + IIR

- Using Spadic 1.0 and readout system shown:



Summary & Outlook

- Spadic is a ‘System on a Chip’ for self triggered charge readout
- Flexible Data Processing
  - IIR Filter
  - Threshold options
  - Neighbour trigger
  - Programmable pulse pattern
  - Time ordered readout & epoch markers
- It implements CBMNet
  - Deterministic Latency Messages & Data & Control over a single link. It includes acknowledge & retransmission of data.
- Status
  - Chip & CBMNet are being commissioned. Everything works so far.
  - Chip will be used for Detector tests & beam test soon



SPADIC

Self triggered Pulse Amplification and Digitization asIC

http://www.spadic.uni-hd.de

Bundesministerium
für Bildung
und Forschung

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