Status of SPADIC 1.0 readout over CBMnet using the Susibo

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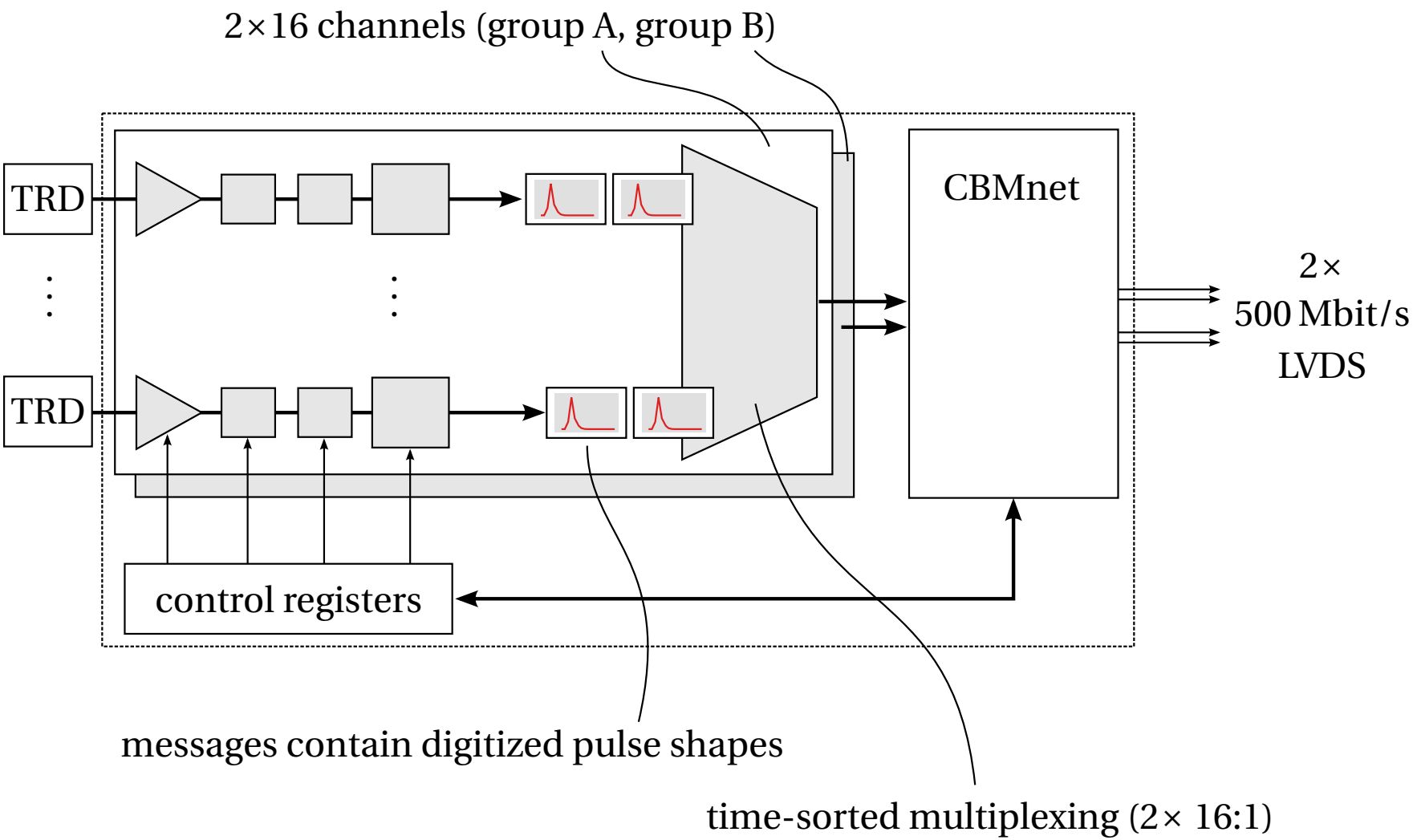
CBM Collaboration Meeting, GSI

09.04.2013

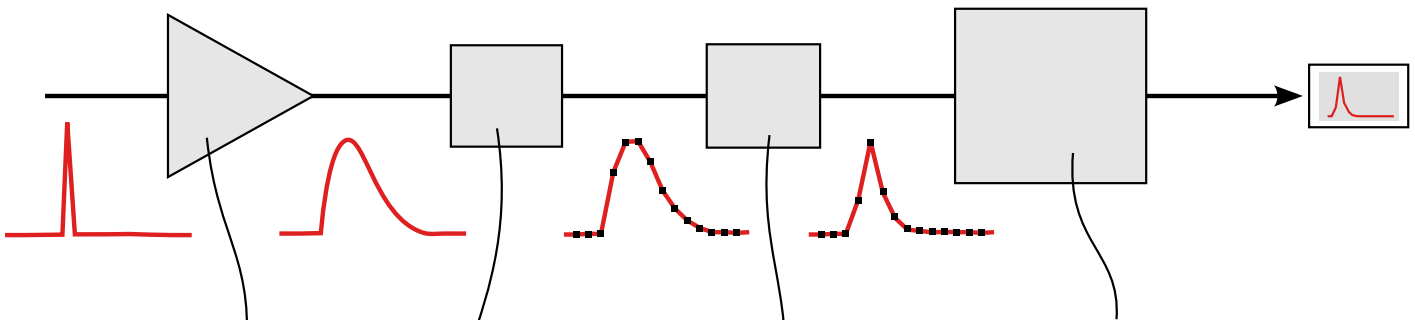
Outline

- Reminder: SPADIC 1.0 principle of operation
- First measurements
- CBMnet readout explained
- Implementation details
- Next steps

Global view


2×16 channels (group A, group B)
TRD
TRD
CBMnet
2×
500 Mbit/s
LVDS
control registers
messages contain digitized pulse shapes
time-sorted multiplexing (2× 16:1)

Channel view



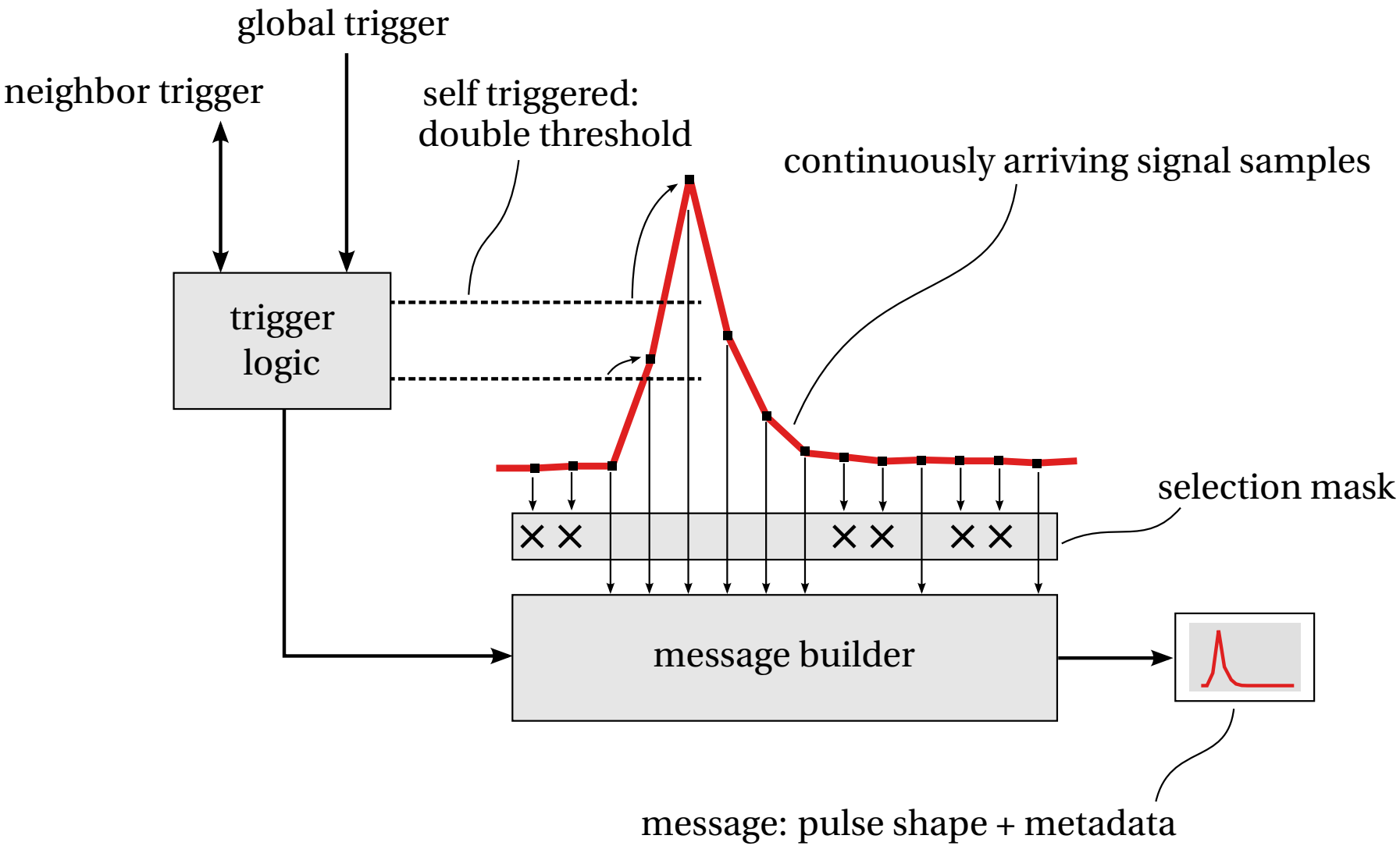
charge amplifier + shaper
$\tau = 80\,\mathrm{ns}$
$\mathrm{ENC} = 800\,\mathrm{e}^-$

ADC
continuously sampling (25 MHz)
9 bit output (resolution ≈ 8 bit)

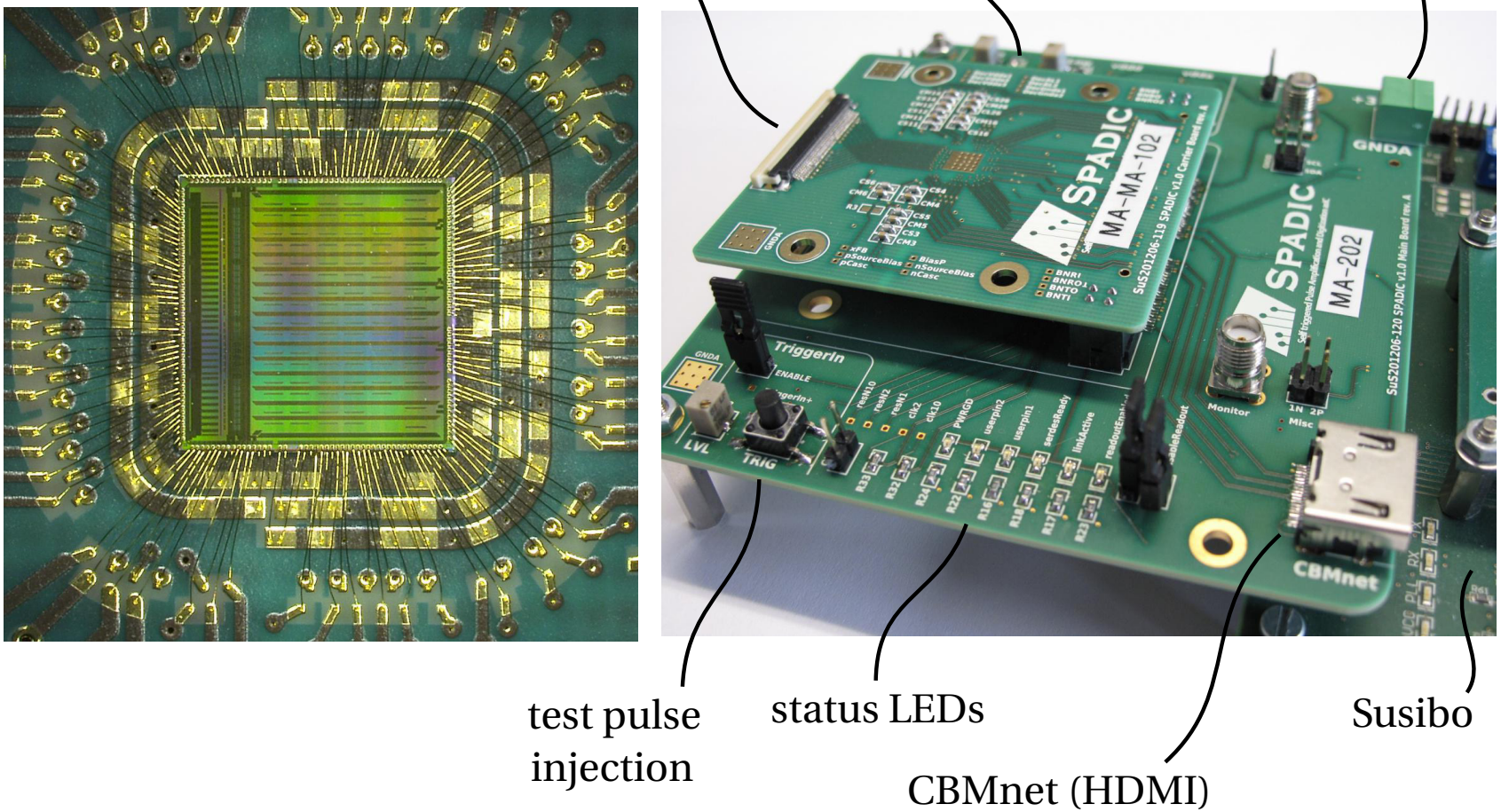
IIR filter
4 first order stages
6 bit coefficients, 16 bit resolution
+ scaling/shifting with saturation logic

Hit logic
+ message builder

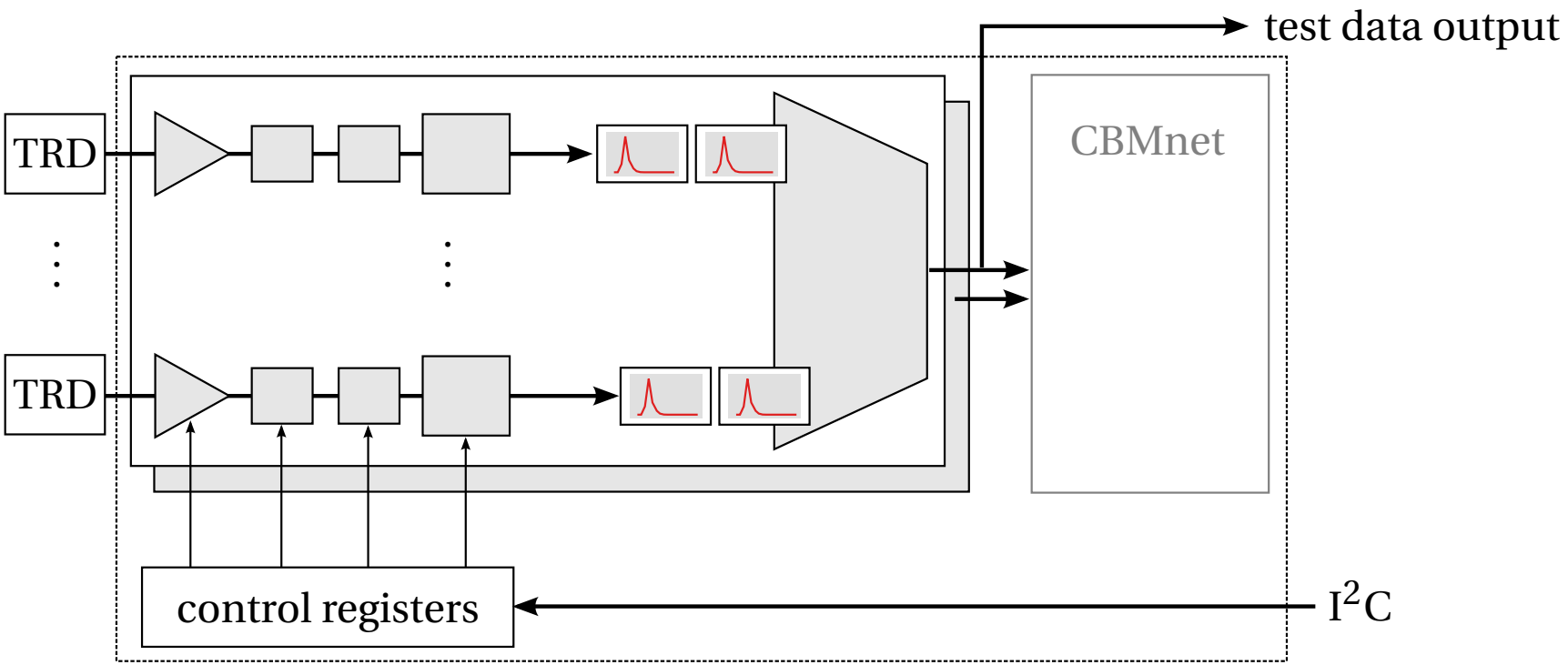
Hit logic


global trigger
neighbor trigger
self triggered:
double threshold
continuously arriving signal samples
trigger
logic
selection mask
message builder
message: pulse shape + metadata

SPADIC 1.0 FEB rev. A



Test setup without CBMnet

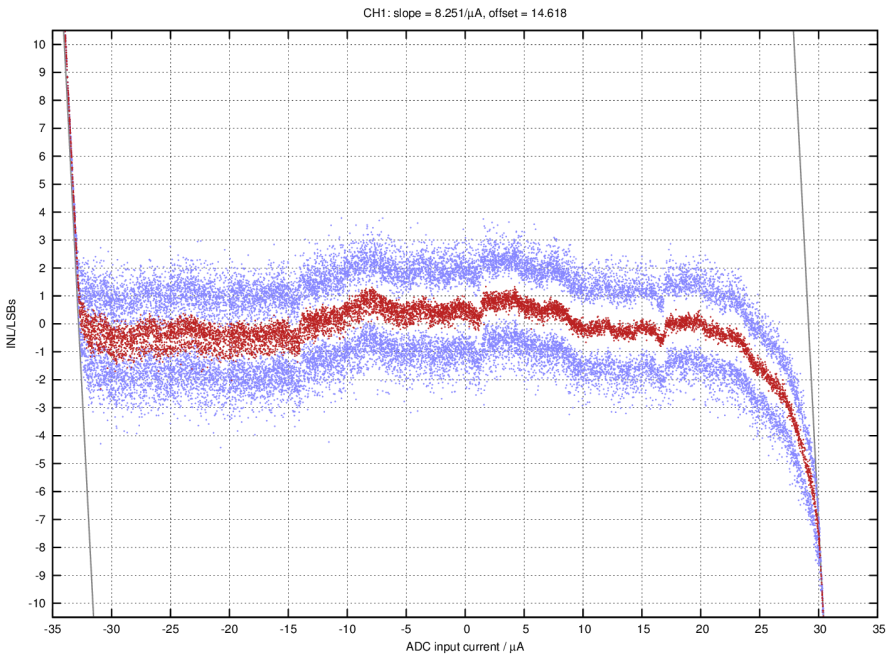


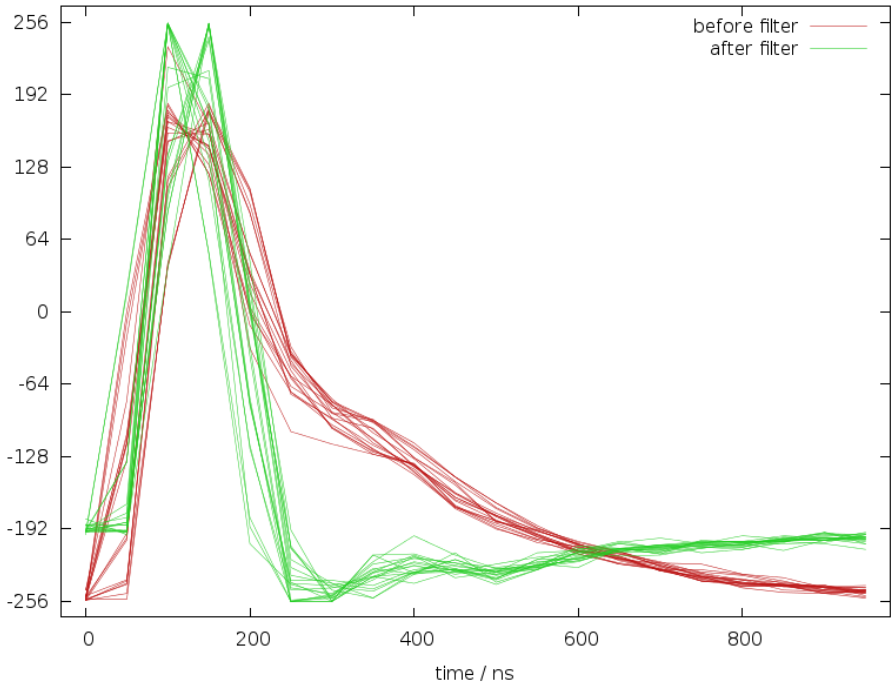
- first measurements made without CBMnet
- no stable connection
- only channel group A

First results

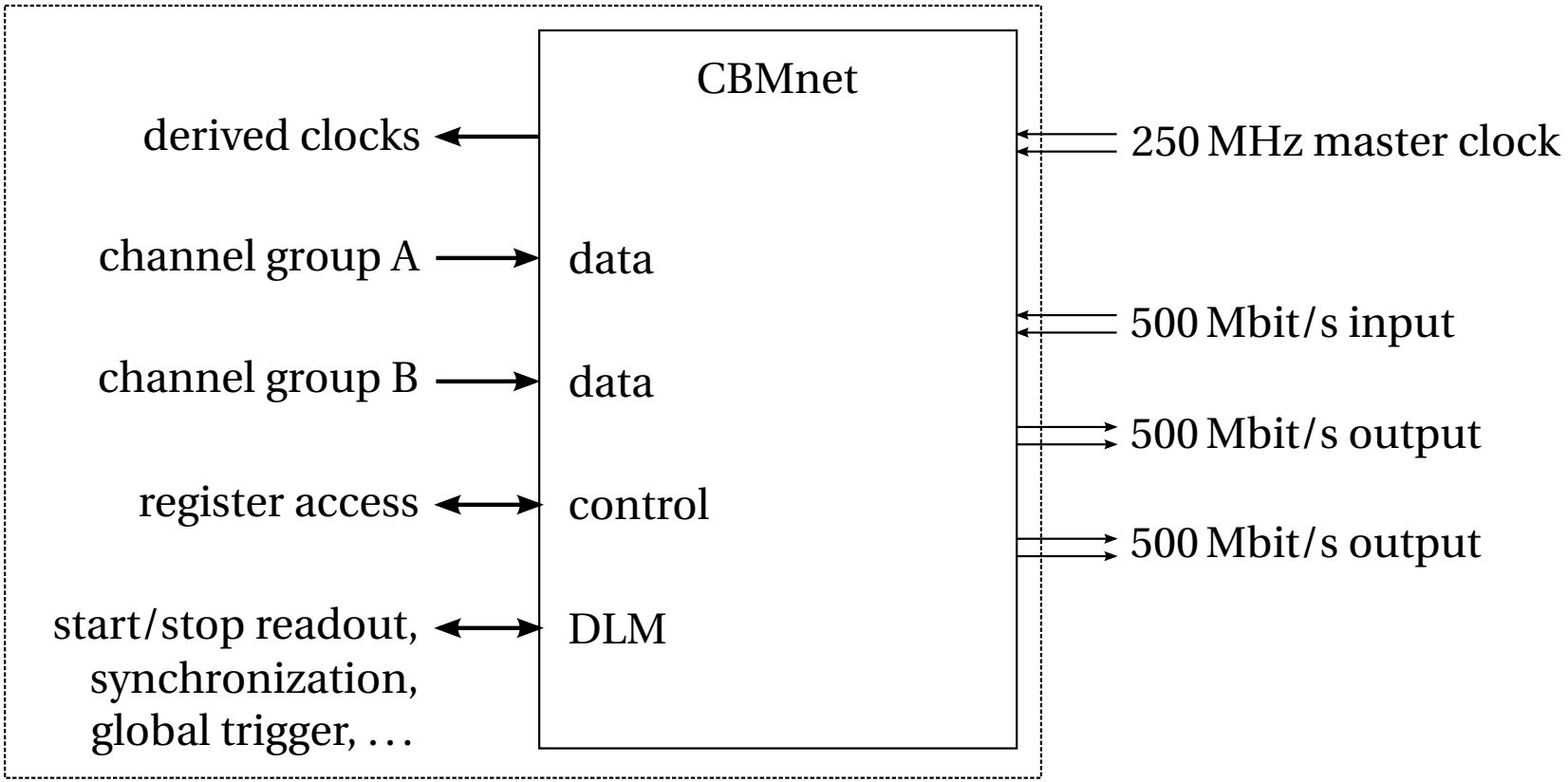
ADC INL curve/measured pulses:

- taken at 20 MHz sample rate, preliminary bias settings
- prove the function of the whole data path



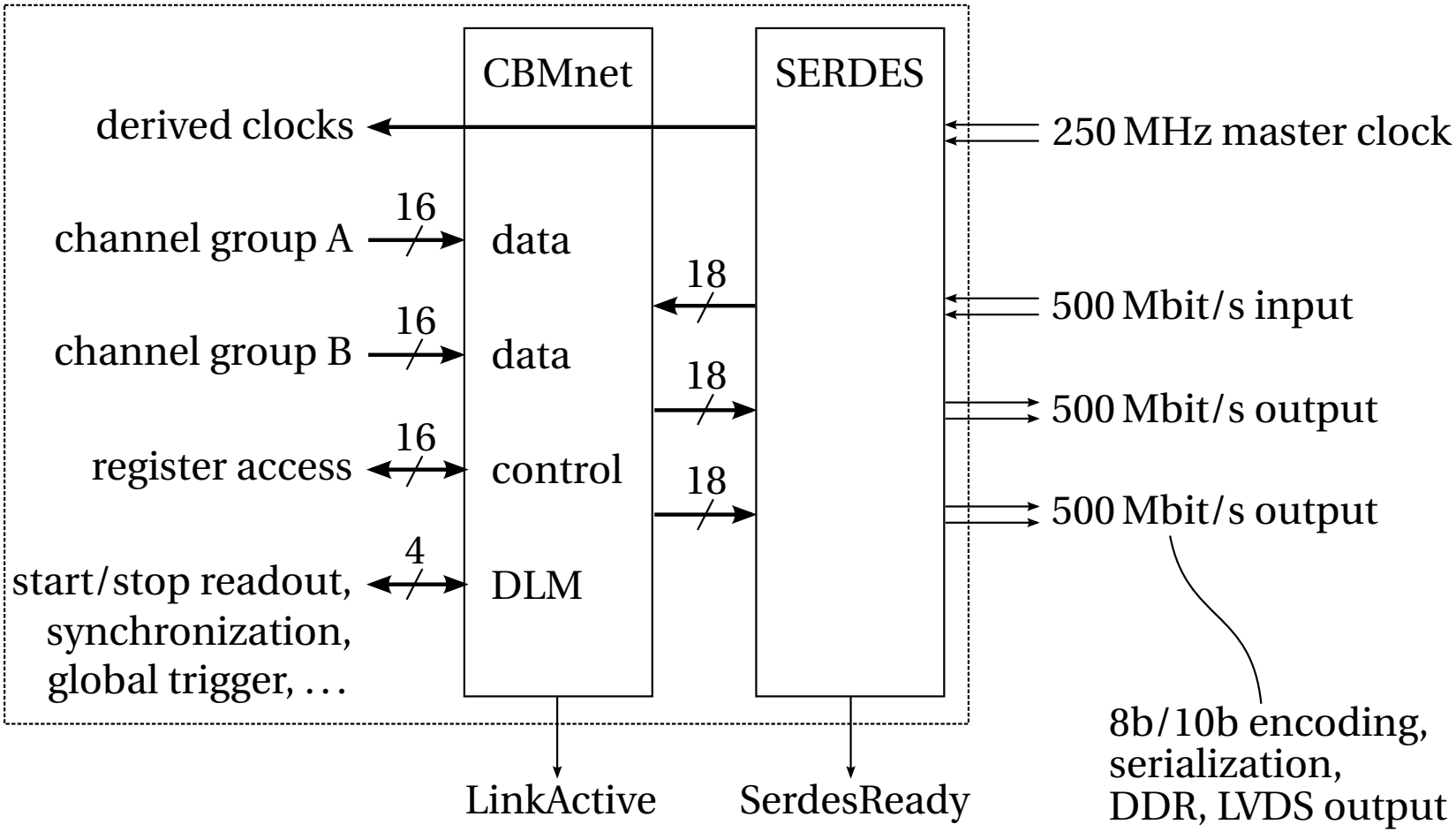


CBMnet from a user's point of view

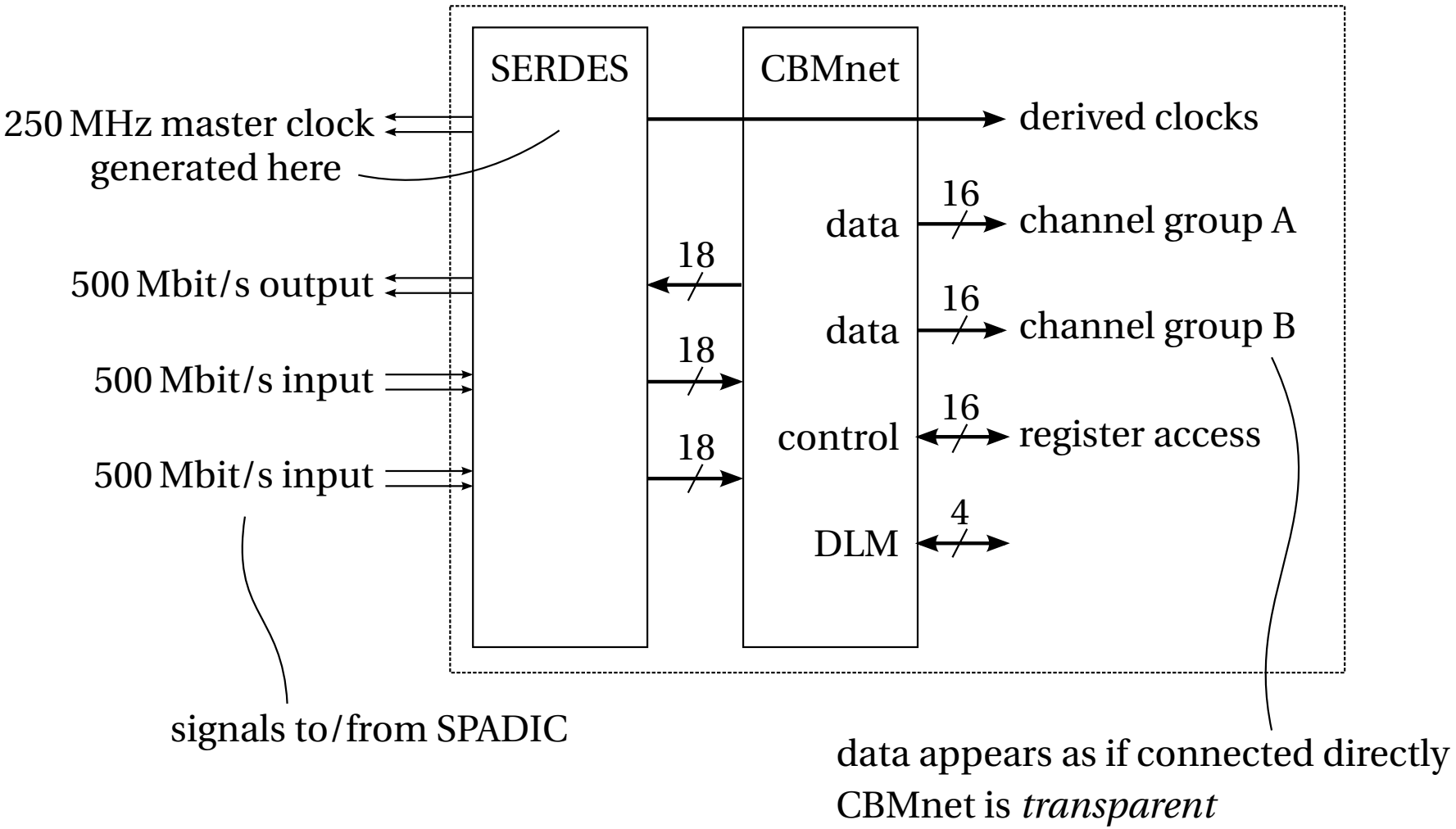


- CBMnet maps logical ports to physical links
- several ports share one link (DLM has priority)

CBMnet: a closer look



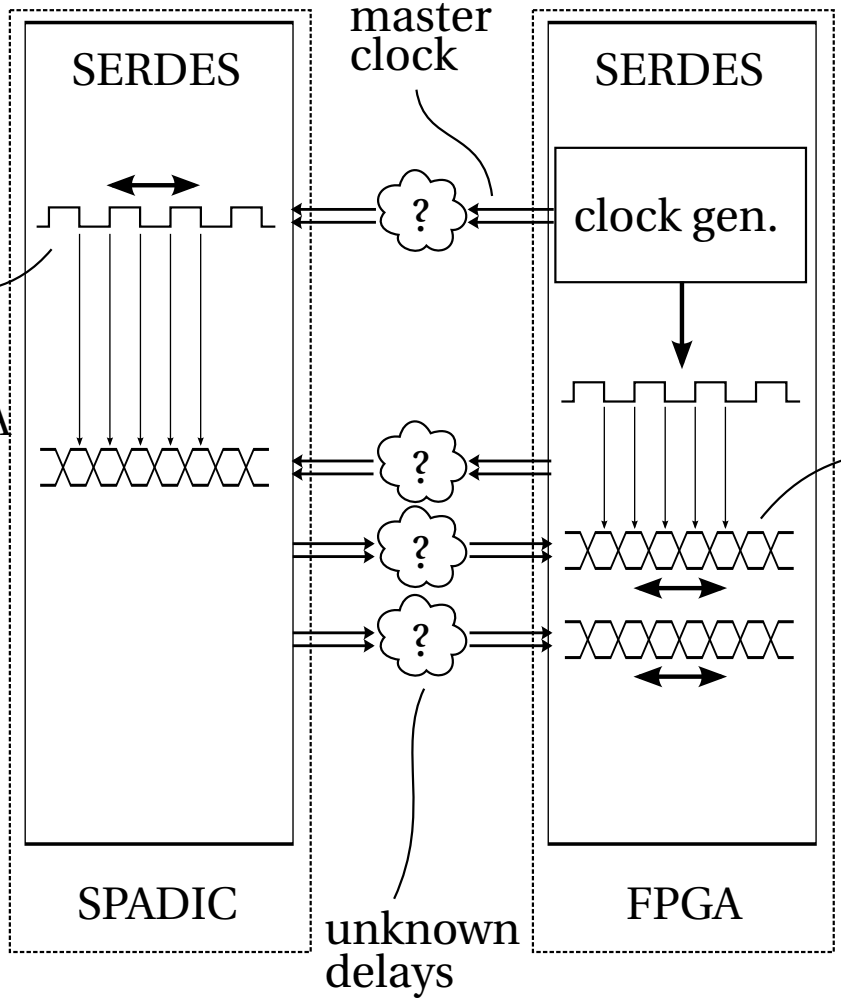
CBMnet: FPGA counterpart



CBMnet FPGA implementation history

- first implementation for SP605
- “did not work” on Susibo (symptoms: SerdesReady/LinkActive LEDs did not turn on)
- to find the problems, knowledge had to be build up first
- SERDES is the key (actual CBMnet block always worked)
- handling of the physical signals has to be correct *and* robust:
  - implementation that worked *sometimes* was found early
  - last problems identified & fixed last week
- selection of problematic details follows

Selected details I: delay adjustments



the ASIC has to sample the signals from the FPGA using the received clock
→ adjust delay of outgoing clock signal

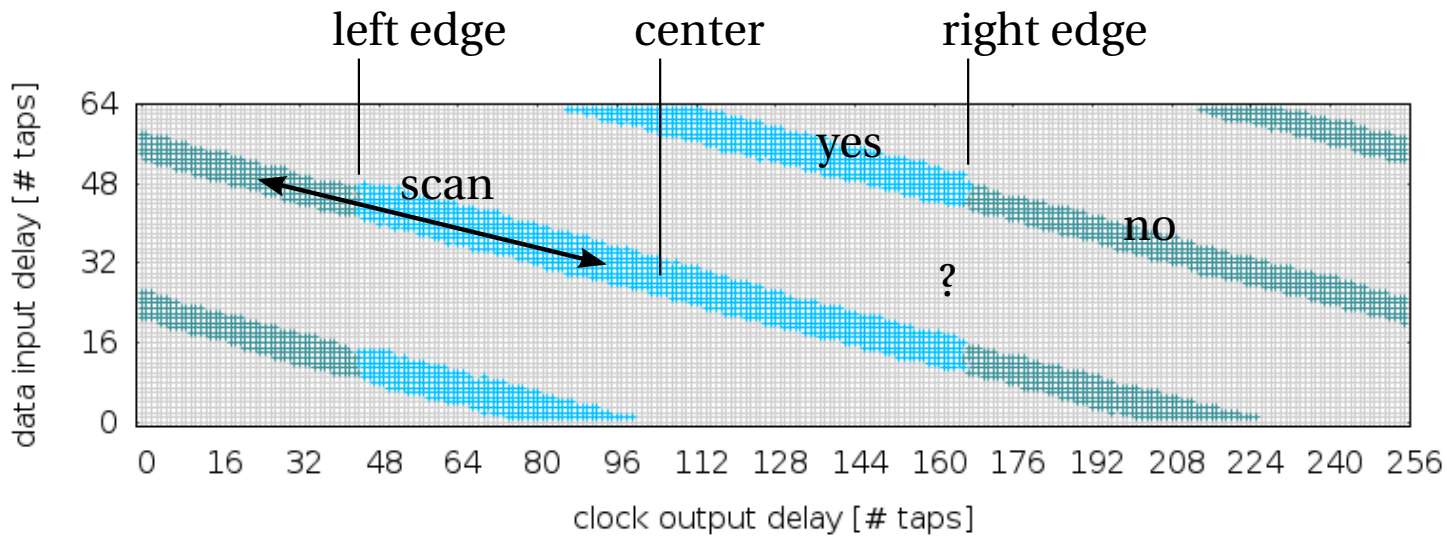
new in Susibo version!

the FPGA has to sample the signals from the ASIC using its own clock
→ adjust delay of incoming data signals

already done in SP605 version

Selected details I: delay adjustments

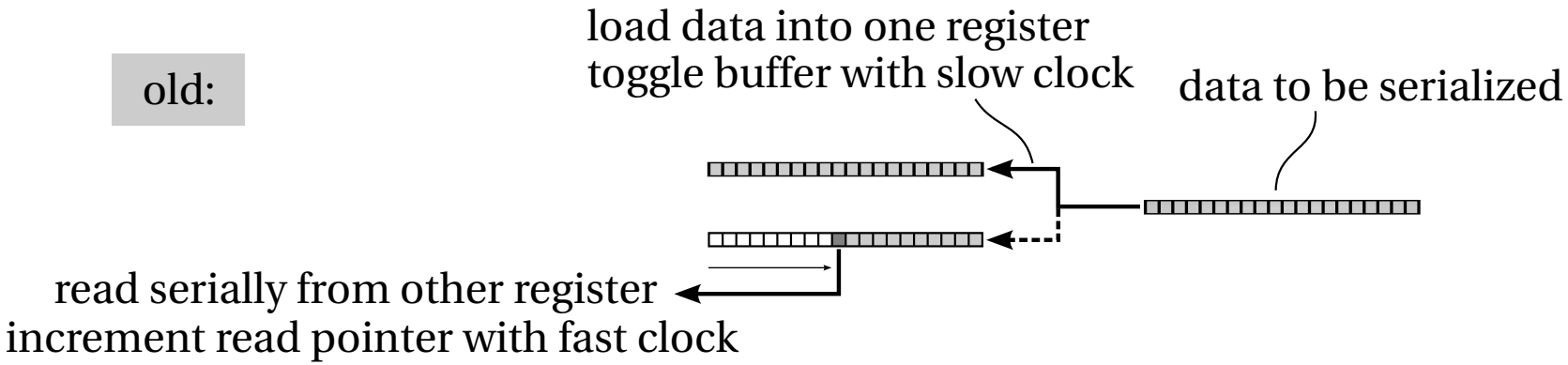
- problem: phase shifting the outgoing clock at the same time shifts the data signal that comes back
- correct values for both delay settings can not be found independently
- FPGA sends pattern, SPADIC tells FPGA if it can detect the pattern ("yes"/"no") – but can the FPGA detect the answer?



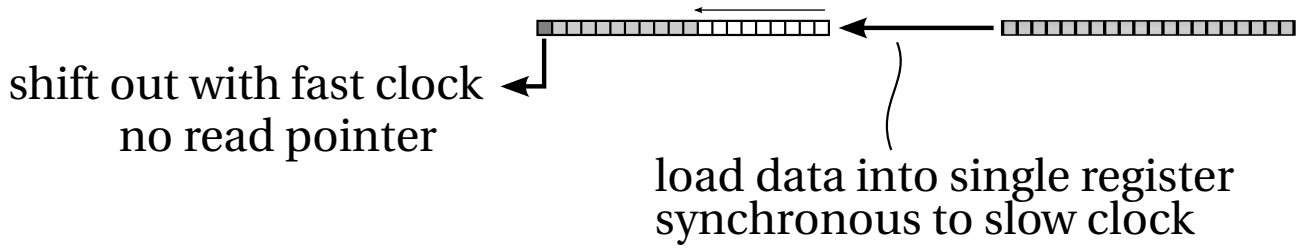
- problem until last week: *reliably* finding the edges (would detect false edges sometimes and end up in the wrong position)

Selected details II: serialization

old:



new:



- old version was not synchronized properly → sometimes a register was overwritten while being read out
- new version is simpler and less error-prone

Selected details III: SERDES handshake

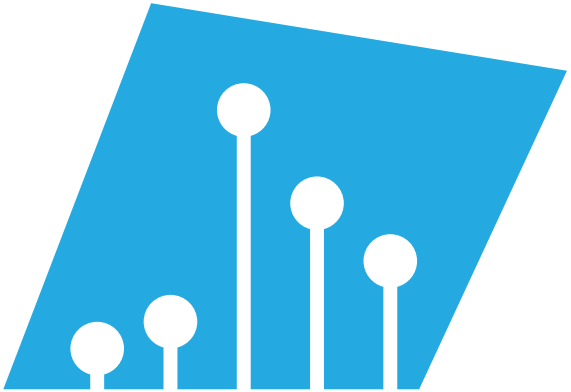
- after both SERDES (ASIC and FPGA) can correctly sample each others' signals (ensured by proper delay settings), they perform a handshake:
  - both send character "A"
  - after enough "A" has been seen, send character "B"
  - when "B" is seen → done (SPADIC signals this by SerdesReady LED)
- *feature:* SERDES on SPADIC side sometimes sends "B" once, and then "A" again → FPGA thinks ASIC is ready, but it's not
- solution: wait for several "B" in a row (found last week)

Summary

- SPADIC 1.0 readout over CBMnet using the Susibo works now
- main difference to original implementation: automatic clock delay adjustment
- final implementation is not really complicated, but identifying and solving all problems took long
- knowledge gained → assistance for other users offered

Next steps

- adapt test software
- make real measurements
- test other hardware configurations (HDMI cables, new FEB, etc.)



SPADIC

Self triggered Pulse Amplification and Digitization asIC

http://spadic.uni-hd.de