SPADIC – Self-triggered charge pulse processing ASIC

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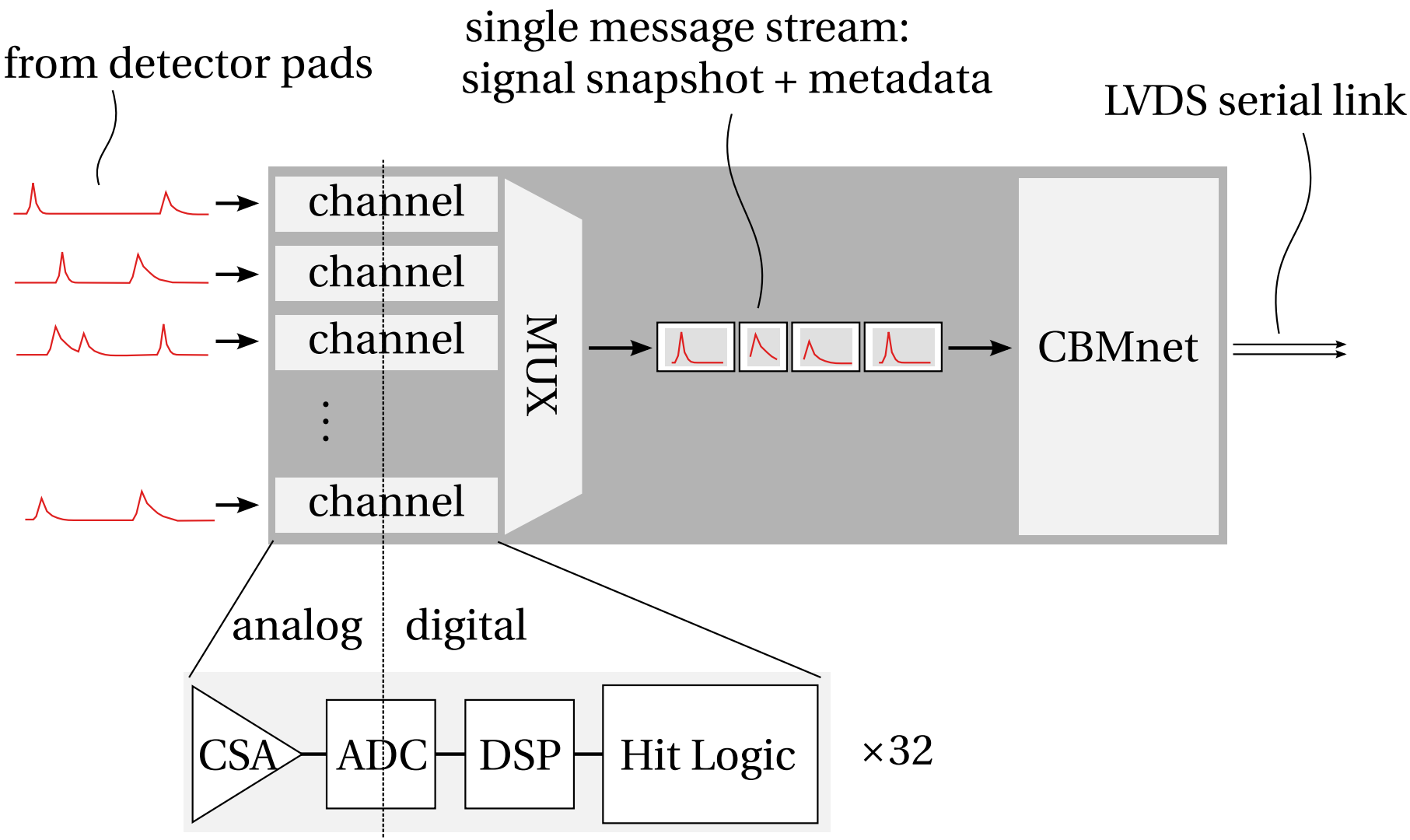
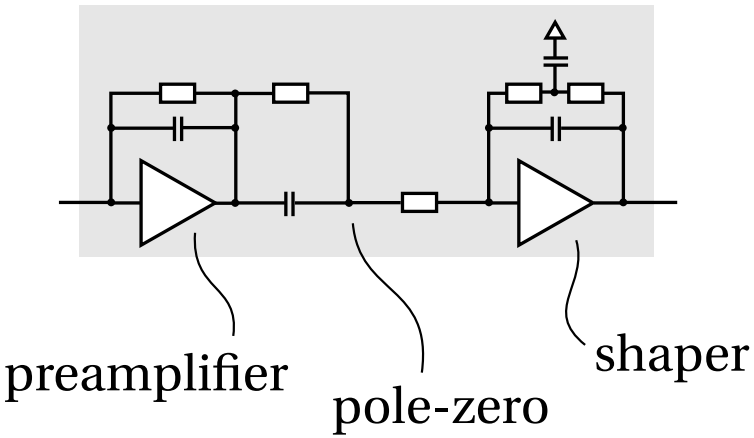
Introduction

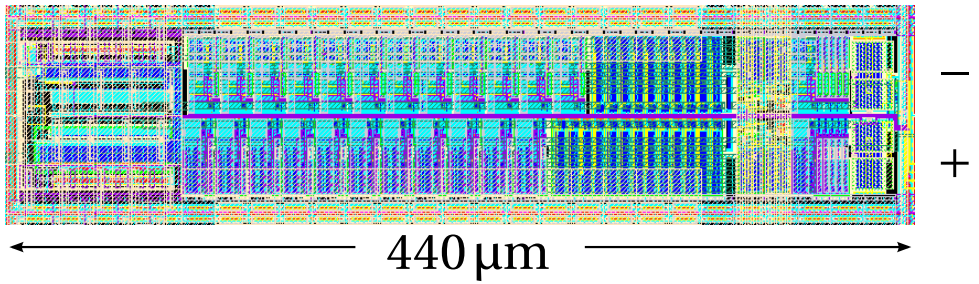
- Self-triggered Pulse Amplification and Digitization ASIC
- main application: TRD readout at CBM (FAIR/GSI)
- development since 2006, latest version 1.0 available since 2012

Concept


from detector pads
single message stream:
signal snapshot + metadata
LVDS serial link
channel
channel
channel
channel
MUX
CBMnet
analog
digital
CSA
ADC
DSP
Hit Logic
×32

Charge sensitive amplifier





- input range: 75 fC
- $h(t) \propto t \cdot e^{-t/\tau}$
- shaping time: $\tau = 80$ ns

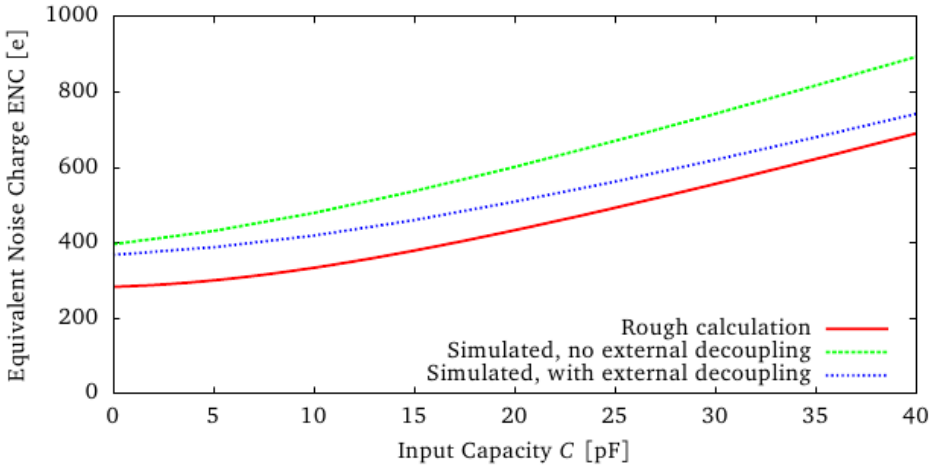
two amplifiers per channel selectable:

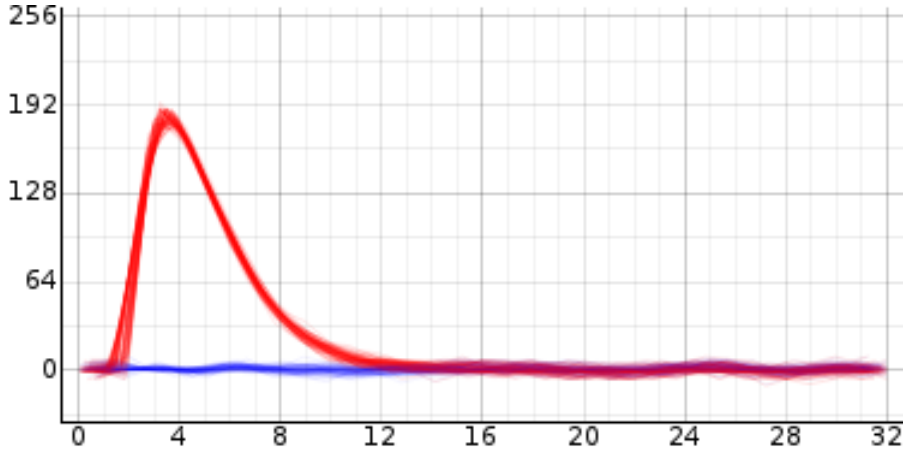
- positive polarity (4 mW)
- negative polarity (10 mW, not optimized)

layout & schematics: modular, scalable

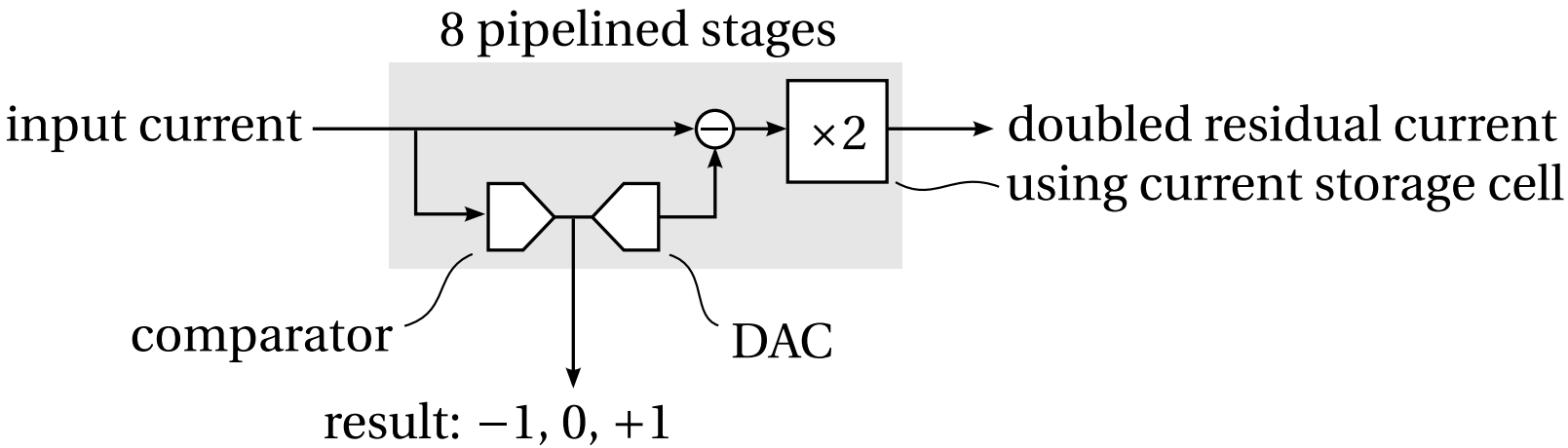
CSA characterization

- simulation + previous testchips:
  ENC = 800 e^- @ 30 pF
  (300 e^- @ 0 pF)
- measurements with latest setup ongoing
- tuning of bias settings → local noise minimum found
- "900 ± 900" e^- → careful calibration of measurement procedure needed to give exact numbers





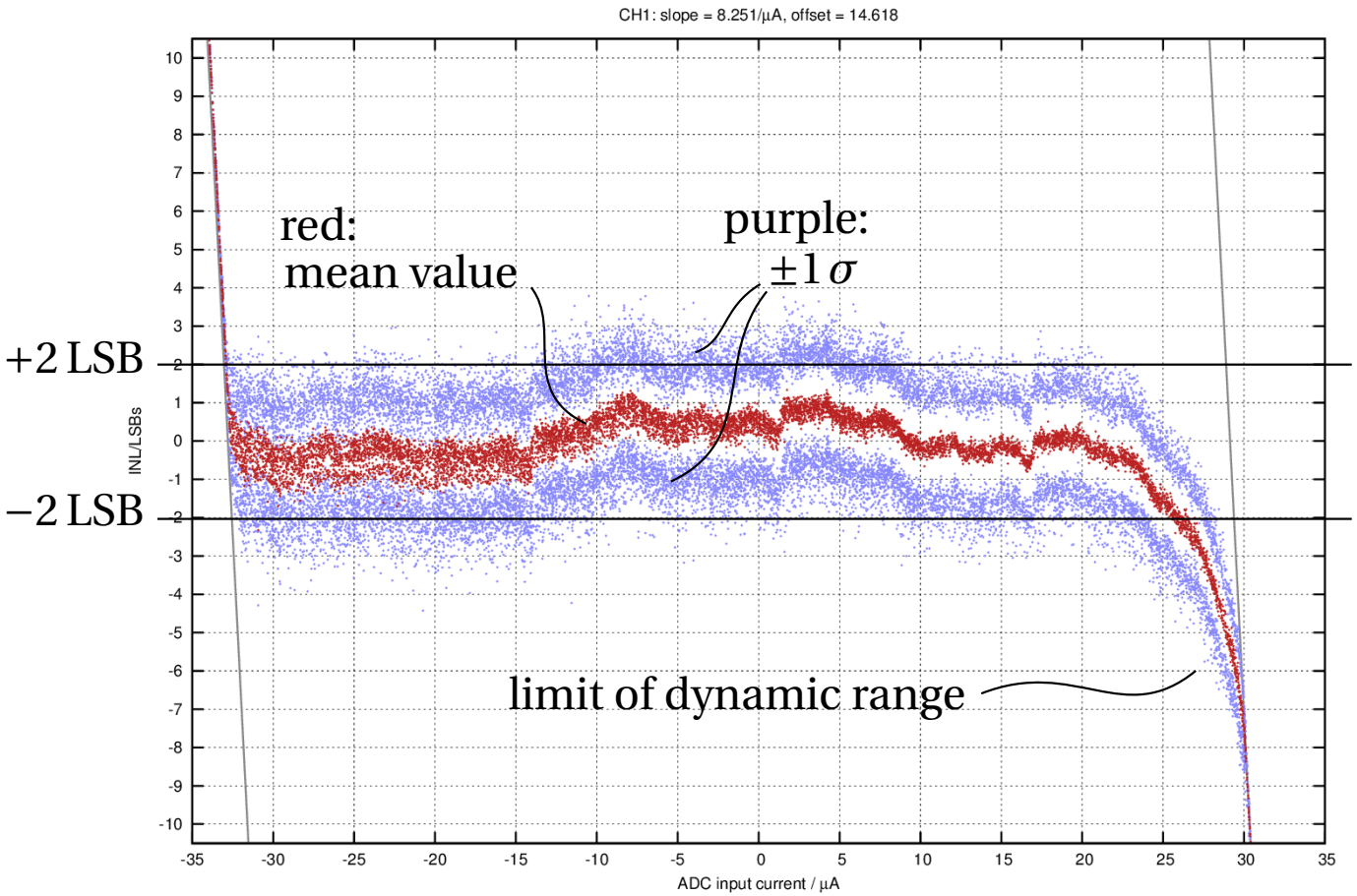
ADC



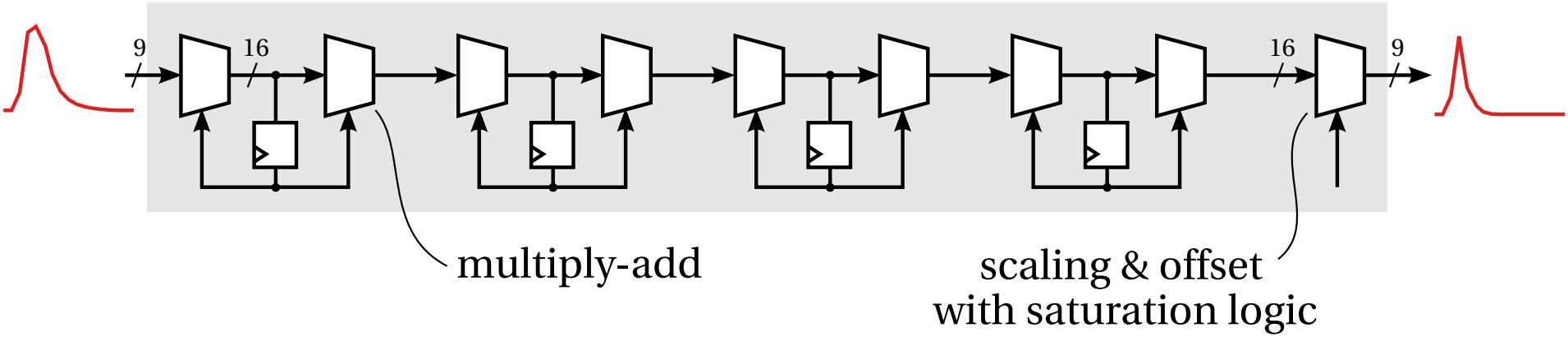
- current mode pipelined design
- 25 MHz sample rate, continuously running
- 9 bit nominal output (2's complement)
- resolution ≈ 8 bits
- 4.8 mW, $400 \times 300\,\mu m^2$

ADC measurements

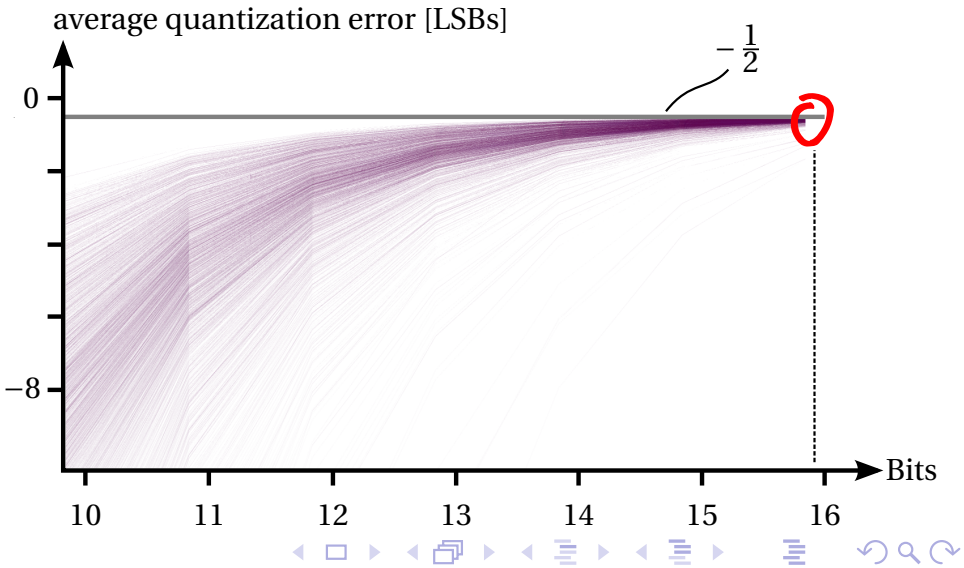
INL + noise: static measurements at 20 MHz sampling rate (preliminary bias settings)



Digital signal processing



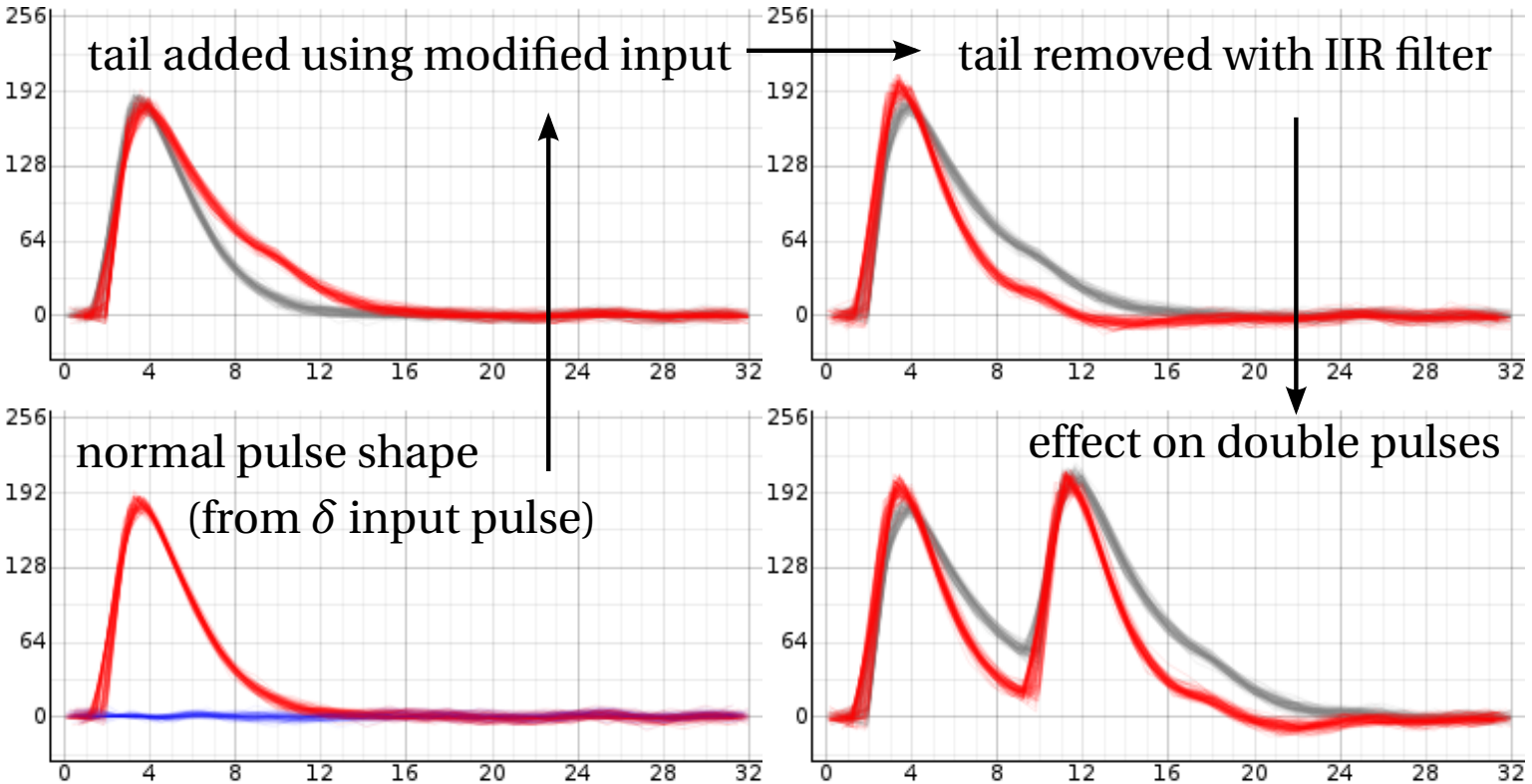
- IIR filter with 4 first order stages
- 16 bit internal resolution
- 6 bit coefficients
- freely programmable $(-\frac{32}{32}, \ldots, +\frac{31}{32})$



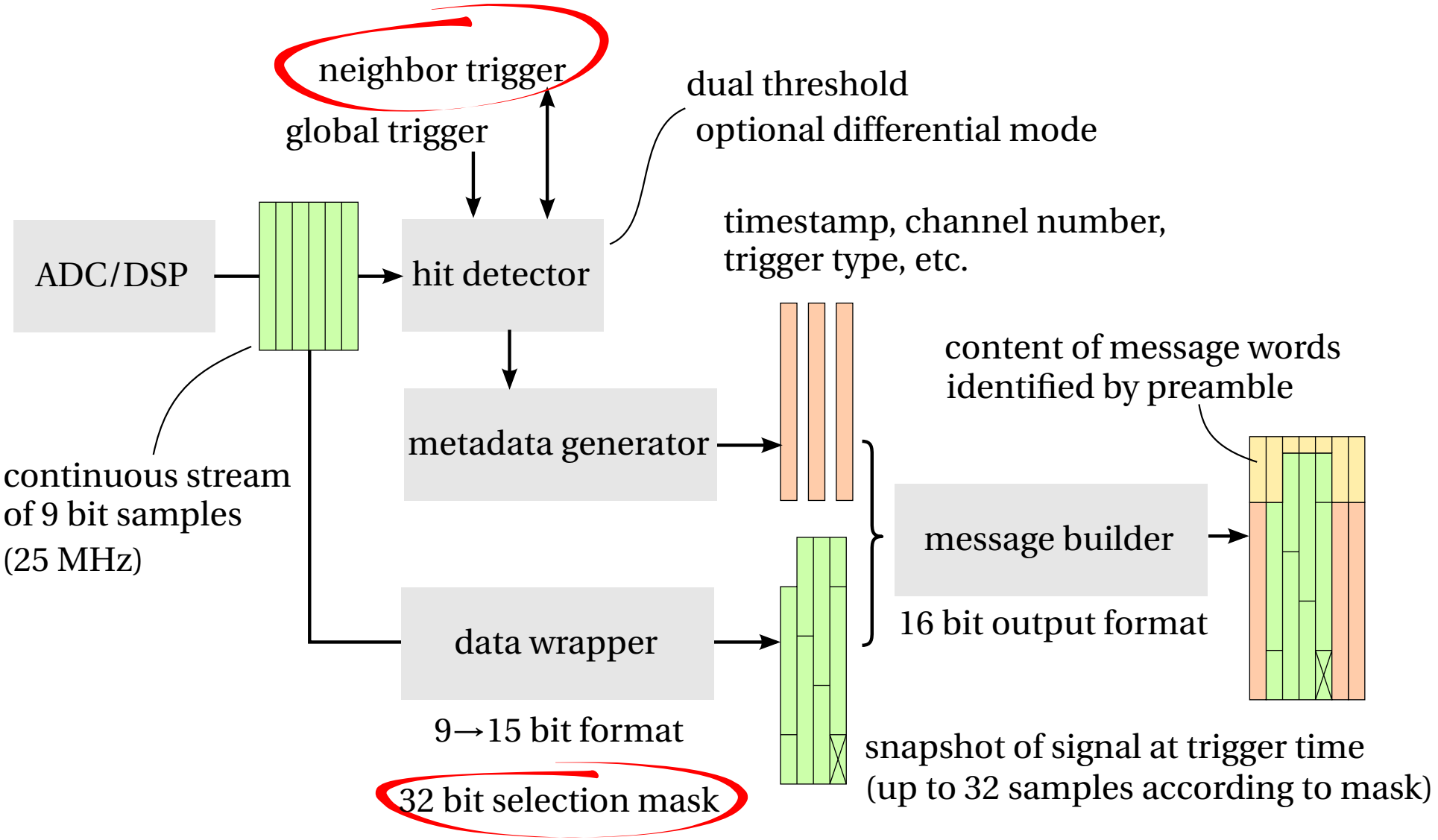
Digital signal processing

purpose: “ion tail” cancellation

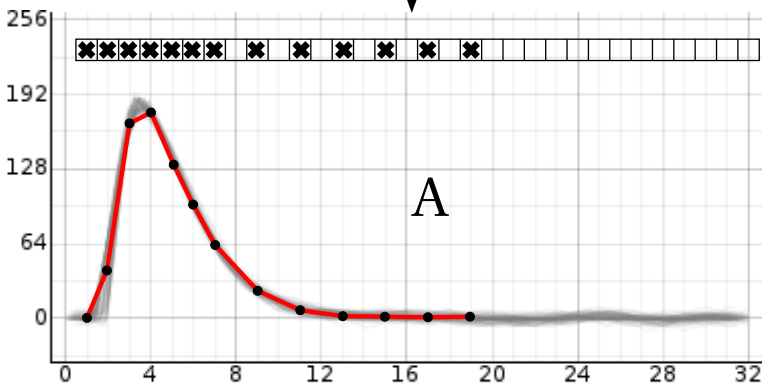
shorten pulses → reduce pileup/help hit logic

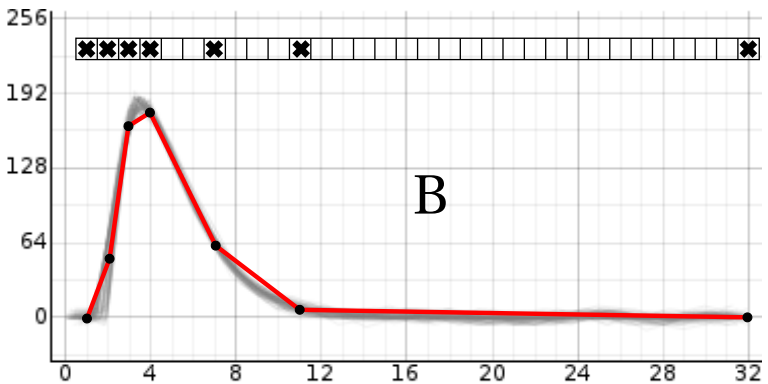


Hit logic


neighbor trigger
global trigger
dual threshold
optional differential mode
ADC/DSP
hit detector
timestamp, channel number,
trigger type, etc.
content of message words
identified by preamble
metadata generator
continuous stream
of 9 bit samples
(25 MHz)
message builder
16 bit output format
data wrapper
9→15 bit format
32 bit selection mask
snapshot of signal at trigger time
(up to 32 samples according to mask)

Selection mask examples





message data (hex)

801F
9082
AEEF
5AFF
3FDF
73E1
2840
007E
0F77
47E2
B350

} 13 samples contained

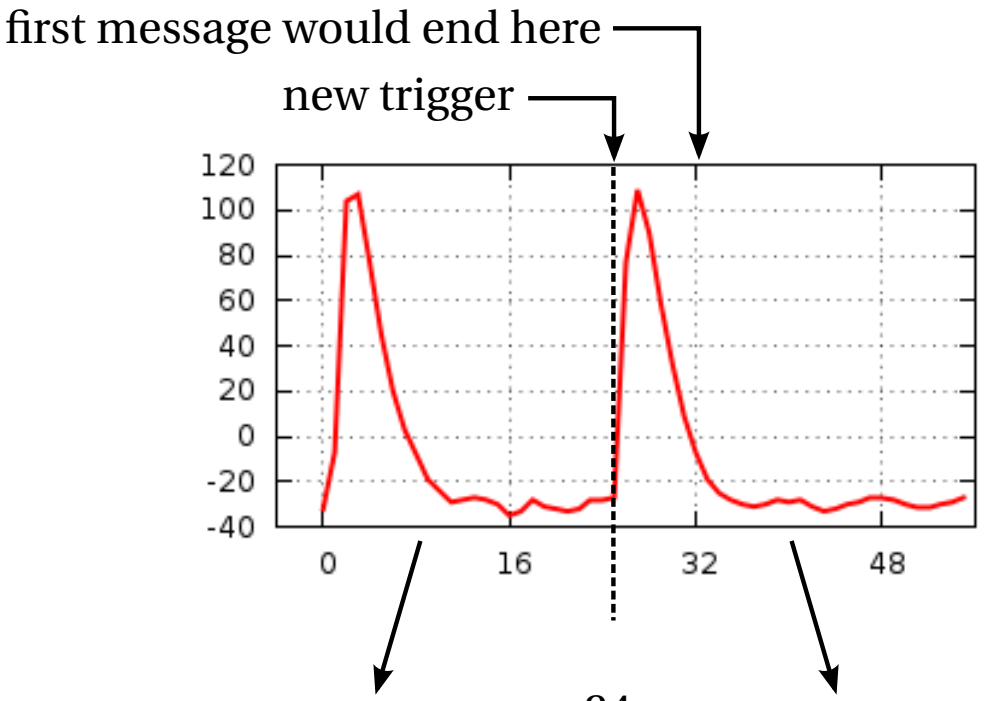
801F
9E4D
AF0F
52FF
3FCA
404F
4200
B1D0

} 7 samples contained

→ allows tradeoff between quality of signal reconstruction and data volume

Multi hits

What happens when a channel is triggered again, before the current message is completed?



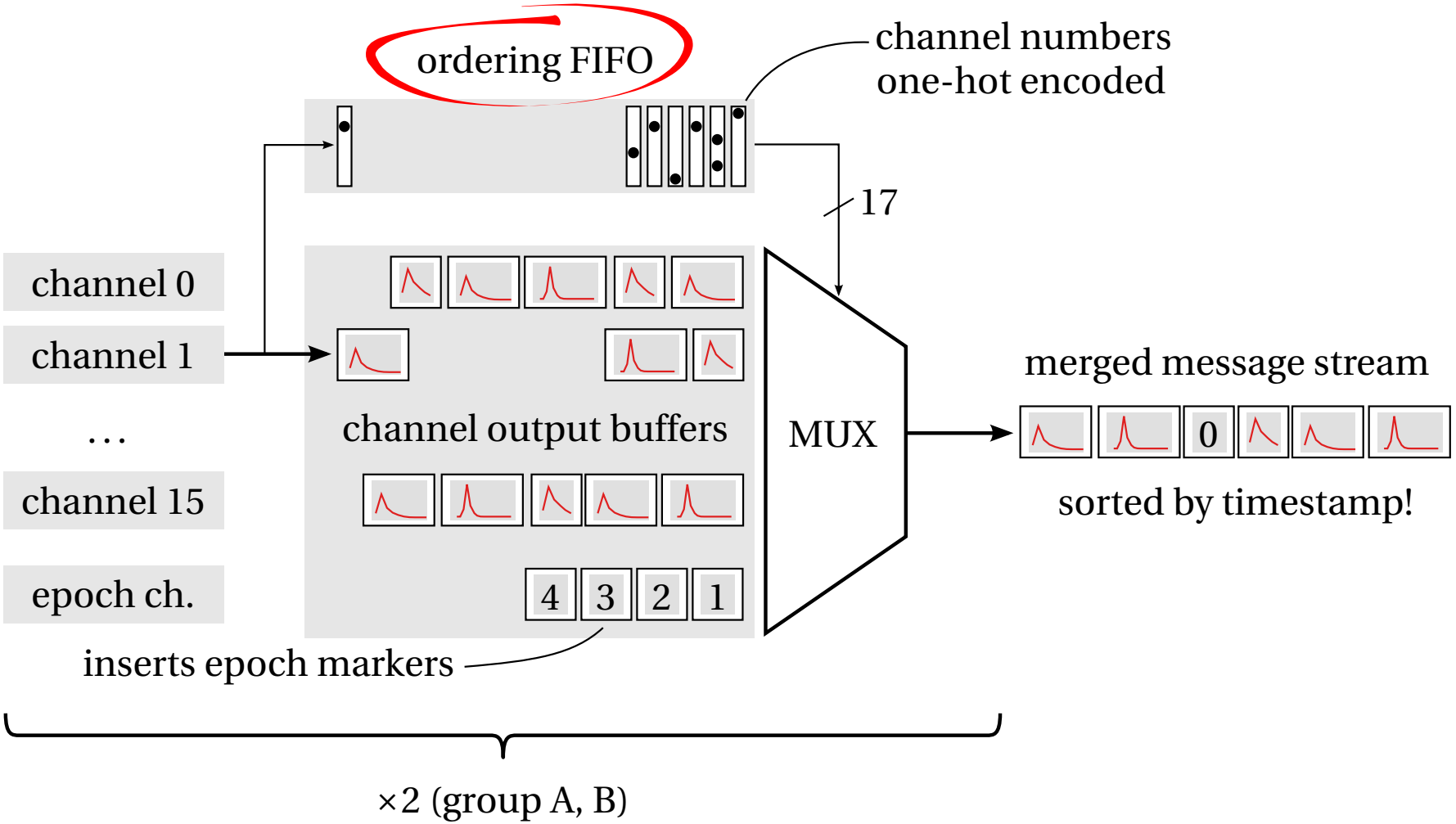
first message is gracefully aborted

selection mask is restarted
(in this example, all samples are selected...)

timestamp: 3031 —+24→ timestamp: 3055
data (24 values): -30, ..., -35
hit type: self triggered
stop type: multi hit

data (32 values): -31, ..., -32
hit type: self triggered
stop type: normal end of message

Message output multiplexing

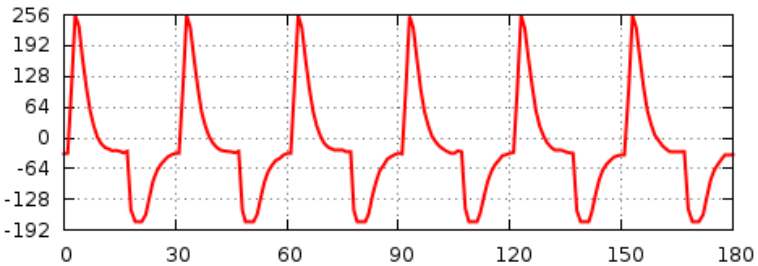


Error handling

What happens when a channel output buffer is full? Test case:

input signal: square wave, period = 30 time bins (>600 kHz hit rate)

reconstructed output signal: no problem with only one channel active



force buffer overflow with neighbor trigger → MUX can't read fast enough

timestamp: 3525
data (30 values): ...
hit type: self triggered
stop type: multi hit

+30

timestamp: 3555
data (20 values): ...
hit type: self triggered
stop type: channel buffer full

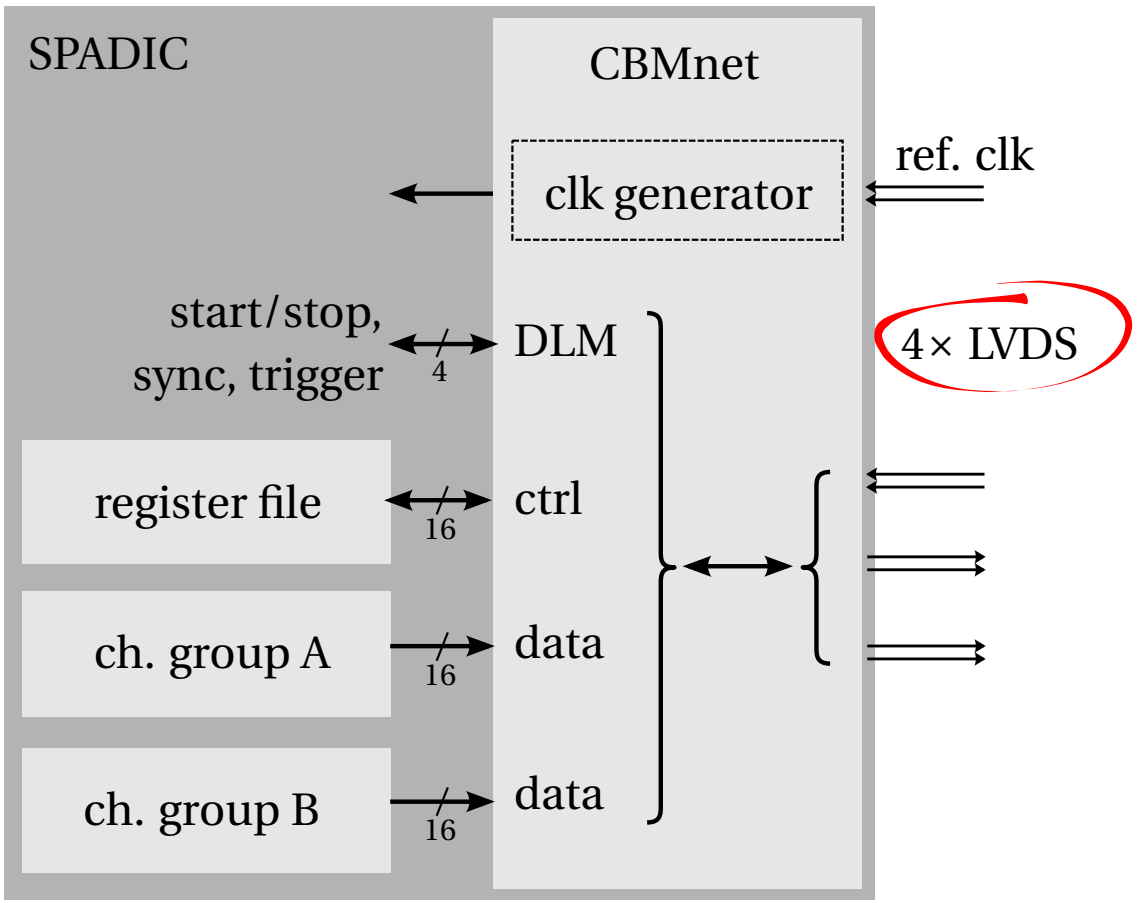
+2 × 30

timestamp: 3615
buffer overflow count: 2

special info message

→ Similarly for ordering FIFO, incl. handling of flipped bits (SEU).

CBMnet interface

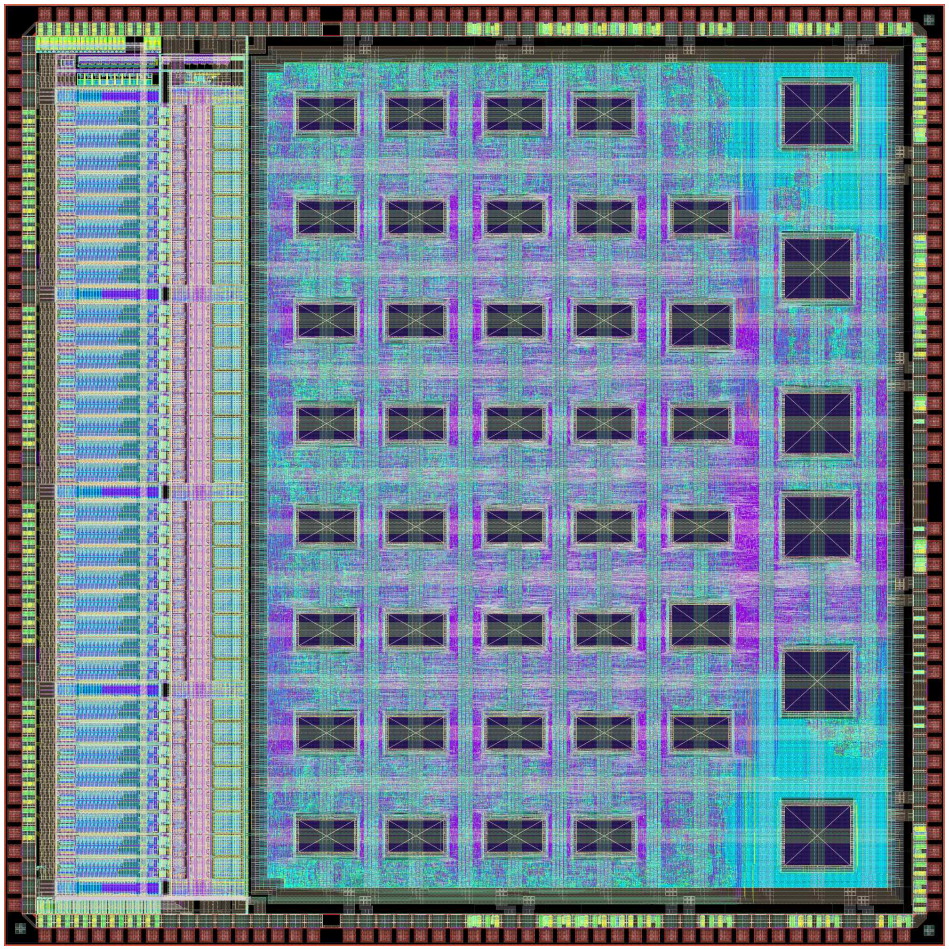


- error checking, retransmission
- *deterministic latency messages (DLM)*
- maps data + control traffic to serial LVDS links
- 500 Mbit/s (DDR), 8b/10b encoded (1 input, 2 outputs)

Current status & lookout

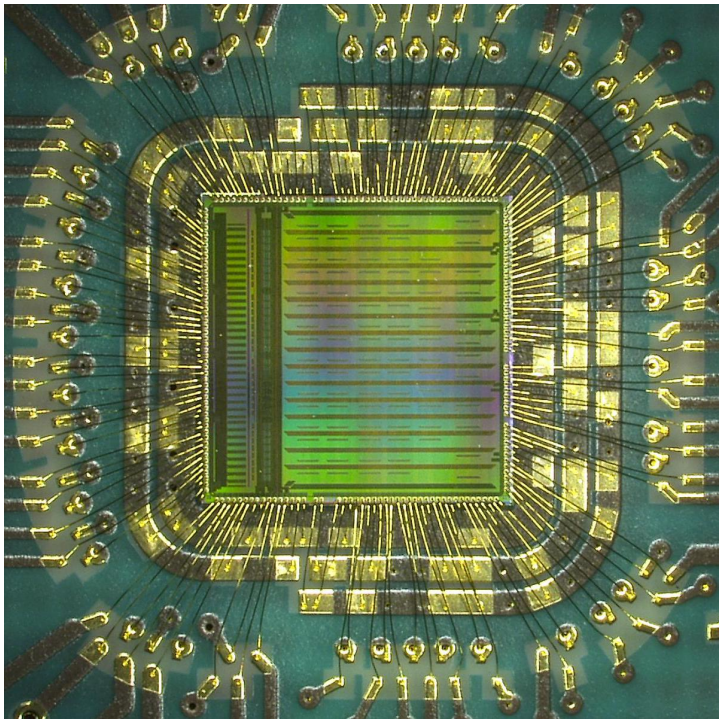
- complete test environment (firmware, software) built up during past months
- all parts/features of the ASIC in operation
- no major bugs discovered that can't be worked around
- characterization of the analog part (CSA, ADC) ongoing
- soon: preparation of multi-chip modules for further beamtests next year

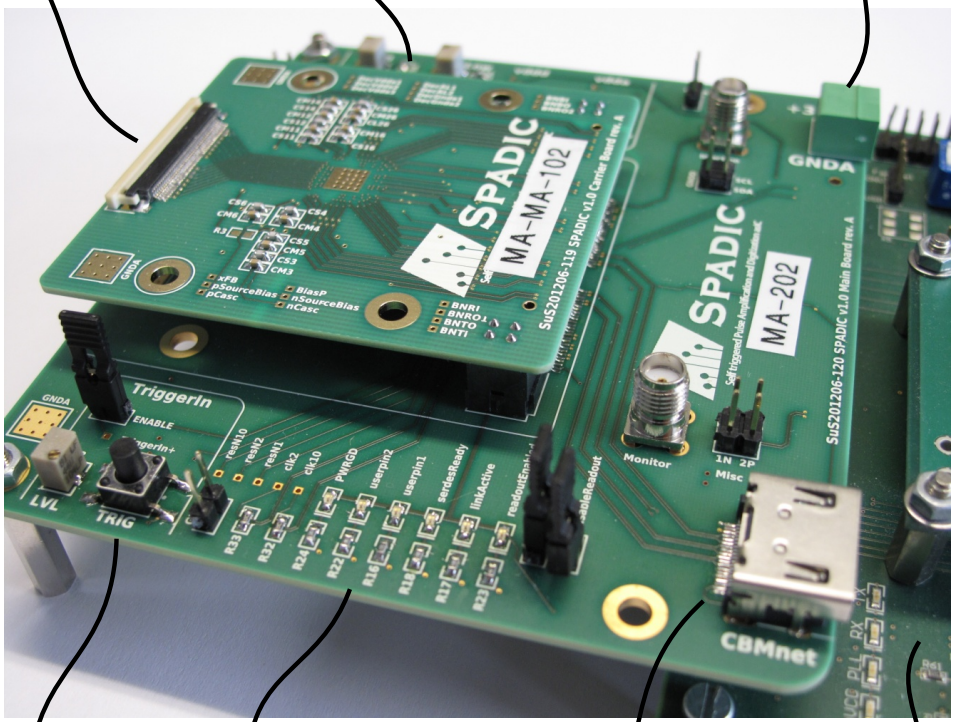
Layout view



- UMC 180 nm
- overall size: $5 \times 5\,\mathrm{mm}^2$
- digital part:
  - $3.5 \times 4.5\,\mathrm{mm}^2$
  - home-made standard cell library
  - 2.5 million transistors, 23k FF, 81k gates
  - 44 Faraday SRAMs
  - total wire length: 14.4 m
  - Power (200 MHz): 600 mW

Test setup





detector

voltage regulators

power

test pulse injection

status LEDs

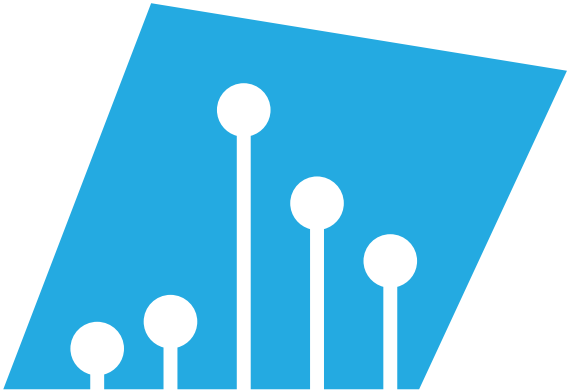
CBMnet (HDMI)

FPGA board *Susibo* → USB

Summary

SPADIC – complete system for charge pulse readout

- 32 channels
- self-triggered recording of whole pulse shapes @ 25 MHz
- programmable selection mask
- neighbor trigger, global trigger
- flexible digital signal processing
- handling of unusual/error conditions (multi hits, buffer overflow, . . .)
- CBMnet interface: reliable data transmission and synchronization features using 4 LVDS pairs



SPADIC

Self triggered Pulse Amplification and Digitization asIC

http://spadic.uni-hd.de