SPADIC – Status and plans

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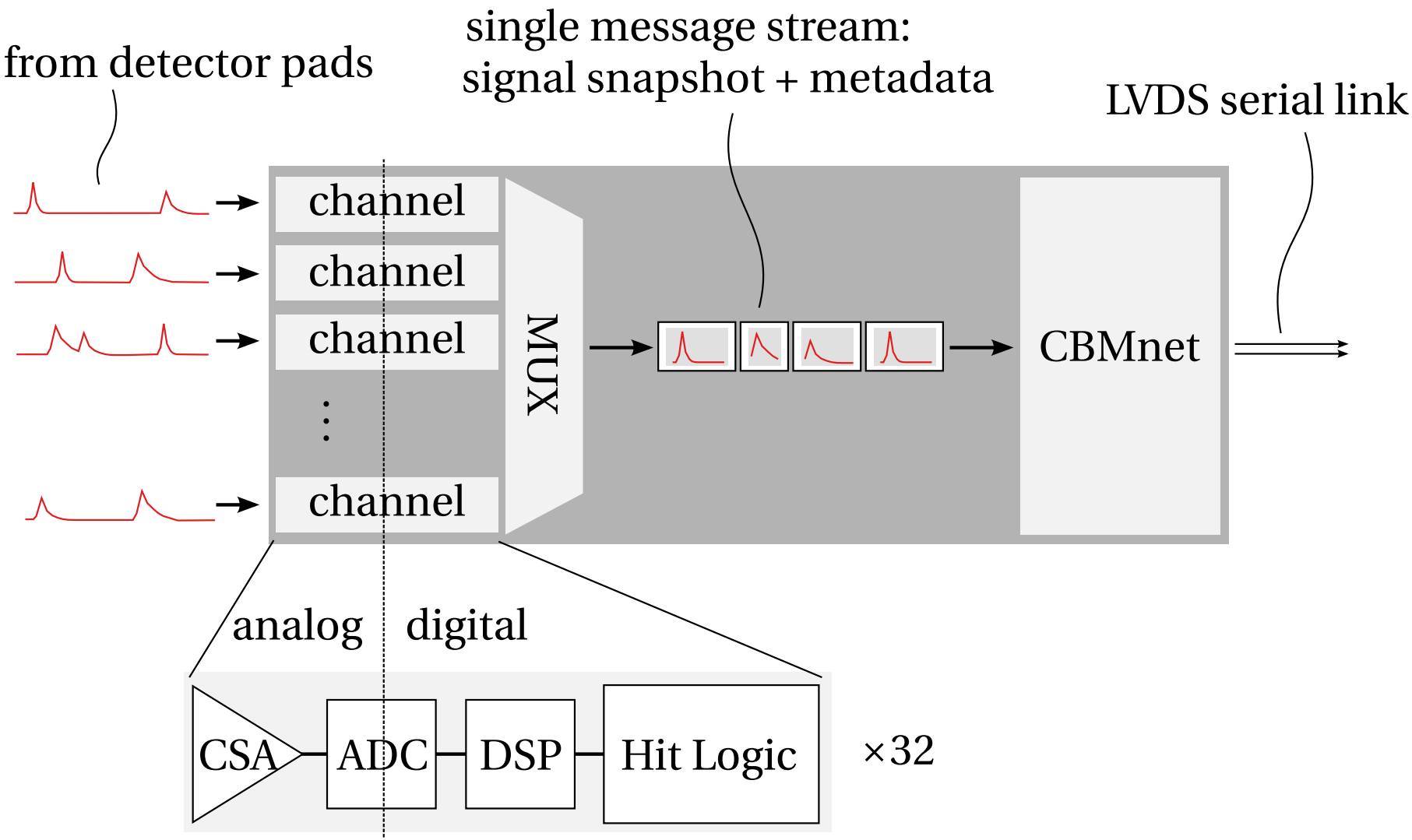
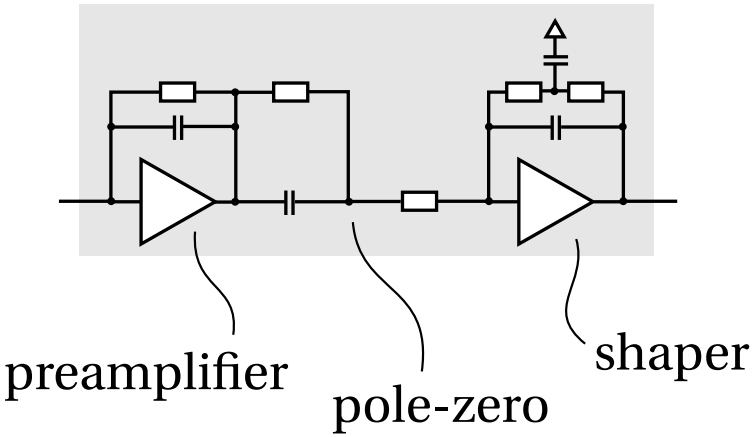
TRD Strategy Meeting

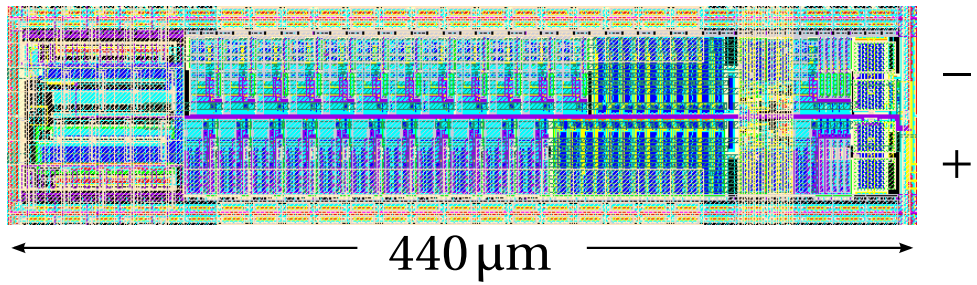
29.11.2013

Reminder: SPADIC 1.0 architecture



Charge sensitive amplifier





- input range: 75 fC
- $h(t) \propto t \cdot e^{-t/\tau}$
- shaping time: $\tau = 80$ ns

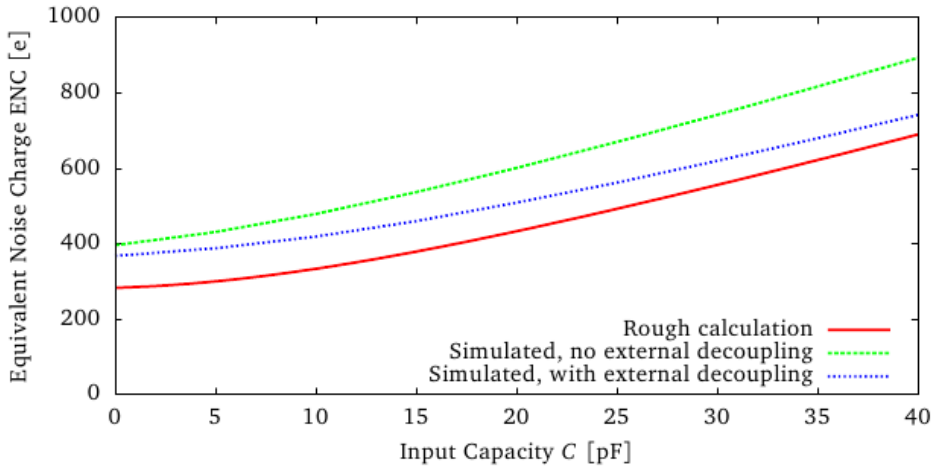
two amplifiers per channel selectable:

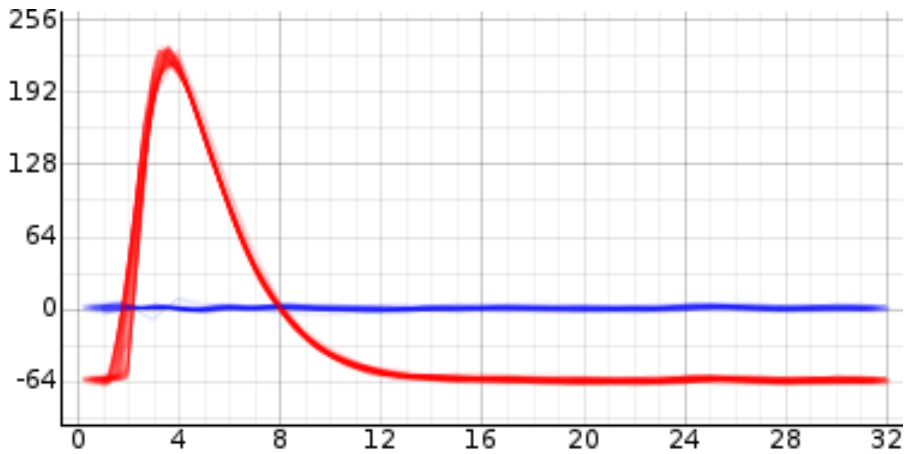
- positive polarity (4–5 mW)
- negative polarity (10 mW, not optimized)

layout & schematics: modular, scalable

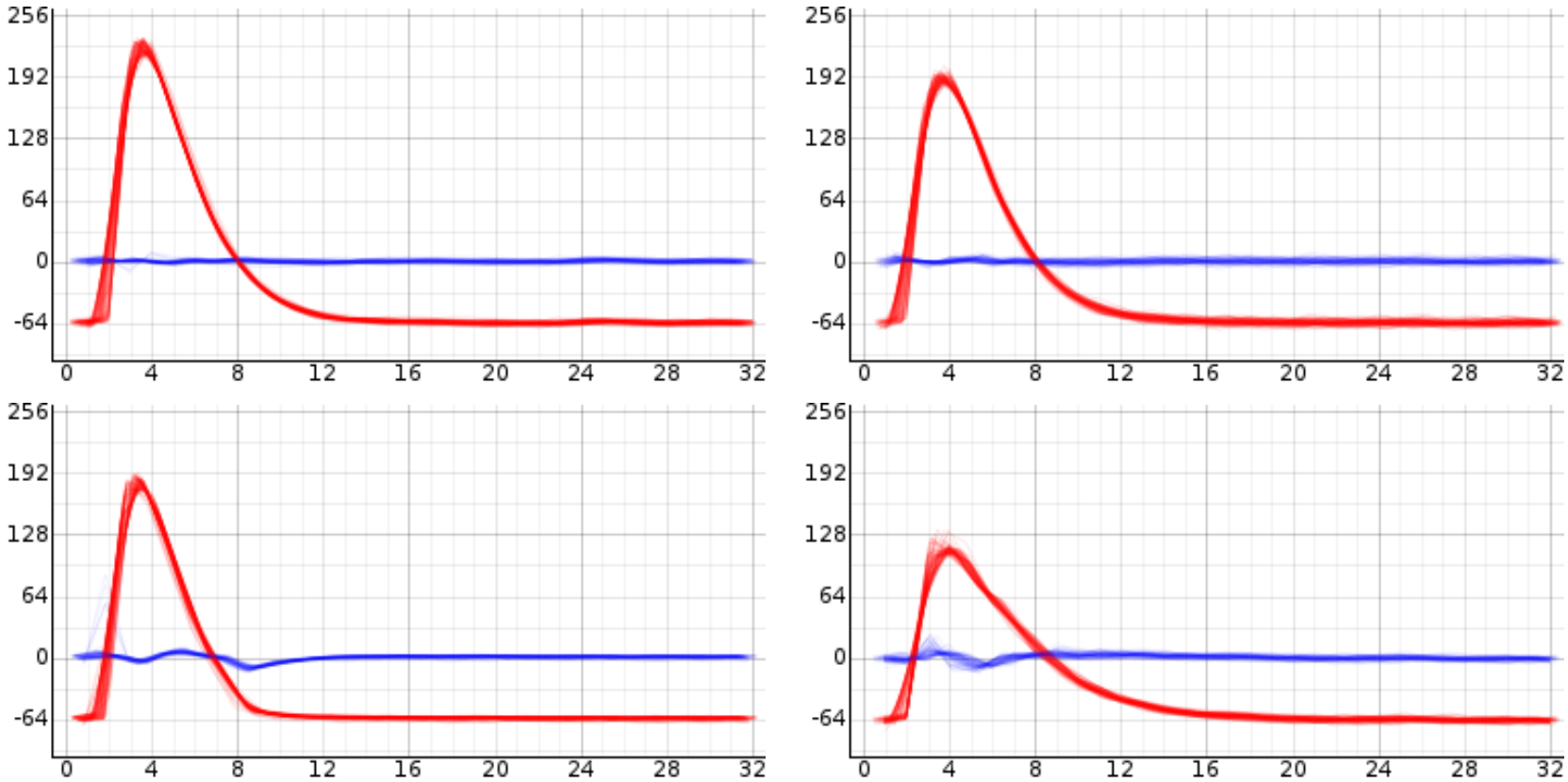
CSA characterization

- simulation + previous testchips:
  ENC = 800 e^- @ 30 pF
  (300 e^- @ 0 pF)
- tuning of bias settings → local noise minimum
- ENC = $\frac{q}{\mathrm{S/N}(q)} = q \cdot \frac{\sigma}{h(q)}$
- $q \stackrel{?}{=} 1.8\,\mathrm{V} \cdot 15(?)\,\mathrm{fF}$
- S/N ≤ 180 (CSA + ADC)

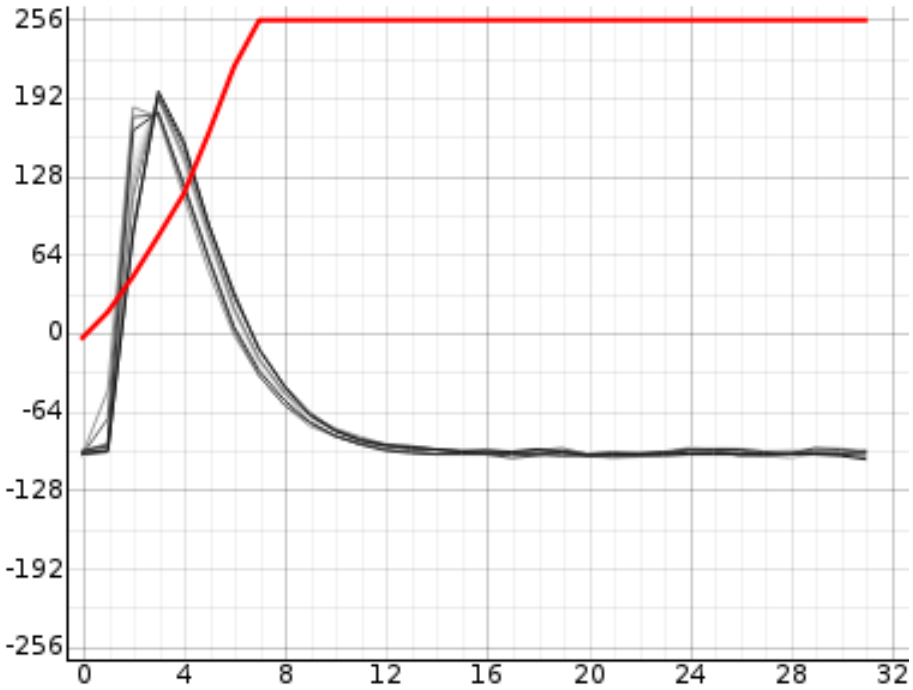




CSA pulse shapes

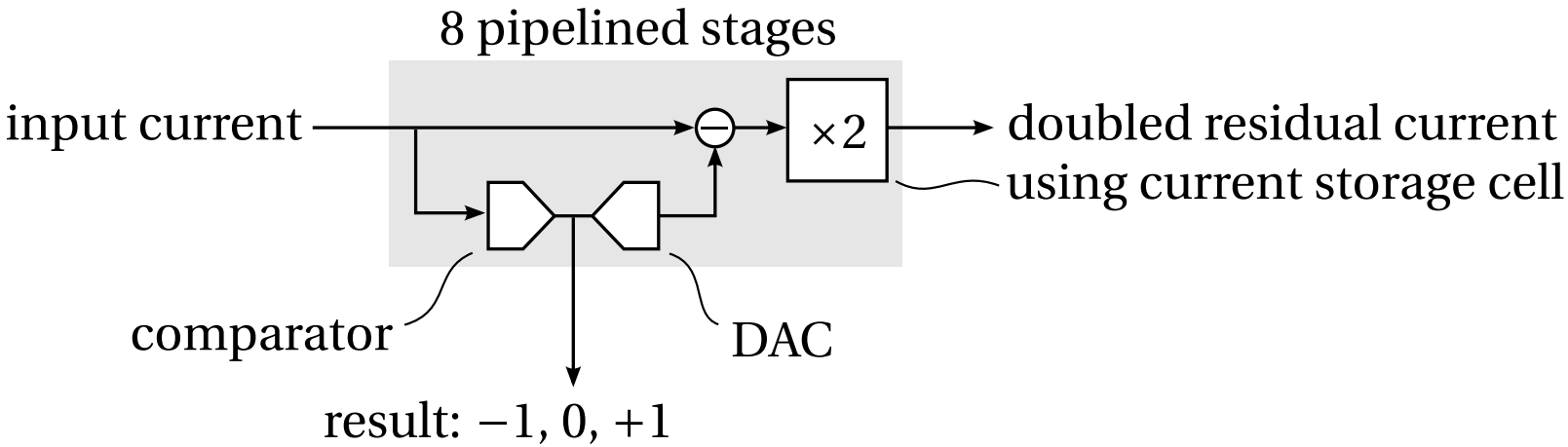


CSA “jump”



- increase R_{FB} → CSA jumps away from op. point
- recover: turn amplifier off/on
- luckily away from good settings

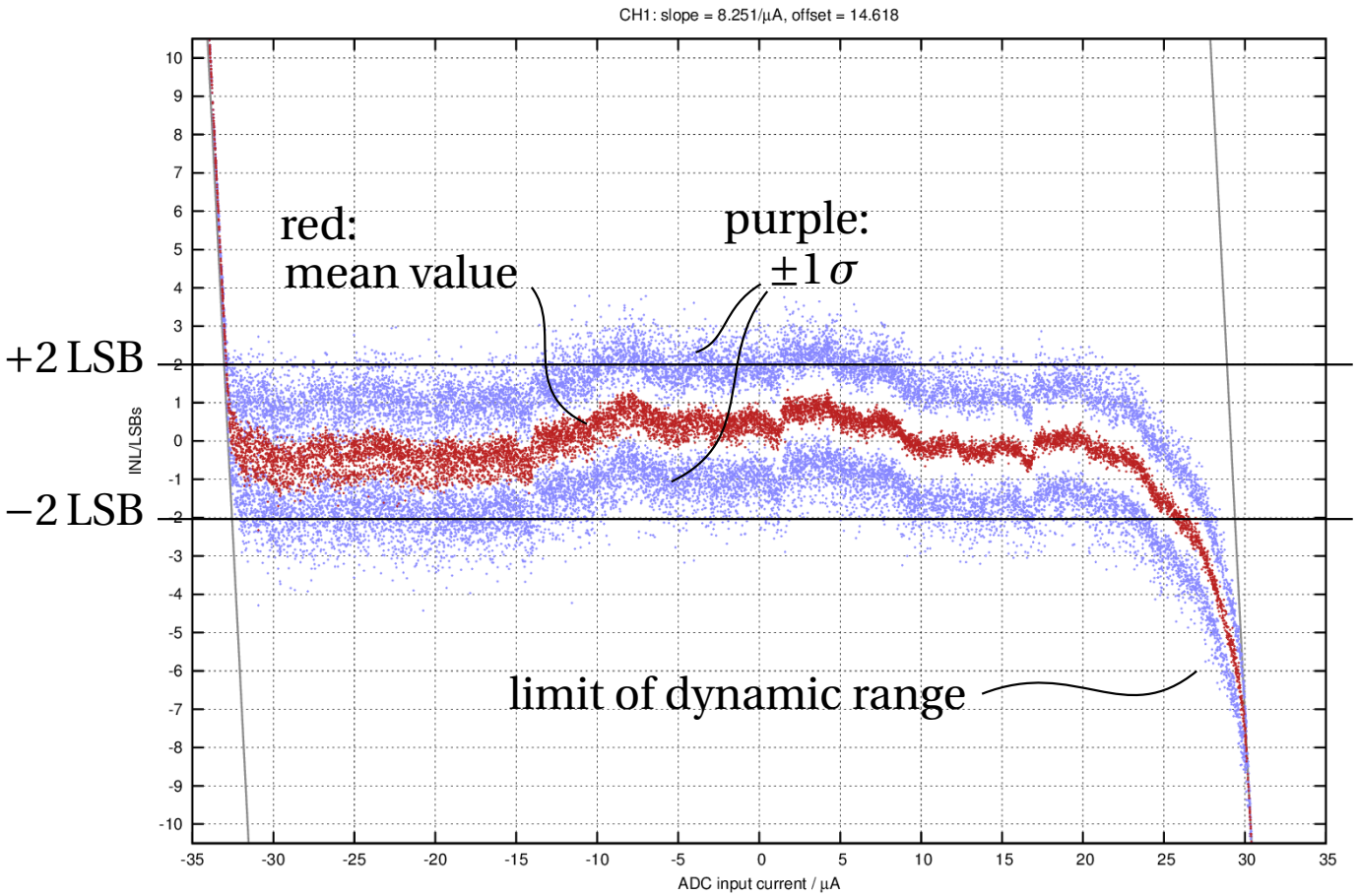
ADC



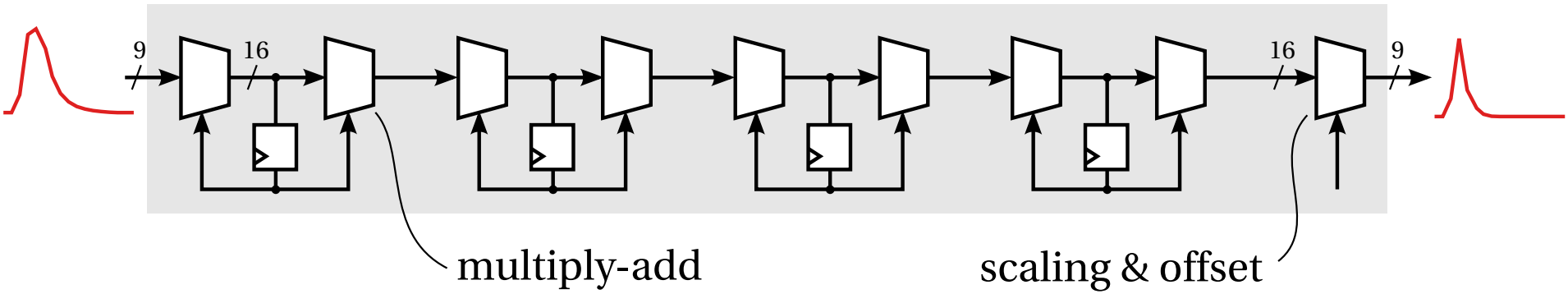
- current mode pipelined design
- 25 MHz sample rate, continuously running
- 9 bit nominal output (2's complement)
- resolution ≈ 8 bits
- 4.8 mW, rad-hard layout, $400 \times 300\,\mu m^2$

ADC measurements

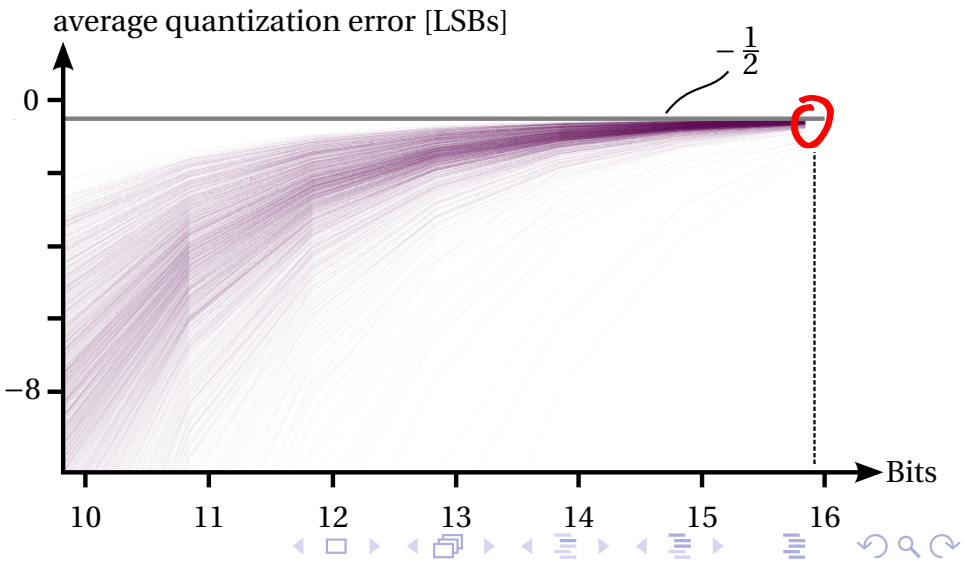
INL + noise: taken at 20 MHz sample rate, preliminary bias settings



Digital signal processing



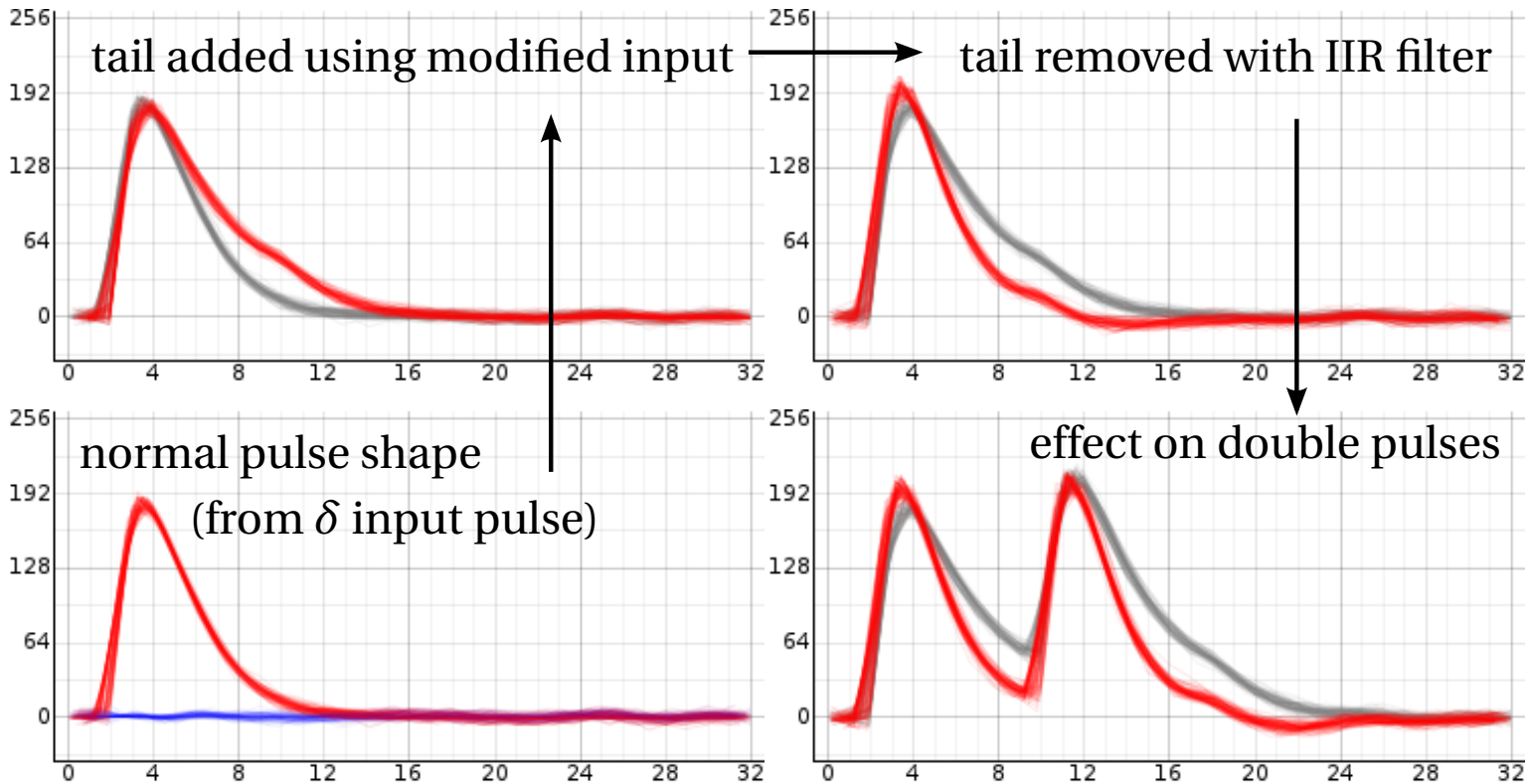
- IIR filter with 4 first order stages
- 16 bit internal resolution
- 6 bit coefficients
- freely programmable $(-\frac{32}{32}, \ldots, +\frac{31}{32})$



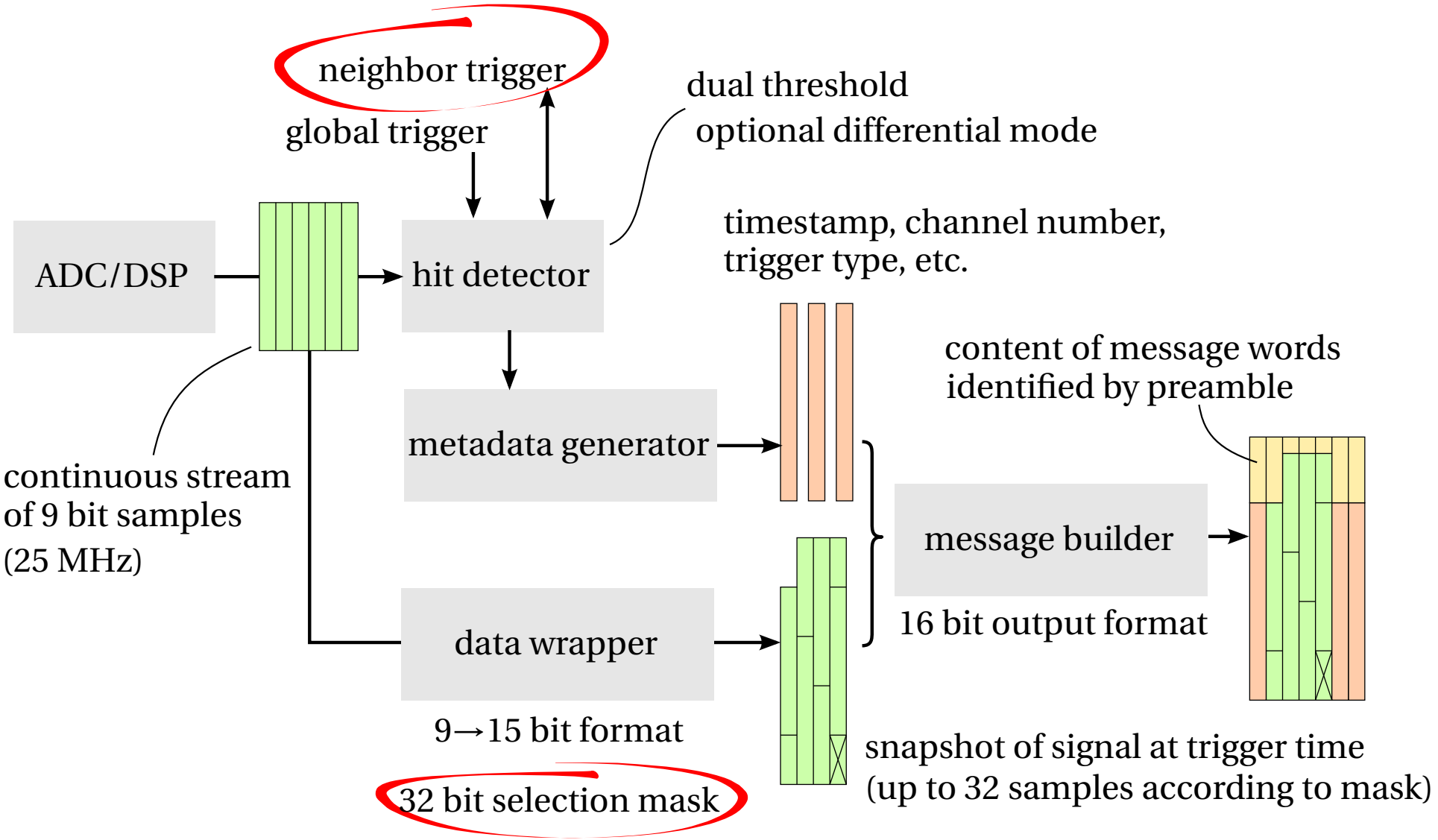
Digital signal processing

purpose: “ion tail” cancellation

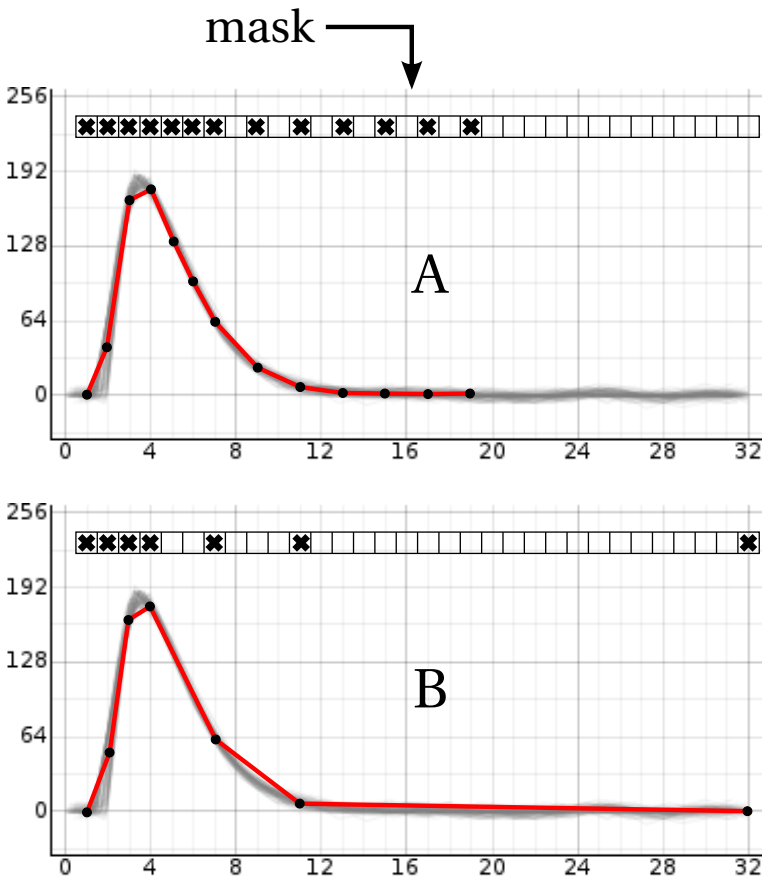
shorten pulses → reduce pileup/help hit logic



Hit logic


neighbor trigger
global trigger
dual threshold
optional differential mode
ADC/DSP
hit detector
timestamp, channel number,
trigger type, etc.
metadata generator
content of message words
identified by preamble
continuous stream
of 9 bit samples
(25 MHz)
message builder
16 bit output format
data wrapper
9→15 bit format
32 bit selection mask
snapshot of signal at trigger time
(up to 32 samples according to mask)

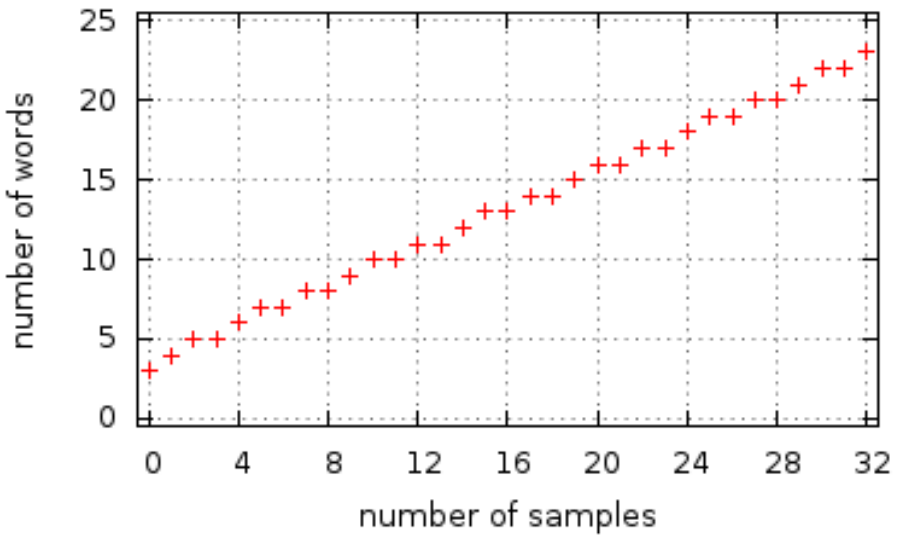
Selection mask examples



→ allows tradeoff between quality of signal reconstruction and data volume

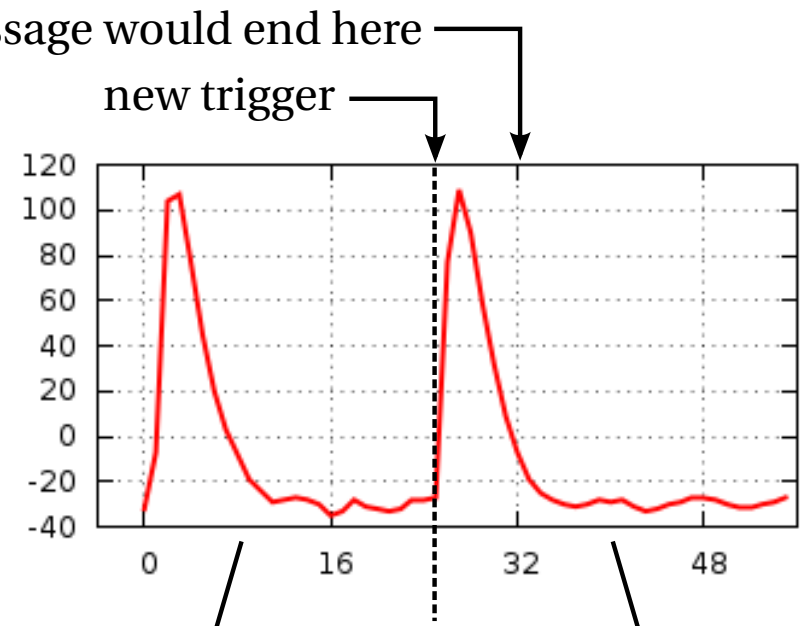
Message size (selection mask)

- $n_{\text{words}} = 3 + \left\lceil \frac{9 \cdot n_{\text{samples}} + 3}{15} \right\rceil, \quad 1 \leq n_{\text{samples}} \leq 32$
- $n_{\text{samples}} = 0$ also works!
- offset: 3 words (channel/group ID, timestamp, hit type, stop type)



Multi hits

What happens when a channel is triggered again, before the current message is completed?



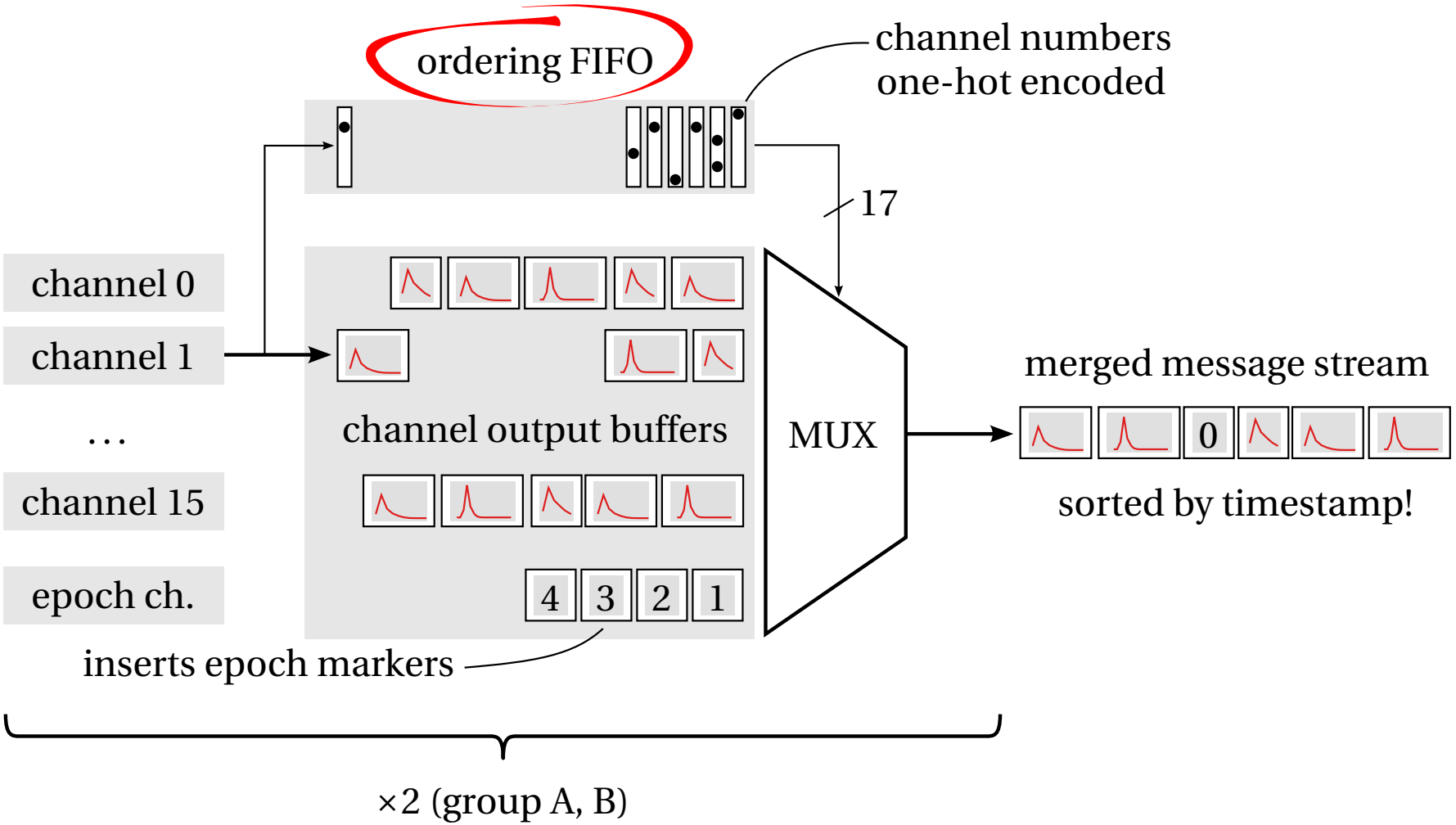
first message is gracefully aborted

selection mask is restarted
(in this example, all bits are selected...)

timestamp: 3031 —+24→ timestamp: 3055
data (24 values): -30, ..., -35
hit type: self triggered
stop type: multi hit

data (32 values): -31, ..., -32
hit type: self triggered
stop type: normal end of message

Message output multiplexing

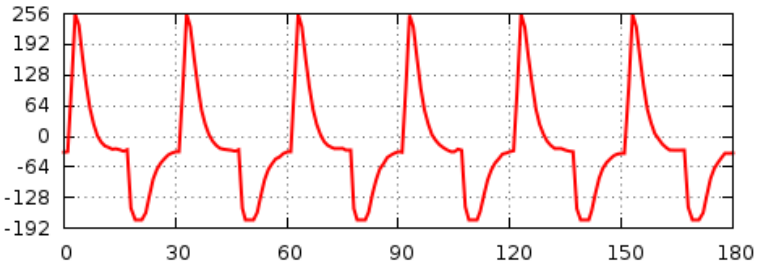


Error handling

What happens when a channel output buffer is full? Test case:

input signal: square wave, period = 30 time bins (>600 kHz hit rate)

reconstructed output signal: no problem with only one channel active



force buffer overflow with neighbor trigger → MUX can't read fast enough

timestamp: 3525
data (30 values): ...
hit type: self triggered
stop type: multi hit

+30

timestamp: 3555
data (20 values): ...
hit type: self triggered
stop type: channel buffer full

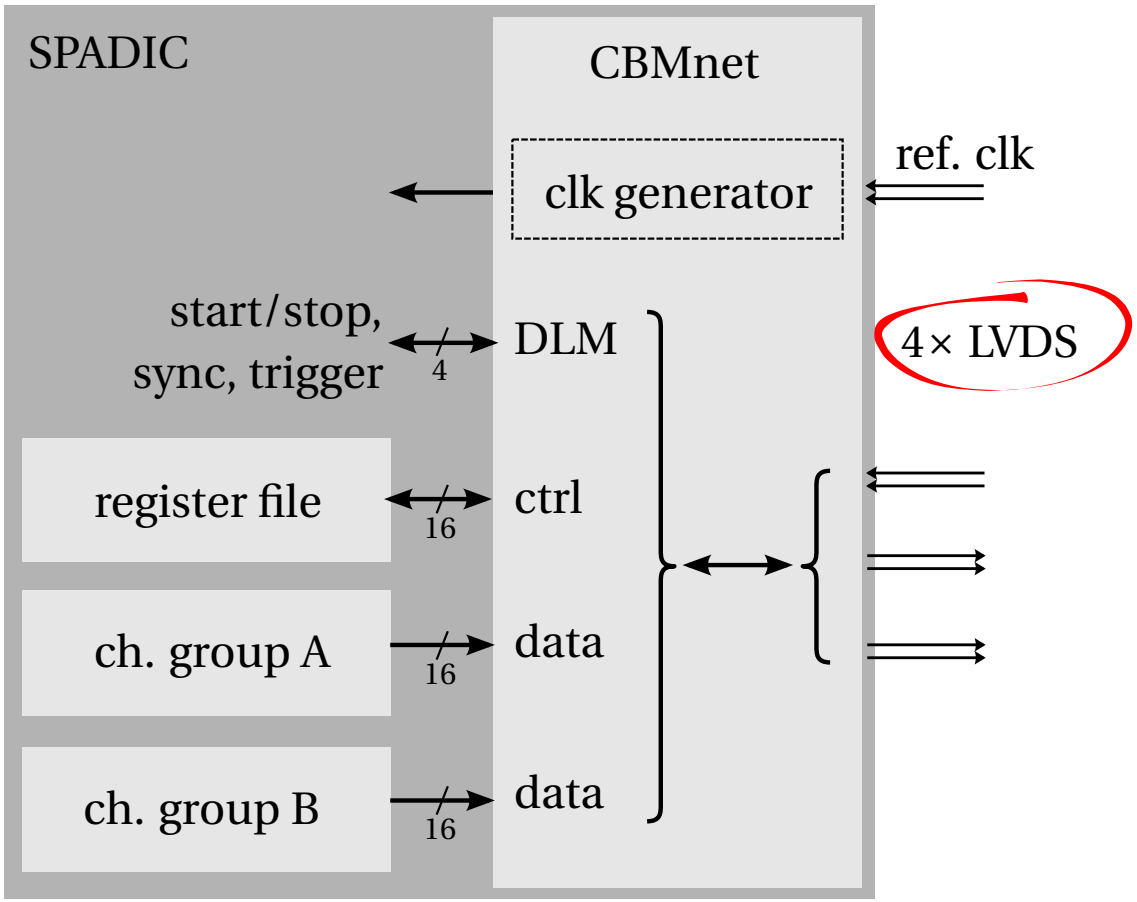
+2 × 30

timestamp: 3615
buffer overflow count: 2

special info message

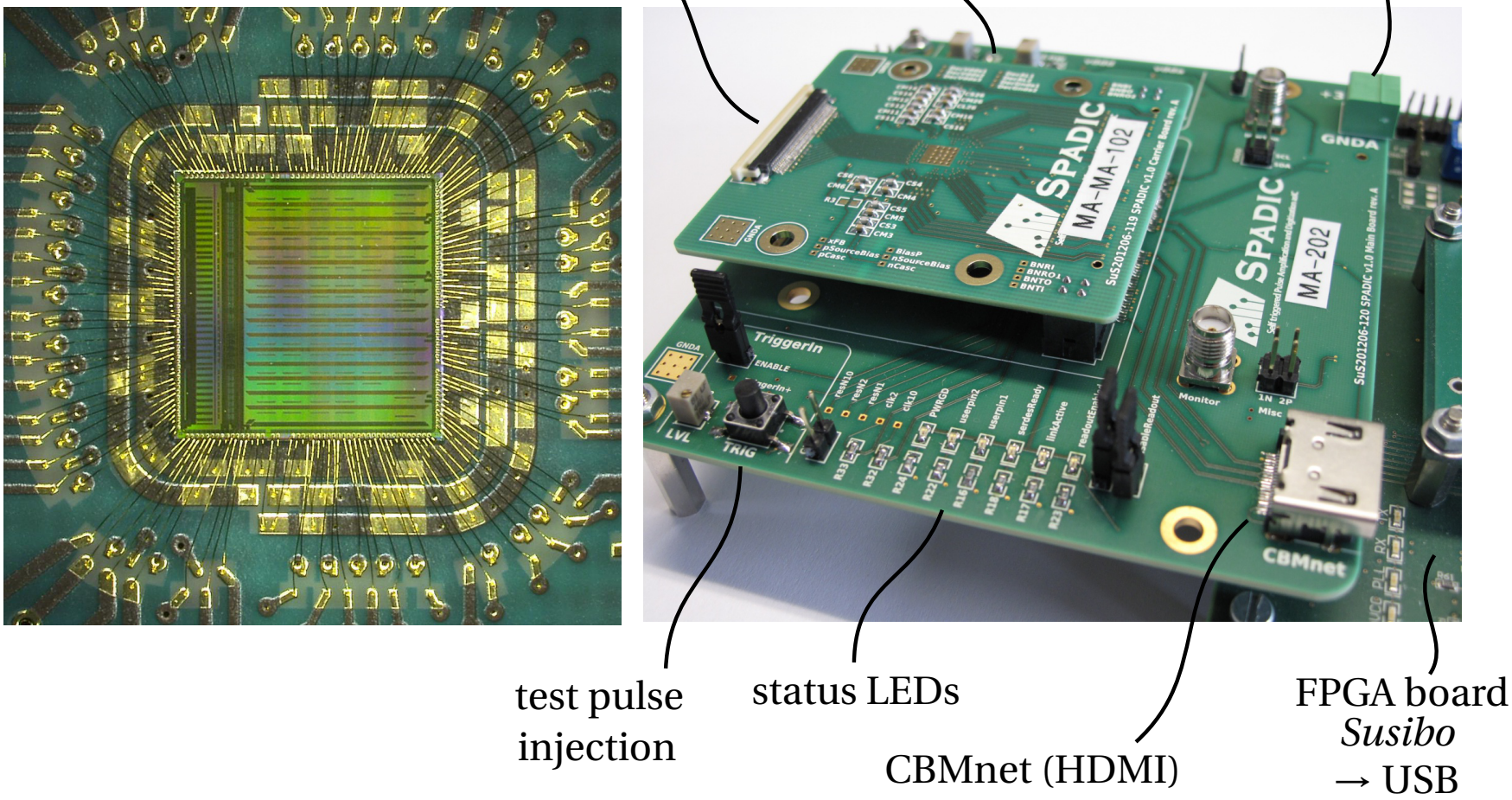
→ Similarly for ordering FIFO, incl. handling of flipped bits (SEU).

CBMnet interface

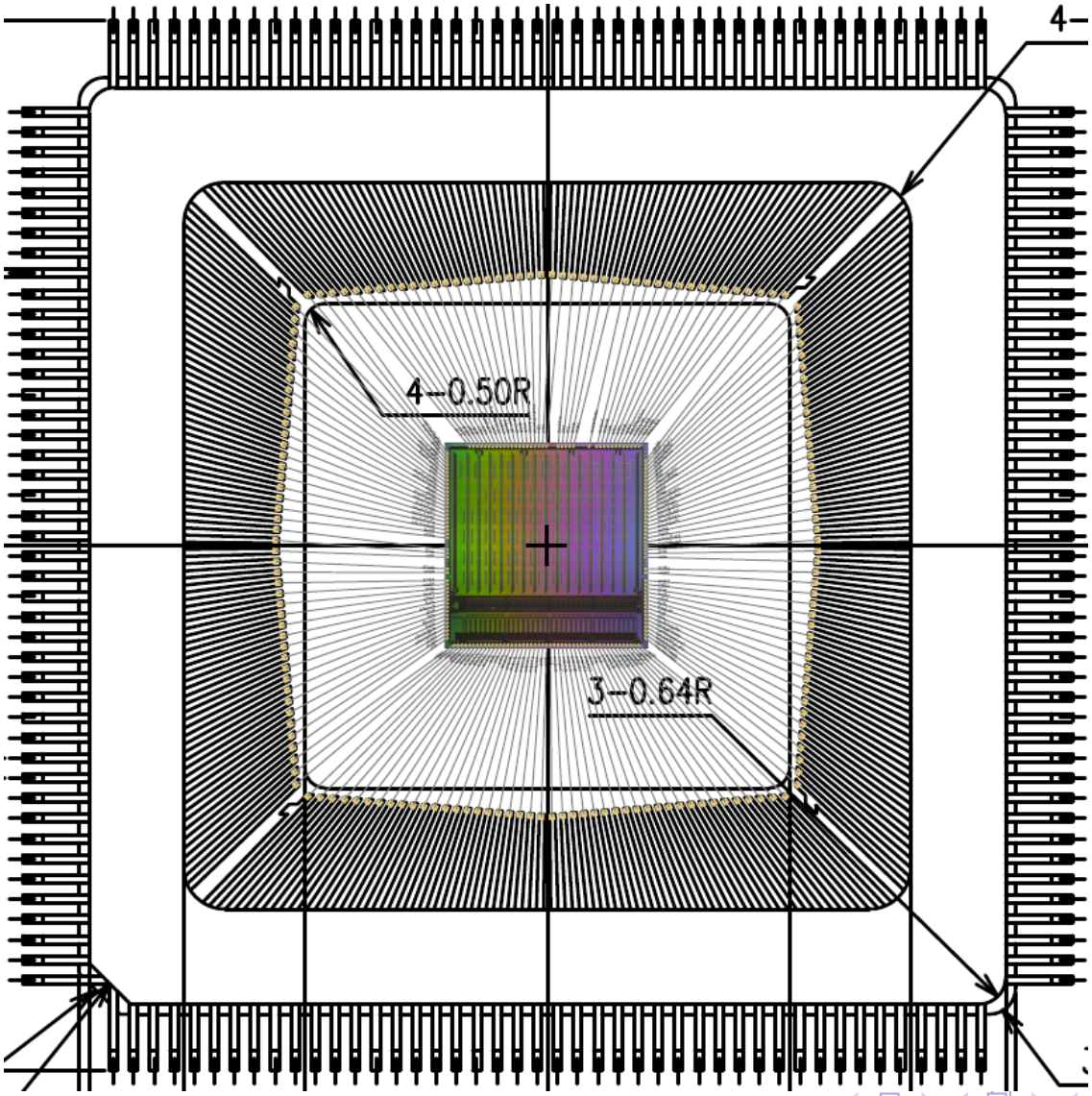


- error checking, retransmission
- *deterministic latency messages (DLM)*
- maps data + control traffic to serial LVDS links
- 500 Mbit/s (DDR), 8b/10b encoded (1 input, 2 outputs)

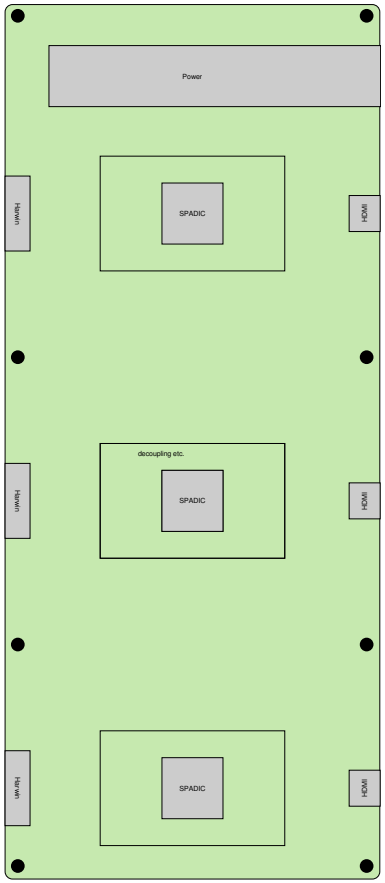
Current test setup “rev. A”



Packaging: QFP176 (23 mm)



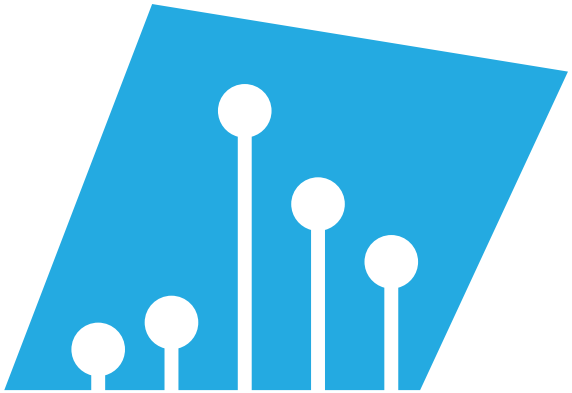
New PCB “rev. B3x”



- 3 packaged SPADICs on PCB
- distance: 114 mm (matching TRD layout)
- PCB size ≈ 15 cm × 40 cm

SPADIC wish list

- some obvious fixes (serializer glitch, CBMnet retransmission, comparator, ...)
- increased input range (75 fC → 200 fC)
- drop/reduce functionality (IIR filter, ...) → needs user experience and/or specification
- CBMnet "3.0" (W. Müller, DAQ Meeting Nov. 21) – should leave SPADIC logic untouched (or I didn't fully understand) → needs proper specification!



SPADIC

Self triggered Pulse Amplification and Digitization asIC

http://spadic.uni-hd.de