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Status of SPADIC development
Part I

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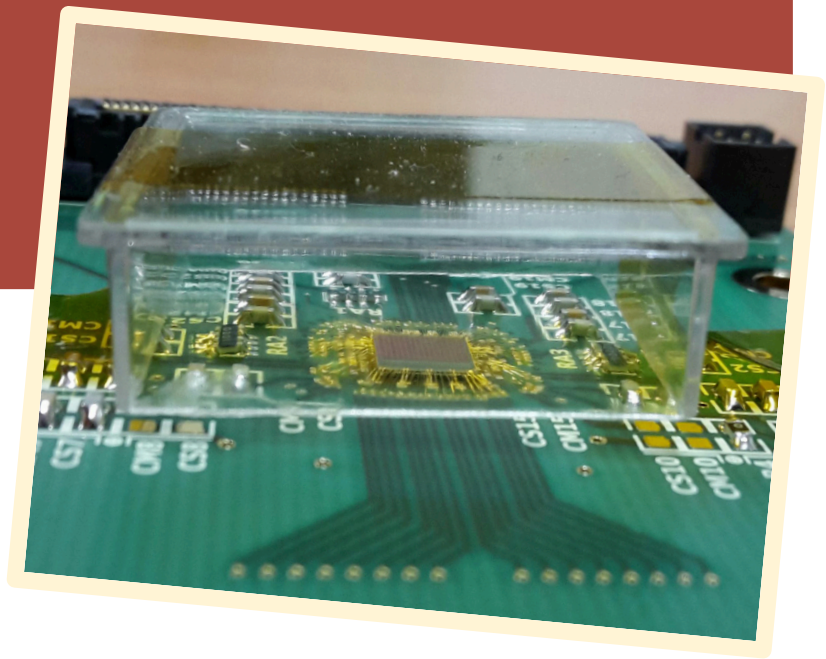
CBM Collaboration Meeting, GSI, 11.04.2016

Overview

- SPADIC 1.1 has been produced
  - "Bugfix" version of SPADIC 1.0
  - Improved synthesis scripts → easier to reuse for SPADIC 2.0
  - Submitted November 2015
  - Available since March 2016 (50 chips now, more in 2-3 months)
  - Testing has just started, but conflicts with…

- SPADIC 2.0 is now under development
  - Major change: CBMnet will be replaced
    DBP over E-Link ("GBTX") instead
  - Reuses & builds upon protocol designed for STS-XYTER
  - Submission is soon™ (engineering run together with other CBM ASICs → C.J. Schmidt, Thursday 11:30 FEE/DAQ Coordination)

SPADIC 1.1 CHANGES



- Updated CBMnet version (no retransmission)
- “Glitch” removal
- Comparator bug fixed
- Amplifier instability (see Part II of this presentation) cured

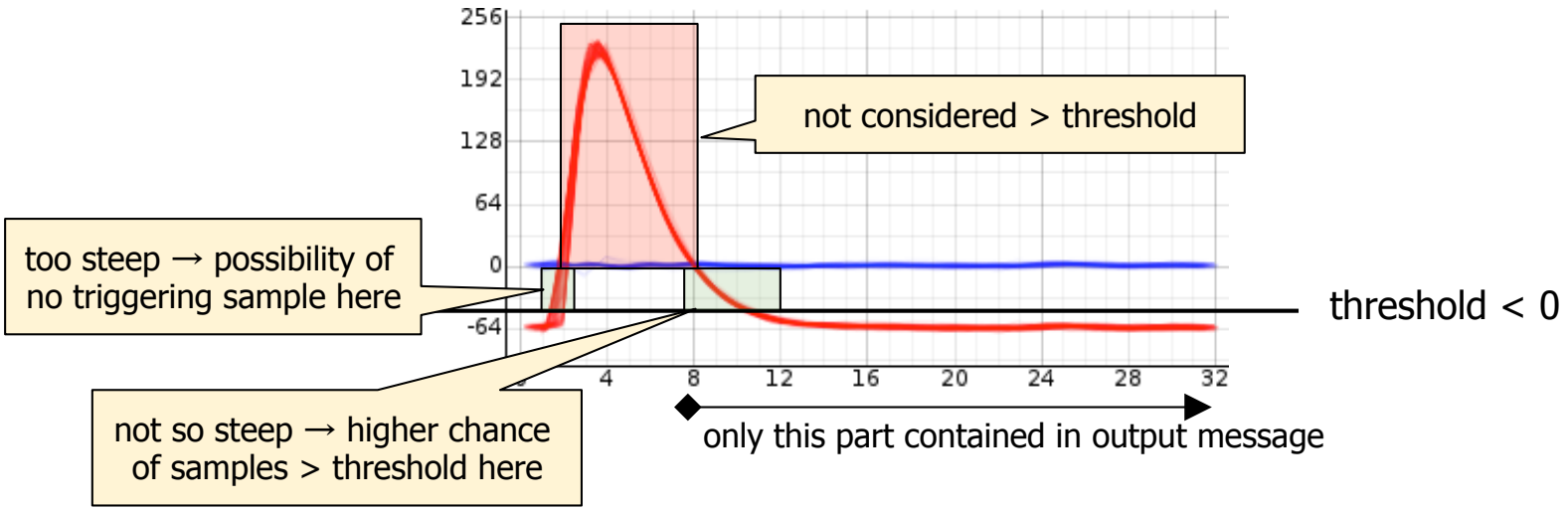
SPADIC 1.1 — First results

- The chip fundamentally works
  - Can initialize CBMnet link with SPADIC 1.0 firmware
  - Can exchange low-level communication (used for analysing the Glitch)
  - Can read/write registers
  - Have seen hit messages (random, at power-on)
- Problem not yet understood
  - After resetting the chip, exactly 28 register read/write operations work. Subsequent read/write requests fail.
  - Glitch behaviour currently studied by new student
  - Need more time to investigate (which I do not have a.t.m. due to SPADIC 2.0)

Unfortunately, (a lot) more than 28 register writes are required to do something useful with the chip :(

Fix of the comparator bug

- Positive signals do not compare “greater than” negative thresholds in SPADIC 1.0
- Was e.g. responsible for behaviour like triggering on the tail of a pulse instead of its rising edge:



- I’m quite sure I fixed it, but cannot prove it yet (because of the 28 register writing limit)

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DEVELOPMENT OF SPADIC 2.0

What's new in SPADIC 2.0?

- Replace CBMnet by (unnamed) interface to the DBP over E-Links (via GBTX)
- Due to GBTX clock frequency restrictions, reduce the ADC sampling rate from 25 to 16 MHz
- Adjust the amplifier shaping time from 80 ns to 250 ns
- Important: finish the design to catch the engineering run
  - Will not be "polished"
  - First prove that the E-Link interface works
  - There will most likely be another version 2.1 with refinements and more complex changes in the logic
- Some simpler adjustments can be done already
  - Send epoch markers unconditionally (was required to trigger them with DLMs, not applicable anymore)
  - Increase the number of "pre-samples" (before the rising edge of a pulse)

Some basics of the E-Link interface

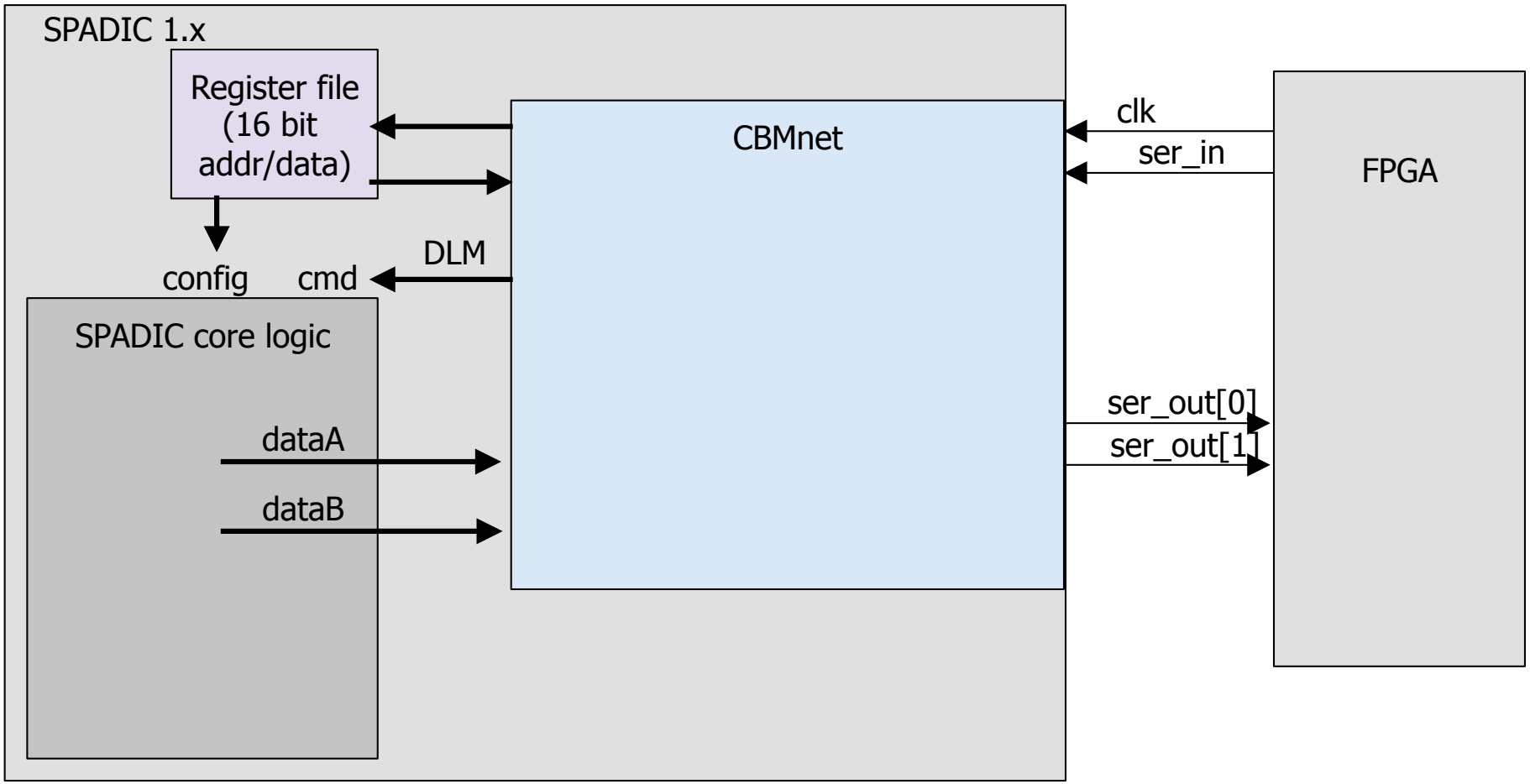
E-Link = Set of electrical signals between ASIC and GBTX: Clock down, Data up, Data down

- GBTX is transparent:
  SPADIC communicates directly with DPB
- A protocol for STS-XYTER ↔ DPB communication has already been devised; it will also be used for SPADIC 2.0
  - This has saved me a huge amount of design effort
- An implementation of this protocol is largely done and available to me

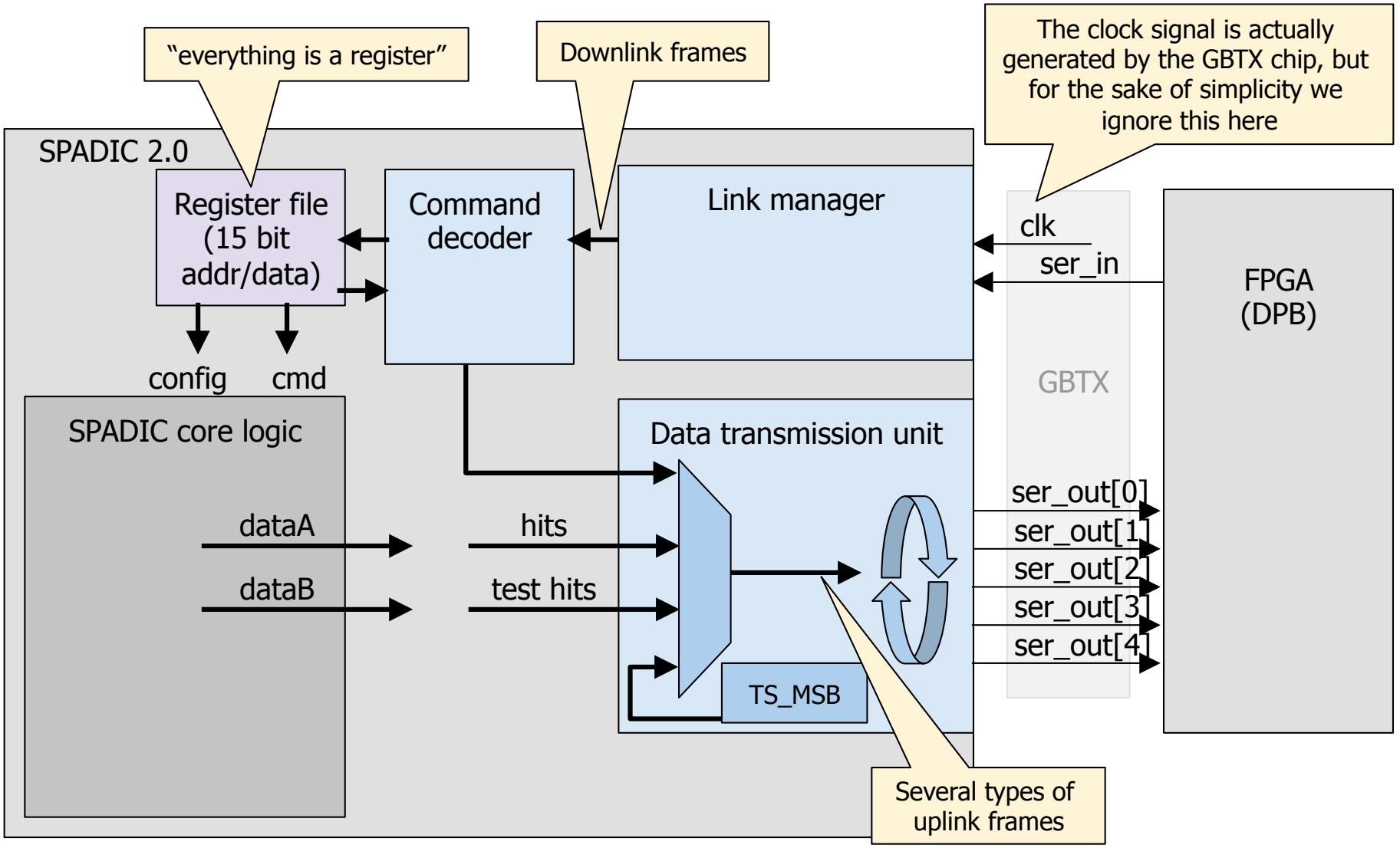
HDL code

  - **Thanks** to the STS-XYTER team (R. Szczygiel et al.)!
    This has been extremely helpful to me
- Necessary adjustments
  - Remove parts specific to STS-XYTER
  - Integrate generic parts with existing SPADIC logic
  - There are simulation test benches which help me check that I do not break anything

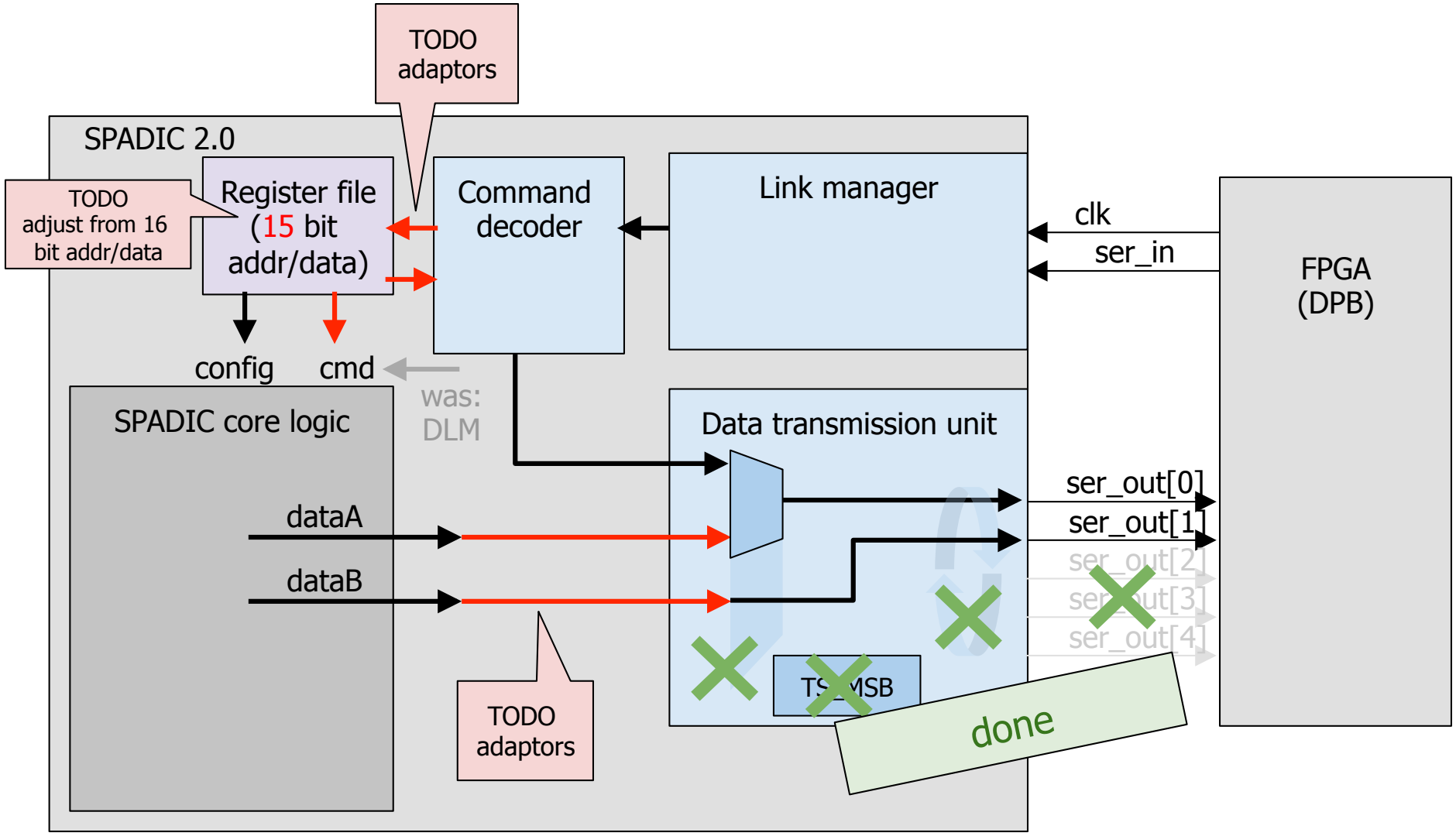
CBMnet in SPADIC 1.x



Inserting the STS-XYTER DPB interface (1)



Inserting the STS-XYTER DPB interface (2)



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Status of SPADIC development
Part II:
Analysis of ‘hang up’ Problem in SPADIC 1.0

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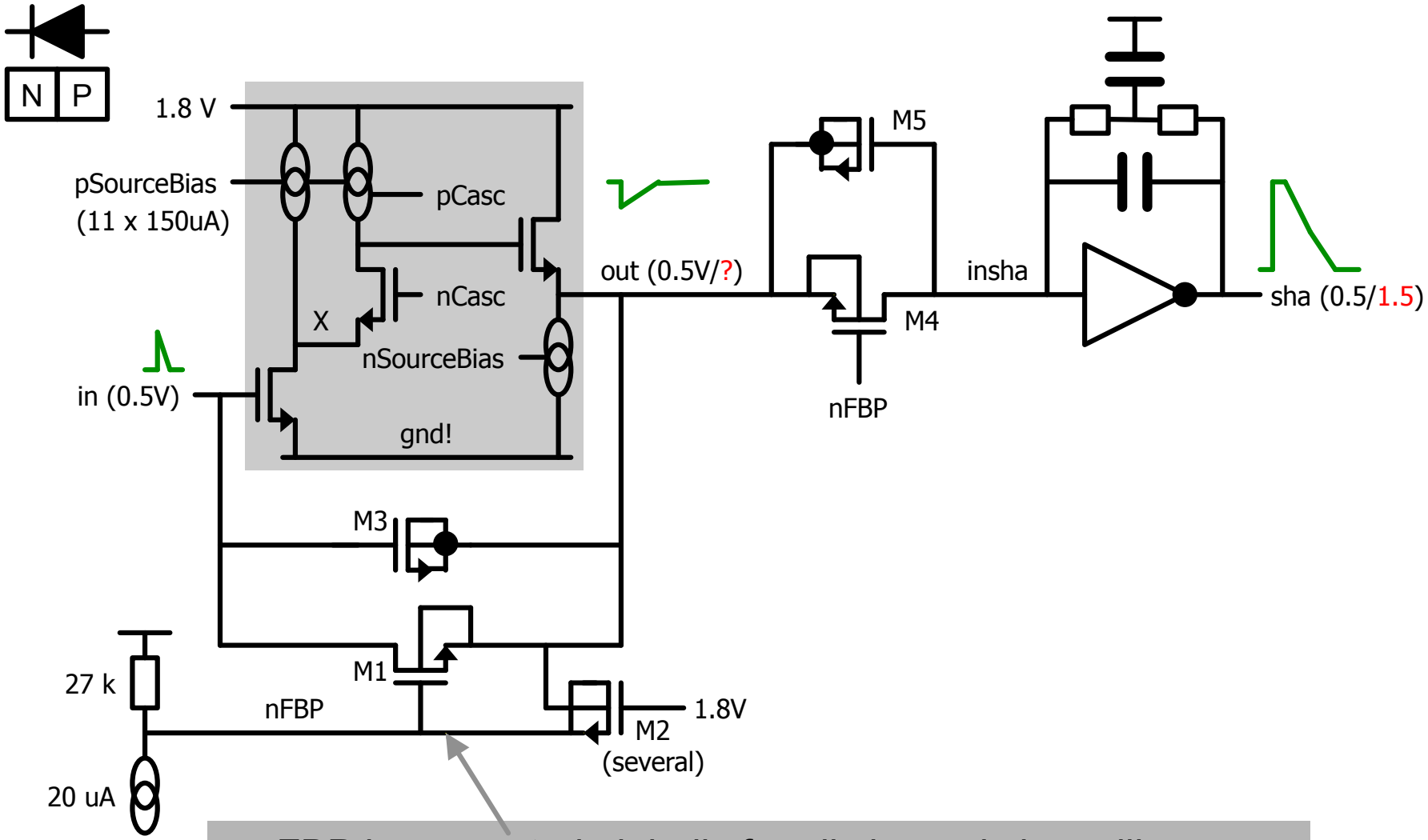
CBM Collaboration Meeting, GSI, 11.04.2016

The Problem & Observations

- In Spadic1.0, the analogue channels sometimes go to a ‘hang up’ mode (named ‘BAD’ here) from which they are hard to recover.

- Some observations:
  1. BAD occurs only in the frontend for *positive* input pulses
  2. BAD is triggered by high DAC settings of nFBP (low nFBP) or pSourceBias
  3. When BAD, shaper output shows high positive voltage (i.e. a 'high' signal)
  4. When BAD, control voltage nFBP drops from nominal ~1.5V to ~0.4V
  5. When BAD, supply current for *one* channel increases from 2-3mA to 10mA
  6. Triggering of BAD does *not* depend on nSourceBias
  7. BAD is *stopped* when pSourceBias is turned off
  8. BAD occurs sooner, if more channels are enabled
  9. There is hysteresis, i.e. it requires very low settings to stop BAD
  10. Input characteristic of one channel (see later) is different if other channels are enabled.

Diagram of Relevant Circuit Elements



nFBP is generated globally for all channels by pulling a (DAC controlled) current through a resistor

Diagram of Relevant Circuit Elements

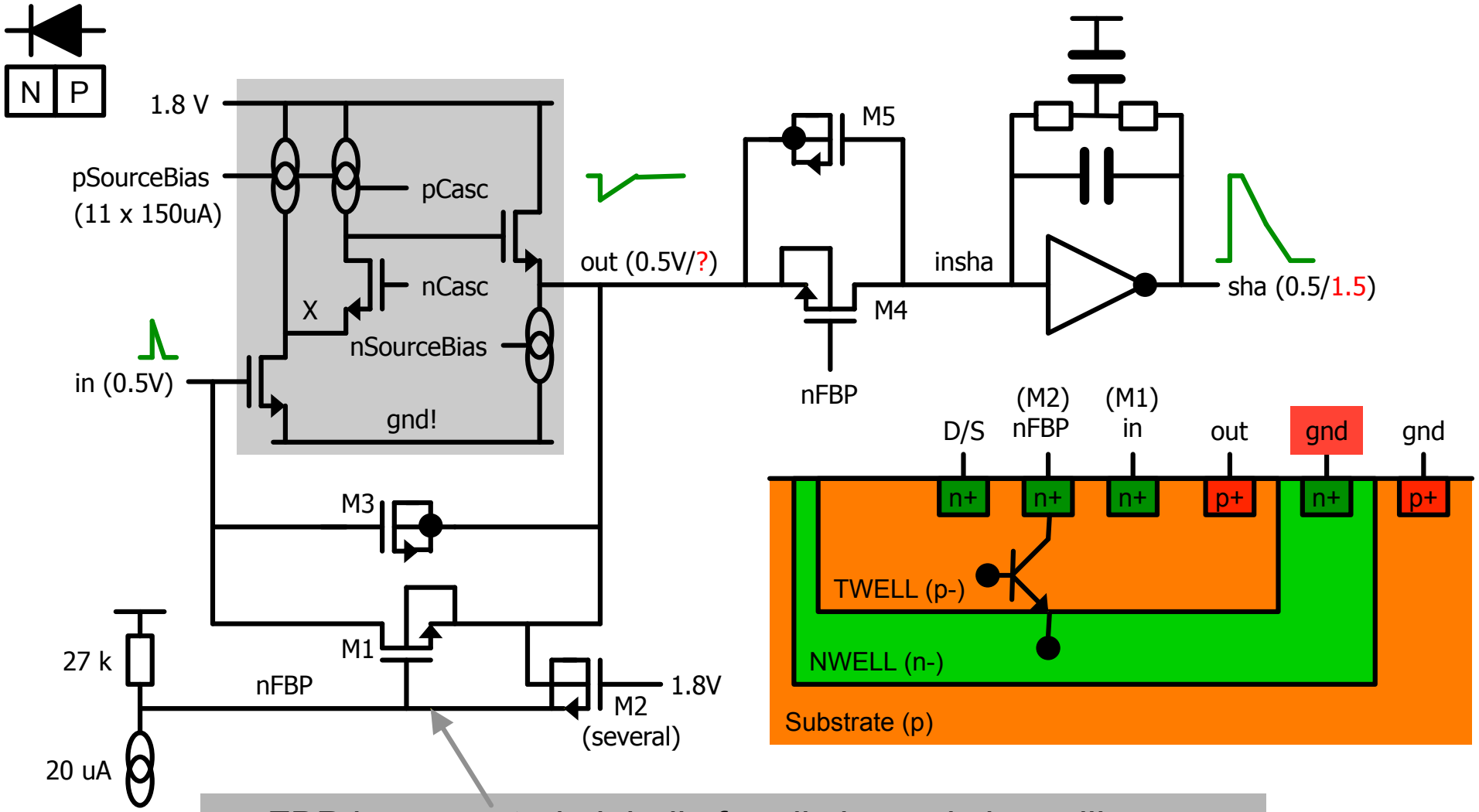


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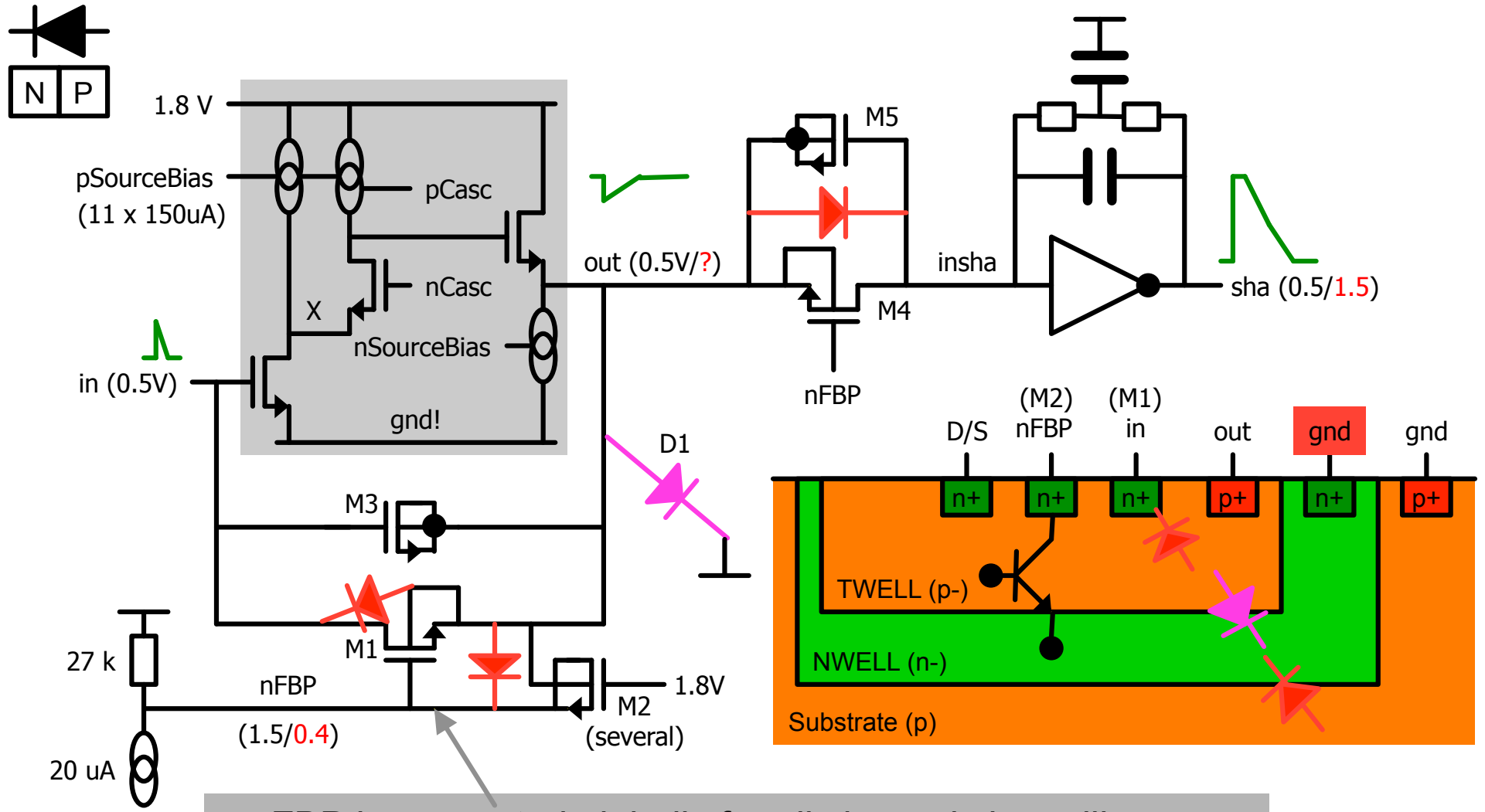
Diagram of Relevant Circuit Elements



nFBP is generated globally for all channels by pulling a (DAC controlled) current through a resistor

The Bug

- The NMOS devices used in the feedback M1-M5 are triple well devices BPW with a cross section as shown.
- Design bug: NWELL is connected to gnd! (instead of vdd!)

- The error state is reached when the SF pulls net *out* high
  - This leads to a high current in the TWELL-NMOS diode D1
  - The high potential at the TWELL opens up the vertical (parasitic) npn-s which pull all n+ implants of the BPWs towards ground: The base-emitter current is very high (10mA) so that even a very low β provides significant collector current in the n+ implants
  - Node nFBP which goes low via M2, so that the feedback in the amplifier is lost.
  - The input is also pulled low (via M1) as well so that the output (SF) goes high. This locks the state.
  - Net insha is also pulled low so that output goes high

Confirmation

- Basically all observations can be understood theoretically
- In addition a new 'prediction' could be confirmed
  (Setting nCasc to 0 triggers BAD because *out* goes high)

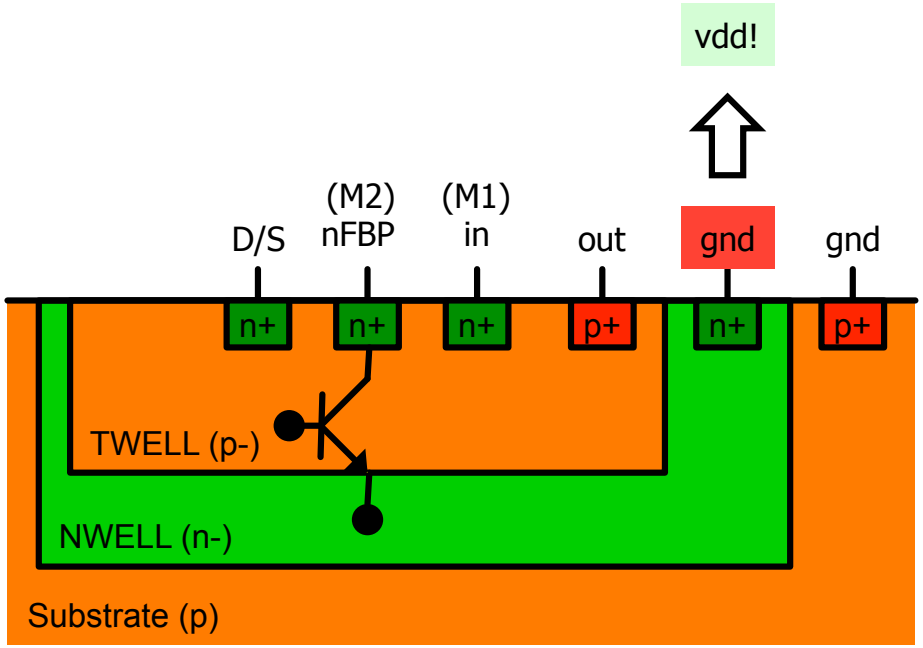
- Simulation is not (easily) possible because the parasitic device is not modelled!

How could this happen? - Design Kit Issue

- The error is NOT seen in simulation because the N_BPW devices have NO NWELL terminal in the schematics!
- In the layout, the NWELL can be connected ANYWHERE! Everything is correct as there is no guideline from the schematic!
- This is a serious risk occurring because the UMC design kit implements the '5-terminal' BPWs as 4 terminal MOS!
- All designers be aware of this issue!!!!

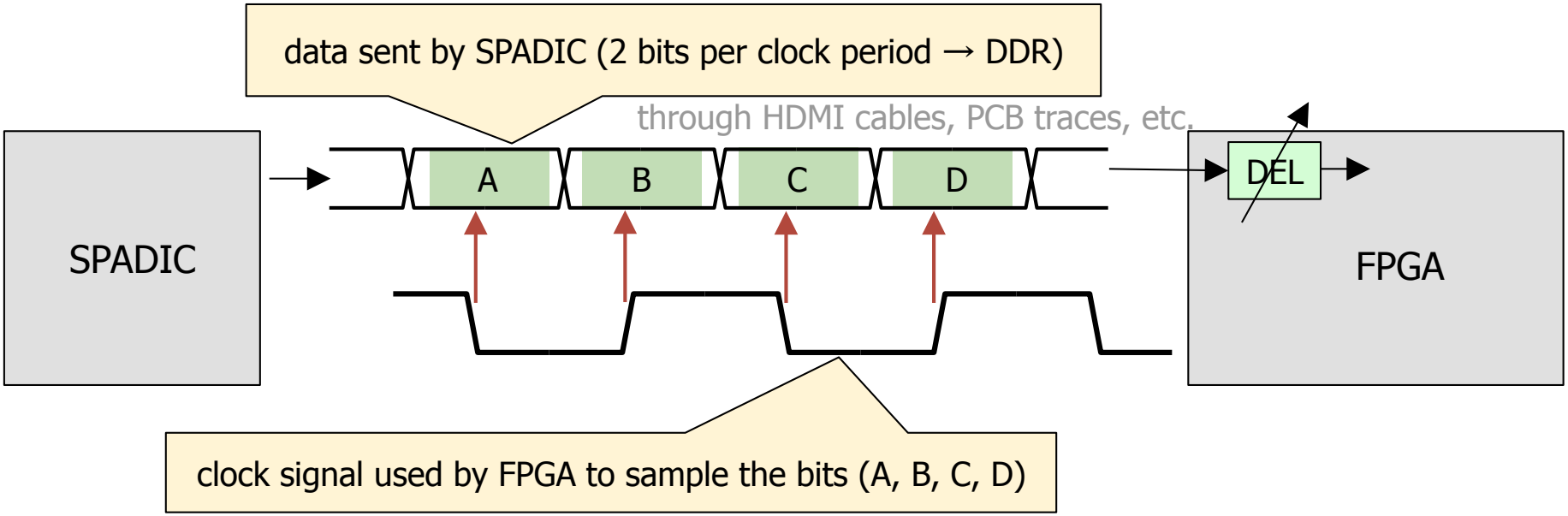
Fix

- Issue was fixed in SPADIC1.1 by connecting the NWELL correctly to vdd!



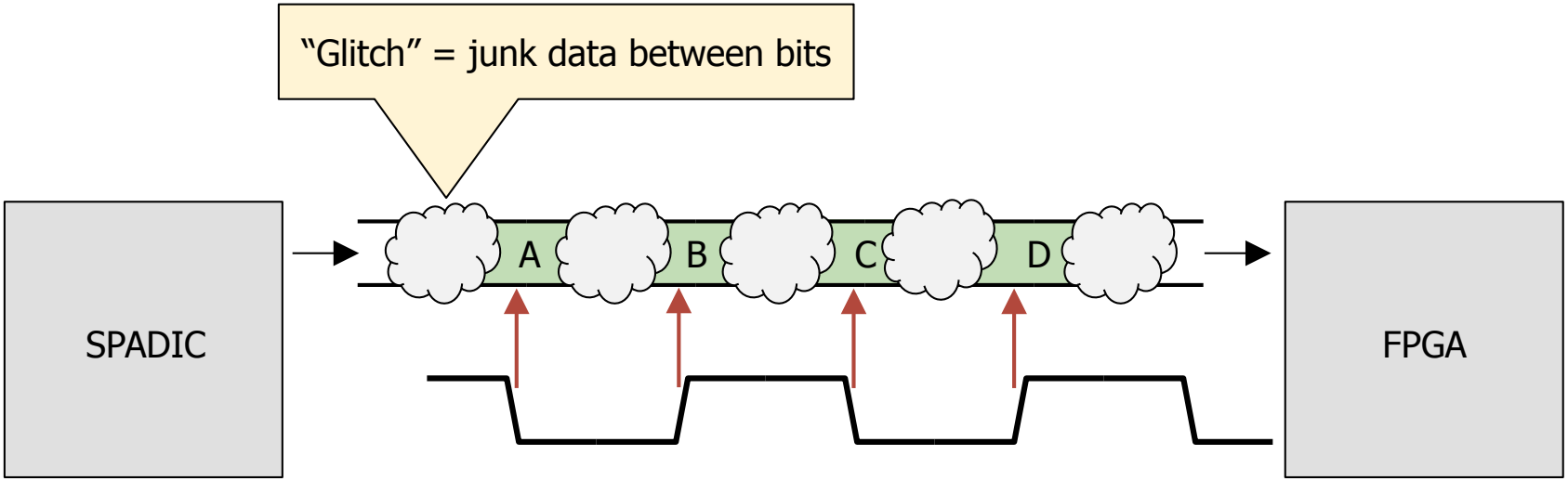
EXTRA SLIDES

The Glitch explained (1)



- clock edge must occur inside green area (while the signal is stable)
- to ensure this, the FPGA can shift the input signal

The Glitch explained (2)



- clock edge must occur inside green area (while the signal is stable)
- to ensure this, the FPGA can shift the input signal
- with the Glitch, the FPGA needs to aim more precisely