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Exercise:
DC Feedback of the Charge Amplifier

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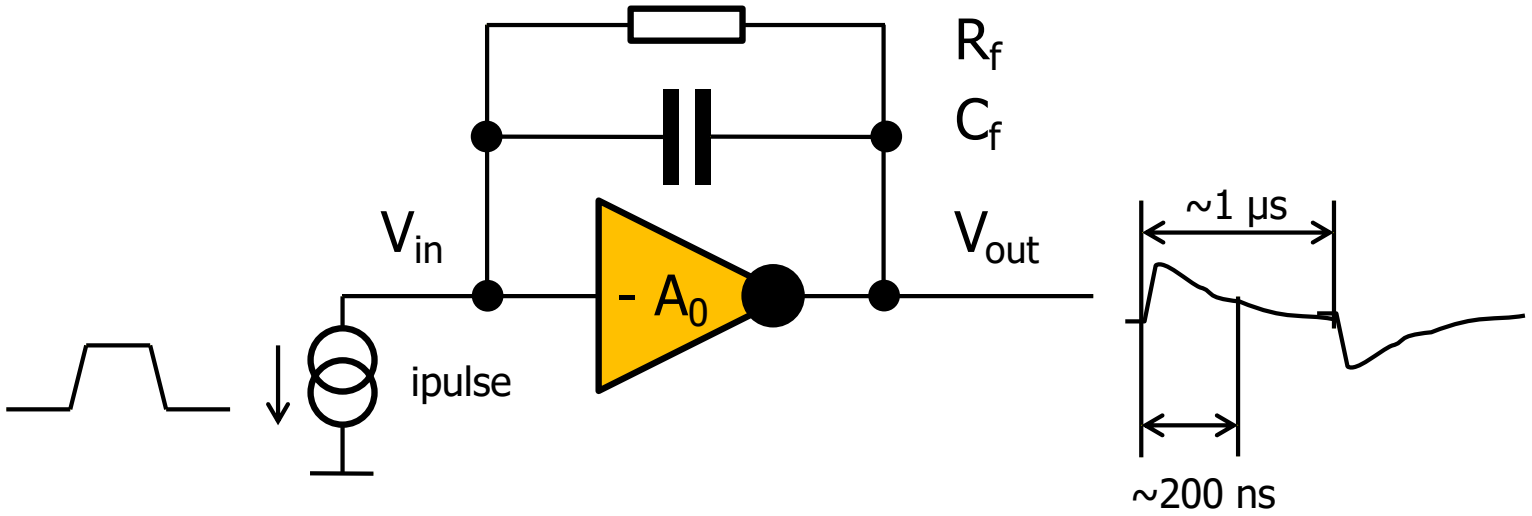
Overview

- We have seen on sheet 1 that the charge sensitive amplifier ('**CSA**') needs a 'DC feedback' which
  - 'discharges C_f'
  - 'removes the signal charge from the input node'

- We want to replace the resistor first by a MOS and then by a more complicated transconductor
  - We will see that the MOS is difficult to bias and unable to cope with both signal polarites
  - We will see that the transconductor allows us to charge the 'resistance' electronically
  - It also gives us a way to get a linear discharge, which can be useful

Reminder

- Start again with an ideal amplifier with gain $-A_0$~100, no detector capacitance and C_f = 50 fF.



- Add two sources ipulse (one shown) which deliver charges of +Qin fC and – Qin fQ (e.g. ± 1fC) so that we get positive and negative output pulses, offset by 1µs
- Chose R_f such that we discharge in roughly 200ns
- How does the time constant change when you vary the input charge from 1 fC to 10 fC ?

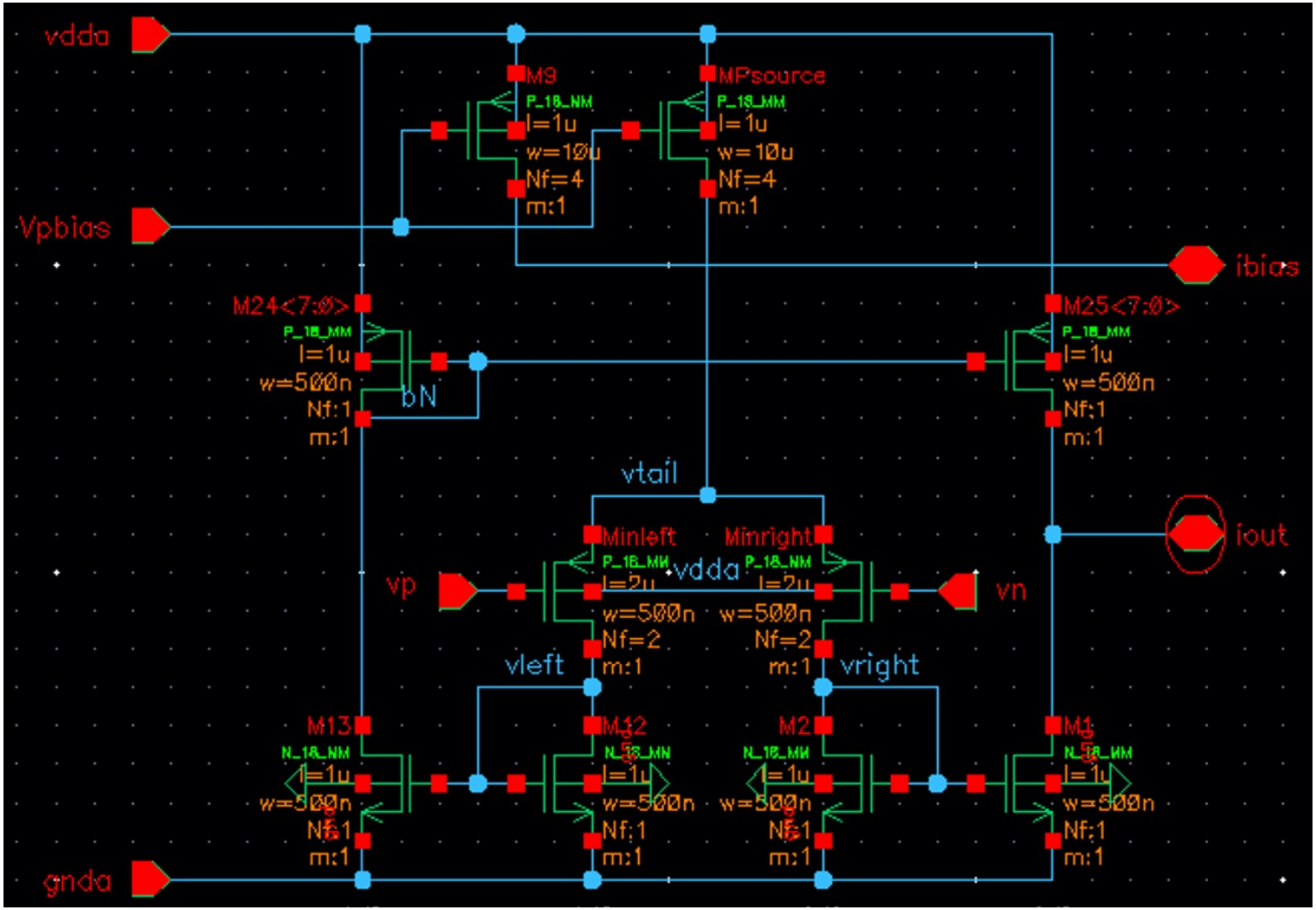
MOS as Feedback Resistor

- Now use an NMOS N_18_MM of W/L = 500nm/200nm instead of the feedback resistor
  - You may want to duplicate the circuit in your schematic so that you keep the resistive feedback as a reference
- Us Qin = 1fC. Find the gate voltage such that you get roughly the same 200ns time constant.

- Does this work for both polarities? Exactly?
- Increase the charge to 20fC. What happens? Explain! This is tricky! Hint: What is V_{GS} of the feedback MOS?
- Go back to 1fC. Change the gate voltage by 50mV (this can easily happen from run to run). How much does the time constant change?
- (The gate voltage sensitivity can be reduced by making the MOS very long. Why?)

The Transconductor

- Our Transconductor is shown here
  - Explanation on next page

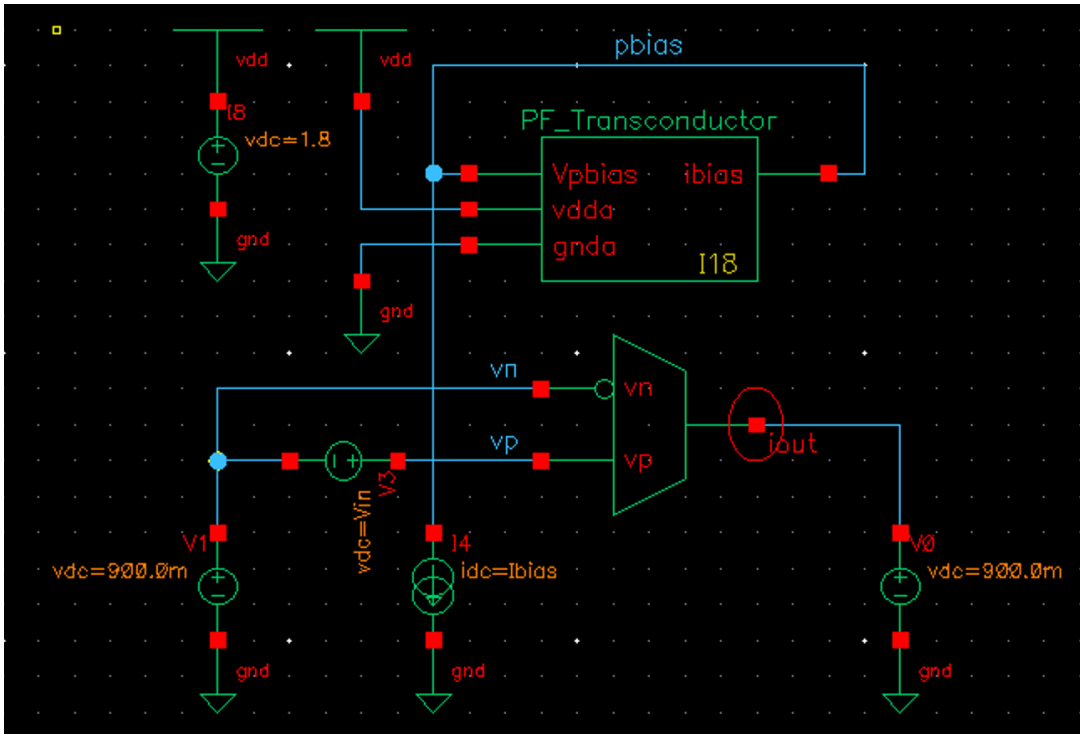


Transconductor

- It is a differential amplifier with PMOS inputs vp and vn
  - MOS are long: W/L = 1u/2u
- The ('tail') bias current comes from Mpsource, with gate bias voltage Vpbias. An identical PMOS M9 provides a current output ibias. By connecting ibias to Vpbias (outside), we generate a PMOS mirror from which we can pull the bias current to ground.
- The currents on the left and the right are mirrored and added at the output.
  NOTE: We will connect the output to a 'fixed' voltage V_{out}.
- In an ideal case, Iout=0 if vp == vn.
- The maximal / minimal output currents should be Ibias. (if all mirrors are 1:1)

Simulating the Transconductor

- Use ibias = 100nA and V_{out} = 0.9V.
- Set vp to 0.9V and vary vn from vp-0.5V … vp+0.5V (DC sweep!)
- Observe I_{out}. What is the transonductance?
- In which (input) dynamic range does the circuit work?



Changing ibias

- Change ibias (1nA…1uA)
- How does the transconductance change ?
- How does the dynamic range change ?

- We see that we can easily get small transconductances, but for small transconductances, the dynamic range is small…

- Difficult: Try ibias = 10uA. Why does the circuit stop working?

DC input range

- We want to see for which input voltages the circuit works.
- Vary vp from -400mV to 900mV (and sweep vn around vp)
  - When does the circuit stop working?
  - Why?
    Hint: What is the saturation condition for the differential PMOS pair?

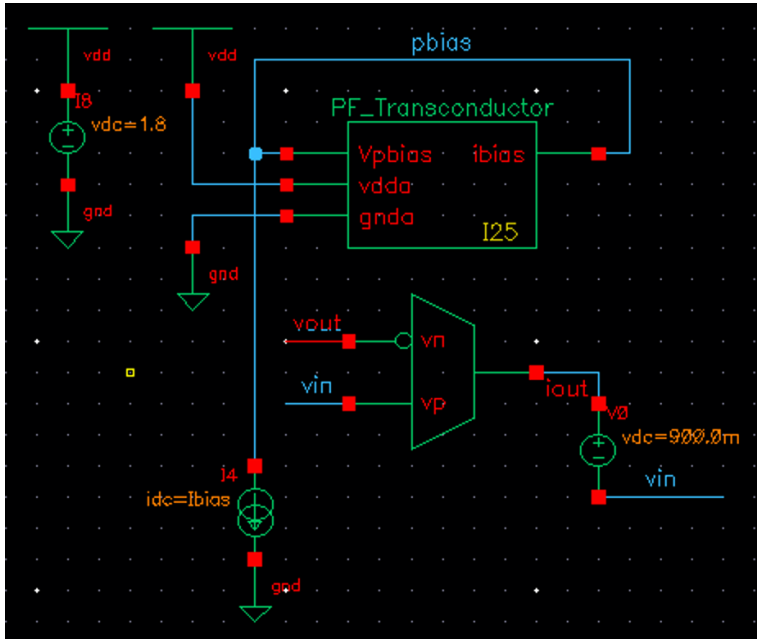
- Replace the lower NMOS mirrors by N_LV_18_MM. These transistors have lower threshold.
  - Difficult: Why does this help?

- We now have a circuit which works well down to 0 at the input.

- Can the output go to 0 as well?

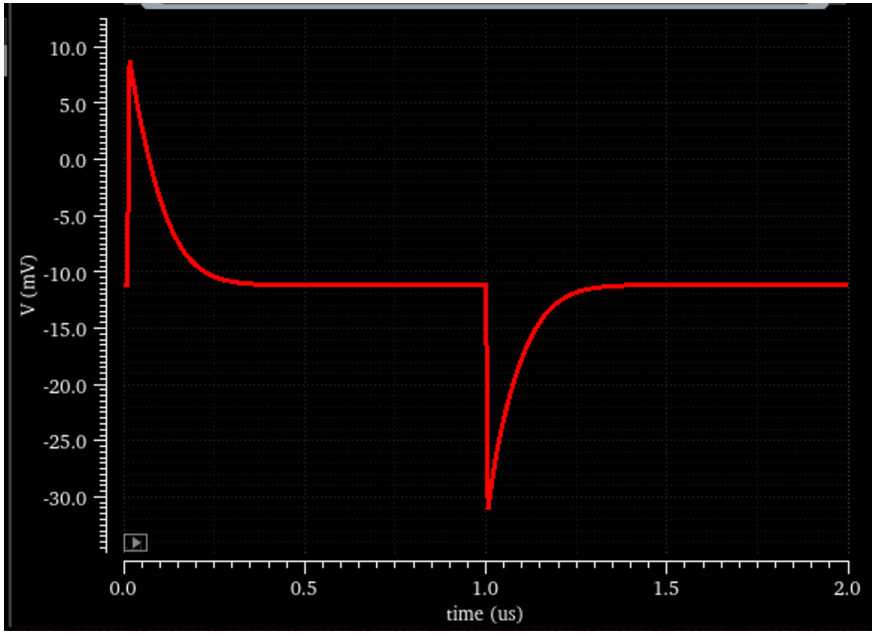
Using the Transconductor in the Charge Amplifier

- Now use the transconductor in the feedback of the CSA
  - (remember how we used a vccs on sheet 1)
- Connect vp and vn to the input and the output of the CSA
  - This will force vp = vn
- As our transconductor cannot drive into ground, use a dc voltage source to shift its output level to 900mV
  - We will not need this later with a real amplifier…



It works!

- Use Qin = 1fC and Ibias = 50nA or so.
- If you did everything correctly, it should work, in principle:



- Vary Ibias and observe how the time constant changes.
- We have a current controlled discharge time !

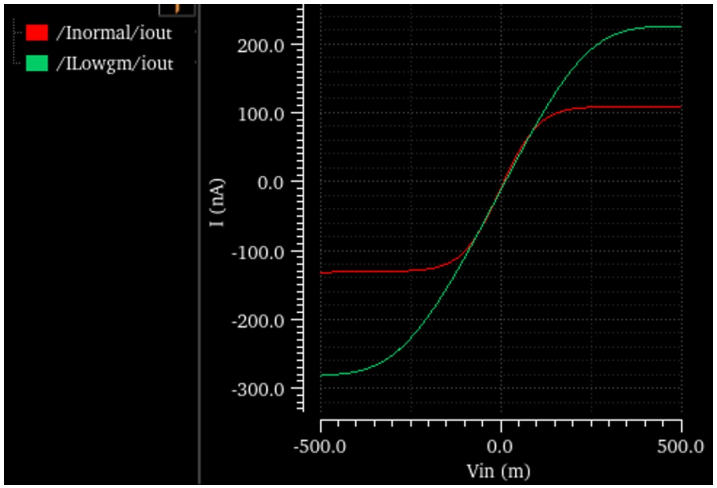
Saturation

- Use 50nA again.
- Increase the input charge from 1 fC to 10 fC and to 30fC
- How do the pulse shapes change?
- Why?
- What happens if you double Ibias?
- Is this what you expect ?

- The constant current discharge can be useful, because the width of the signal becomes proportional to the input charge.
  - Try this: Ibias=50nA, Qin = 10,20,30 fQ

Optional: Back to RC Shape

- The ‘saturation’ occurs quite early because the linear input range of our transconductor is small for small Ibias
  - For experts: The input diff. pair is in weak inversion
- If we increase Ibias, the range gets better, BUT the transconductance increases and we get a too fast discharge. (input pair gets into strong inversion)
- A trick can solve this:
  - Use a ‘large’ Ibias current in the differential pair
  - Use a current mirror in the output branch to divide this current down to 1/8 or less



- Try this in a 2nd transconductor. Compare in a dc simulation to your first version. Is the input range wider for same transconductance? (You must use different Ibias currents!)

No more analogLib tricks

- Finally, use a NMOS gain stage instead of the vcvs in the main CSA.
  - For instance W/L = 5u/500n biased at 5uA

- The input will now settle to a voltage around the NMOS threshold
- The transconductor output drives into that voltage so that you do bot need the 900mV shift and more.