Parasitic Extraction

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Parasitic Extraction

- **Parasitics** are ‘devices’ which are not intended but intrinsic to any physical representation of a circuit
- For instance: interconnect traces have
  - Resistance
  - Capacitance to their surrounding
  - Inductivity
- **Parasitics** sound bothersome, and they are!
- The circuit schematic does (in first order) not include any physical layout information
  - ‘Full custom’ circuit design usually bare schematics first
  - Digital place and route tools might use estimates already in the placement phase
- Only after the layout exact parasitics can be extracted
- Simulation with *annotated* parasitics models the circuit behavior most accurately
Effects of Parasitics in Digital Circuits

Parasitic capacitors between signal wires cause cross talk.

RC causes extra propagation delay.

Charging of extra capacitance costs increases the power consumption.
Relevance of Parasitics

Technology Evolution:
- Decreasing interconnect feature size increases parasitics
  - \( d \downarrow \rightarrow C_{\text{side}} \uparrow \) (\( C \sim 1/d \))
  - \( w \downarrow \rightarrow C_{\text{up,down}} \downarrow \)
  - Aspect ratios \( (h/w) \uparrow \rightarrow \) trying to keep \( R \) const,
  - \( h \uparrow \rightarrow C_{\text{side}} \uparrow \uparrow \)
- Decreasing transistor feature size \( \rightarrow \) weaker drivers
- \( \rightarrow \) Parasitics become more relevant (can even become dominant) as feature sizes shrink
PARASITIC EXTRACTION TUTORIAL
Overview / Requirements

- This tutorial shows how to:
  - Run different extraction types
  - Analyze the results
  - Simulate with extracted parasitics

- We will use the tool ASSURA QRC

- Required inputs are:
  - A schematic view
  - A layout view (a ‘standalone’ layout view cannot be extracted)
  - A **clean** LVS

- Open the layout to extract and run an LVS or open an existing LVS result (Assura → Open Run)
Extraction Setup

- Now select: QRC → Run Assura – Quantus QRC...

- We will use the default output type ‘Extracted View’
- The ‘Extracted View’ can be analyzed with the GUI and is most illustrative for the tutorial
- Other output view types are possible, e.g.:
  - Netlist in spice / spectre format
  - SPEF - Standard Parasitic Exchange Format (input for static timing analysis for digital designs)

The resulting parasitic components to use can be specified in this area. All defaults are fine.
The ‘Extraction Type’ defines which components to extract and determines the complexity of the result.

We will use:

- C only
- RC

The ‘Cap Coupling Mode’ specifies the ‘backside’ of the extracted capacitors.

- **Decoupled**: all capacitors couple against **ONE** specified ‘Ref Node’ which MUST be specified and be present in the cell.  
  → Less accuracy but also less complexity, no cross coupling can be simulated.

- **Coupled**: all capacitors are extracted as they are  
  → Higher complexity and cross coupling can be simulated.
To remember the extraction type I like to add it to the view name: (in the ‘Setup’ tab), e.g.

- `av_extracted_C` (for decoupled C only)
- `av_extracted_CC` (for coupled C only)
- `av_extracted_RCC` (for coupled RCC)
In the ‘Filtering’ tab the ‘chopping’ of the parasitic elements can be controlled
- Minimum resistor values
- Minimum capacitor values
- …

Can be used to reduce complexity or increase accuracy of the extraction

The default values are fine for us

Now we can start the extraction!
The Extracted View

- Open the extracted view (default: av_extracted) with the library manager
- It looks like a layout but contains devices and parasitic elements

Parasitic resistor (cell ‘presistor’).

The type of the metal lines is ‘net’ (not drawing as in the layout).

NFET as in the schematic.
Enable the ‘Net’ Layers (UMC specific)

- Right click here
- Check here to show only used layers
- Click here to enable all layers
Examining the Parasitics

To enable the ‘Parasitics’ option in the menu bar do:
Menu bar → Launch → Parasitics
Reporting Parasitics

- First select Parasitics → Setup
- This enables the ‘Report Parasitics’ options

Enter the reference node for decoupled reporting
Example Net Report

- Select: Parasitics \(\rightarrow\) Report Parasitics \(\rightarrow\) Net
- Select some net in the extracted view
- A detailed net report is shown

![Net Report Example]

- If resistances were extracted the nets now have numbered segments

- Select some entry to highlight the parasitic element in the extracted view
Simulating an Extracted View

- Set up a simulation schematic
  - Instantiate the symbol of the cell which you have extracted
  - Add power sources, signal sources, etc.

- Launch → ADE
  - Go to Session → Environment
  - In the Switch View List add the view name of your extracted view (default: ‘av_extracted’) somewhere BEFORE ‘schematic’ → the netlister now prefers ‘av_extracted’ over ‘schematic’

- Setup a transient simulation as usual and simulate
Viewing the Simulation Results

- Select results as usual
  - ADE Menu Bar → Outputs → Select From Schematic
  - You can descend into the av_extracted view and select nets

- Use the ‘Results Browser’
  - ADE Menu Bar → Tools → Results Browser
  - Browse through the ‘tran’ folder
EXERCISE: PARASITIC SIMULATION
Exercise: Signal Delay & Integrity

- **Step 1:** Create the following (or similar) schematic

- **Step 2:** Draw the according layout
  - Draw the in_n and in_n_n nodes in parallel @ minimum pitch and width for at least 100µm
  - Make the layout LVS clean
  - DRC does not matter for now…
Exercise: Signal Delay & Integrity

- **Step 3: Extract the layout**
  - Run all three extraction types and save them to separate views
    - C only decoupled → av_extracted_C
    - C only coupled → av_extracted_CC
    - RC coupled → ac_extracted_RC

- **Step 4: Analyze the extracted view**
  - How big is the total coupling capacitance between your in_n and in_n_n node?

- **Step 4: Simulate the schematic and all 3e extracted views**
  - HINT: You can copy the results after the simulation
    - cd /tmp/ADE-sim-vlsiXX/
    - cp –r psf someNewName
    - You can then reopen them in the ‘Results Browser’
  - Can you see any cross coupling in the waveforms?
  - What is the difference in the propagation delays between the plain schematic and your layout?
In larger designs, you may only want to include parasitics to some cells. This can be controlled with a 'config' view.

Create a new cell view of type 'config view'.
- File -> new -> cell view
- View is 'schematic'
- The tool associated is the 'Hierarchy editor'
- Use Spectre as simulator

In the Tree/Table view panel you can select which view is used for simulation for each cell.

To simulate, you must open ADC from the config view.
Alternatively, when doing a simulation on the schematic, switch to config in Design-...