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Readout Architectures

P. Fischer, Heidelberg University

Pixel Readout for HEP (here: LHC)

- Requirements
  - Event rate = 40 MHz
  - Not all events are read out:
    Store them on chip until a *trigger* signal picks (few) events
  - Trigger fraction ~ 1%
  - Trigger latency = 100 Events (ATLAS) ... 160 (CMS)
  - Allow several consecutive triggers
    (→ readout of a triggered event is not completed)
  - Reduce hit losses from
    - Busy pixels
    - Buffer full conditions
    - ...
  - Reduce Power
  - Pixel size = 50 x 400 μm^2 (1^{st} generation ATLAS, now 250 (?)) /
    150 x 100 μm^2 (1^{st} gen. CMS)

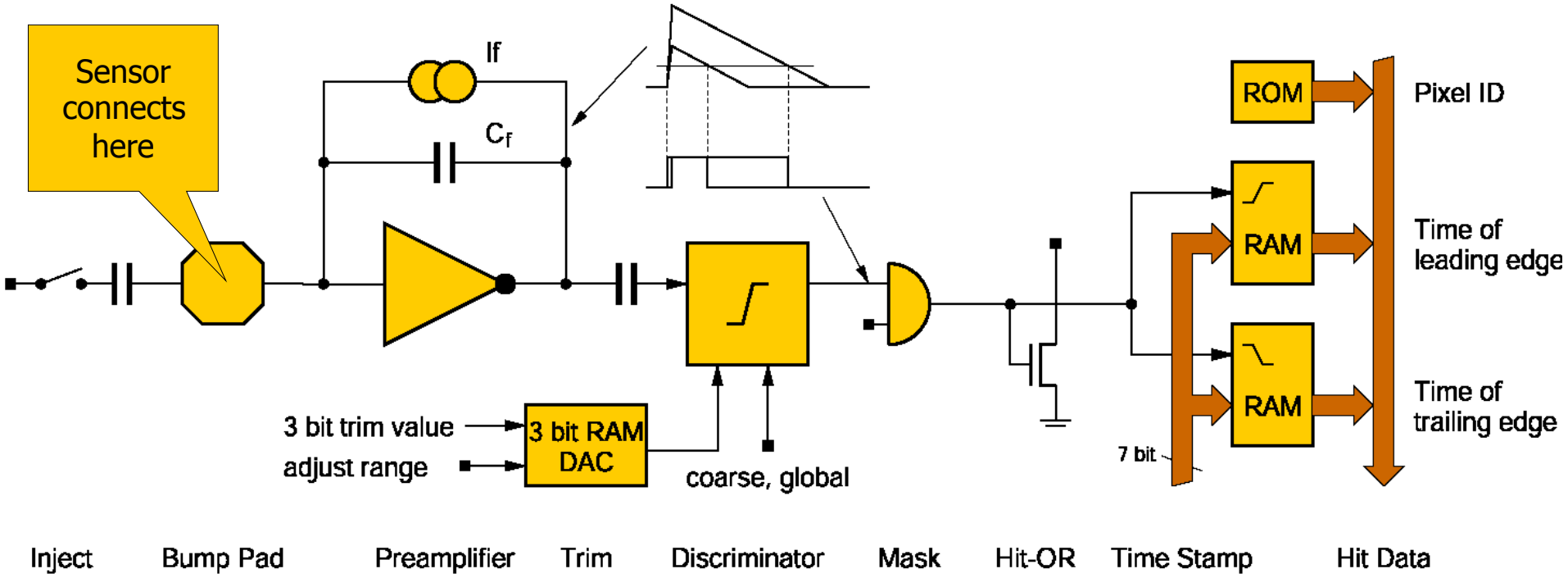
DETAIL EXAMPLE: ATLAS PIXEL

Pixel Analog Part

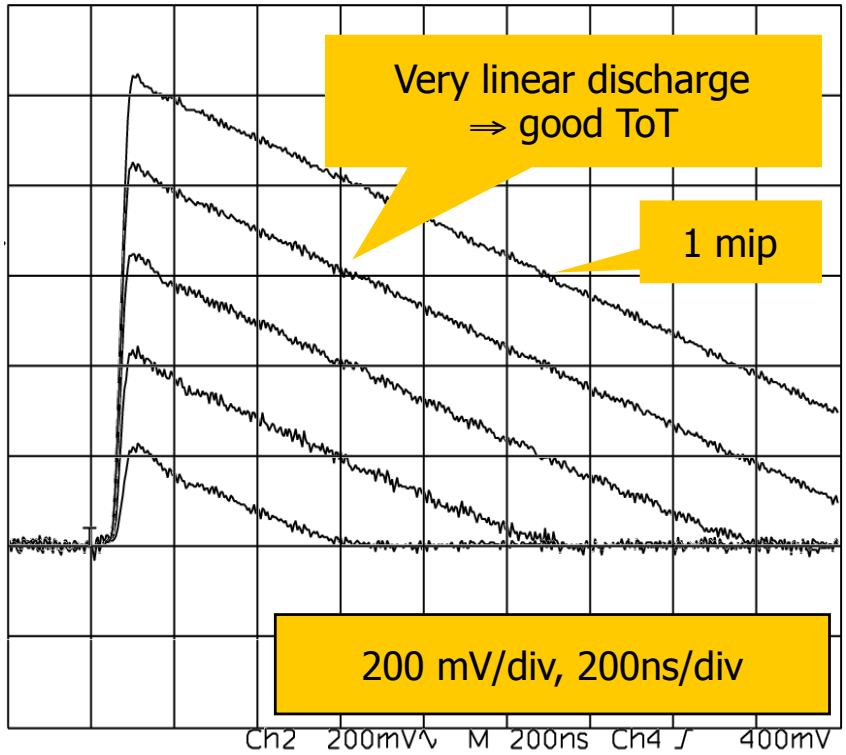
feedback uses constant current
- high stability for fast shaping
- tolerates > 100 nA leakage
- linear decay

Analog information
- measure width of hit
- works nicely due to linear discharge

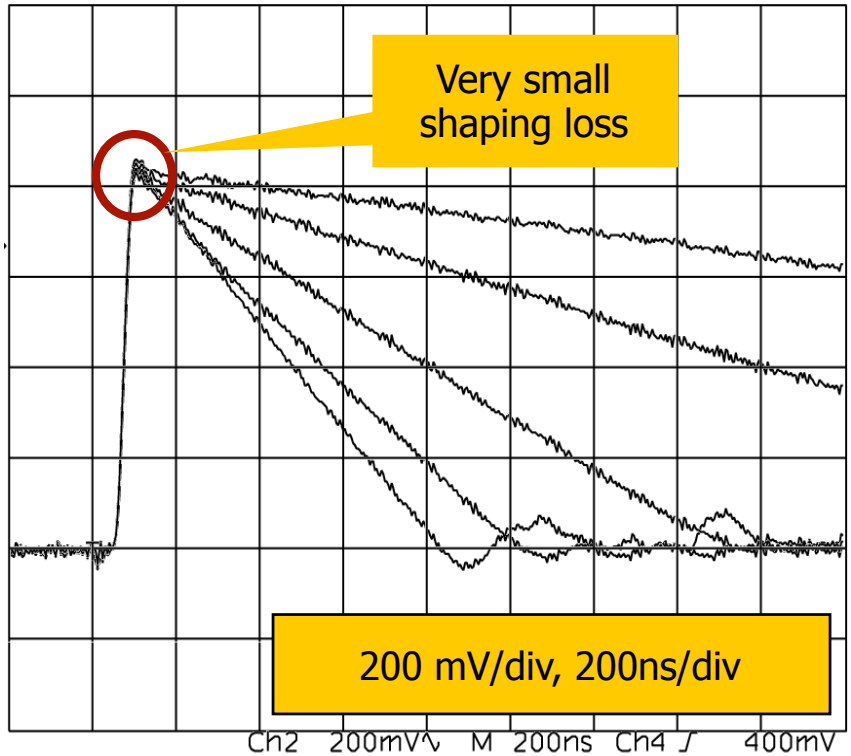
Individual adjustment of
- Threshold
- feedback current (FEI)
- ranges are adjustable



Preamplifier Pulse Shapes with Linear Discharge



Different injected charges

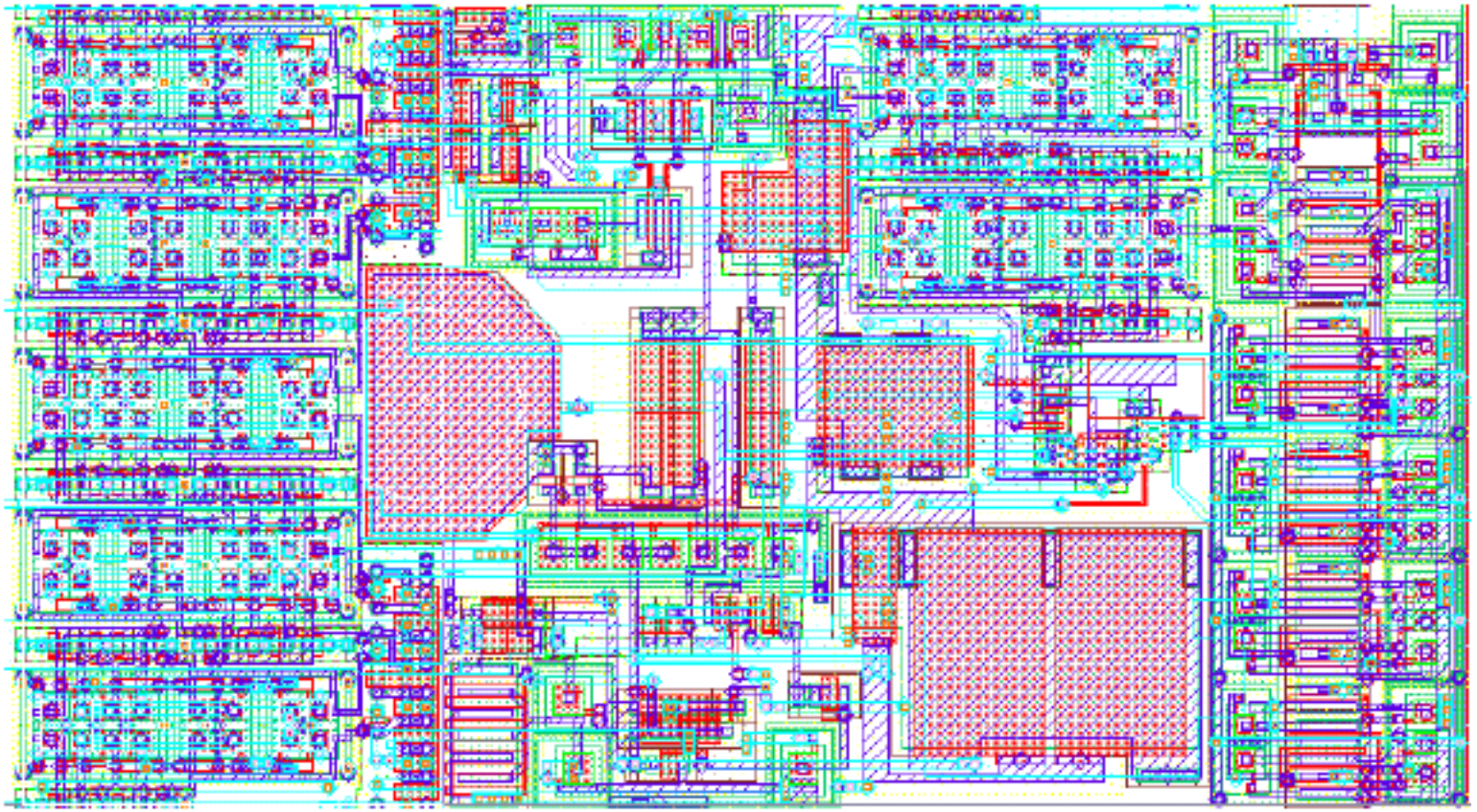


Different feedback currents

(Measured on FED test chip with internal chopper, no sensor)

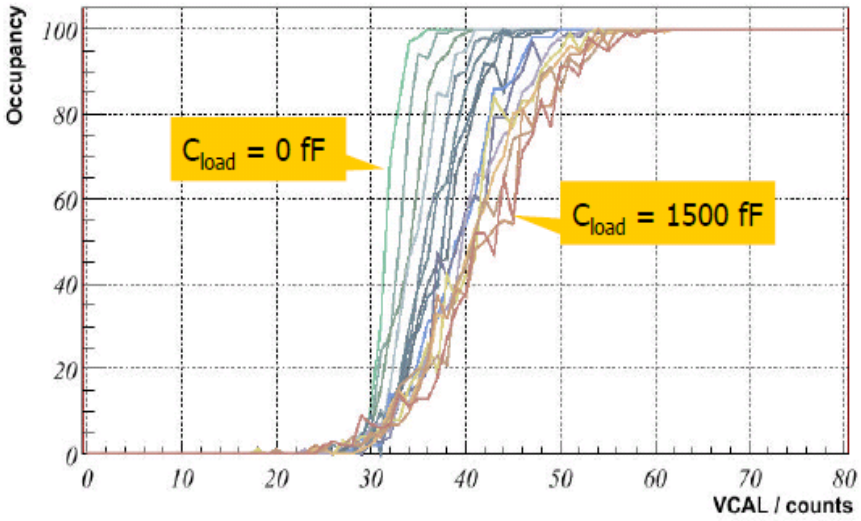
Pixel Layout (FEI – 1)

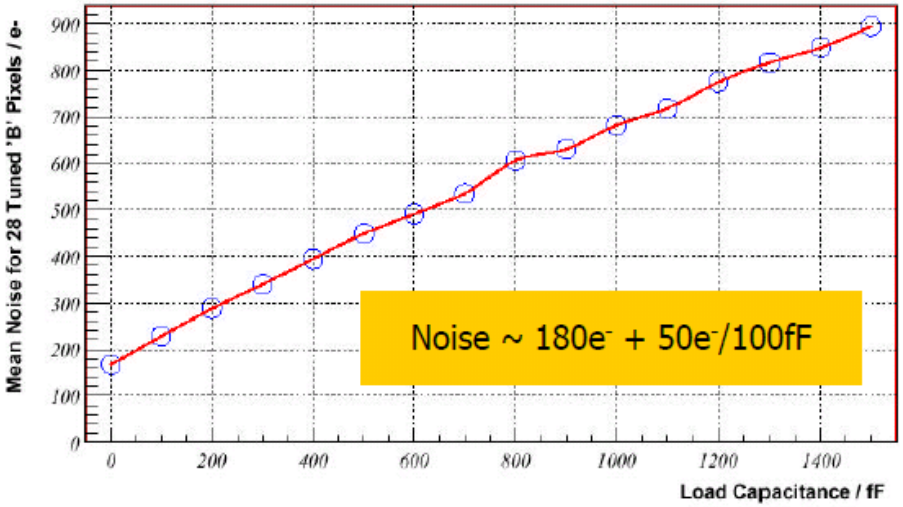
- 0.25 µm technology
- Analogue part occupies 50 × 90 µm^2
- The rest (pixel is 50 × 400 µm^2) is for readout



Noise vs. Capacitive Load

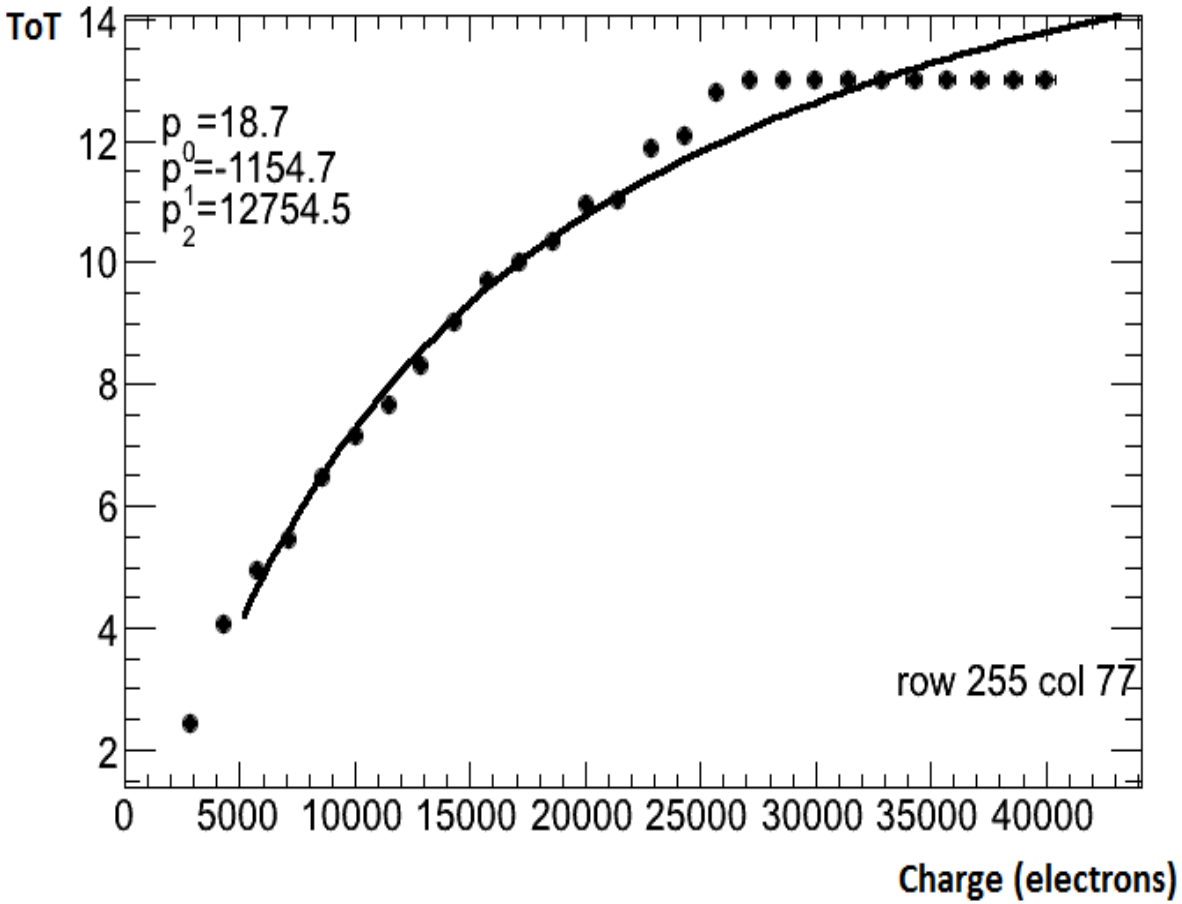
- Measure hit probability for increasing input charges





ToT Measurement (FEI-4)

- 3-4 Bit resolution – Enough for monitoring & some hit position interpolation



Data Readout

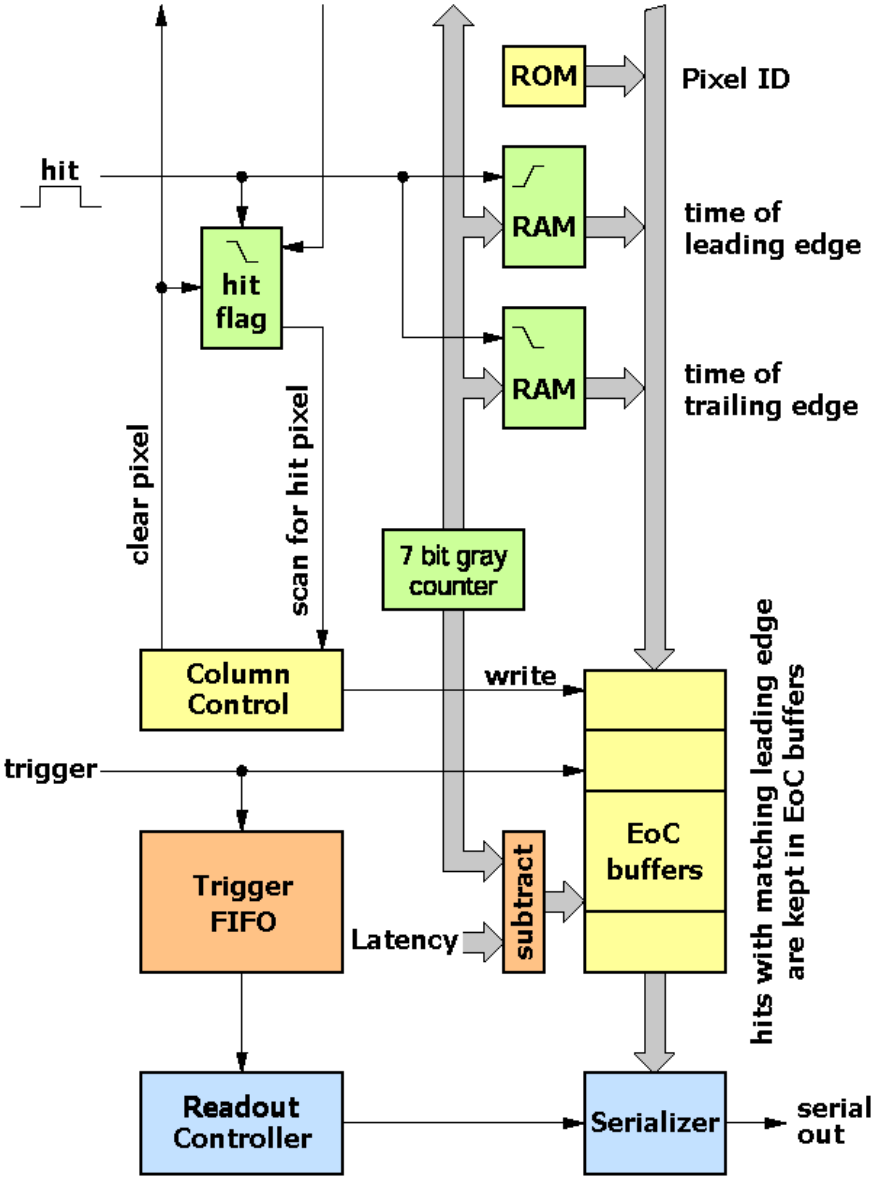
4 simultaneous tasks are running permanently:

- A time stamp (7bit Gray Code) is distributed to all pixels
- When a pixel is hit, the time of rising and trailing edges are stored in the pixel

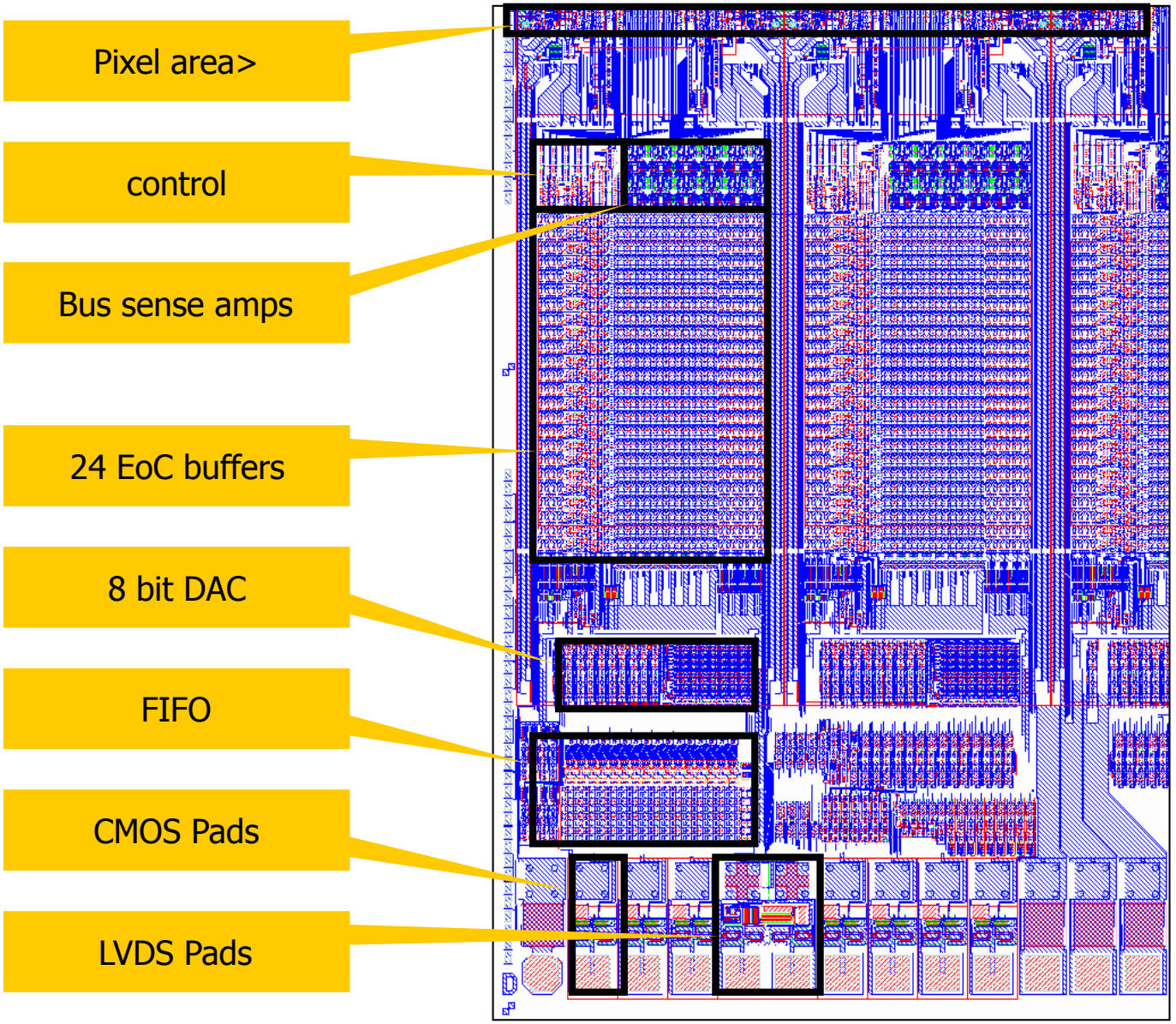
- The hit is flagged to the periphery with a fast asynchronous scan
- Time information and pixel number are written into a buffer pool (common to a column pair)
- The hit in the pixel is cleared

- If a trigger arrives, the time of the hit (leading edge data) is compared to the time for hits associated to this trigger. Valid hits are flagged, older hits are deleted.
- The trigger is queued in a FIFO

- All valid hits of a trigger are sent out serially. All triggers in the FIFO are processed.



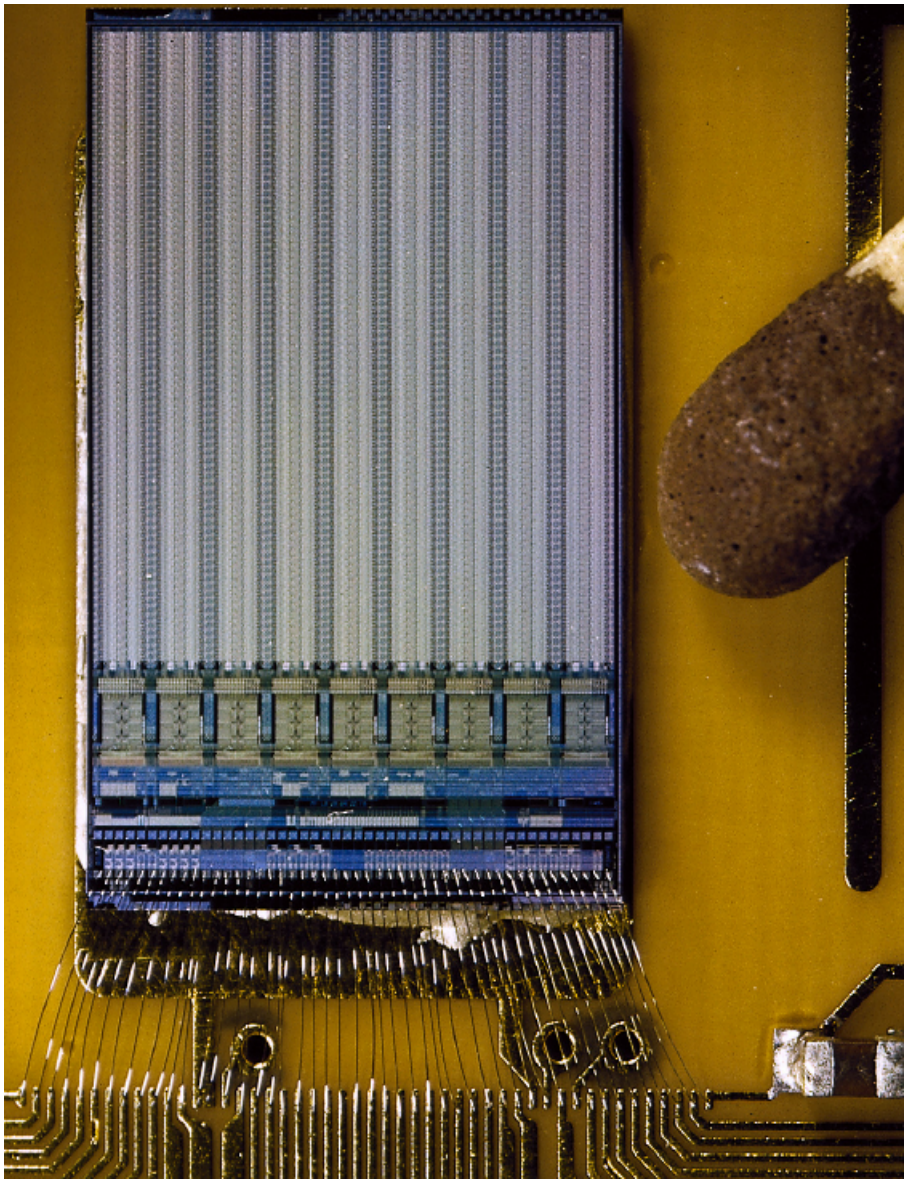
Layout of FED chip (bottom left)



(Early) ATLAS Front End Chip

- Chip size: 7.4mm x 11mm
- Pixels: 18 x 160 = 2880
- Pixel size: 50µm x 400µm
- Operates at 40 MHz
- Zero suppression in every pixel
- Data is buffered until trigger arrives
- Serial control and readout LVDS IO

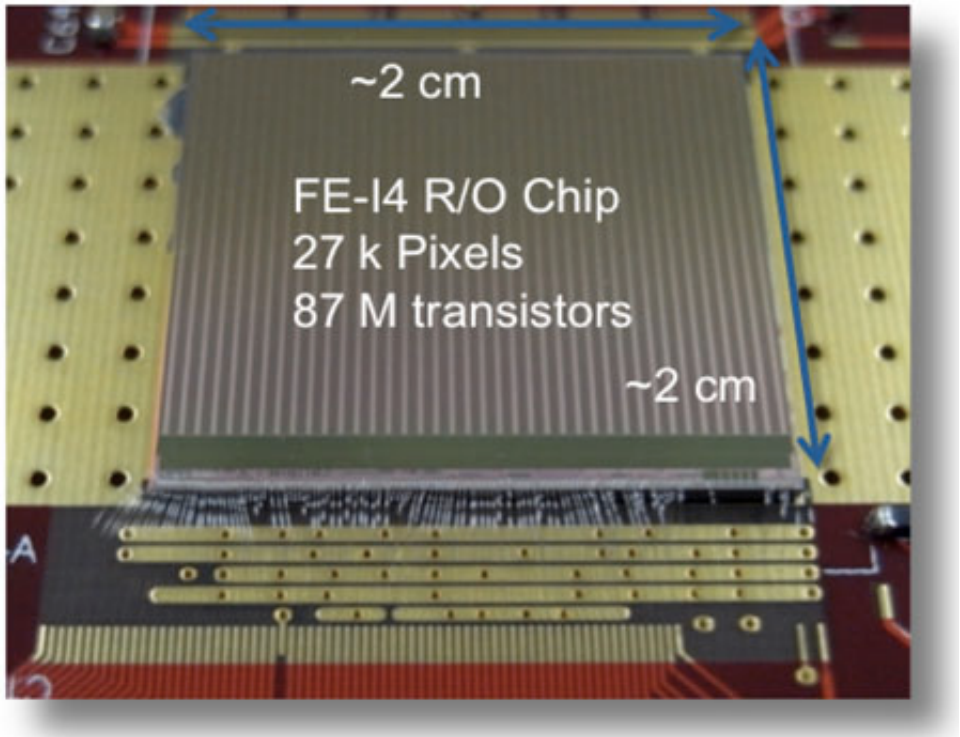
- Analog part with
  - 40 µW power dissipation / Pixel
  - ~200 e noise
  - Amplitude measured via pulse width

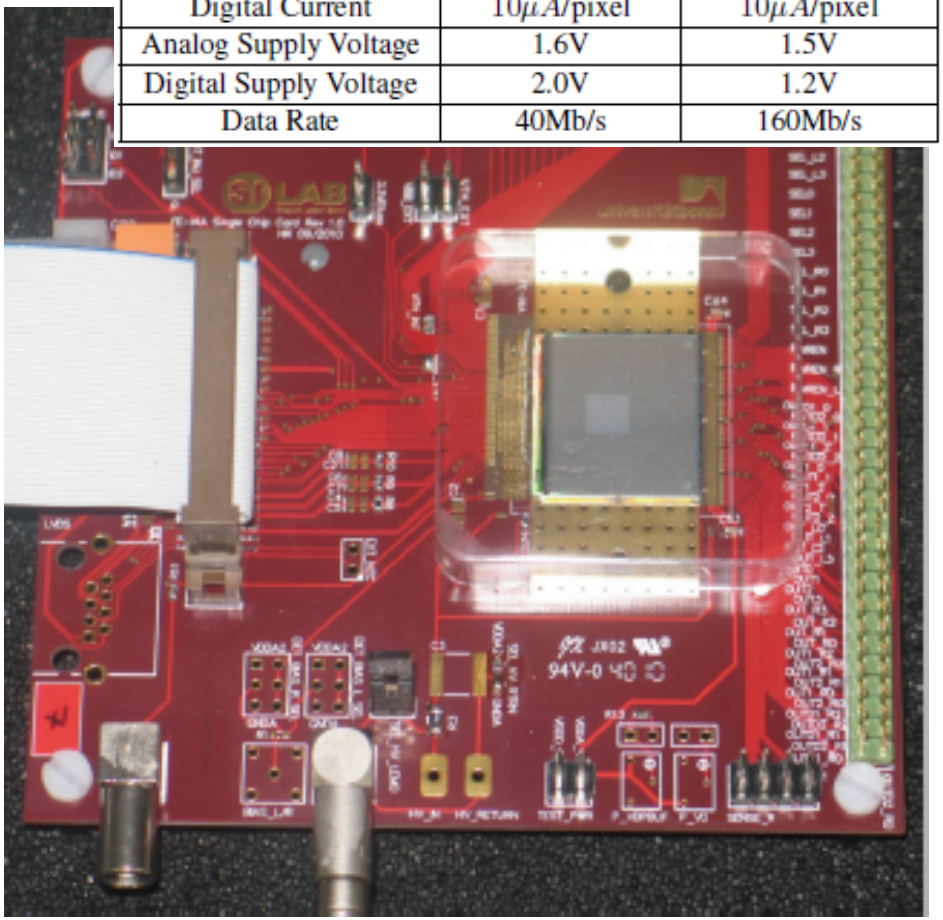


FEI-4

- Latest Chip generation uses
  - 130 nm technology
  - Much larger chip (~2 cm^2)

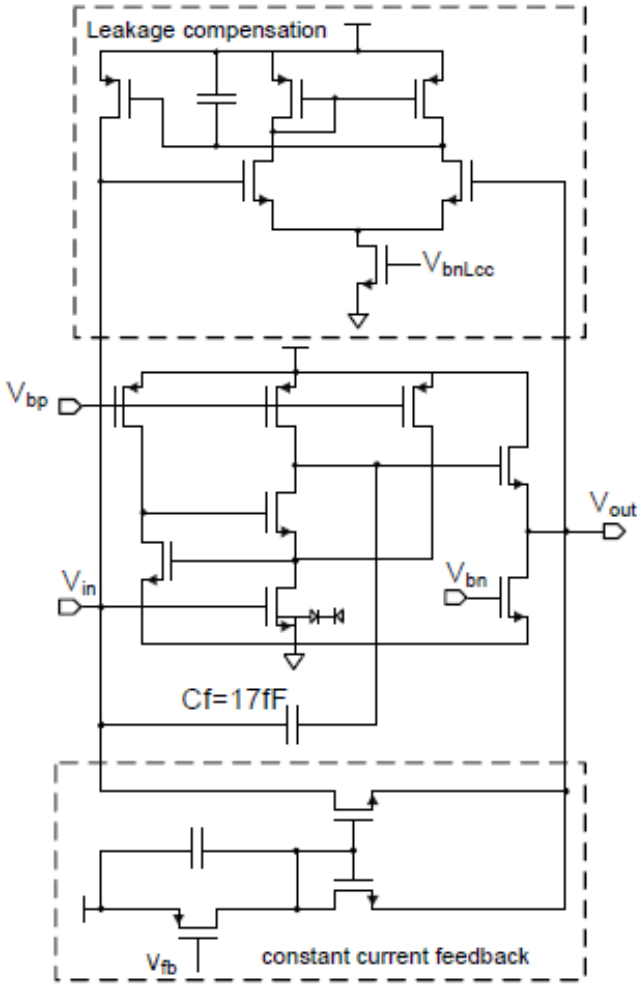
	FE-I3	FE-I4
Pixel Size	$50 \times 400 \mu m^2$	$50 \times 250 \mu m^2$
Pixel Array	18×160	80×336
Chip Size	$7.6 \times 10.8 mm^2$	$20.0 \times 18.6 mm^2$
Active Fraction	74%	89%
Analog Current	$16 \mu A$/pixel	$10 \mu A$/pixel
Digital Current	$10 \mu A$/pixel	$10 \mu A$/pixel
Analog Supply Voltage	1.6V	1.5V
Digital Supply Voltage	2.0V	1.2V
Data Rate	40Mb/s	160Mb/s





FEI-4 Frontend

- Contains a leakage compensation circuit & constant current discharge in feedback of preamplifier

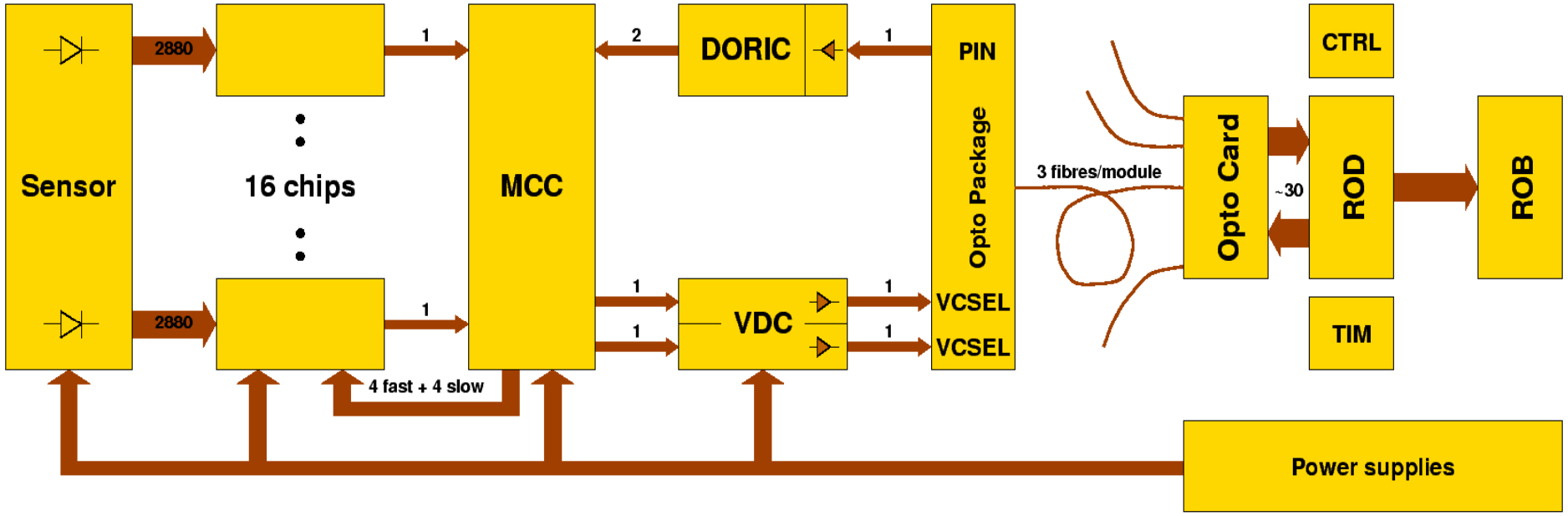


Leakage Compensation
('Krummenacher scheme')

Regulated straight cascode
+
Source follower

Constant Current Feedback
(+ 'magic' capacitor)

Other Electronic Components of the Pixel System

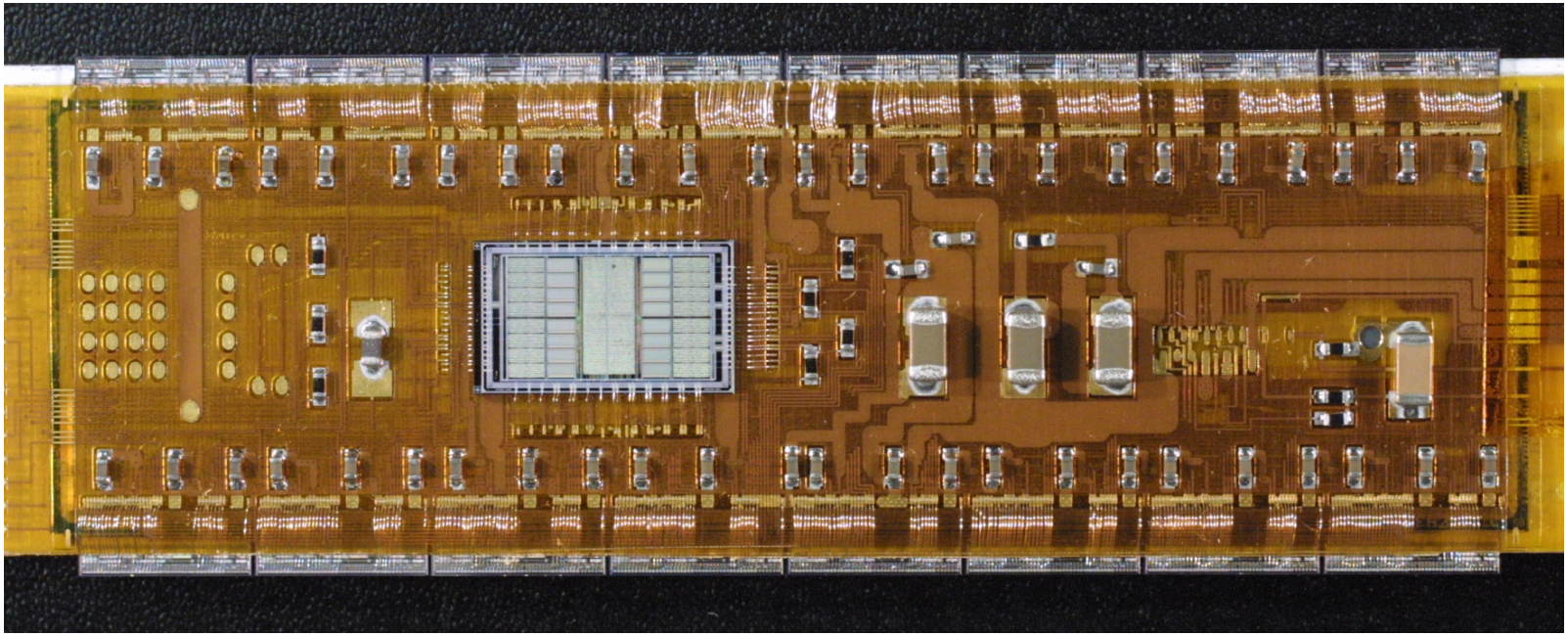


1	Sensor	
16	front end chips	(FE)
1	module controller chip	(MCC)
2	VCSEL driver chips	(VDC)
1	PIN diode receiver	(DORIC)

Optical receivers
Readout Drivers (ROD)
Readout Buffers (ROB)
Timing Control (TIM)
Slow Control, Supplies

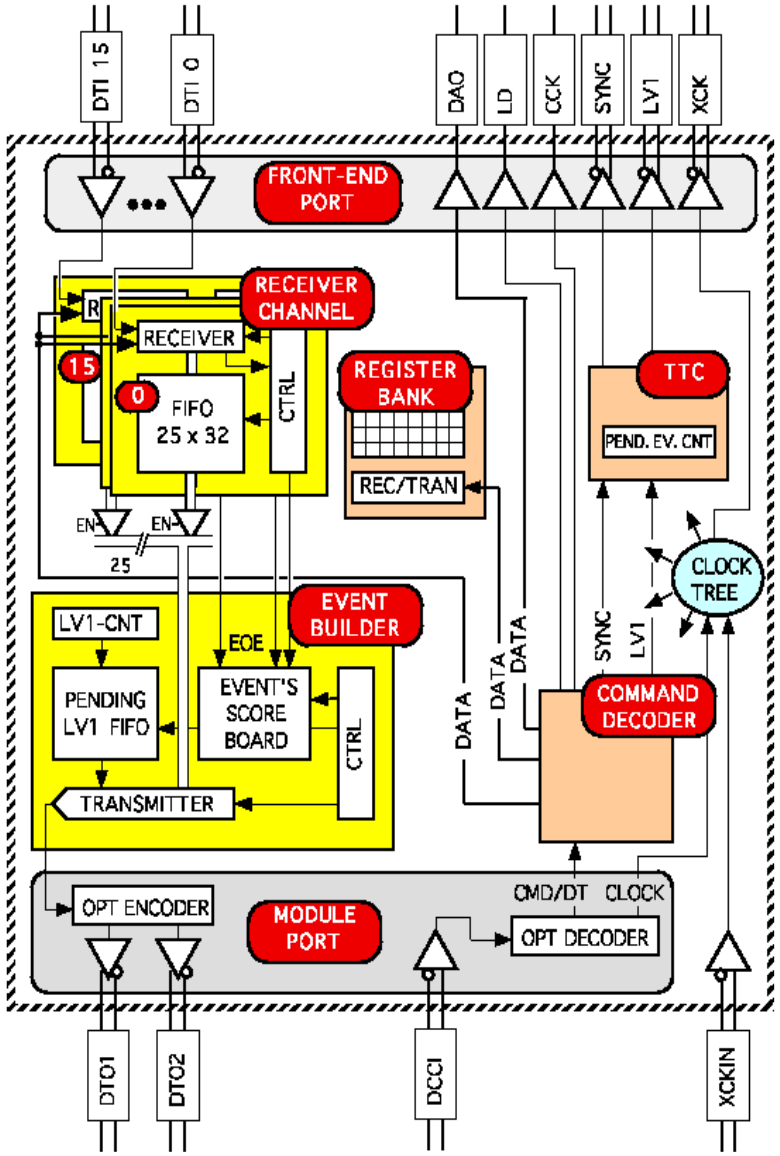
Module Controller Chip

- The Module Controller (MCC)
  - Collects data from all FEI chips
  - When data for one event is complete, send full event to DAQ
  - Receives trigger 6 slow control information from DAQ & passes it to FEI chips



MCC Details: Event building & Control

- Decode data/command signal (from DORIC)
  - configuration data
  - ‚slow' commands
  - ‚fast' commands (trigger, SYNC, ...)
- Generate control signals for FE chips
- Receive serial data from 16 FE chips, accumulate data in FIFOs
- Check consistency of event (‚score board')
- Build complete module event
- Send event to DAQ (via VDC)
- Error handling, fault conditions (disable defective FE chips, ...)



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OTHER HEP / LHC PIXEL READOUTS

DELPHI Experiment (@ LEP)

- One of the first pixel detectors in 3µm technology
- Hits are stored, readout via column/row scan

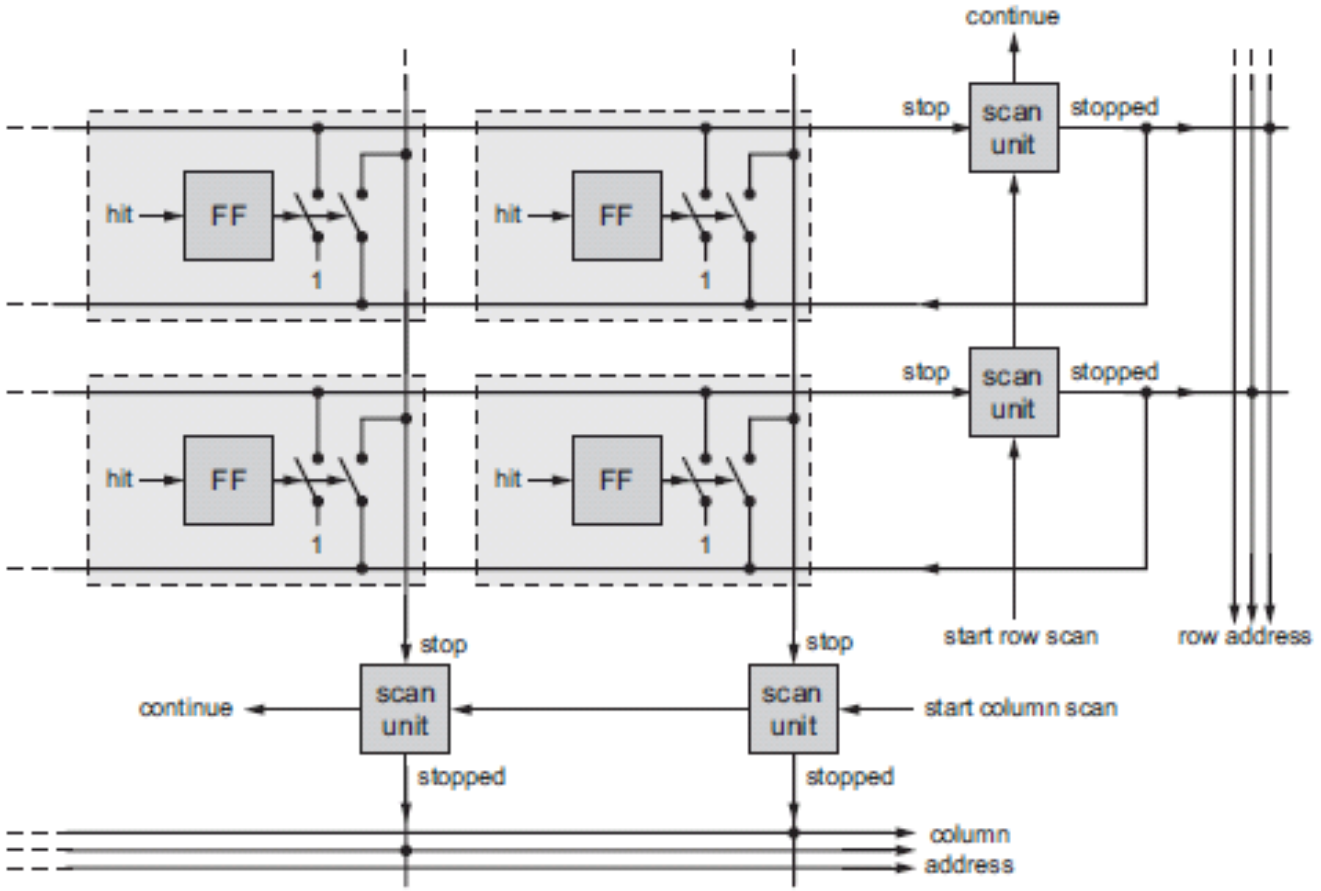


Fig. 3.35. The readout architecture of the DELPHI pixel chip

Omega Experiment (Early version): Timer

- Hit starts a 'one shot' (= timer) which elapses after Latency
  - Two timer versions are shown
- Trigger at that moment starts a readout
- Double buffer eliminates dead time

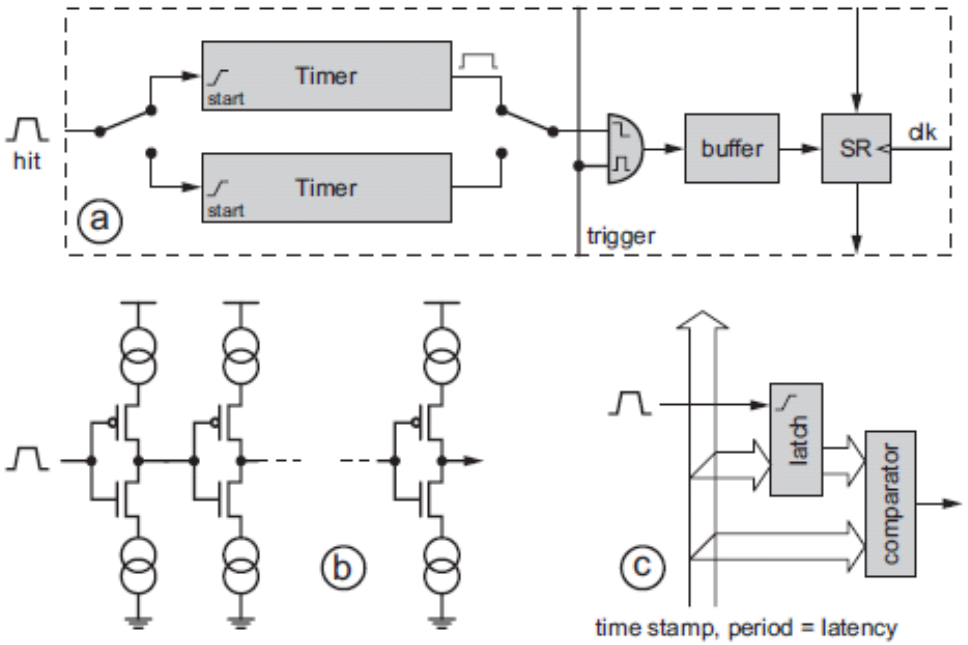


Fig. 3.36. Readout using timers in the pixel (**a**). The timers can be implemented as chains of current deprived inverters (**b**) or by using an external time stamp in a purely digital solution (**c**)

Early ATLAS

- Simple architecture for ‘coarse’ 0.8µm technology

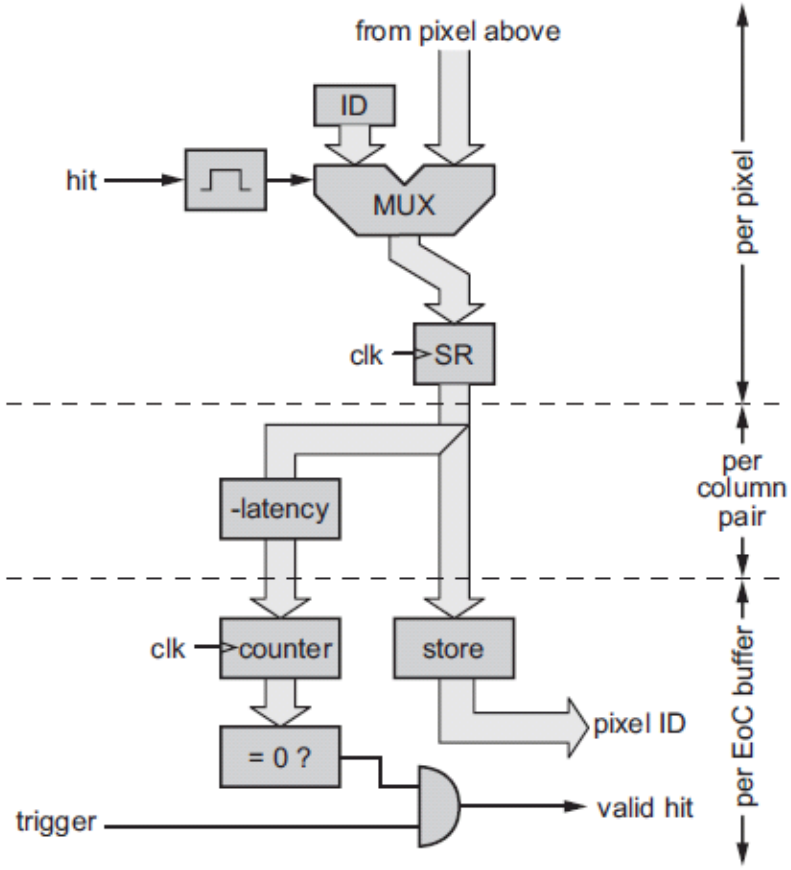


Fig. 3.37. The “conveyor belt” architecture uses a digital shift register to transport the ID of a hit pixel to the bottom of the column where it arrives after exactly ID clocks pulses. The trigger coincidence is performed after (latency-ID) further clock pulses in buffers at the bottom of the chip

CMS 'Column Drain'

- Analogue Readout

Store analogue peak value in pixel

Transfer analogue value to analogue buffer

Time of hits is stored globally. Readout then finds all hits for one time stamp / this must be quick!)

Detail: Do not store time stamp, but pointer to a time stamp → less bits required

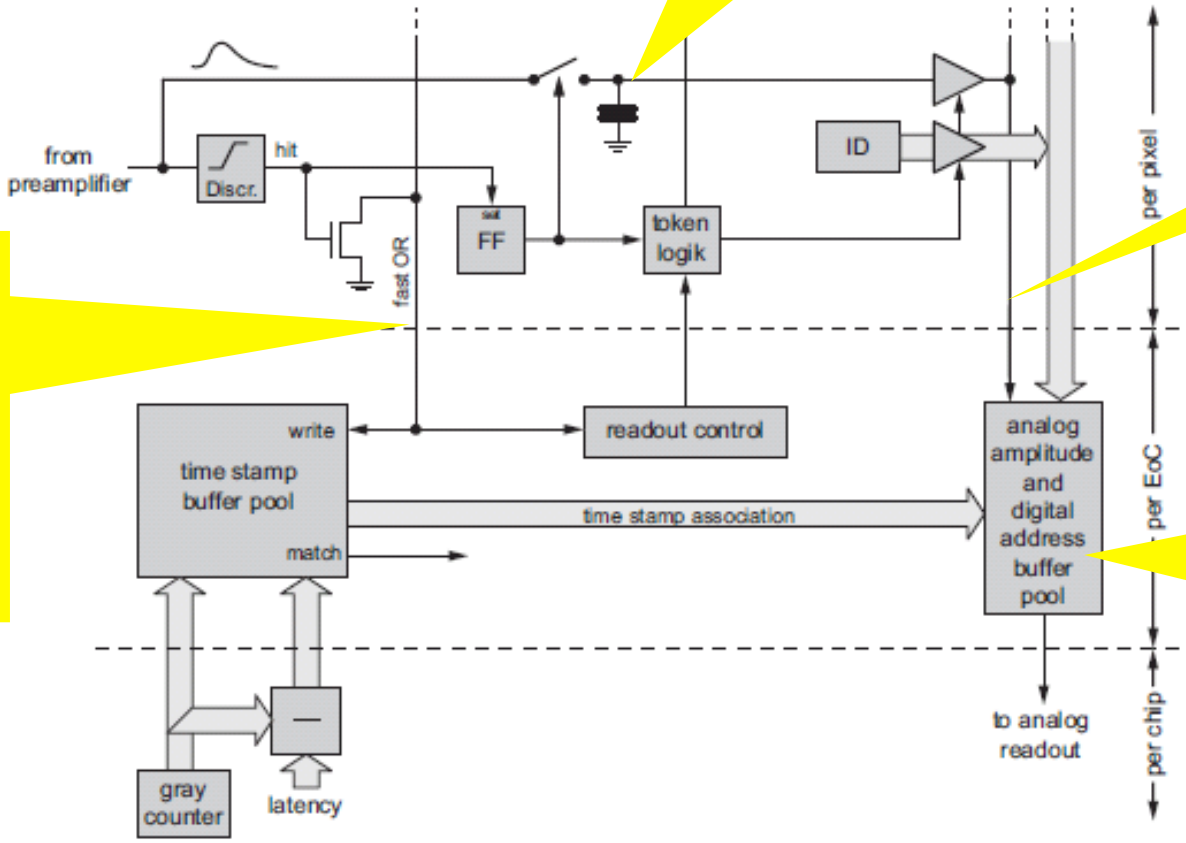


Fig. 3.39. The Column Drain Readout transfers the amplitude and address of hits to buffers in the EoC which are associated to a single digital buffer holding the time stamp of the event

Fermilab FPIX

- Pixels are associated to a time stamp (4 possible)

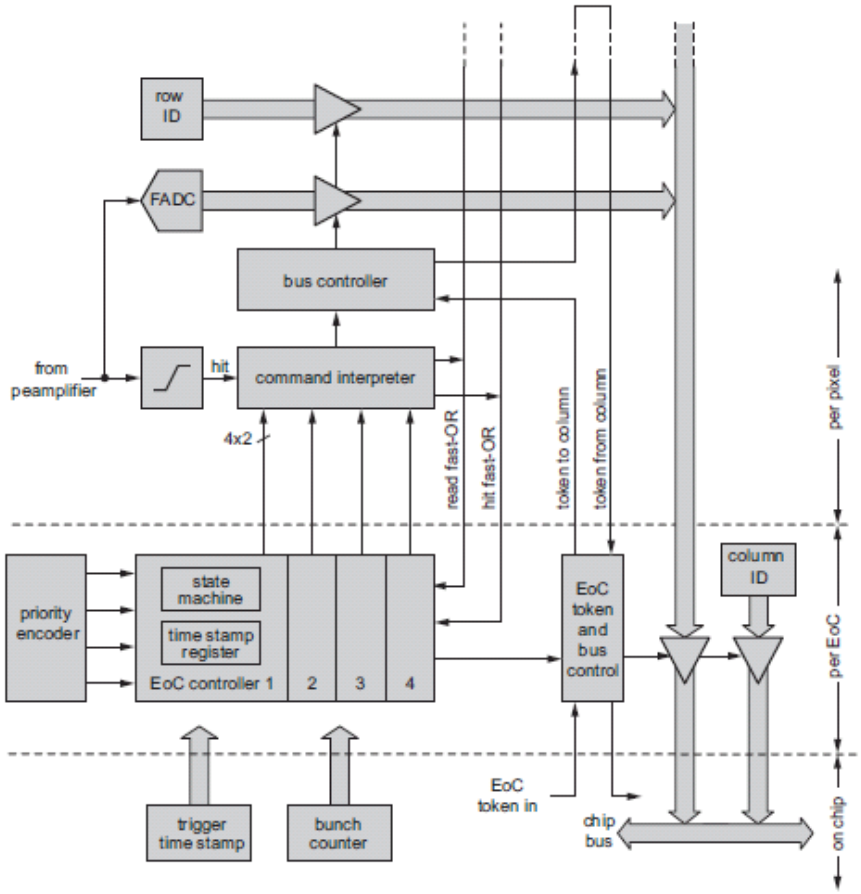
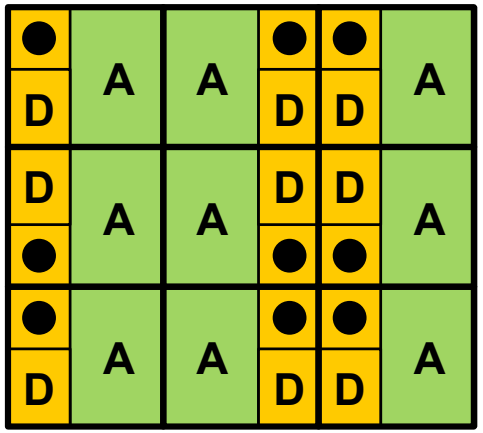


Fig. 3.40. The FPIX chip family uses several simple readout controllers in the end of the column part. All hits within a column occurring at the same bunch crossing are associated to one of the four available controllers where the time stamp is stored

More Pixel Detectors

Challenges for Pixel Readouts

- Small available size
  - (less of a problem with modern technologies)
- Limited Power
  - 10-50µW per pixel in continuous mode
  - Influences a lot the cooling infrastructure
- Crosstalk
  - Analogue and digital part close together
  - Pixels often flipped



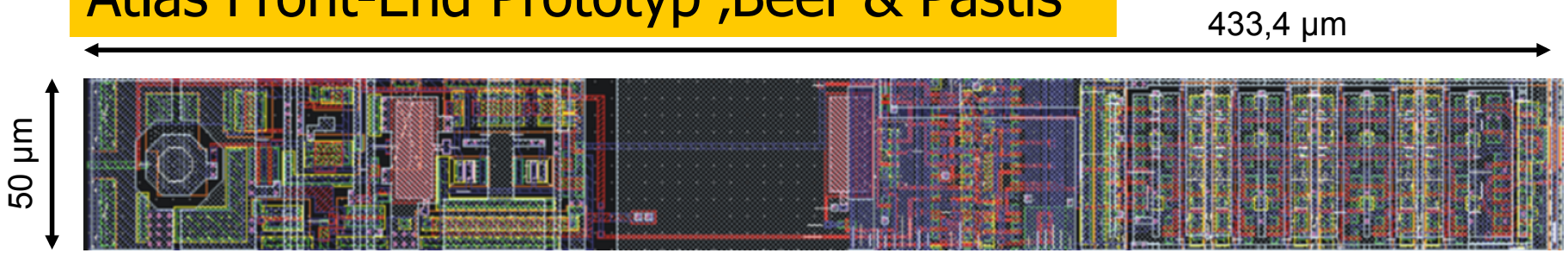
- Low noise hit rate (→ noise, threshold dispersion)
- Power & signal distribution
  - Access often only from one side to allow module construction
- Large Chips
  - reduce dead space between pixels
  - High prototyping cost (~ chip area)
- Bumping

Readout Concepts for Pixel Detectors

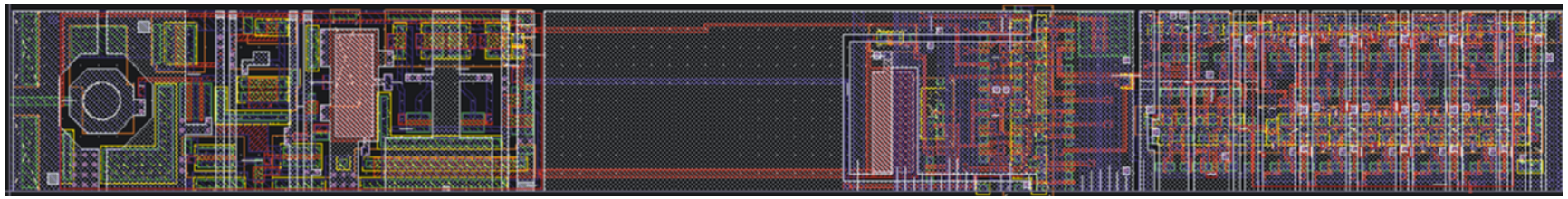
- Analog Storage & Sequential Readout
  - + Amplitude available, Simple → small pixels, low digital noise
    → Good Resolution by Interpolation, Energy information
  - - Slow
  - - Requires Trigger (can use 'rolling shutter' mode)
- Counting
  - + Fast, No Trigger required
  - - Complex, mixed analogue / digital, large pixels
- Burst Storage – Analogue / Digital (XFEL)
  - + Fast
  - - Larger pixels, complex
  - • Special purpose
- Triggered (for instance LHC architectures)
  - - Complex
  - • Special Purpose

Example: From ATLAS to Counting Pixel

Atlas Front-End Prototyp ‚Beer & Pastis'



Xray chip MPEC 1.1

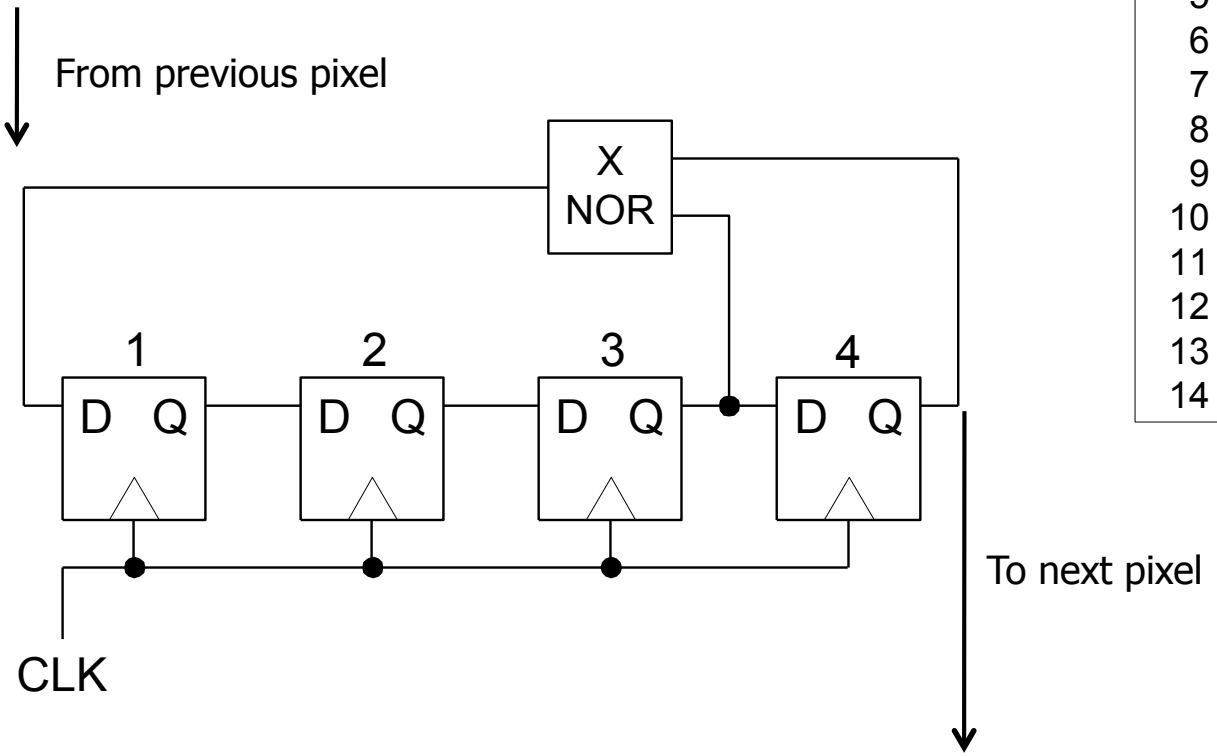


Technology: AMS 0.8µ CMOS

Counter Detail

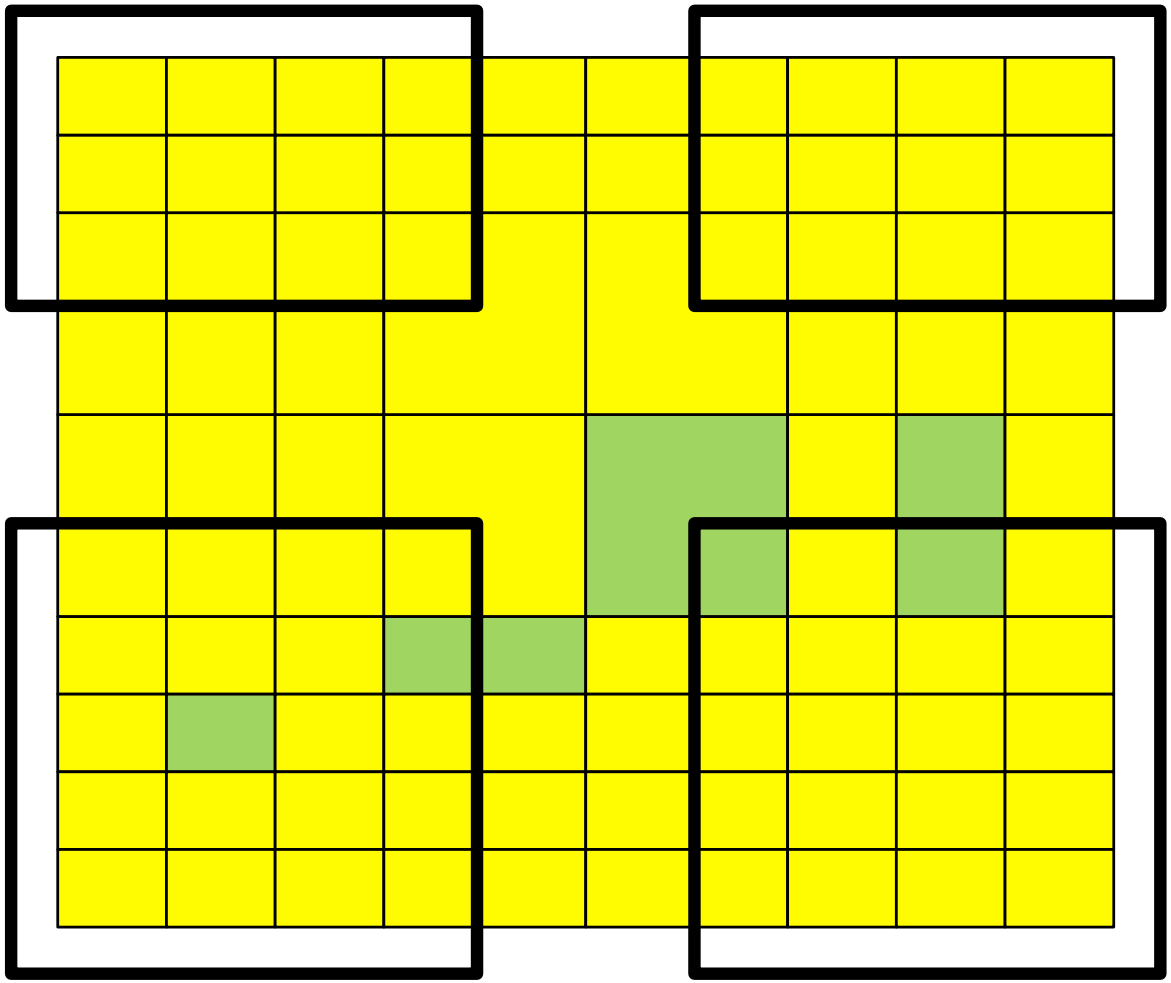
- Linear Feedback Shift Register:
  - Simple, compact, includes readout
- Requires lookup table for decoding

Clk	Register
0	0 0 0 0
1	1 0 0 0
2	1 1 0 0
3	1 1 1 0
4	0 1 1 1
5	1 0 1 1
6	1 1 0 1
7	0 1 1 0
8	0 0 1 1
9	1 0 0 1
10	0 1 0 0
11	1 0 1 0
12	0 1 0 1
13	0 0 1 0
14	0 0 0 1



Module with several chips

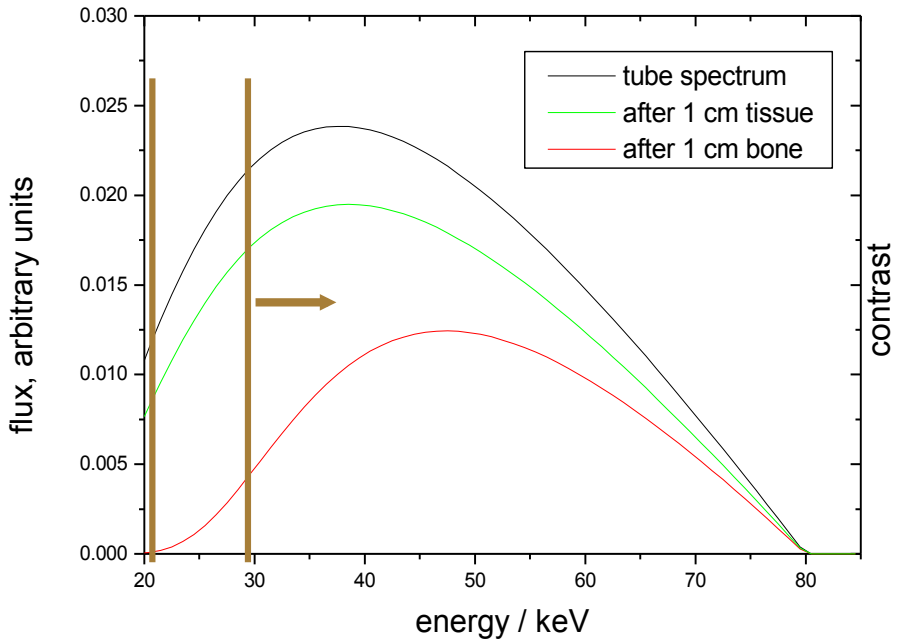
- Gap between chip is ‘filled’ with larger pixel
  - Strongly reduced resolution: larger pixels AND larger noise!



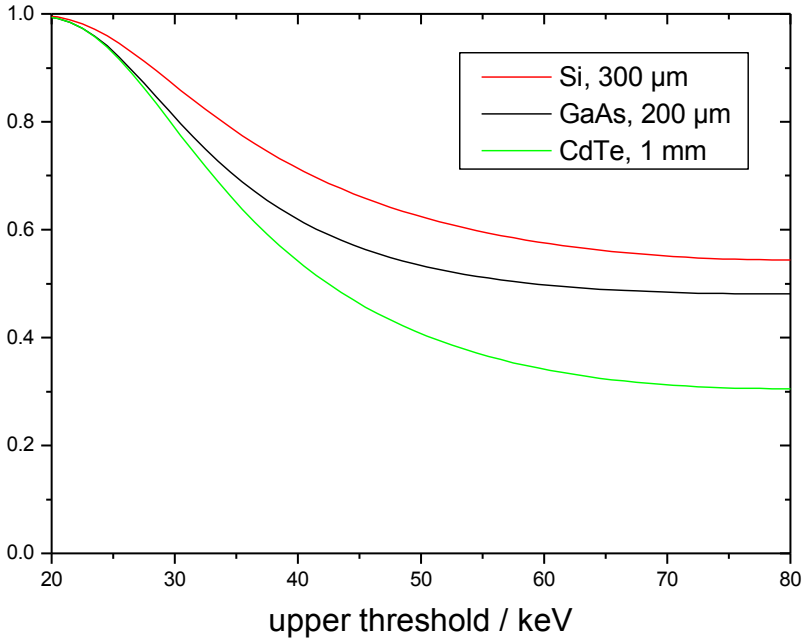
Note: ATLAS uses
‘ ganged’ pixels

Special: Energy Window with 2 Thresholds

- Idea: Spectrum changes shape after different materials
- Estimate spectrum by counting low / high Energy X-rays.



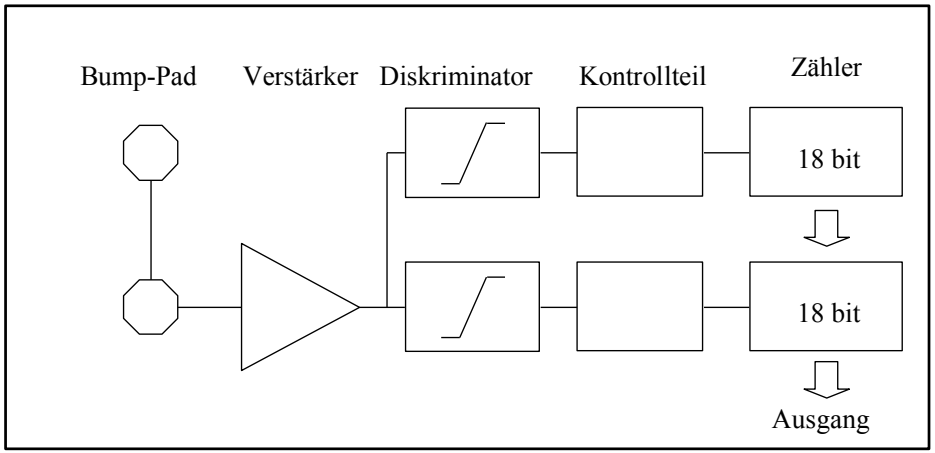
Spectrum of transmitted X-rays

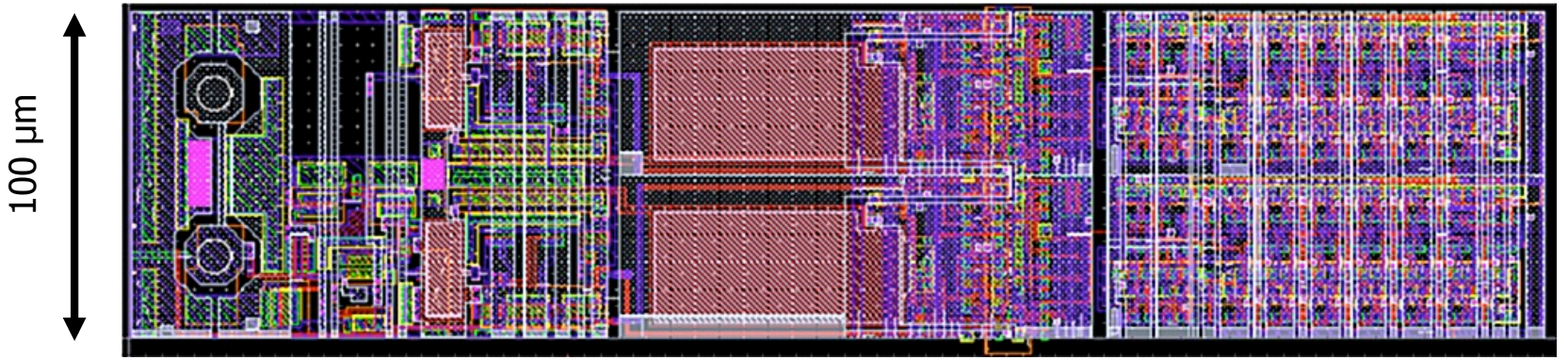


Contrast Enhancement

Implementation: MPEC 1.D

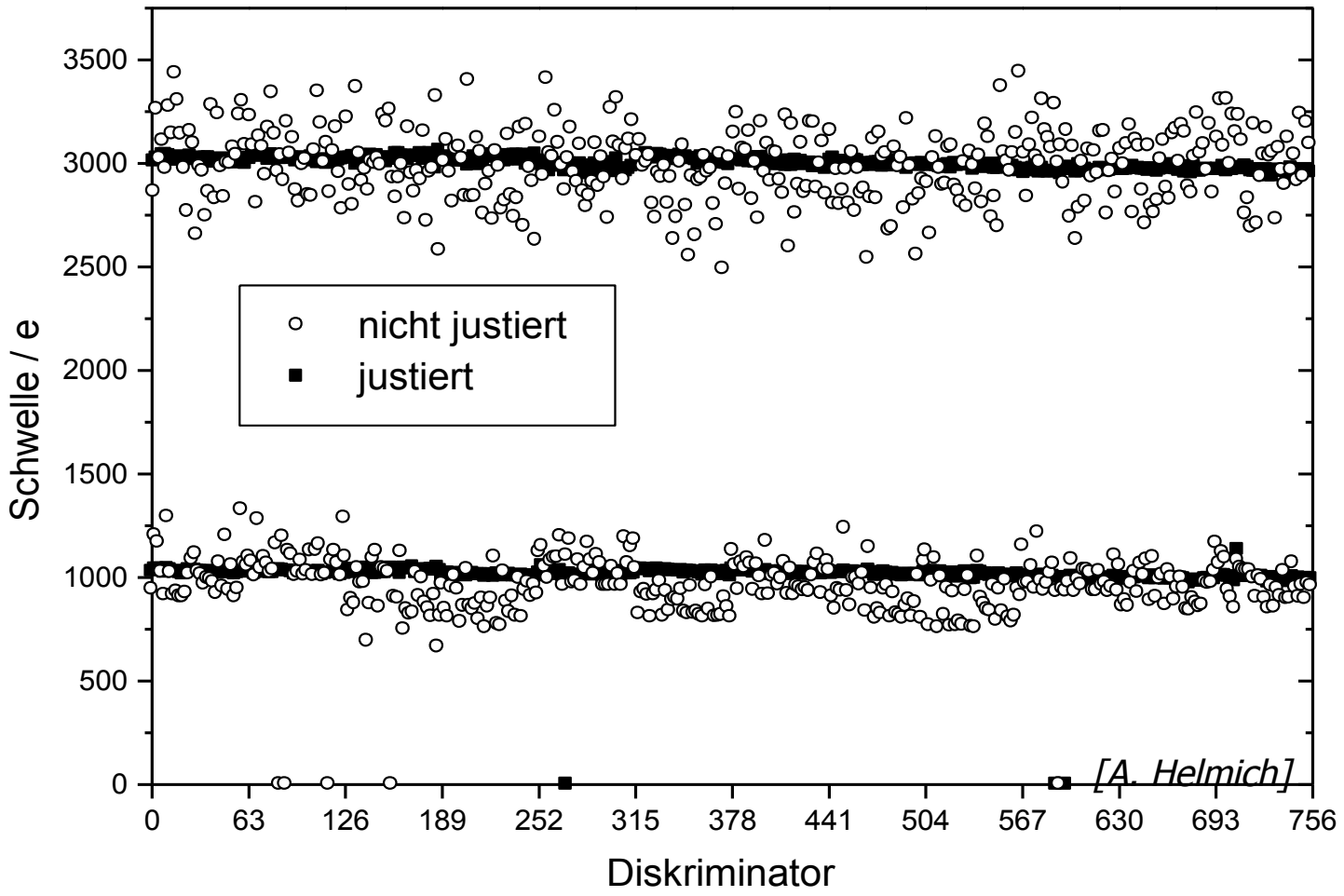
- Two Thresholds, two counters
- For prototype: Merge two pixels in MPEC 1.1





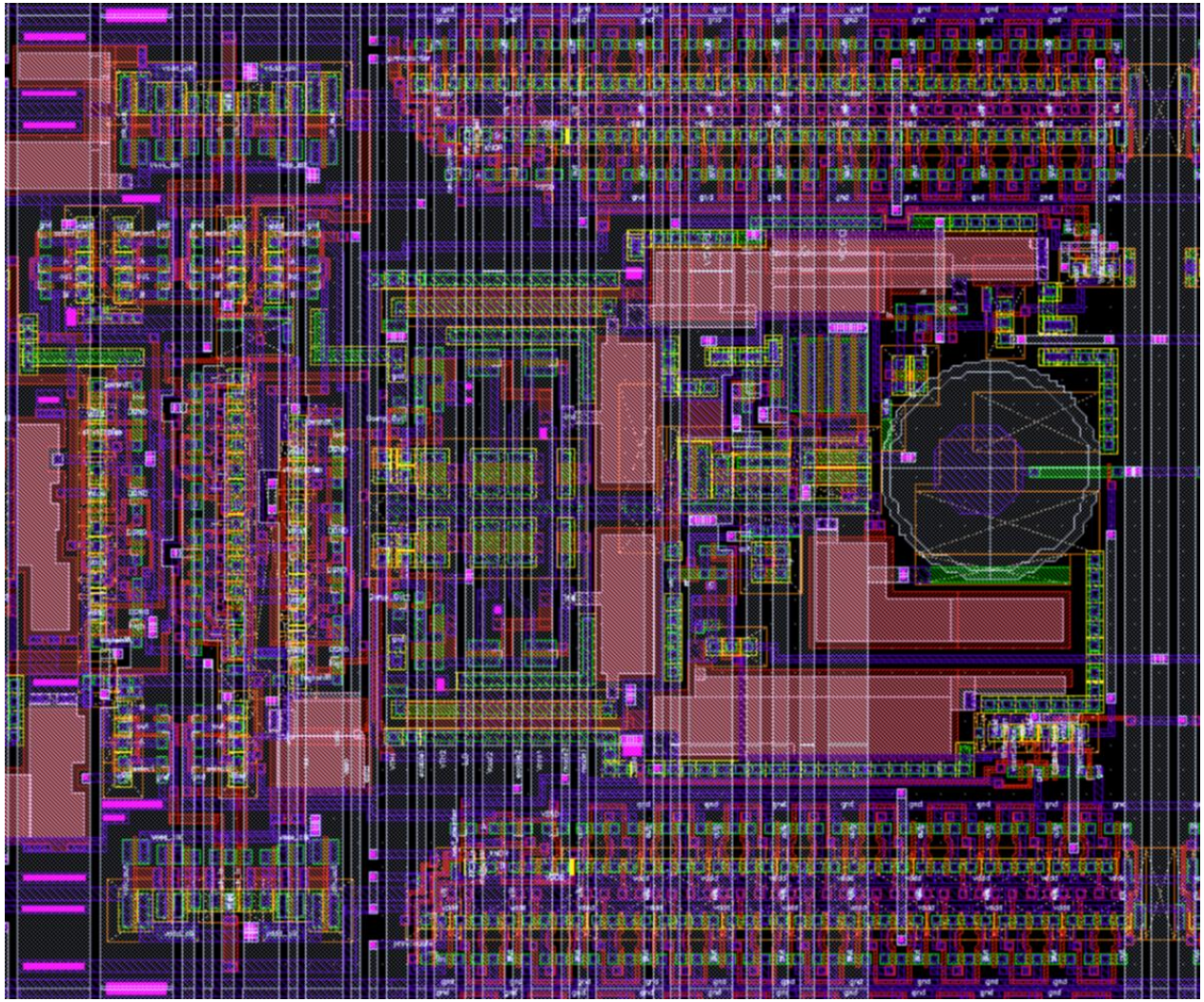
MPEC 1.D – Two Thresholds

- Thresholds must be well defined: Need good ‘trim’

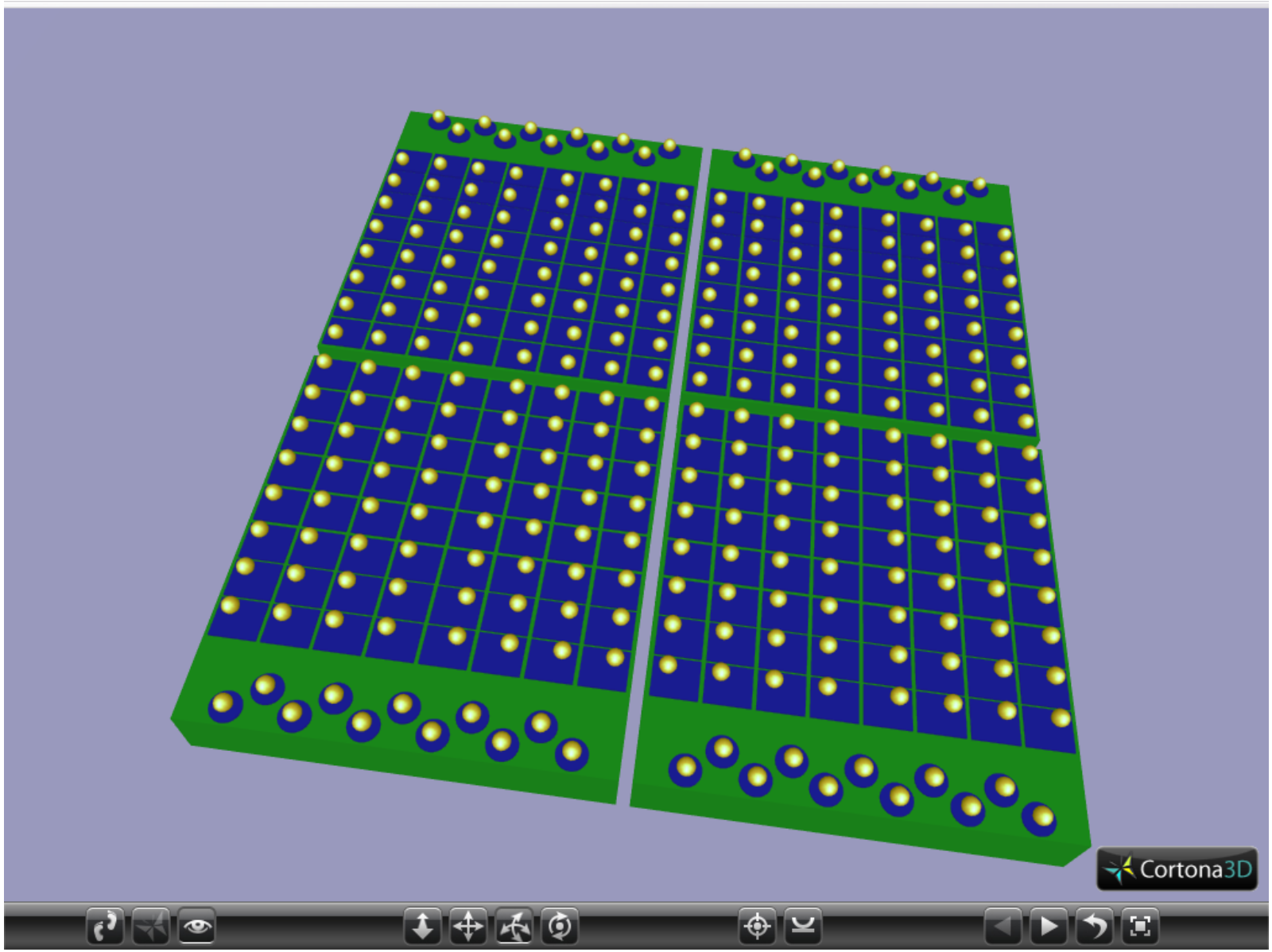


Pixel Layout (MPEC 2.x)

- Here: Square Pixel with large (convenient) bump pad

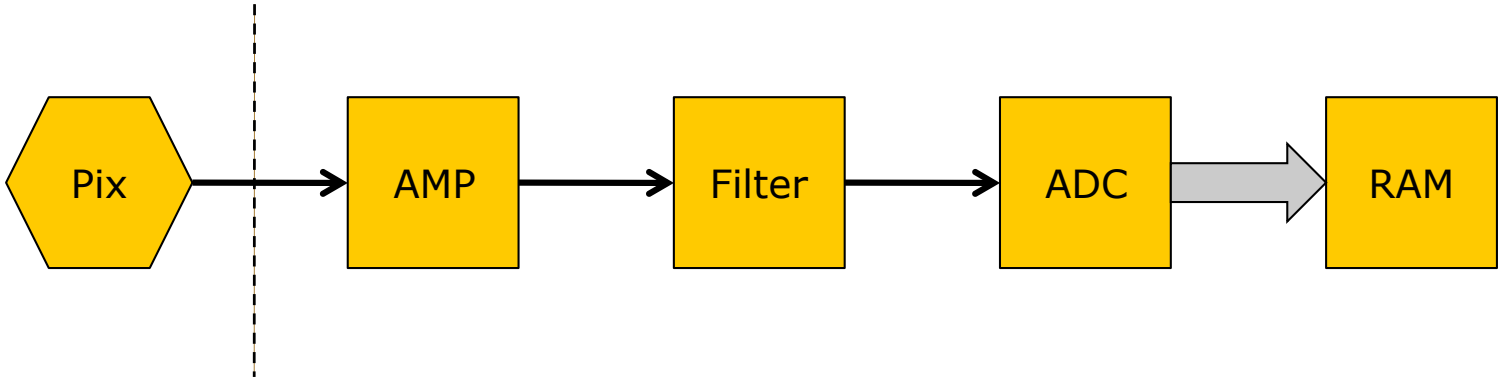


Pixel Readout for XFEL

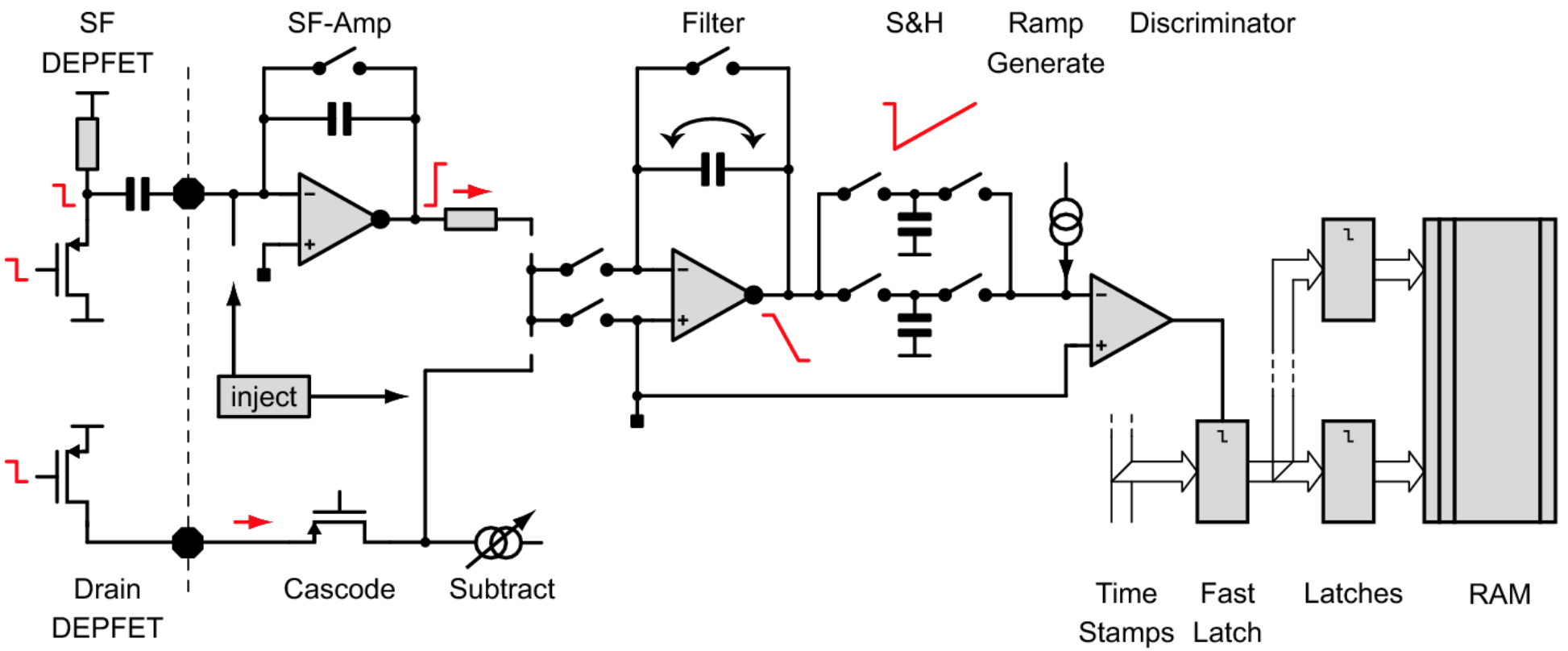


What is Special ?

- Very low noise → DEPFET, trapezoidal filter
- Dynamic range of > 10^4 → special shape of internal gate
- 5 MHz ↔ 150Gbps (4096 pix, 8Bit) → **local storage**
- Store many words → **digital** storage → **ADC** required
- Read during 100 ms gap → 200 Mbps per chip ✪
- Bunch of 0.6 ms, 100 ms gap → Power cycling
- Low Energy X-rays, 450µm sensor → no TID problem on chip



Pixel Circuit Details



FE Alternatives:

- Source Follower Readout with U → I Converter (top)
- Current Readout (bottom)

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STRIP DETECTORS

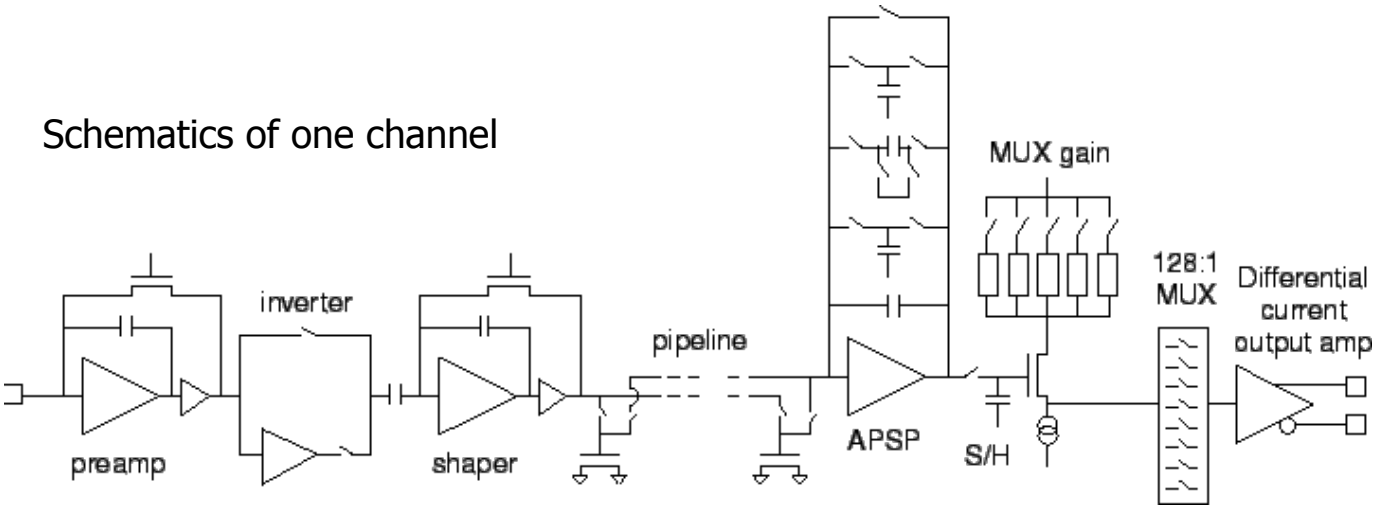
Readout Concepts for Strip Detectors

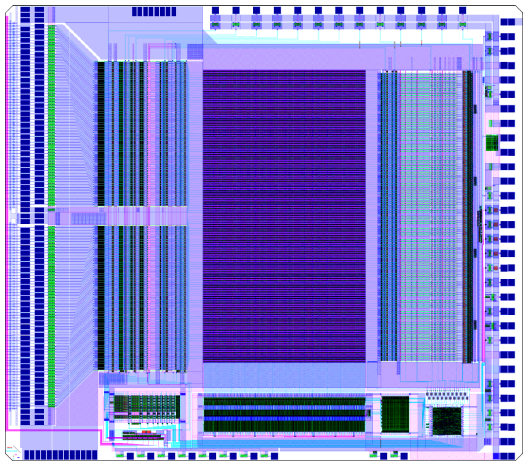
- ‘Sample & Hold’ + Analogue Readout
  - Amplitude available, Simple
    + small chip
    + small digital noise
    + good resolution by Interpolation, Energy information
    - Slow
    - Requires (normally) Trigger (can use ‘rolling shutter’ mode)
- Analogue Ring Buffer & Trigger & Readout
  - Commonly used
- Counting
  - Special Applications (Mythen @ SLS @ PSI for Synchrotron radiation)
- Self Triggered
  - Coming up

APV25 Readout Chip

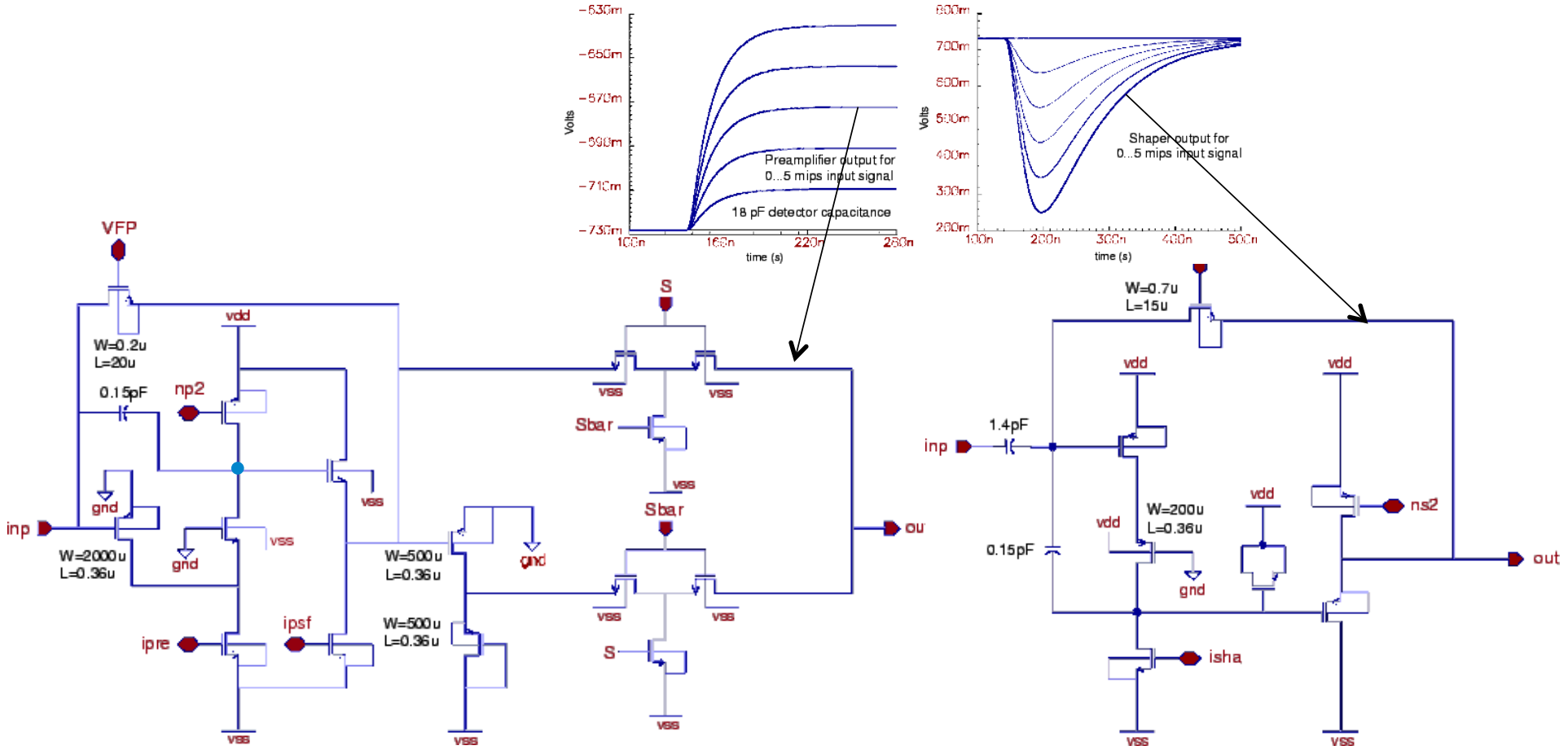
- Developed for CMS by IC London and RAL (UK)
- 0.25 µm CMOS process (>100 MRad tolerant)
- 128 channels
- 50 ns shaping time: slower than needed to reduce noise. Recover pulse information by 'deconvolution' in 'APSP'
- Noise: 250 e + 36 e/pF
- analog pipeline ('ring buffer') to store pulse samples. Read out several samples along shaping curve

Schematics of one channel





APV Circuit Detail: Preamplifier / Shaper

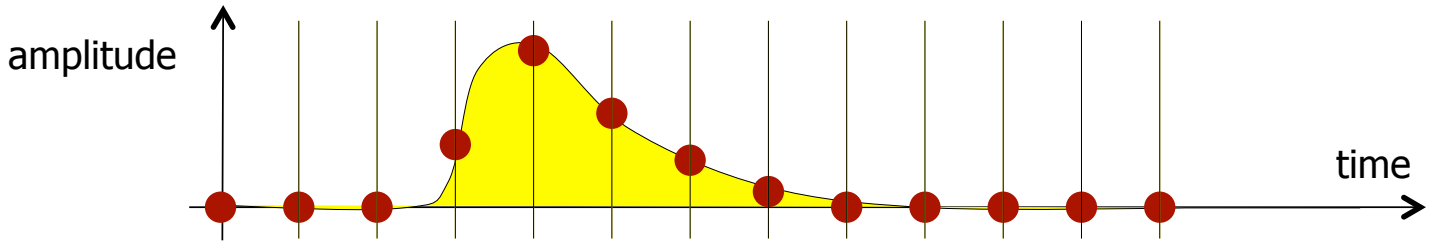


Classical 'folded Cascode'	Source Follower	Inverter	Switches	'straight Cascode'	Source follower
0.9 mW	0.12 mW	0.12 mW		0.25 mW	

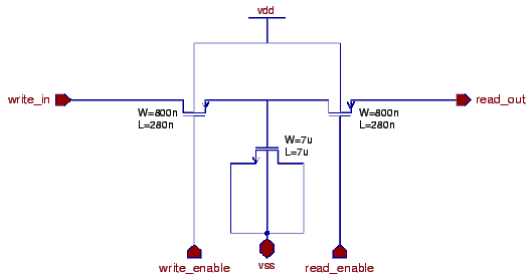
www.hephy.at/user/friedl/diss/html/node32.html

APV: Ring Buffer Operation

- Shaper output is sampled with 40 MHz



- Analogue voltages are stored in 192 capacitors (per channel) until the trigger decision arrives



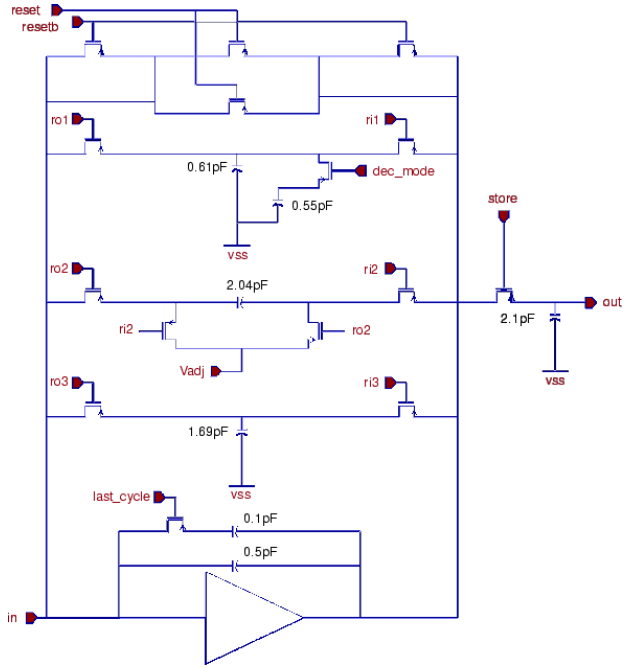
- 3 samples around peak are passed to ‘pulse processor’
- Reading out all pulses takes long (5µs). Therefore, new triggers must be accepted before readout is done. Up to 32 triggers can be accepted. Needed storage cells are flagged and not overwritten by later events!

APV: Analogue Pulse Processor

- LHC has a bunch repetition of 25 ns, but APV has a shaping (peaking) time of 50 ns to save power / reduce noise
- In order to find out to which bunch crossing this pulse belongs, it is possible to derive the (delta) input pulse to the amplifier by 'deconvolution'
  - (the output of the shaper is the input signal folded / convolved with the impulse response of the system)
- This can be achieved (in the case of a CR-RC shaper) by adding 3 samples with different weights:

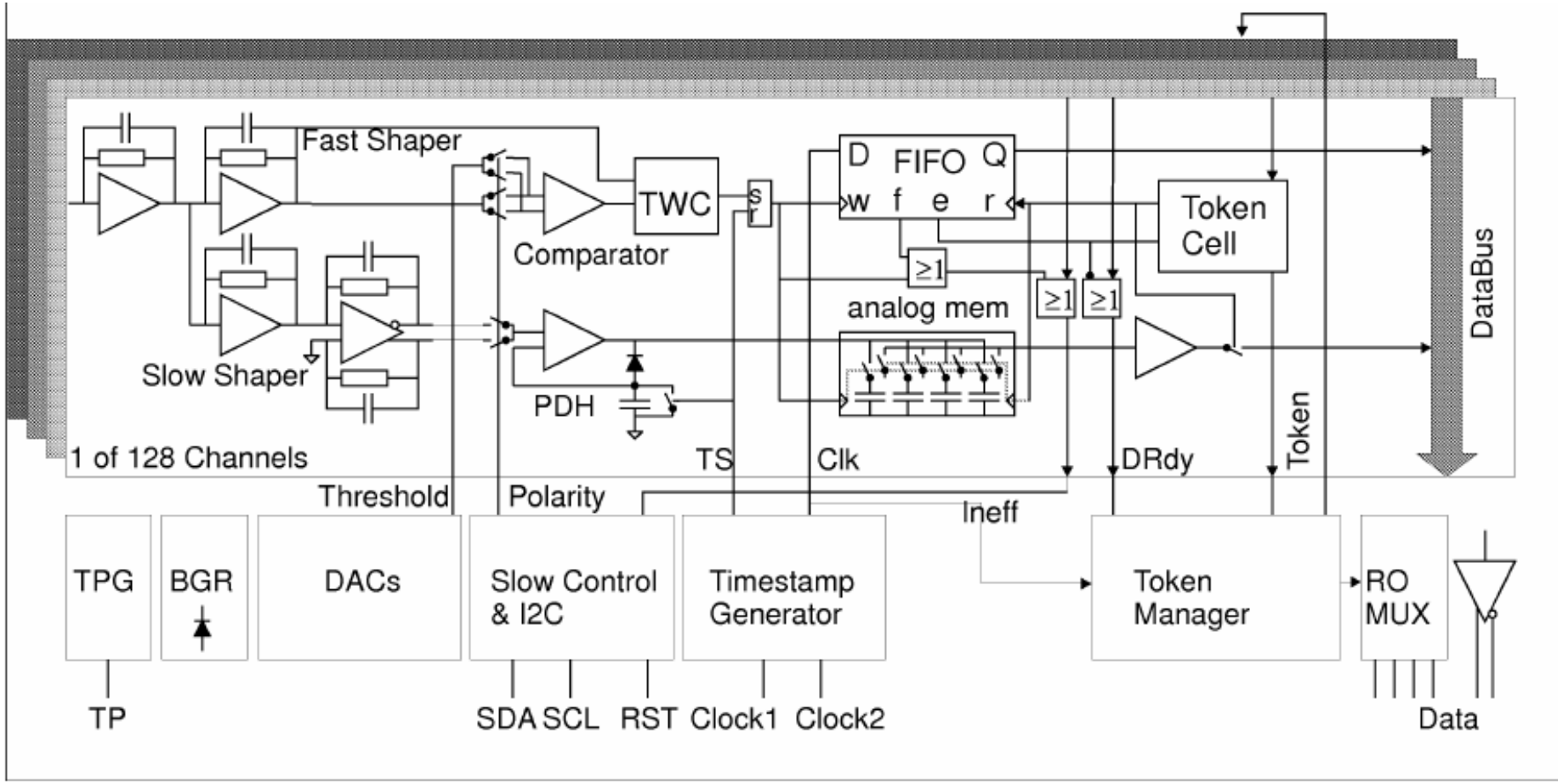
$$d_k = w_3\, p_{k-2} + w_2\, p_{k-1} + w_1\, p_k \quad .$$

- The right circuit stores the voltages p_k on (scaled feedback) capacitors and adds them in the last step
  - W_2 is negative so that the middle cap must be flipped

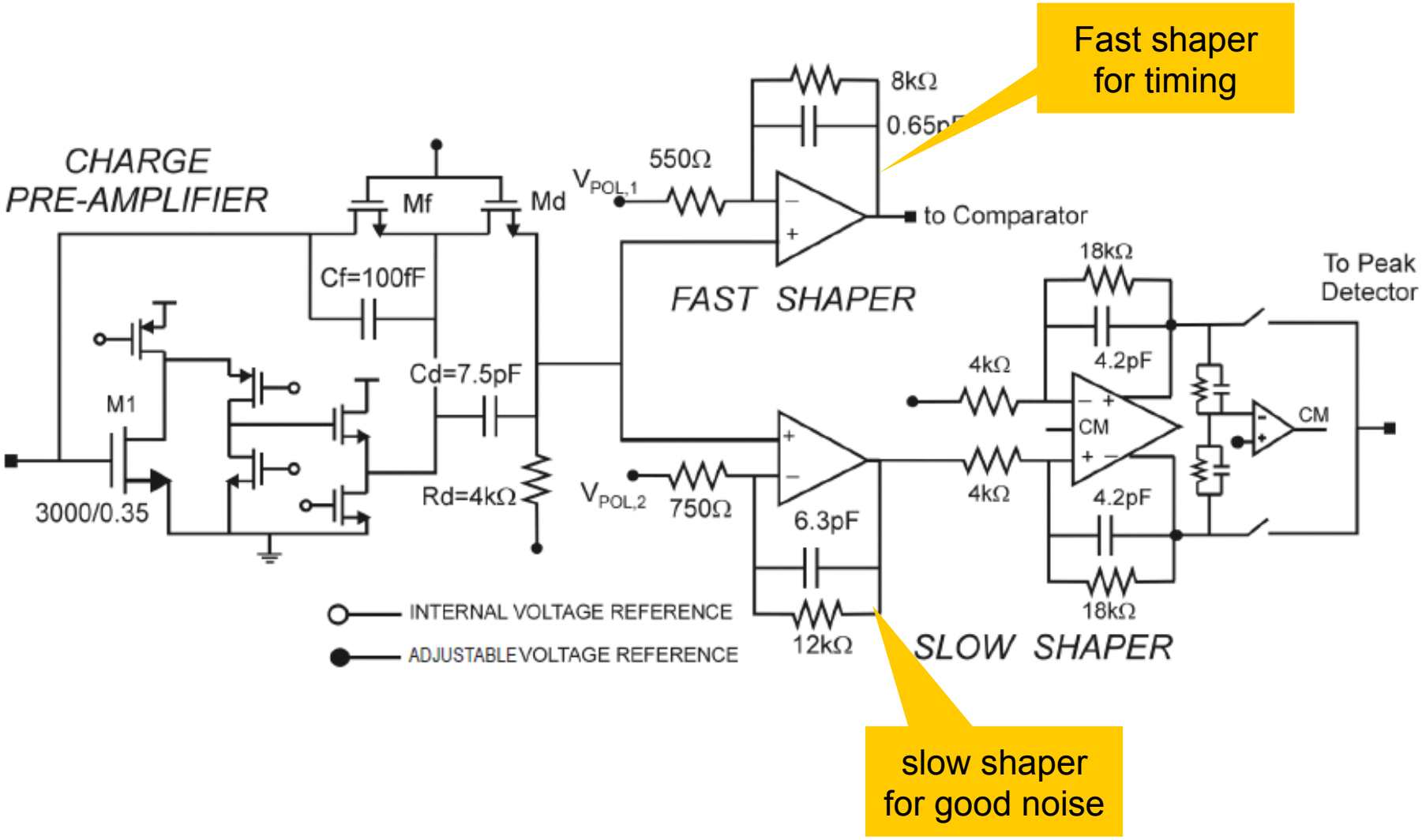


Self Triggered Strips : XYTER

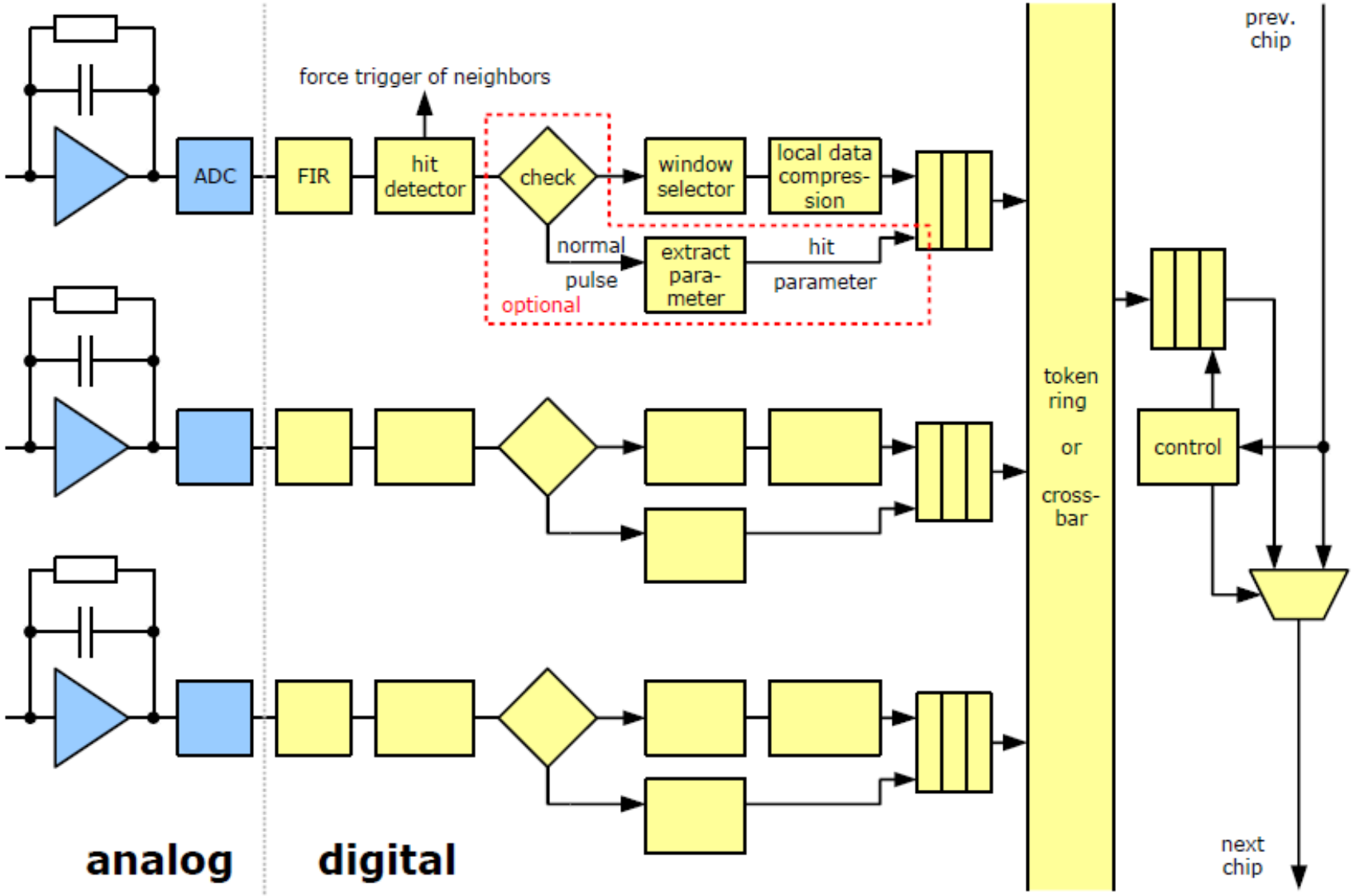
- Hits are detected automatically
- Need a ‘time stamp’ to associate them to correct events
- Want analogue Amplitude



XYTER Analogue Front End



Self Triggered Strips with ADC (CBM TRD)



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RADIATION DAMAGE IN ELECTRONICS

Radiation Damage to the Electronics

- Chips are often traversed by particles
  → this '*irradiation*' can be **very** high

- Three types of effects:

  1. *Permanent* damage of crystal by nuclear reactions
     Mainly caused by heavy particles.
     Damage depends on particle type and energy.
     Damage can be well scaled 'NIEL hypothesis' to a reference of *1MeV neutrons*
     Particle flux for non-ionizong energy loss (NIEL) given in **'neutron equivalents'**

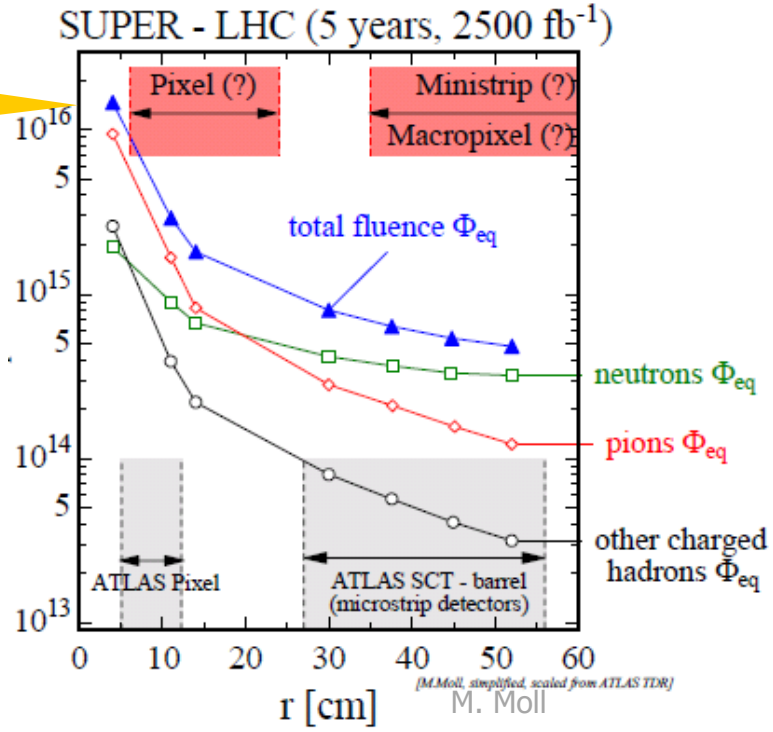
  2. *Permanent* generation of e-h pairs: **'Total Ionizing Dose'**
     (TID, given in Gray = Gy = J/kg or rad = 0.01 Gy)
     Leads to upcharging of isolators → high fields, threshold shifts

  3. *Transient* local deposition of large charges: **'Single Event Effects'**

Damage at LHC

- Numbers for LHC inner layers
  - TID: 50-100 Mrad = 0.5-1 MGy
  - NIEL: 3×10^{15} neutrons '1MeV equivalent' / cm^2

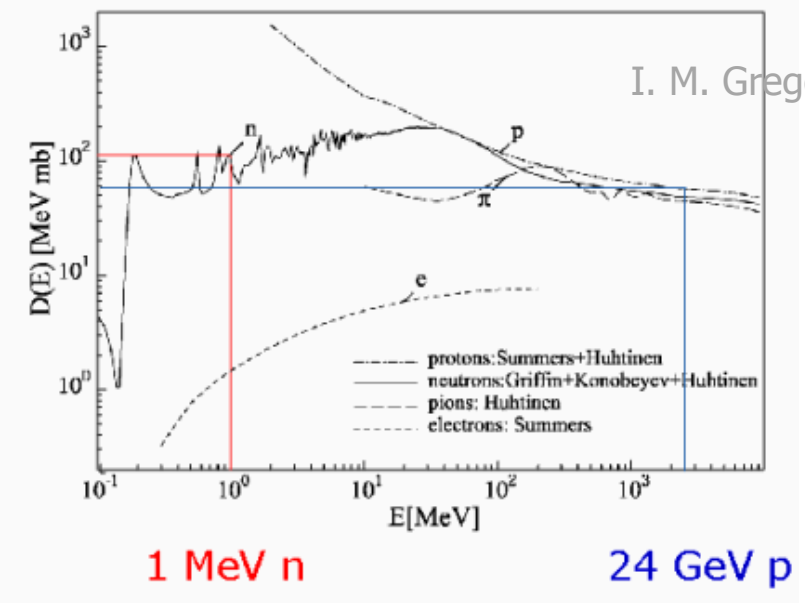
10^{16} at Super-LHC



- For comparison:
  - Space experiments ~ 100krad.
  - Commercial devices ~ 10krad.

1. NIEL

- Bulk damage as a function of particle energy & type (in silicon!):
  - Example: 24 GeV protons cause ~1.7 x less damage than 1MeV neutrons



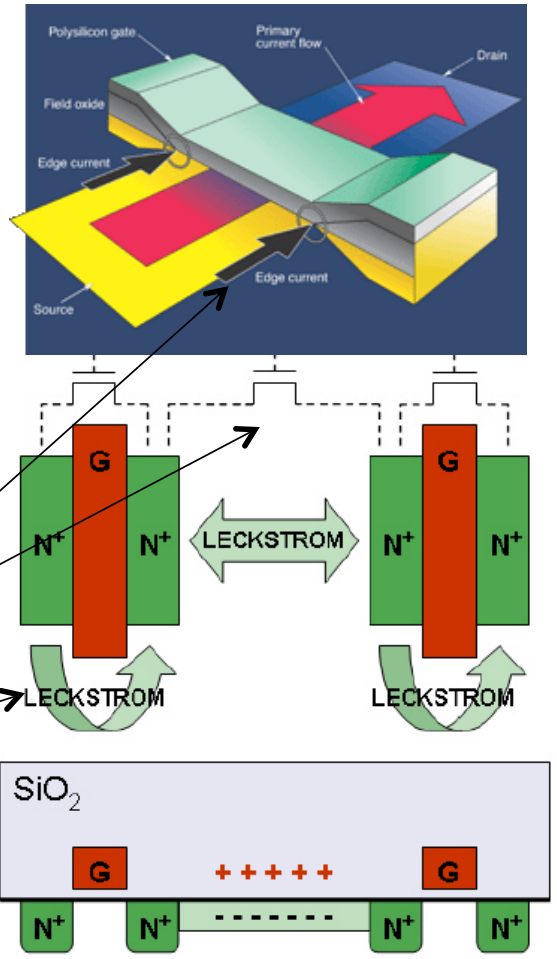
- NIEL is mostly relevant for sensor (change of bulk doping, type inversion, leakage current, trapping / carrier lifetime),
- Is *NOT* relevant for (MOS) electronics (but for bipolars)

2. Total Ionizing Dose (TID)

- *Ionizing* radiation creates *electron-hole pairs* in isolators. Electrons can drift away, holes are stuck ('low' mobility) or are trapped at interface (cannot 'escape' the isolator)
  →
- Oxides become **positively charged**

Consequences:

1. At GATE oxide:
   Threshold voltage shift
   - decreasing for NMOS – cannot be turne
   - increasing for PMOS – low current
2. At other 'field oxides':
   - creation of parasitic NMOS
   - leakage 'around' NMOS



TID: Solutions

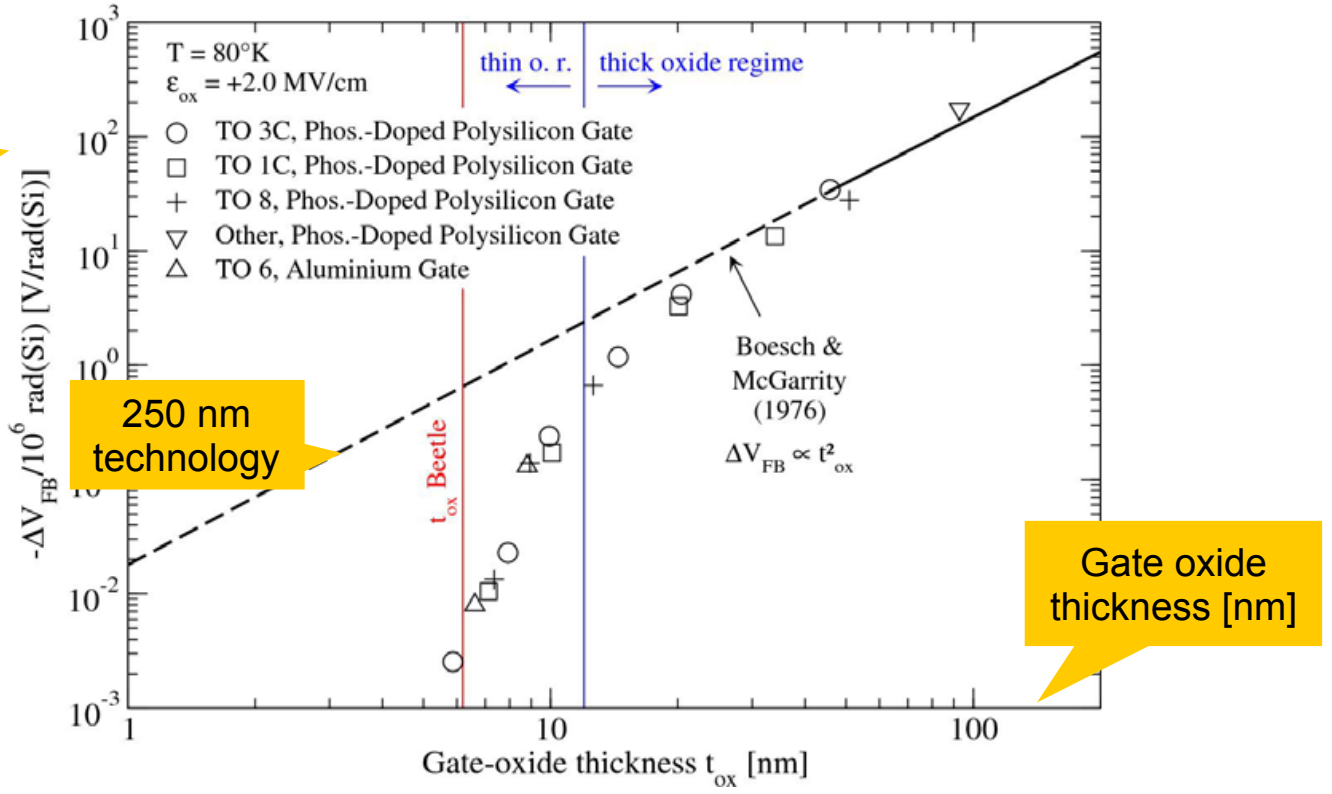
- Two possible Solutions:

1. use specialized 'radiation hard' technology (DMILL, Honeywell), which provide technologies for military & space applications and offer them for the 'public'
   - We have done a full FE chip (2 submissions) in DMILL. We have dropped this technology mainly because of the extremely poor yield.
   - vendors die out
2. Use a technology with very thin gate oxides ('deep-submicron technology' = DSM, Lgate ≤ ¼µm) and design with special layout rules.
   - 'hardening by design'
   - This create 'radiation tolerant' chips
     ATLAS chips operational up to 100 Mrad, as required…

Reduction of Threshold Voltage Shift

- When gate oxides become very thin, the holes can escape the isolator by tunneling (as well as the electrons)
  - Upcharging & threshold voltage shift is reduced
- This has already been observed / predicted 1976!
- Conclusion: Problem disappears for technology < 250 nm!

Threshold voltage shift per Mrad

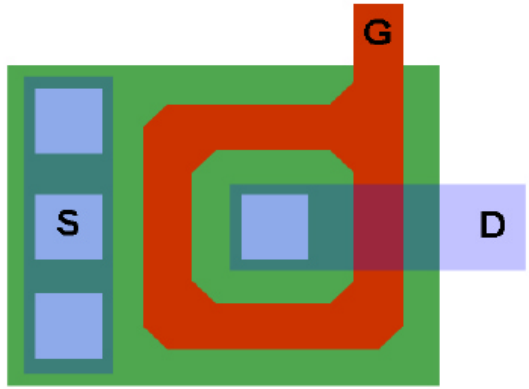


250 nm technology

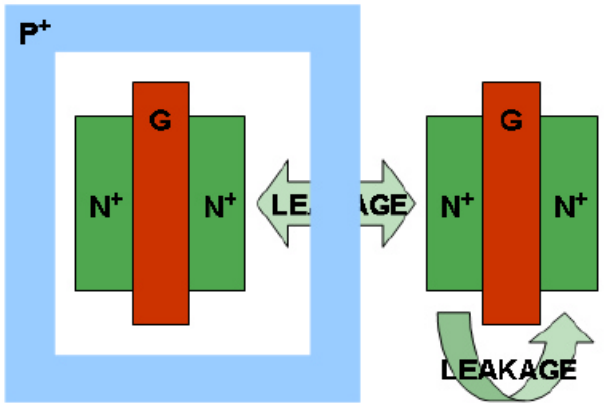
Gate oxide thickness [nm]

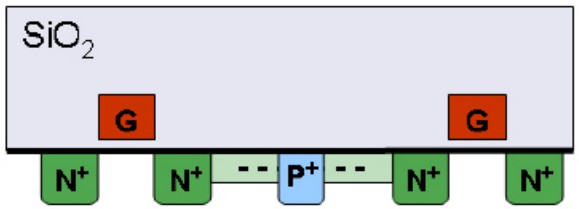
Remedies for Field Oxide Leakage

- Enclosed NMOS (other shapes are possible!)
- Guard rings between NMOS with drains on different potential
- Special FF design / redundancy / voting / hamming... for SEU / SET



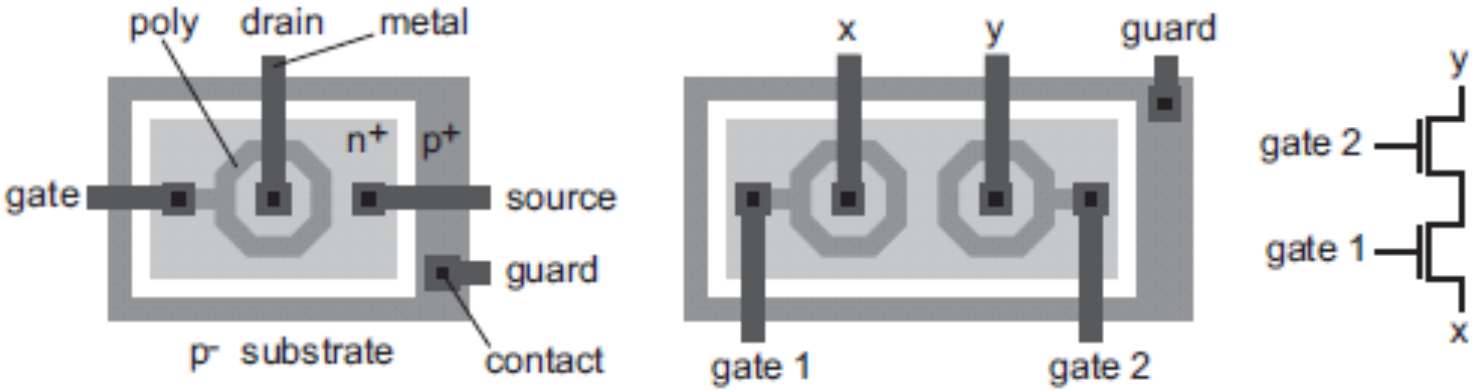
- Consequences:
  - need special extraction files
  - larger area (x4 for digital designs)
  - larger caps -> often more power in digital (x4)
  - Hard to make good NMOS current source (large L no possible)
  - Hard to make good NMOS switches (very asymmetric & large caps)



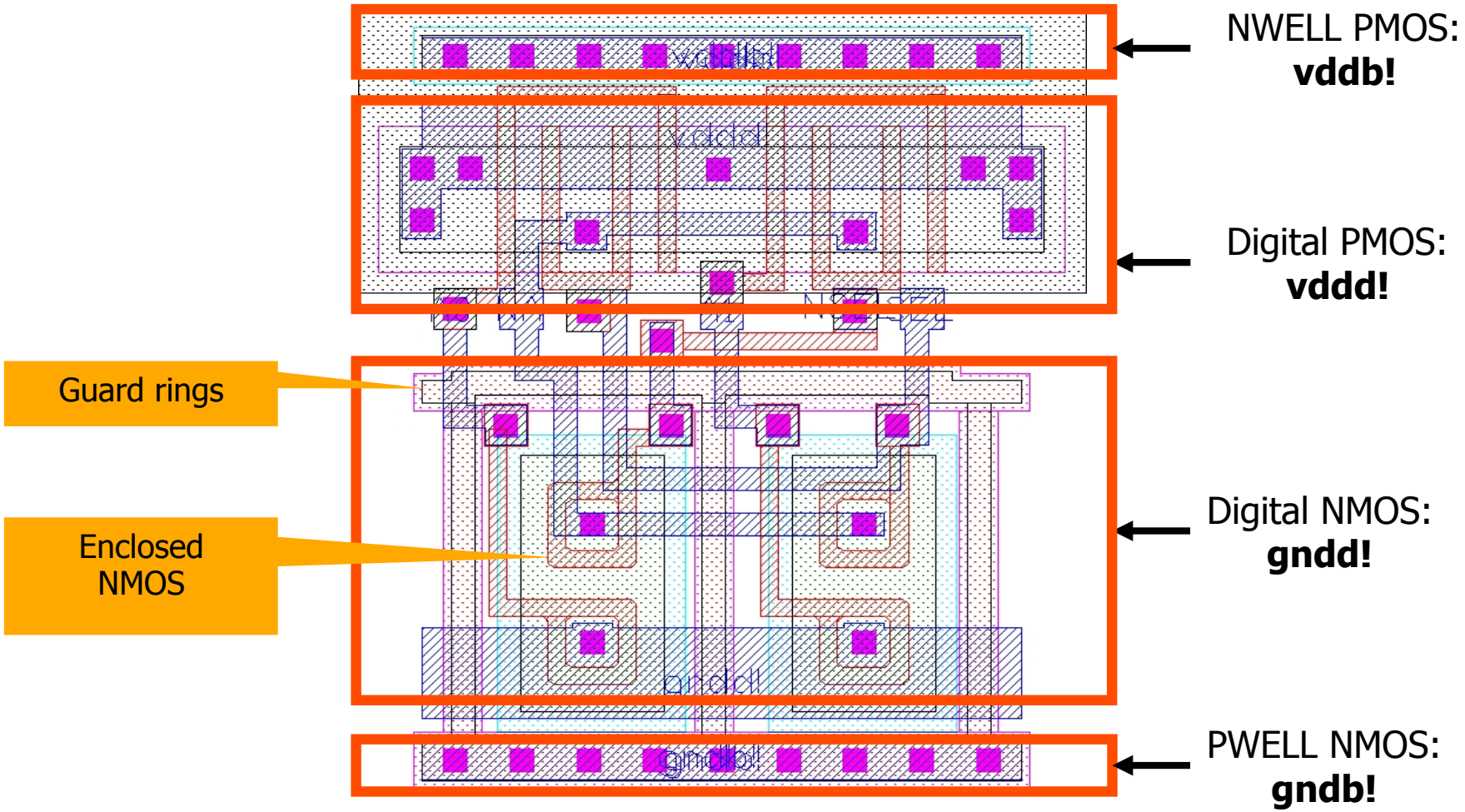


Typical MOS Layouts

- CAD Tools have problems to extract these ‘annular’ or ‘enclosed’ devices...

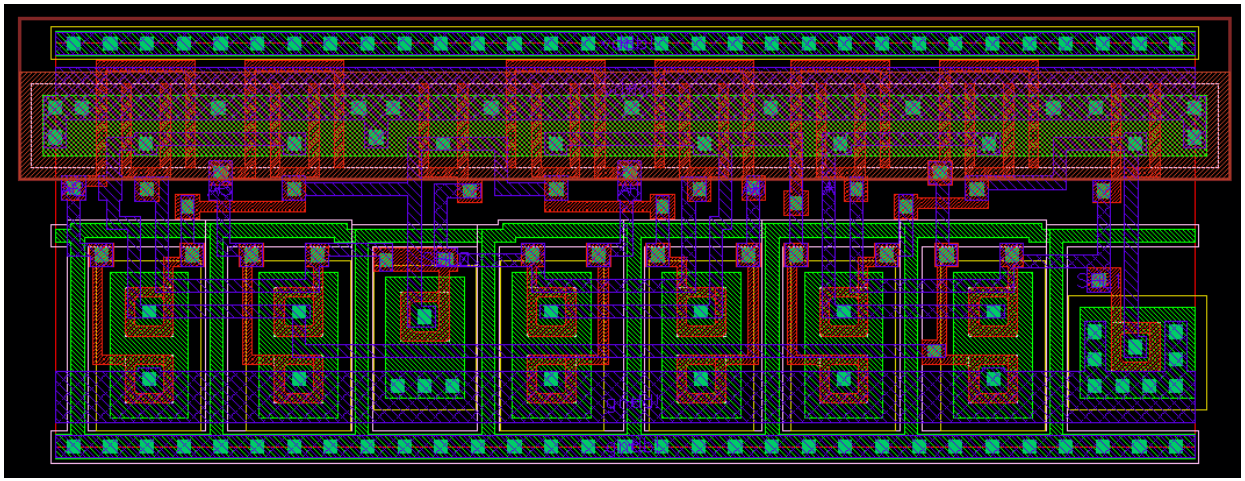


Example: radhard MUX2->1

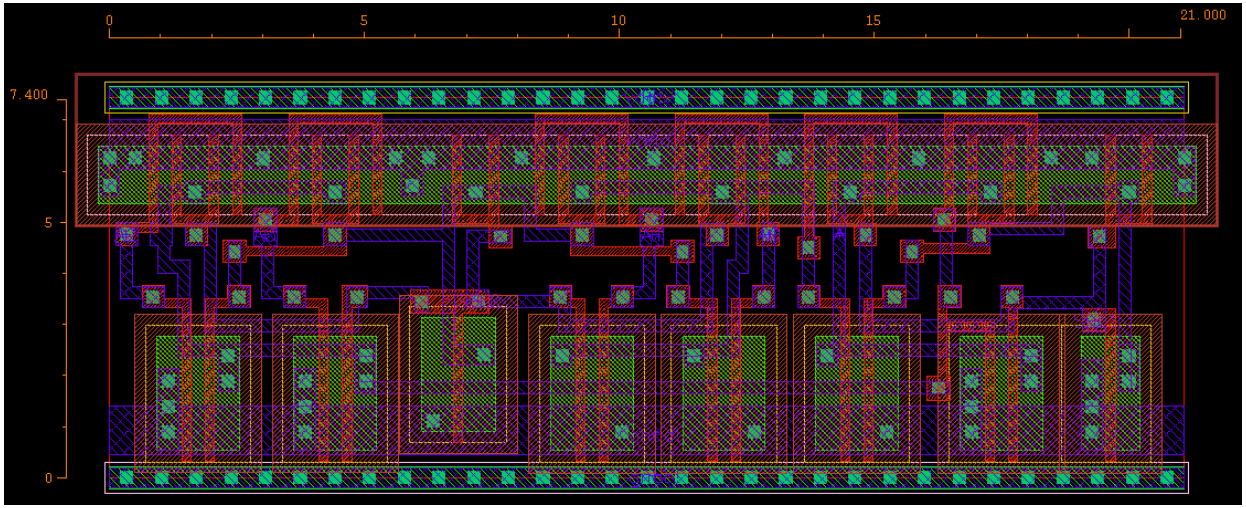


Radhard vs. Normal Layout

- We want to compare both types.
  Therefore made cells with equal transistor / layout size:

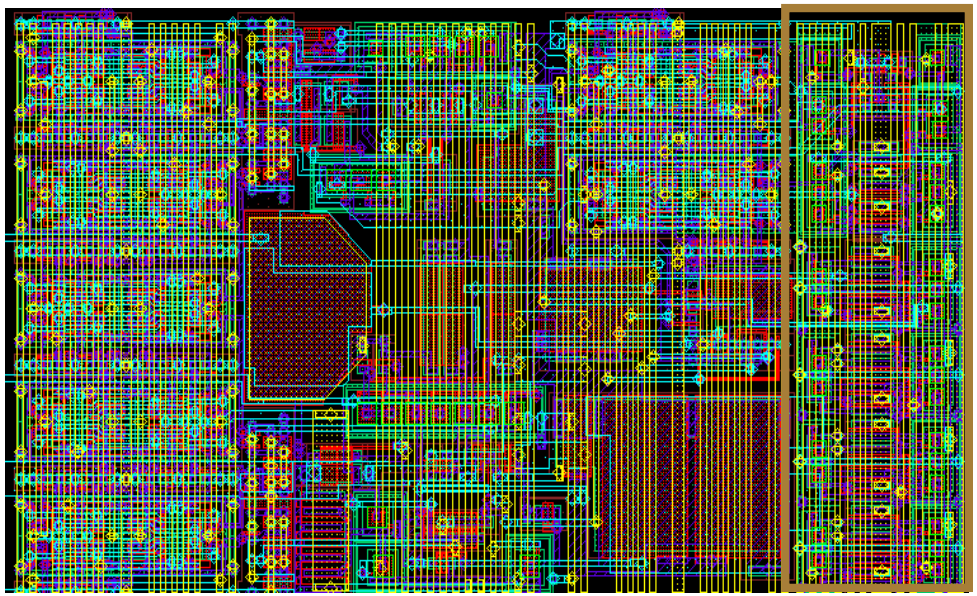


Hard

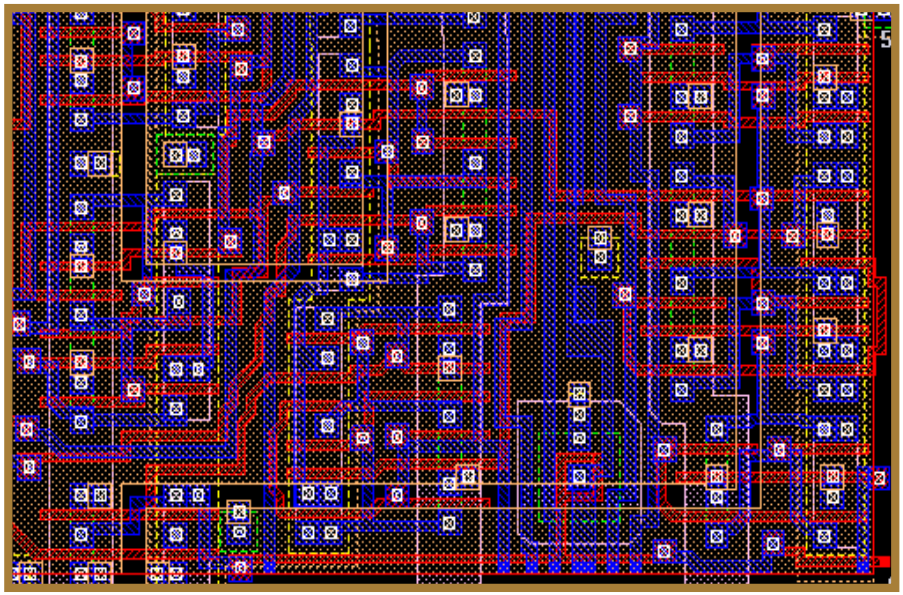


Normal

Layout comparison: 0.8µm ⇔ annular 0.25µm



Pixel of ATLAS FE chip

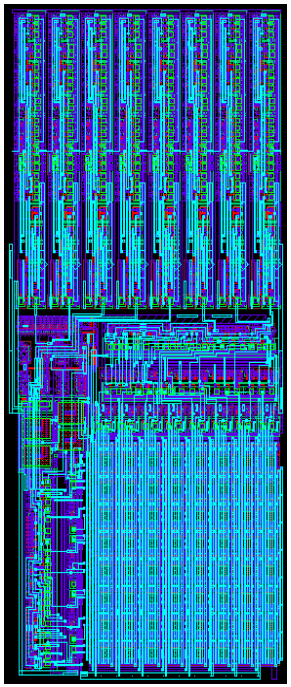


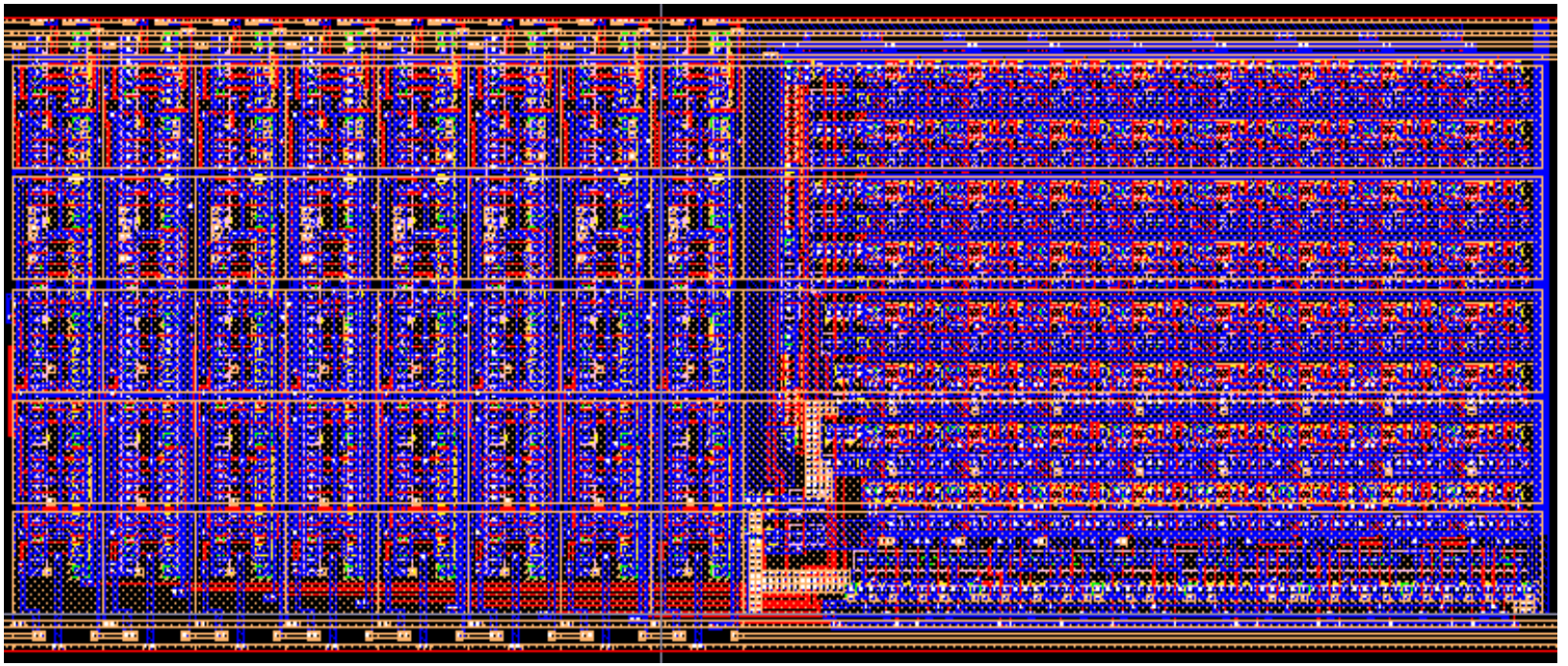
0.25µm:
63 devices, 16x50 µm2
< 1 day work

DMILL:
59 devices, 90x50 µm2
> 1 week work

We got a x 6 gain the density (full custom digital) with much less layout effort

Example: 8 bit DAC 0.8µm ⇔ annular 0.25µm

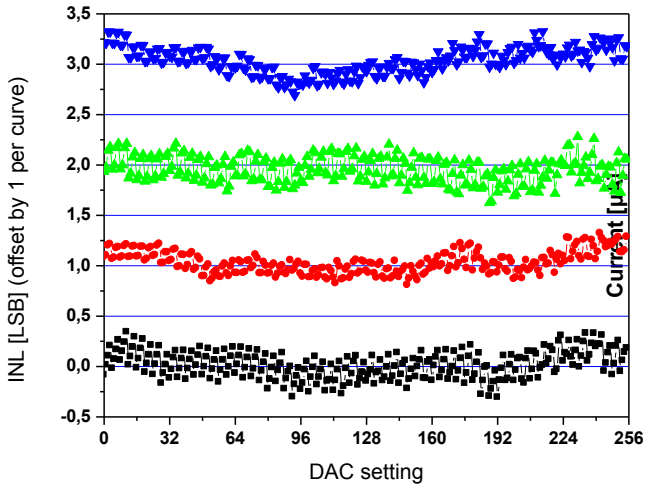


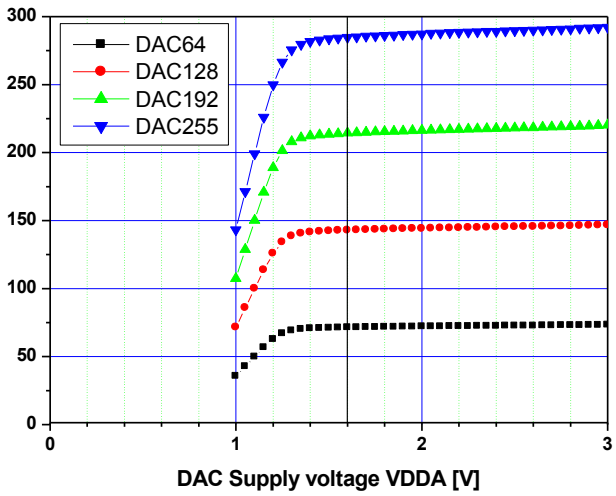


0.25µm
80x200 µm2

DMILL
500x200 µm2

gain x 6 in mixed mode full custom layout

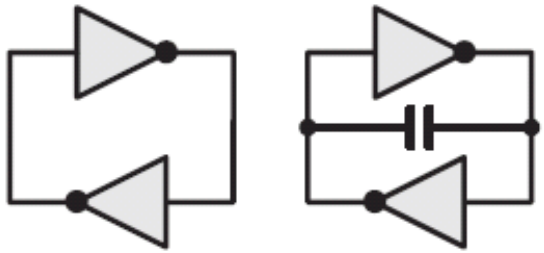




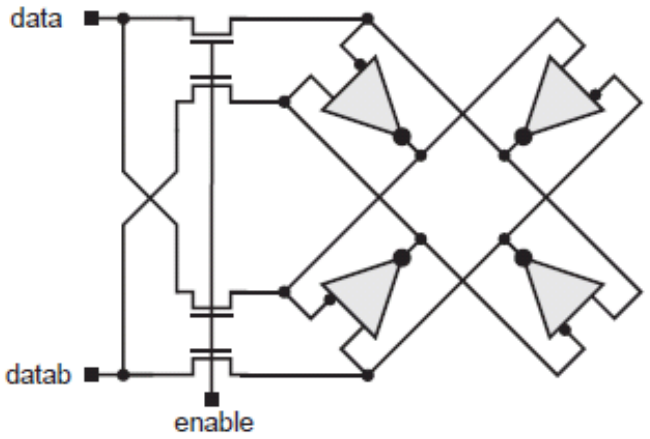
3. Single Event effects

- Large local charge deposition can lead to
  - SET: single event transient = spike on signal
  - SEU: single event upset = bit flip
  - SEGR: single event gate rupture (really?)

- Most relevant: SEU.
- Protection of Bits:
  - Protect cells
  - Add redundancy

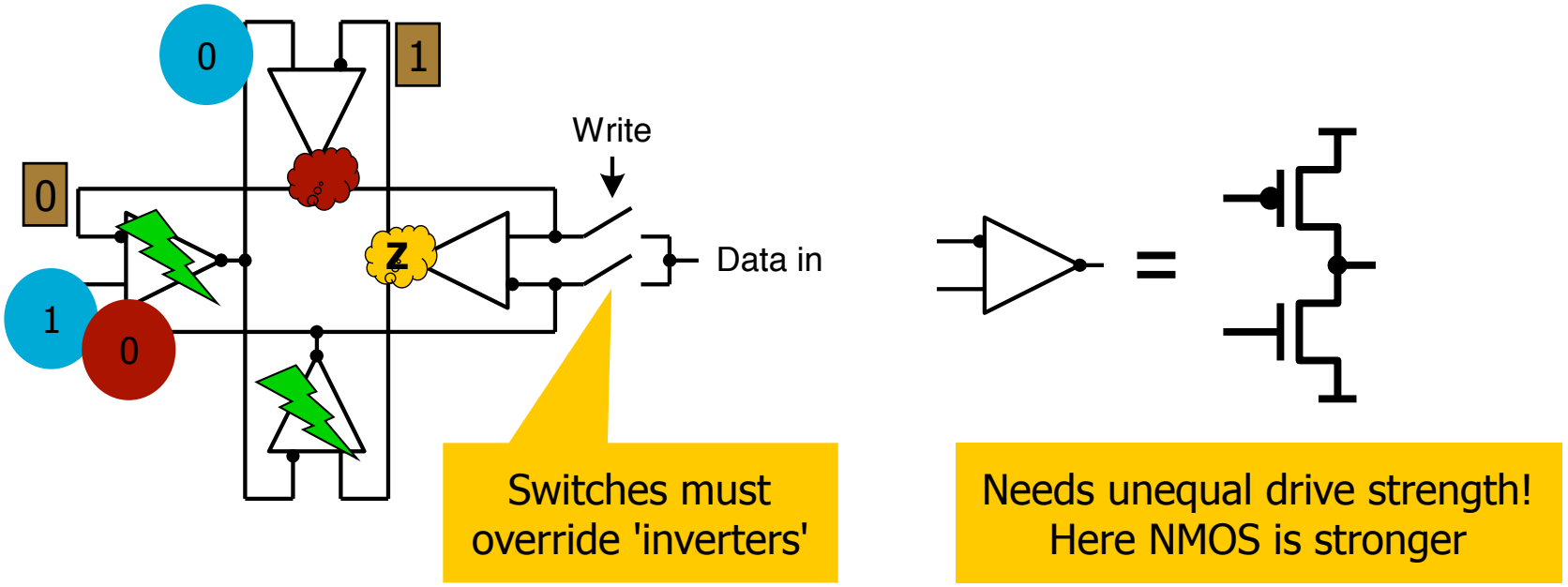


- Protected storage cells:
  - Large capacitance
  - DICE cell
  - …



SEU tolerant design

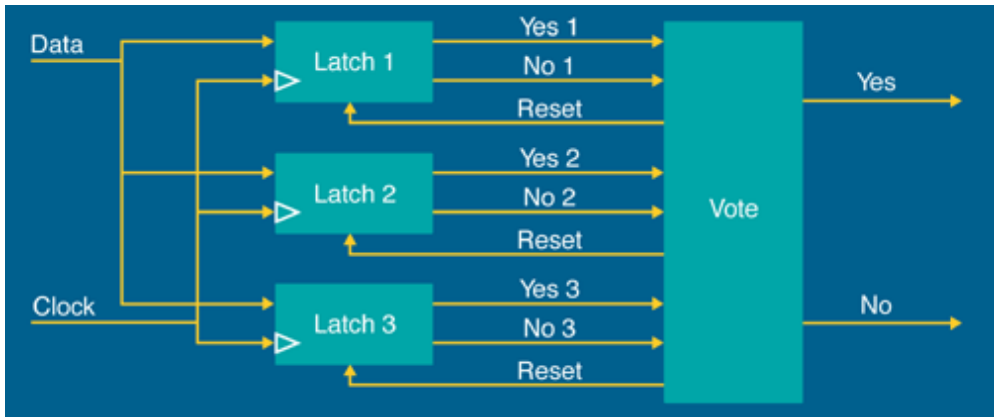
- The 'Dual interlock storage cell' (DICE) cell is a clever latch which needs simultaneous writing to two nodes in order to flip.
- Devices: 8 NMOS, 4 PMOS (no reset)
- Note that redundant nodes must be separated in layout!



(Calin, Nicolaidis, Velazco, IEEE Trans. Nucl. Sci., Vol.43, No.6, 1996)

Adding Redundancy to protect stored bits

- Most simple: Triple Mode Redundancy & Voter
  - A flip in *one* latch has no effect on voter output
  - It can be detectred and corrected for !

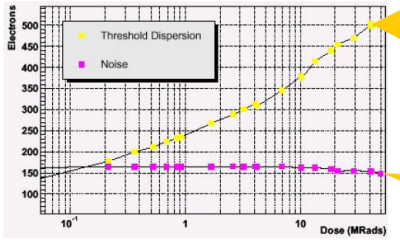


- Drawback: Large Overhead
- Better: Use larger words & Hamming protection
  - For d data bits and p protection bits, must satisfy $d+p+1 \leq 2^p$ to *detect* an error. One extra bit allows to *correct* for the error
  - For instance for d = 8 data bits, need p = 4 protection bits to detect: $d + p + 1 = 8 + 4 + 1 = 13 < 16 = 2^4 = 2^p$
  - Note that the protection bits are protected themselves as well!

Radiation Hardness of the FEI-1 chip

Radiation hardness studies

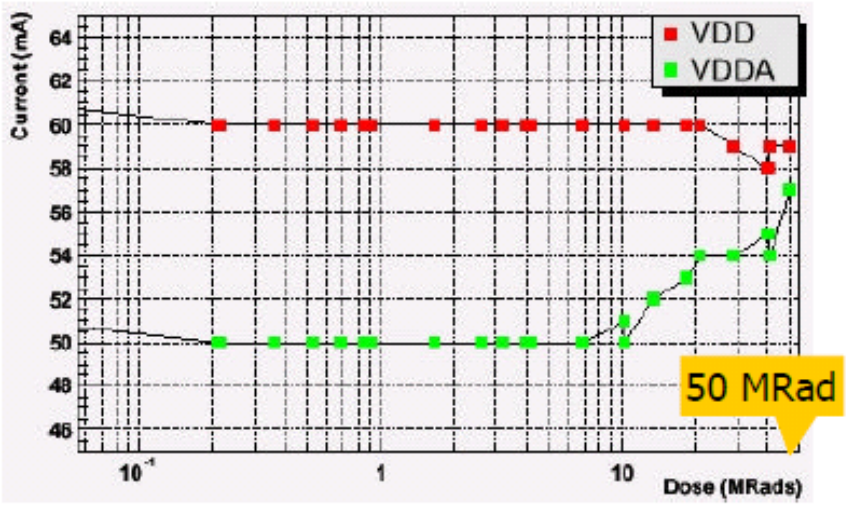
- Irradiations have been performed at LBNL (88" Cyclotron) and at CERN PS
- Dose was up to 50/60 Mrad (This is expected after 10 years of LHC operation)
- The bare chips were operated during irradiation
- Chips are still fully functional after this dose
- Some (preliminary) results:

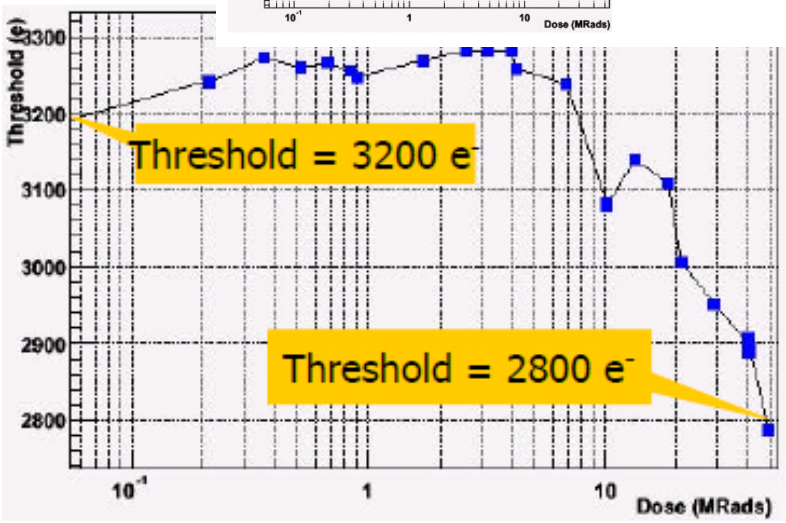


Threshold dispersion on tuned chip increases (chip can be re-tuned)

This radiation-induced Mismatch needs to be understood!

No change in noise !





Small change in analog and digital supply currents

Small change in threshold (no change in bias settings!)